Freescale Semiconductor
Technical Data

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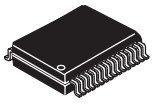
System Basis Chip with LIN Transceiver

33689D

SYSTEM BASIS CHIP WITH LIN



DWB SUFFIX
EW SUFFIX (PB-FREE)
98ARH99137A
32-PIN SOICW

The 33689 is a SPI-controlled System Basis Chip (SBC) that combines many frequently used functions in an MCU-based system plus a Local Interconnect Network (LIN) transceiver. Applications include power window, mirror, and seat controls. The 33689 has a 5.0 V, 50 mA low dropout regulator with full protection and reporting features. The device provide full SPI-readable diagnostics and a selectable timing watchdog for detecting errant operation.

The LIN transceiver waveshaping circuitry can be disabled for higher data rates. One 50 mA and two 150 mA high-side switches with output protection are available to drive inductive or resistive loads. The 150 mA switches can be pulse-width modulated (PWM).

Two high-voltage inputs are available for contact monitoring or as external wake-up inputs. A current sense operational amplifier is available for load current monitoring.

The 33689 has three operational modes:

- Normal (all functions available)
- Sleep (VDD OFF, wake-up via LIN bus or wake-up inputs)
- Stop (VDD ON, wake-up via MCU, LIN bus, or wake-up inputs)

Features

- Full-Duplex SPI Interface at Frequencies up to 4.0MHz
- LIN Transceiver Capable to 100kbps with Waveshaping Capability
- 5.0 V Low Dropout Regulator Full Fault Detection and Protection
- One 50 mA and Two 150 mA Protected High-Side Switches
- Current Sense Operational Amplifier
- The 33689 is compatible with LIN 2.0 Specification Package.
- Pb-Free Packaging Designated by Suffix Code EW

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33689DDWB/R2	-40℃ to 125℃	32 SOICW
MCZ33689DEW/R2		

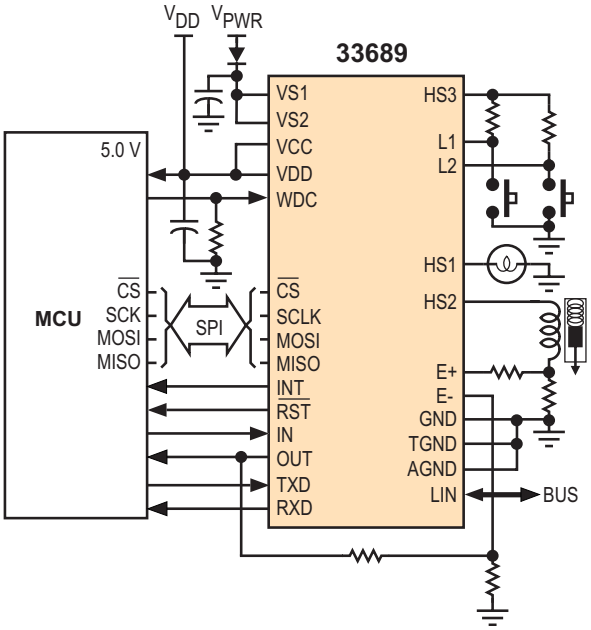


Figure 1. 33689 Simplified Application Diagram

INTERNAL BLOCK DIAGRAM

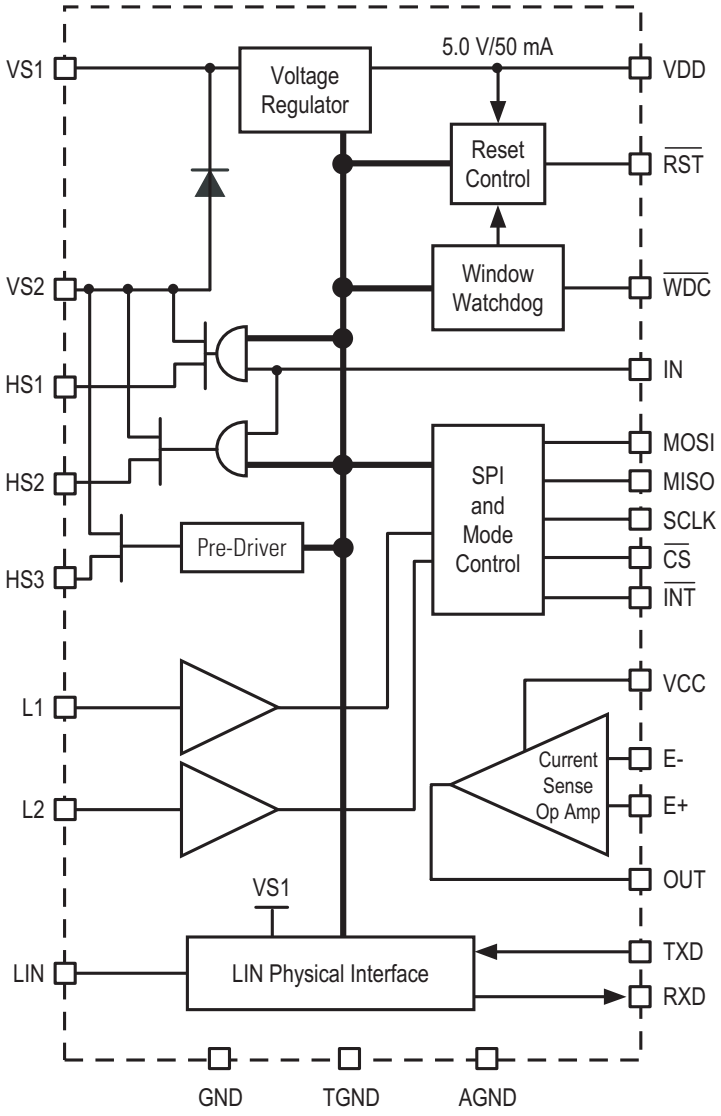


Figure 2. 33689 Simplified Internal Block Diagram

PIN CONNECTIONS

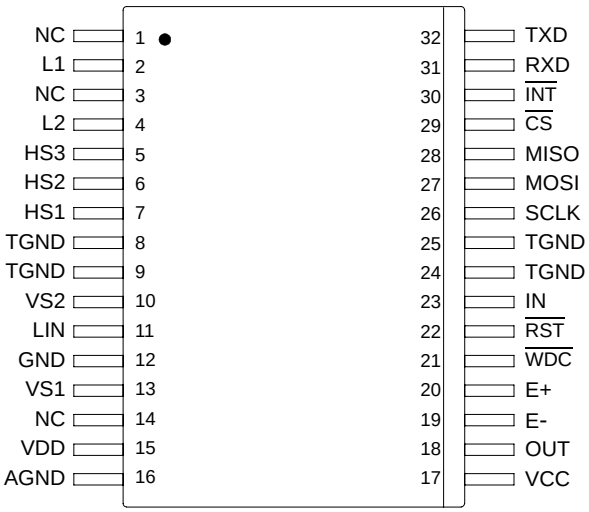


Figure 3. 33689 32-SOICW Pin Connections

Table 1. 33689 32-SOICW Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 19.

Pin	Pin Name	Formal Name	Pin Function	Definition
1, 3, 14	NC	No Connect	N/A	No internal connection to these pins.
2, 4	L1, L2	Level Inputs 1 and 2	Input	Inputs from external switches or from logic circuitry.
5–7	HS3–HS1	High-Side Driver Outputs 3 through 1	Output	High-side (HS) drive power outputs. SPI-controlled for driving system loads.
8, 9, 24, 25	TGND	Thermal Ground	N/A	Thermal ground pins for the device.
10	VS2	Voltage Supply 2	Input	Supply pin for the high-side switches HS1, HS2, and HS3.
11	LIN	LIN Bus	Input/Output	Bidirectional pin that represents the single-wire bus transmitter and receiver.
12	GND	Ground	N/A	Electrical ground pin for the device.
13	VS1	Voltage Supply 1	Input	Supply pin for the 5.0 V regulator, the LIN physical interface, and the internal logic.
15	VDD	5.0 V Regulator Output	Output	Output of the 5.0 V regulator.
16	AGND	Analog Ground	N/A	Analog ground pin for voltage regulator and current sense operational amplifier.
17	VCC	Power Supply In	Input	5.0 V supply for the internal current sense operational amplifier.
18	OUT	Amplifier Output	Output	Output of the internal current sense operational amplifier.
19	E-	Amplifier Inverted Input	Input	Inverted input of the internal current sense operational amplifier.
20	E+	Amplifier Non-Inverted Input	Input	Non-inverted input of the internal current sense operational amplifier.
21	$\overline{\text{WDC}}$	Watchdog Configuration (Active Low)	Reference	Configuration pin for the watchdog timer.

Table 1. 33689 32-SOICW Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 19.

Pin	Pin Name	Formal Name	Pin Function	Definition
22	$\overline{\text{RST}}$	Reset Output (Active LOW)	Output	5.0 V regulator and watchdog reset output pin.
23	IN	PWM Input Control	Input	External input PWM control pin for high-side switches HS1 and HS2.
26	SCLK	Serial Data Clock	Input	Clock input for the SPI of the 33689.
27	MOSI	Master Out Slave In	Input	SPI data received by the 33689.
28	MISO	Master In Slave Out	Output	SPI data sent to the MCU by the 33689. When $\overline{\text{CS}}$ is HIGH, pin is in the high-impedance state.
29	$\overline{\text{CS}}$	Chip Select (Active LOW)	Input	SPI control chip select input pin.
30	$\overline{\text{INT}}$	Interrupt Output (Active LOW)	Output	This output pin reports faults to the MCU when an enabled interrupt condition occurs.
31	RXD	Receiver Output	Output	Receiver output of the LIN interface and reports the state of the bus voltage.
32	TXD	Transmitter Input	Input	Transmitter input of the LIN interface and controls the state of the bus output.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
V_{PWR} Supply Voltage at VS1 and VS2			V
Continuous	V_{SUPDC}	-0.3 to 27	
Transient (Load Dump)	V_{SUPTR}	40	
Supply Voltage at VDD and VCC	V_{DD}	-0.3 to 5.5	V
Output Current at VDD	I_{DD}	Internally Limited	A
Logic Input Voltage at MOSI, SCLK, $\overline{CS}$, IN, and TXD	V_{INLOG}	-0.3 to V_{DD}+0.3	V
Logic Output Voltage at MISO, $\overline{INT}$, $\overline{RST}$, and RXD	V_{OUTLOG}	-0.3 to V_{DD}+0.3	V
Input Voltage at E+ and E-	V_{E+}/V_{E-}	-0.3 to 7.0	V
Input Current at E+ and E-	I_{E+}/I_{E-}	±20	mA
Output Voltage at OUT	V_{OUT}	-0.3 to V_{CC}+0.33	V
Output Current at OUT	I_{OUT}	±20	mA
Input Voltage at L1 and L2			V
DC Input with a 33 kΩ Resistor	V_{LXDC}	-18 to 40	
Transient Input with External Component (per ISO7637 Specification) (See Figure 4, page 6)	V_{LXTR}	±100	
Input/Output Voltage at LIN			V
DC Voltage	V_{BUSDC}	-18 to 40	
Transient Input Voltage with specified External Component (per ISO7637 Specification) (See Figure 4, page 6)	V_{BUSTR}	-150 to 100	
DC Output Voltage at HS1 and HS2			V
Positive	V_{HS+}	V_{VS2} + 0.3	
Negative	V_{HS-}	Internally Clamped	
DC Output Voltage at HS3	V_{HS3}	-0.3 to V_{VS2} + 0.3	V
ESD Voltage, Human Body Model (1)	V_{ESD1}		V
GND Configured as Ground. TGND and AGND Configured as I/O Pins			
LIN, L1, and L2		±4000	
All Other Pins		±2000	
ESD Voltage, Charge Device Model (1)	V_{ESD2}		V
Corner Pins (Pins 1, 16, 17, and 32)		±750	
All other Pins (Pins 2–15 and 18–31)		±500	

Notes

1. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), ESD2 testing is performed in accordance with the Charge Device Model, Robotic (C_{ZAP} = 4.0 pF).

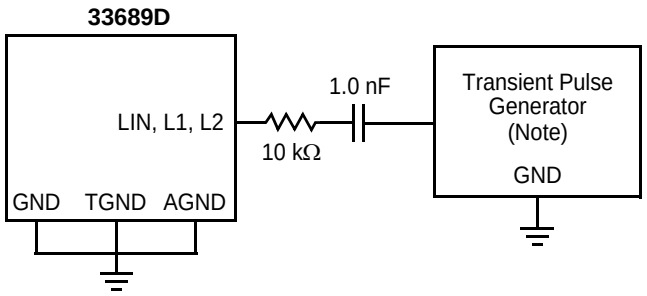
Table 2. Maximum Ratings(continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
THERMAL RATINGS			
Operating Temperature Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Storage Temperature	T_{STG}	-55 to 165	°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	80	℃/ W
Peak Package Reflow Temperature During Solder Mounting (2)	T_{SOLDER}	240	℃

Notes

2. Pin soldering temperature is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause permanent damage to the device.



Note Waveform per ISO 7637-1. Test Pulses 1, 2, 3a, and 3b.

Figure 4. ISO 7637 Test Setup for LIN, L1, and L2 Pins

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VS1 AND VS2 INPUT PINS (DEVICE POWER SUPPLY)					
Supply Input Voltage					V
Nominal DC	V_{SUP}	5.5	—	18	
Load Dump	V_{SUPLD}	—	—	40	
Jump Start (3)	V_{SUPJS}	—	—	27	
Supply Input Current (4)					
Normal Mode, I_{OUT} at VDD = 10 mA, LIN Recessive State	$I_{SUP(NORM)}$	—	5.0	8.0	mA
Sleep Mode, VDD OFF, V_{SUP} ≤ 13.5 V	I_{SLEEP}	—	35	45	μA
Stop Mode, VDD ON with I_{OUT} < 100 μA, V_{SUP} ≤ 13.5 V	I_{STOP}	—	60	75	μA
Input Threshold Voltage (Normal Mode, Interrupt Generated)					V
Fall Early Warning, Bit VSUV Set	V_{SUVEW}	5.7	6.1	6.6	
Overvoltage Warning, Bit VSOV Set	V_{SOVW}	18	19.75	20.5	
Hysteresis (5)	V_{HYS}				
VSUV Flag		—	1.0	—	V
VSOV Flag		—	220	—	mV
VDD OUTPUT PIN (EXTERNAL 5.0 V OUTPUT FOR MCU USE) (6)					
Output Voltage	V_{DDOUT}				V
I_{DD} from 2.0 mA to 50 mA, 5.5 V < V_{SUP} < 27 V		4.75	5.0	5.25	
Dropout Voltage (7)	V_{DDDROP}				V
I_{DD} = 50 mA		—	0.1	0.2	
Output Current Limitation (8)	I_{DD}	50	120	200	mA
Overtemperature Pre-warning (Junction)	T_{PRE}				°C
Normal Mode, Interrupt Generated, Bit VDDT Set		120	135	160	
Thermal Shutdown (Junction)	T_{SD}				°C
Normal Mode		165	170	—	

Notes

3. Device is fully functional. All features are operating. An overtemperature fault may occur.
4. Total current (I_{VS1} + I_{VS2}) at VS1 and VS2 pins is measured at the ground pins.
5. Parameter guaranteed by design; however, it is not production tested.
6. Specification with external capacitor 2.0 μF < C < 10 μF and 200 mΩ ≤ ESR ≤ 10 Ω. Normal mode. Low ESR electrolytic capacitor values up to 47 μF can be used.
7. Measured when the voltage has dropped 100 mV below its nominal value.
8. Internally limited. Total 5.0 V regulator current. A 5.0 mA current for the Current Sense Operational Amplifier operation is included. Digital outputs are supplied from VDD.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VDD OUTPUT PIN (5.0 V OUTPUT FOR MCU USE) (CONTINUED) (9)					
Temperature Threshold Difference Normal Mode (T_{SD} - T_{PRE})	T_{DIFF}	20	30	40	°C
V_{SUP} Range for Reset Active 0.5 V < V_{DD} < V_{DD} ($V_{\overline{RSTTH}}$)	V_{SUPR}	4.0	—	—	V
Line Regulation 5.5 V < V_{SUP} < 27 V, I_{DD} = 10 mA	V_{LR1}	—	20	150	mV
Load Regulation 1.0 mA < I_{DD} < 50 mA	V_{LD1}	—	10	150	mV
VDD OUTPUT PIN IN STOP MODE					
Output Voltage (10) I_{DD} ≤ 2.0 mA	V_{DDS}	4.75	5.0	5.25	V
Output Current Capability (11)	I_{DDS}	4.0	8.0	14	mA
Line Regulation 5.5 V < V_{SUP} < 27 V, I_{DD} = 2.0 mA	V_{LRS}	—	10	100	mV
Load Regulation 1.0 mA < I_{DD} < 5.0 mA	V_{LDS}	—	40	150	mV
$\overline{RST}$ OUTPUT PIN IN NORMAL AND STOP MODES					
Reset Threshold Voltage	$V_{\overline{RSTTH}}$	4.5	4.7	V_{DD}-0.2	V
Low-Level Output Voltage I_O = 1.5 mA, 4.5 V < V_{SUP} < 27 V	V_{OL}	0.0	—	0.9	V
High-Level Output Current 0.0 V < V_{OUT} < 0.7 V_{DD}	I_{OH}	—	-275	—	µA
Reset Pulldown Current Internally Limited, V_{DD} < 4.0 V, $V_{\overline{RST}}$ = 4.6 V	$I_{PD\overline{RST}}$	1.5	—	8.0	mA
IN INPUT PIN					
Low-Level Input Voltage	V_{IL}	-0.3	—	0.3 V_{DD}	V
High-Level Input Voltage	V_{IH}	0.7 V_{DD}	—	V_{DD} +0.3	V
Input Current 0.0 V < V_{IN} < V_{DD}	I_{IN}	-10	—	10	µA

Notes

9. Specification with external capacitor 2.0 µF < C < 10 µF and 200 mΩ ≤ ESR ≤ 10 Ω. Normal mode. Low ESR electrolytic capacitor values up to 47 µF can be used.
10. When switching from Normal mode to Stop mode or from Stop mode to Normal mode, the voltage can vary within the output voltage specification.
11. When I_{DD} is above I_{DDS}, the 33689 enters the Reset mode.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
MISO SPI OUTPUT PIN					
Low-Level Output Voltage I_{OUT} = 1.5 mA	V_{OL}	0.0	—	1.0	V
High-Level Output Voltage I_{OUT} = 250 µA	V_{OH}	V_{DD} - 0.9	—	V_{DD}	V
Tri-Stated MISO Output Leakage Current 0.0 V < V_{MISO} < V_{DD}	I_{HZ}	-2.0	—	2.0	µA
MOSI, SCLK, $\overline{CS}$ SPI INPUT PINS					
Low-Level Input Voltage	V_{IL}	-0.3	—	0.3 V_{DD}	V
High-Level Input Voltage	V_{IH}	0.7 V_{DD}	—	V_{DD} +0.3	V
Pullup Input Current on $\overline{CS}$ $V_{\overline{CS}}$ = 4.0 V	$I_{PU\overline{CS}}$	-100	—	-20	µA
MOSI, SCLK Input Current 0.0 V < V_{IN} < V_{DD}	I_{IN}	-10	—	10	µA
$\overline{INT}$ OUTPUT PIN					
Low-Level Output Voltage I_O = 1.5 mA	V_{OL}	0.0	—	0.9	V
High-Level Output Voltage I_O = -250 µA	V_{OH}	V_{DD} - 0.9	—	V_{DD}	V
$\overline{WDC}$ PIN					
External Resistor Range	R_{EXT}	10	—	100	kΩ
HS1 AND HS2 HIGH-SIDE OUTPUT PINS					
Output Clamp Voltage I_{OUT} = -100 mA	V_{CL}	-6.0	—	—	V
Output Drain-to-Source ON Resistance T_A = 25°C, I_{OUT} -150 mA T_A = 125°C, I_{OUT} -150 mA T_A = 125°C, I_{OUT} -120 mA	$R_{DS(ON)}$	— — —	2.0 — 3.0	2.5 4.5 4.0	Ω
Output Current Limitation	I_{LIM}	300	430	600	mA
Overtemperature Shutdown (12)	T_{OTSD}	155	—	190	°C
Output Leakage Current	I_{LEAK}	—	—	10	µA

Notes

12. When overtemperature occurs, switch is turned off and latched off. Flag is set in SPI Register. Refer to description on page 26.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HS3 HIGH-SIDE OUTPUT PIN					
Output Drain-to-Source ON Resistance	$R_{DS(ON)}$				Ω
T_A = 25°C, I_{OUT} -50 mA		—	5.5	7.0	
T_A = 125°C, I_{OUT} -50 mA		—	—	10	
T_A = 125°C, I_{OUT} -30 mA		—	10	14	
Output Current Limitation	I_{LIM}	60	100	200	mA
Overtemperature Shutdown (13)	T_{OTSD}	155	—	190	°C
Output Leakage Current	I_{LEAK}	—	—	10	µA
OUT, E+, AND E- PINS AT CURRENT SENSE OPERATIONAL AMPLIFIER					
Input Voltage – Rail-to-Rail at E+ and E-	V_{IMC}	-0.1	—	V_{CC} +0.1	V
Output Voltage Range at OUT	V_{OUT}				V
With ±1.0 mA Output Load Current		0.1	—	V_{CC} -0.1	
With ±5.0 mA Output Load Current		0.3	—	V_{CC} -0.3	
Input Bias Current	I_B	—	—	250	nA
Input Offset Voltage	V_{IO}	-15	—	15	mV
Input Offset Current	I_O	-100	—	100	nA
L1 AND L2 INPUT PINS					
Low-Voltage Detection Input Threshold Voltage	V_{THL}				V
5.5 V < V_{SUP} < 6.0 V		2.0	2.5	3.0	
6.0 V < V_{SUP} < 18 V		2.5	3.0	3.5	
18 V < V_{SUP} < 27 V		2.7	3.2	3.7	
High-Voltage Detection Input Threshold Voltage	V_{THH}				V
5.5 V < V_{SUP} < 6.0 V		2.7	3.3	3.8	
6.0 V < V_{SUP} < 18 V		3.0	4.0	4.5	
18 V < V_{SUP} < 27 V		3.5	4.2	4.7	
Input Hysteresis	V_{HYS}				V
5.5 V < V_{SUP} < 27 V		0.5	—	1.3	
Input Current	I_{IN}				µA
-0.2 V < V_{IN} < 40 V		-10	—	10	

Notes

13. When overtemperature occurs, switch is turned off and latched off. Flag is set in SPI Register. Refer to description on page 26.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
RXD OUTPUT PIN (LIN PHYSICAL LAYER)					
Low-Level Output Voltage I_{OUT} ≤ 1.5 mA	V_{OL}	 0.0	 —	 0.9	V
High-Level Output Voltage I_{OUT} ≤ 250 µA	V_{OH}	 3.75	 —	 5.25	V
TXD INPUT PIN (LIN PHYSICAL LAYER)					
Low-Level Input Voltage	V_{IL}	—	—	1.5	V
High-Level Input Voltage	V_{IH}	3.5	—	—	V
Input Hysteresis	V_{INHYS}	50	145	300	mV
Pullup Current Source 1.0 V < V_{TXD} < 3.5 V	I_{PUTXD}	 -100	 —	 -20	µA
LIN PHYSICAL LAYER, TRANSCEIVER					
Transceiver Output Voltage Dominant State, TXD LOW, External Bus Pullup 500 Ω Recessive State, TXD HIGH, I_{OUT} = 1.0 µA	 V_{LINDOM} V_{LINREC}	 — V_{SUP}-1.0	 — —	 1.4 —	V
Pullup Resistor to VSUP In Normal Mode and in Sleep and Stop Modes When Not Disabled by SPI	R_{PU}	 20	 30	 47	kΩ
Pullup Current Source In Sleep and Stop Modes When Pullup Disabled by SPI	I_{PULIN}	 —	 1.3	 —	µA
Output Current Shutdown Threshold	I_{OUTSD}	50	75	150	mA
Leakage Output Current to GND VS1 and VS2 Disconnected, V_{LIN} = 18 V Recessive State, 8.0 V < V_{SUP} < 18 V, 8.0 V < V_{LIN} < 18 V GND Disconnected, V_{GND} = V_{SUP}, V_{LIN} = -18 V	$I_{BUSLEAK}$	 — 0.0 -1.0	 1.0 3.0 —	 10 20 1.0	 µA µA mA
LIN PHYSICAL LAYER, RECEIVER					
Receiver Input Threshold Voltage Dominant State, TXD HIGH, RXD LOW Recessive State, TXD HIGH, RXD HIGH Center (V_{BUSDOM}-V_{BUSREC})/2 Hysteresis (V_{BUSDOM}-V_{BUSREC})	 V_{BUSDOM} V_{BUSREC} V_{BUSCNT} V_{BUSHYS}	 0.0 0.6 0.475 —	 — — 0.5 —	 0.4 1.0 0.525 0.175	V_{SUP}
Bus Wake-Up Threshold	V_{BUSWU}	—	0.5	—	V_{SUP}

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE CHARACTERISTICS					
SPI Operation Frequency	f_{SPI}	0.25	—	4.0	MHz
SCLK Clock Period	t_{PSCLK}	250	—	N/A	ns
SCLK Clock High Time	t_{WSCLKH}	125	—	N/A	ns
SCLK Clock Low Time	t_{WSCLKL}	125	—	N/A	ns
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	t_{LEAD}	100	—	N/A	ns
Falling Edge of SCLK to $\overline{CS}$ Rising Edge	t_{LAG}	100	—	N/A	ns
MOSI to Falling Edge of SCLK (Data Setup Time)	$t_{SI(SU)}$	40	—	N/A	ns
Falling Edge of SCLK to MOSI (Data Hold Time)	$t_{SI(HOLD)}$	40	—	N/A	ns
MISO Rise Time (14) C_L = 220 pF	t_{RSO}	—	25	50	ns
MISO Fall Time (14) C_L = 220 pF	t_{FSO}	—	25	50	ns
Time from Falling or Rising Edge of $\overline{CS}$ to: (14) MISO Low Impedance (Enable) MISO High Impedance (Disable)	 $t_{SO(EN)}$ $t_{SO(DIS)}$	 0.0 0.0	 — —	 50 50	ns
Time from Rising Edge of SCLK to MISO Data Valid (14) 0.2 V_{DD} ≤ MISO ≥ 0.8 V_{DD}, C_L = 100 pF	t_{VALID}	0.0	—	50	ns
$\overline{RST}$ OUTPUT PIN IN NORMAL AND STOP MODES					
Reset Duration After VDD HIGH	$t_{DUR\overline{RST}}$	0.65	1.0	1.35	ms
$\overline{WDC}$ PIN					
Watchdog Period Accuracy Using an External Resistor (Excluding Resistor Tolerances) (15)	$ACC_{\overline{WDC}}$	-15	—	15	%
Watchdog Time Period (15) 10 kΩ External Resistor 100 kΩ External Resistor No External Resistor, $\overline{WDC}$ Open, Normal Mode	$t_{\overline{WDC}}$	 — — 107	 10.558 99.748 160	 — — 215	ms

Notes

14. Parameter guaranteed by design; however, it is not production tested.
15. Watchdog time period calculation formula: $t_{\overline{WDC}}$ = 0.991 * R + 0.648 (R in kΩ and $t_{\overline{WDC}}$ in ms).

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE OPERATIONAL AMPLIFIER					
Supply Voltage Rejection Ratio (16)	SVR	60	—	—	dB
Common Mode Rejection Ratio (16)	CMR	70	—	—	dB
Gain Bandwidth (16)	GBP	1.0	—	—	MHz
Output Slew Rate	SR	0.5	—	—	V/µs
Phase Margin	PHMO	40	—	—	deg.
Open Loop Gain (16)	OLG	—	85	—	dB
L1 AND L2 INPUT PINS					
Wake-Up Filter Time (16)	t_{WUF}	8.0	20	38	µs
STATE MACHINE TIMING					
Delay Between $\overline{CS}$ LOW-to-HIGH Transition (at End of SPI Stop Command) and Stop Mode Activation (16)	t_{STOP}				µs
Minimum Watchdog Period		1.4	—	5.0	
No Watchdog Selected		6.0	—	30	
Maximum Watchdog Period		12	—	50	
Interrupt Low-Level Duration	$t_{\overline{INT}}$	7.0	10	13	µs
Internal Oscillator Frequency Accuracy (All Modes, for Information Only)	f_{OSC}	-35	—	35	%
Normal Request Mode Time-Out (Normal Request Mode)	t_{NRTOUT}	97	150	205	ms
Delay Between SPI Command and HS1 or HS2 Turn On (17), (18)	t_{SHSON}				µs
Normal Mode, V_{SUP} > 9.0 V, V_{HS} ≥ 0.2 V_{VS2}		—	—	20	
Delay Between SPI Command and HS1 or HS2 Turn Off (17), (18)	t_{SHSOFF}				µs
Normal Mode, V_{SUP} > 9.0 V, V_{HS} ≤ 0.8 V_{VS2}		—	—	20	
Delay Between SPI Command and HS3 Turn On (17), (19)	t_{SHSON}				µs
Normal Mode, V_{SUP} > 9.0 V, V_{HS} ≥ 0.2 V_{VS2}		—	—	20	
Delay Between SPI Command and HS3 Turn Off (17), (19)	t_{SHSOFF}				µs
Normal Mode, V_{SUP} > 9.0 V, V_{HS} ≤ 0.8 V_{VS2}		—	—	20	
Delay Between Normal Request and Normal Mode After a Watchdog Trigger Command (Normal Request Mode) (16)	t_{SNR2N}	7.0	15	30	µs
Delay Between $\overline{CS}$ Wake-Up ($\overline{CS}$ LOW to HIGH) in Stop Mode and:					µs
Normal Request Mode, VDD ON and $\overline{RST}$ HIGH	$t_{WU\overline{CS}}$	15	40	80	
First Accepted SPI Command	t_{WUSPI}	90	—	N/A	
Delay Between Interrupt Pulse in Stop Mode After Wake-Up and First Accepted SPI Command	$t_{S1STSPI}$	30	—	N/A	µs
Minimum Time Between Rising and Falling Edge on the $\overline{CS}$	$t_{2\overline{CS}}$	15	—	—	µs

Notes

16. Parameter guaranteed by design; however, it is not production tested.
17. When IN input is set to HIGH, delay starts at falling edge of clock cycle #8 of the SPI command and start of device activation/deactivation. 30 mA load on high-side switches. Excluding rise or fall time due to external load.
18. When IN is used to control the high-side switches, delays are measured between IN and HS1 or HS2 ON/OFF. 30 mA load on high-side switches, excluding rise or fall time due to external load.
19. Delay between turn on or turn off command and HS ON or HS OFF, excluding rise or fall time due to external load.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER: BUS DRIVER TIMING CHARACTERISTICS FOR NORMAL SLEW RATE (20)					
Propagation Delay TXD to LIN (21)					µs
Dominant State Minimum Threshold (50% TXD to 58.1% V_{SUP})	t_{DOMMIN}	—	—	50	
Dominant State Maximum Threshold (50% TXD to 28.4% V_{SUP})	t_{DOMMAX}	—	—	50	
Recessive State Minimum Threshold (50% TXD to 42.2% V_{SUP})	t_{RECMIN}	—	—	50	
Recessive State Maximum Threshold (50% TXD to 74.4% V_{SUP})	t_{RECMAX}	—	—	50	
Propagation Delay Symmetry					µs
t_{DOMMIN} - t_{RECMAX}	dt1s	-10.44	—	—	
t_{DOMMAX} - t_{RECMIN}	dt2s	—	—	11	
LIN PHYSICAL LAYER: BUS DRIVER TIMING CHARACTERISTICS FOR SLOW SLEW RATE (20)					
Propagation Delay TXD to LIN (22)					µs
Dominant State Minimum Threshold (50% TXD to 61.6% V_{SUP})	t_{DOMMIN}	—	—	100	
Dominant State Maximum Threshold (50% TXD to 25.1% V_{SUP})	t_{DOMMAX}	—	—	100	
Recessive State Minimum Threshold (50% TXD to 38.9% V_{SUP})	t_{RECMIN}	—	—	100	
Recessive State Maximum Threshold (50% TXD to 77.8% V_{SUP})	t_{RECMAX}	—	—	100	
Propagation Delay Symmetry					µs
t_{DOMMIN} - t_{RECMAX}	dt1s	-22	—	—	
t_{DOMMAX} - t_{RECMIN}	dt2s	—	—	23	
LIN PHYSICAL LAYER: BUS DRIVER FAST SLEW RATE					
LIN High Slew Rate (Programming Mode)	dv/dt Fast	—	13	—	V/µs
LIN PHYSICAL LAYER, TRANSCEIVER					
Output Current Shutdown Delay (23)	t_{OUTDLY}	—	10	—	µs

Notes

20. 7.0 V < V_{SUP} < 18 V, bus load C0 and R0 1.0 nF/1.0 kΩ, 6.8 nF/660 Ω, 10 nF/500 Ω. 50% of TXD signal to LIN signal threshold. See Figure 5, page 16.
21. See Figure 7, page 17.
22. See Figure 8, page 17.
23. Parameter guaranteed by design; however, it is not production tested.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER: RECEIVER CHARACTERISTICS AND WAKE-UP TIMINGS					
Propagation Delay LIN to RXD (24)					µs
Dominant State (LIN LOW to RXD LOW)	t_{RDOM}	—	3.0	6.0	
Recessive State (LIN HIGH to RXD HIGH)	t_{RREC}	—	3.0	6.0	
Symmetry (t_{RDOM} - t_{RREC})	t_{RSYM}	-2.0	—	2.0	
Bus Wake-Up Deglitcher (Sleep and Stop Modes) (25)	t_{PROPWL}	30	70	90	µs
Bus Wake-Up Event Reported					µs
From Sleep Mode (26)	t_{WU}	—	30	—	
From Stop Mode (27)	t_{WU}	—	20	—	

Notes

24. Measured between LIN signal threshold V_{INL} or V_{INH} and 50% of RXD signal.
25. See Figures 9 and 10, page 18.
26. t_{WU} is typically 2 internal clock cycles after a LIN rising edge is detected. In Sleep Mode, the measurement is done without a capacitor connected to the regulator. The delay is measured between the V_{SUP}/2 rising edge of the LIN bus and when V_{DD} reaches 3.0 V. The V_{DD} rise time is strongly dependent upon the decoupling capacitor at V_{DD} pin. See Figure 9, page 18.
27. t_{WU} is typically 2 internal clock cycles after a LIN rising edge is detected. In Stop Mode, the delay is measured between the V_{SUP}/2 rising edge of the LIN bus and the falling edge of the $\overline{INT}$ pin. See Figure 10, page 18.

TIMING DIAGRAMS

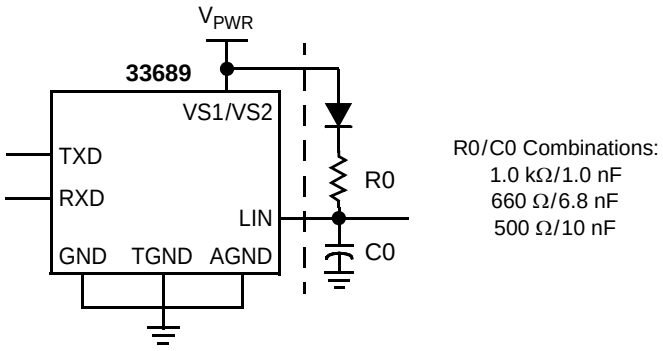
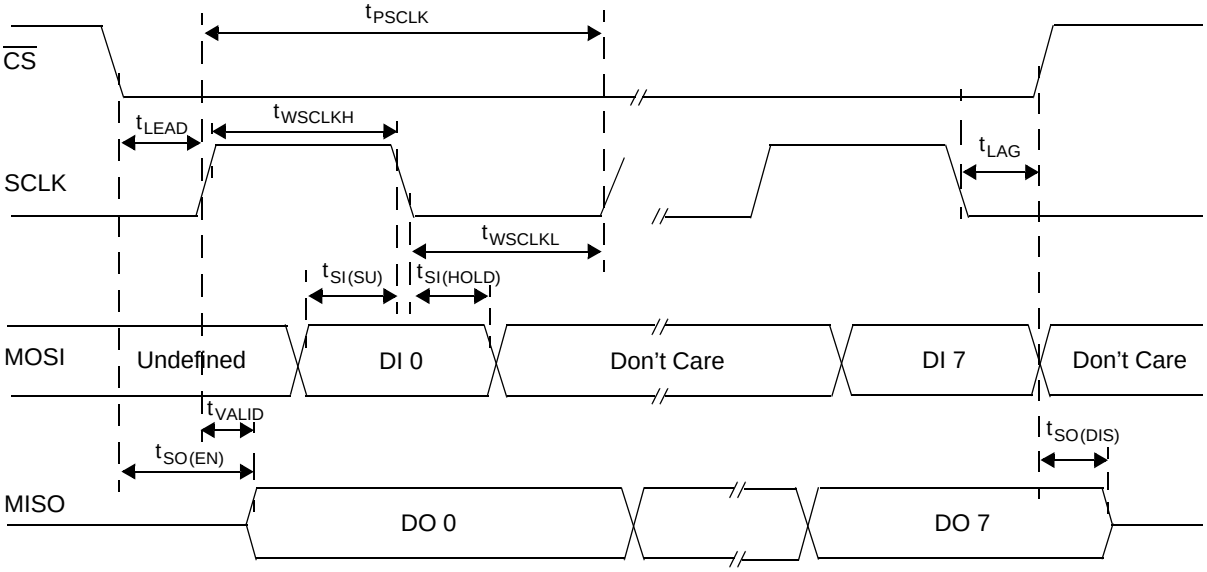


Figure 5. Test Circuit for Timing Measurements



Note Incoming data at MOSI pin is sampled by the 33689 at SCLK falling edge. Outgoing data at MISO is set by the 33689 at SCLK rising edge (after t_{VALID} delay time).

Figure 6. SPI Timing Characteristics

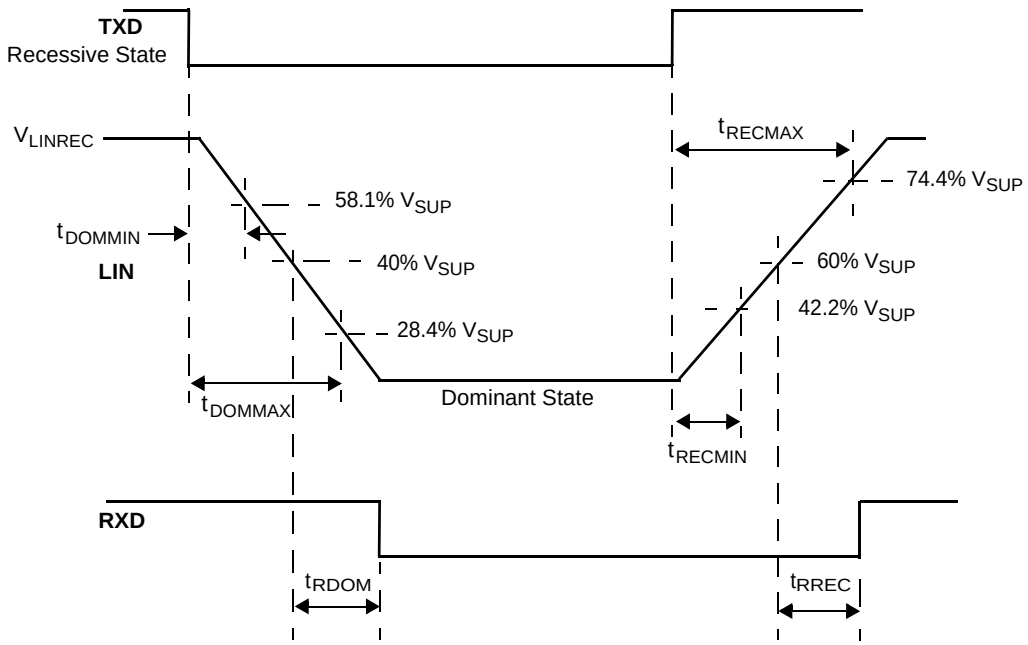


Figure 7. Timing Characteristics for Normal LIN Output Slew Rate

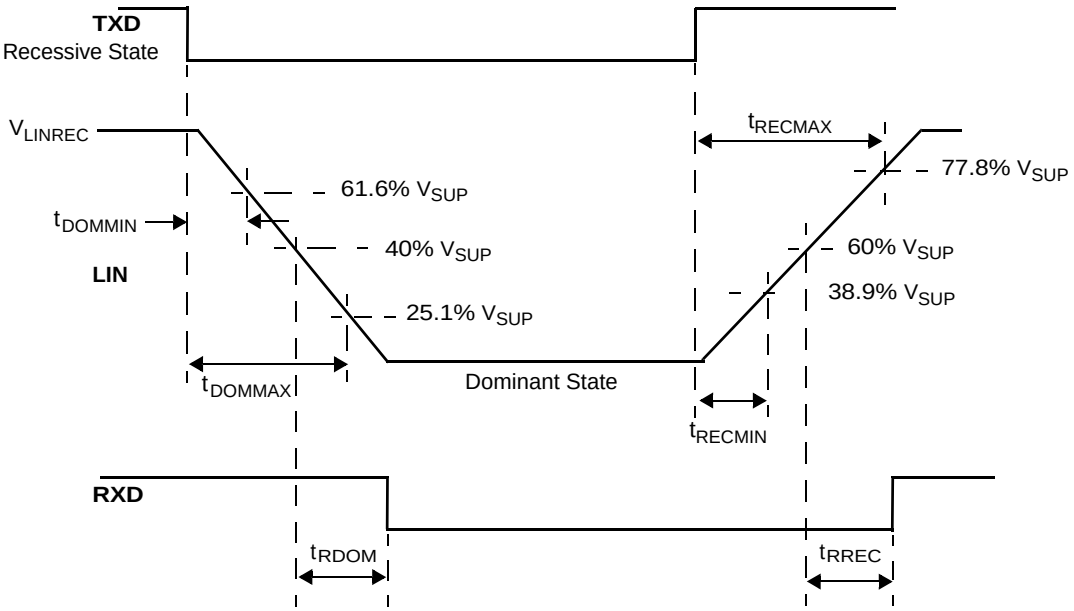


Figure 8. Timing Characteristics for Slow LIN Output Slew Rate

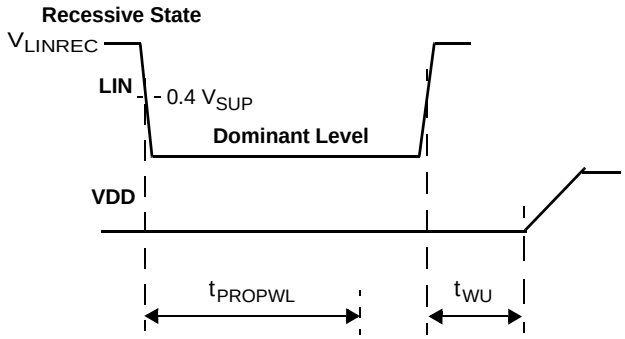


Figure 9. LIN Bus Wake-Up Behavior, Sleep Mode

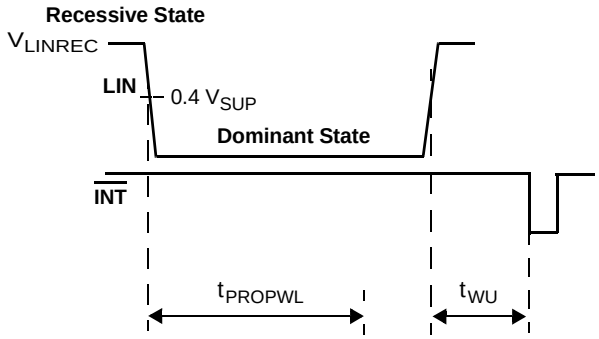


Figure 10. LIN Bus Wake-Up Behavior, Stop Mode

FUNCTIONAL DESCRIPTION

INTRODUCTION

A System Basis Chip (SBC) is a monolithic IC combining many functions found in standard microcontroller-based systems; e.g., power management, communication interface, system protection, and diagnostics.

The 33689 is a SPI-controlled SBC combining many functions with a LIN transceiver for slave node applications. The 33689 has a 5.0 V, 50 mA regulator with undervoltage reset, output current limiting, overtemperature pre-warning, and thermal shutdown. An externally selectable timing Window Watchdog is also included.

The LIN transceiver has waveshaping that can be disabled when high data rates are warranted. A single 50 mA and two 150 mA fully protected high-side switches with output clamping are available for switching inductive or resistive loads. The 150 mA switches are PWM capable.

Two high-voltage inputs can be used to monitor switches or provide external wake-up. An internal current sense operational amplifier is available for load current monitoring.

FUNCTIONAL PIN DESCRIPTION

LEVEL 1 AND LEVEL 2 INPUT PINS (L1 AND L2)

These pins are used to sense external switches and to wake up the 33689 from Sleep or Stop mode. During Normal mode, the state of these pins can be read through the SPI Register. (Refer to the section entitled SPI Interface and Register Description on page 24 for information on the SPI Register.)

HIGH-SIDE DRIVER OUTPUT PINS 1 AND 2 (HS1 AND HS2)

These two high-side switches are able to drive loads such as relays or lamps. They are protected against overcurrent and overtemperature and include internal clamp circuitry for inductive load protection. Switch control is done through selecting the correct bit in the SPI Register. HS1 and HS2 can be PWM-ed if required through the IN input pin. The internal circuitry that drives both high-side switches is an AND function between the SPI bit HS1 (or HS2) and the IN input pin.

If no PWM control is required, the IN pin must be connected to the VDD pin.

HIGH-SIDE DRIVER OUTPUT PIN 3 (HS3)

This high-side switch can be used to drive small lamps, Hall sensors, or switch pullup resistors. Control is done through the SPI Register only.

No direct PWM control is possible on this pin.

This high-side switch features current limit to protect it against overcurrent and short circuit conditions. It is also protected against overtemperature.

VOLTAGE SUPPLY PINS 1 AND 2 (VS1 AND VS2)

The 33689 is supplied from a battery line or other supply source through the VS1 and VS2 pins. An external diode is required to protect against negative transients and reverse battery. The 33689 can operate from 4.5 V and under the jump start condition at 27 V DC. Device functionality is guaranteed down to 4.5 V at VS1 and VS2 pins. These pins sustain standard automotive voltage conditions such as load dump at 40 V.

LIN BUS PIN (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

VOLTAGE SOURCE PIN (VDD)

The VDD pin is the 5.0 V supply pin for the MCU and the current sense operational amplifier.

CURRENT SENSE OPERATIONAL AMPLIFIER PINS (E+, E-, VCC, AND OUT)

These are the pins of the single-supply current sense operational amplifier.

- The E+ and the E- input pins are the non-inverting and inverting inputs of the current sense operational amplifier, respectively.
- The OUT pin is the output pin of the current sense operational amplifier.
- The VCC pin is the +5.0 V single-supply connection for the current sense operational amplifier.

The current sense operational amplifier is enabled in Normal mode only.

WATCHDOG CONFIGURATION PIN ($\overline{\text{WDC}}$)

The $\overline{\text{WDC}}$ pin is the configuration pin for the internal watchdog. A resistor is connected to this pin. The resistor value defines the watchdog period. If the pin is left open, the watchdog period is fixed to its default value (150 ms typical). If no watchdog function is required, the $\overline{\text{WDC}}$ pin must be connected to GND.

RESET OUTPUT PIN ($\overline{\text{RST}}$)

The $\overline{\text{RST}}$ pin is the 5.0 V regulator and Watchdog reset output pin.

PWM INPUT CONTROL PIN (IN)

The IN pin is the external PWM control pin for the HS1 and HS2 high-side switches.

SERIAL DATA CLOCK PIN (SCLK)

The SCLK pin is the SPI clock input pin. MISO data changes on the negative transition of the SCLK. MOSI is sampled on the positive edge of the SCLK.

MASTER OUT SLAVE IN PIN (MOSI)

The MOSI pin receives SPI data from the MCU. This data input is sampled on the positive edge of SCLK.

MASTER IN SLAVE OUT PIN (MISO)

The MISO pin sends data to an SPI-enabled MCU. Data on this output pin changes on the negative edge of the SCLK. When $\overline{\text{CS}}$ is HIGH, this pin enters the high-impedance state.

CHIP SELECT PIN ($\overline{\text{CS}}$)

The $\overline{\text{CS}}$ pin is the chip select input pin for SPI use. When this signal is high, SPI signals are ignored. Asserting this pin LOW starts an SPI transaction. The transaction is completed when this signal returns HIGH.

INTERRUPT OUTPUT PIN ($\overline{\text{INT}}$)

The $\overline{\text{INT}}$ pin is used to report 33689 faults to the MCU. Interrupt pulses are generated for:

- Voltage regulator temperature pre-warning
- HS1, HS2, or HS3 thermal shutdown
- VS1 or VS2 overvoltage (20V typical)
- VS1 or VS2 undervoltage (6.0V typical)

If an interrupt is generated, then when the next SPI read operation is performed bit D7 in the SPI Register will be set to logic [1] and bits D6:D0 will report the interrupt source.

In cases of wake-up from the Stop mode, $\overline{\text{INT}}$ is set LOW in order to signal to the MCU that a wake-up event from the L1, L2, or LIN bus pin has occurred.

RECEIVER OUTPUT PIN (RXD)

The RXD pin is the receiver output of the LIN interface and reports the state of the bus voltage (RXD LOW when LIN bus is dominant, RXD HIGH when LIN bus is recessive).

TRANSMITTER INPUT PIN (TXD)

The TXD pin is the transmitter input of the LIN interface and controls the state of the bus output (dominant when TXD is LOW, recessive when TXD is HIGH).

GROUND PINS (GND, TGND, AND AGND)

The 33689 has three different types of ground pins.

- The GND pin is the electrical ground pin for the device.
- The AGND is the analog ground pin for the voltage regulator and current sense operational amplifier.
- The four TGND pins are the thermal ground pins for the device.

Important The GND, the AGND, and the four TGND pins must be connected together to a ground external to the 33689.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

WINDOW WATCHDOG

The window watchdog can be configured using an external resistor at $\overline{WDC}$ pin. The watchdog is cleared through MODE1 and MODE2 bit in the SPI Register (refer to Table 2, page 24; also refer to the section entitled Functional Pin Description on page 19.

A watchdog clear is only allowed in the open window (see Figure 1). If the watchdog is cleared in the closed window or has not been cleared at the end of the open window, the watchdog will generate a reset on the $\overline{RST}$ pin and reset the whole device.

Note The watchdog clear in Normal request mode (150 ms) (first watchdog clear) has no window.

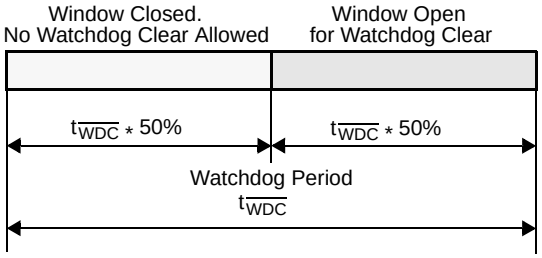


Figure 1. Window Watchdog Operation

Window Watchdog Configuration

If the $\overline{WDC}$ pin is left open, the default watchdog period is selected (typ. 150 ms). If no watchdog function is required, the $\overline{WDC}$ pin must be connected to GND.

The watchdog timer's period is calculated using the following formula:

$t_{\overline{WDC}} = 0.991 * R + 0.648$ (with R in kΩ and $t_{\overline{WDC}}$ in ms).

VDD VOLTAGE REGULATOR

The 33689 chip contains a low-power, low dropout voltage regulator to provide internal power and external power for the MCU. The on-chip regulator consist of two elements, the main voltage regulator and the low-voltage reset circuit.

The VDD regulator accepts an unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD pin to provide the 5.0 V to the microcontroller.

Current Limit (Overcurrent) Protection

The voltage regulator has current limit to protect the device against overcurrent and short circuit conditions.

Overtemperature Protection

The voltage regulator also features overtemperature protection that has an overtemperature warning (Interrupt - VDDT) and an overtemperature shutdown.

Stop Mode

During Stop mode, the Stop mode regulator supplies a regulated output voltage. The Stop mode regulator has a limited output current capability.

Sleep Mode

In Sleep mode, the voltage regulator external VDD is turned off.

VDD VOLTAGE REGULATOR TEMPERATURE PREWARNING

VDD voltage regulator temperature prewarning (VDDT) is generated if the voltage regulator temperature is above the T_{PRE} threshold. It will set the VDDT bit in the SPI Register and an interrupt will be initiated. The VDDT bit remains set as long as the error condition is present.

During Sleep and Stop modes the VDD voltage regulator temperature prewarning circuitry is disabled.

HIGH-SIDE SWITCH THERMAL SHUTDOWN

The high-side switch thermal shutdown HSST is generated if one of the high-side switches HS1:HS3 is above the HSST threshold. It will shutdown all high-side switches and set the HSST flag in the SPI Register, and an interrupt will be initiated. The HSST bit remains set as long as the error condition is present. During Sleep and Stop modes the high-side switch thermal shutdown circuitry is disabled.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

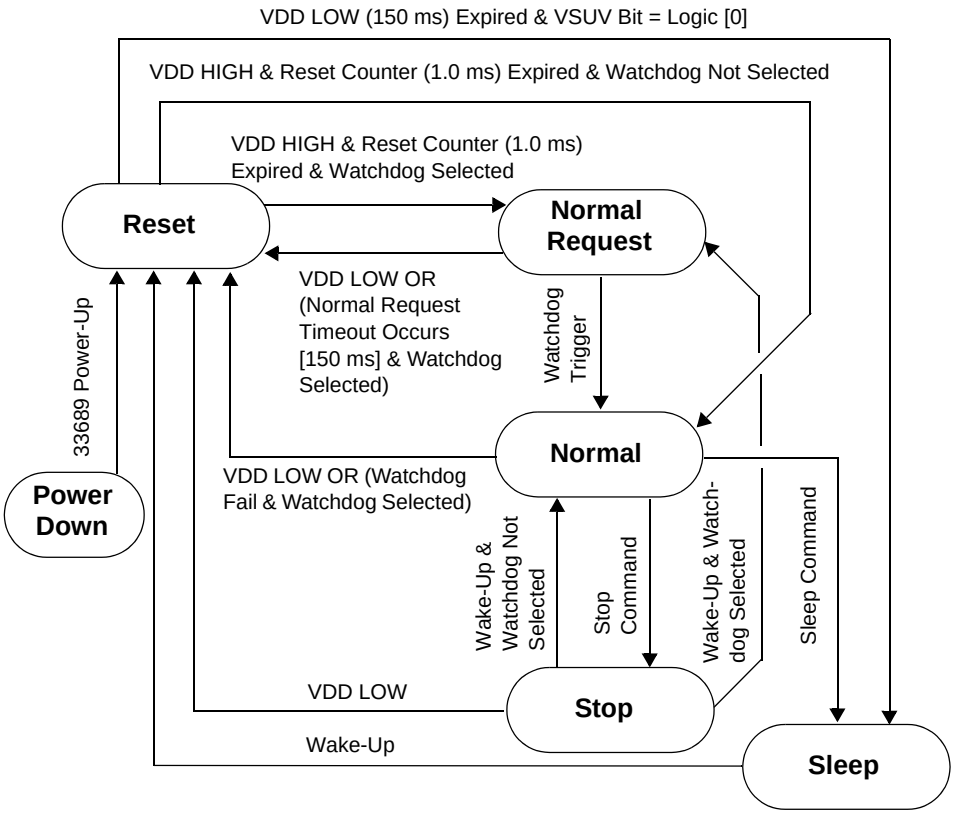
As described below and depicted in Figure 1 below and Table 1 on page 23, the 33689 has three operational modes: Normal, Sleep, and Stop. Operational modes are controlled by MODE1 and MODE2 bits in the SPI Register (refer to Logic Commands and Registers on page 24). In additional, there are two transitional modes: Reset and Normal Request.

RESET MODE

At power up, the 33689 switches automatically to Reset Mode for 1 ms if V_{DD} goes high. If V_{DD} stays low, after 150 ms the 33689 goes in Sleep Mode.

NORMAL REQUEST MODE

Before entering in Normal Request Mode, the 33689 stays for 1 ms in Reset Mode. In this mode, the LIN bus can transmit and receive information.



Legend
Watchdog Selected: External resistor between $\overline{WDC}$ pin and GND or $\overline{WDC}$ pin open.
Watchdog Not Selected: $\overline{WDC}$ pin connected to GND.
Watchdog Fail: Watchdog trigger occurs in closed window or no SPI Watchdog trigger command.
Stop Command: SPI stop command.
Sleep Command: SPI sleep request followed by SPI sleep command.
Wake-Up: L1 or L2 state change or LIN bus wake-up or $\overline{CS}$ rising edge.

Figure 1. 33689 Modes State Diagram

NORMAL MODE

In Normal Mode, the 33689 has slew rate and timing compatible with the LIN protocol specification. The LIN bus can transmit and receive information. The V_{DD} regulator is ON and the watchdog function can be enabled.

SLEEP AND STOP MODE

To safely enter Sleep or Stop modes and to ensure that these modes are not inadvertently entered due to noise issues during SPI transmission, a dedicated sequence must be sent twice: data with the bits controlling the LIN bus and the device mode.

Entering Sleep Mode

First and second SPI commands (with bit D6=1, D7=1, D5 =0 or 1, D1=0, and D0=0) 11x00000 must be sent.

Entering Stop Mode

First and second SPI commands (with bit D6=1, D7=1, D5 =0 or 1, D1=0, and D0=1) 11x00001 must be sent.

Sleep or Stop modes are entered after the second SPI command. Register bit D5 must be set accordingly.

Table 1. Operational Modes and Associated Functions

Device Mode	VDD Voltage Regulator	Wake-Up Capabilities	$\overline{\text{RST}}$ Output	Watchdog Function	HS1, HS2, HS3	LIN Interface	Operational Amplifier
Reset	VDD: ON	N/A	LOW for 1.0 ms typical, then HIGH (if VDD above threshold)	Disabled	OFF	Recessive only	Not active
Normal Request	VDD: ON	N/A	HIGH. Active LOW if VDD undervoltage occurs and if Normal Request timeout (if Watchdog enabled)	150 ms timeout if Watchdog enabled	ON or OFF	Transmit and receive	Not active
Normal	VDD: ON	N/A	HIGH. Active LOW if VDD undervoltage occurs or if Watchdog fail (if Watchdog enabled)	Window Watchdog if enabled	ON or OFF	Transmit and receive	Active
Stop	VDD: ON (Limited current capability)	LIN and state change on L1:L2 inputs	Normally HIGH. Active LOW if VDD undervoltage occurs	Disabled	OFF	Recessive state with Wake capability	Not active
Sleep	VDD: OFF (Set to 5.0 V after Wake-Up to enter Normal Request)	LIN and state change on L1:L2 inputs	LOW. Go to HIGH after Wake-Up and VDD within specification	Disabled	OFF	Recessive state with Wake capability	Not active

LOGIC COMMANDS AND REGISTERS

SPI INTERFACE AND REGISTER DESCRIPTION

As shown in Figure 2, the SPI is an 8-bit SPI. All data is sent as bytes. The MSB, D7, is sent first. The minimum time between two rising edges on the $\overline{CS}$ pin is 15 μs.

During an SPI data communication, the state of MISO reports the state of the 33689 at time of a $\overline{CS}$ HIGH-to-LOW transition. The status flags are latched at a $\overline{CS}$ HIGH-to-LOW transition.

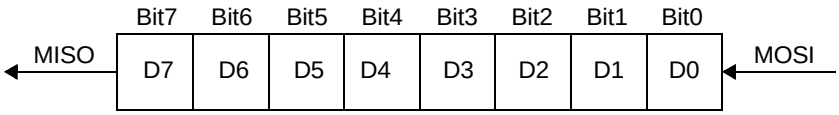


Figure 2. Data Format Description

The following tables describe the SPI Register bits, showing reset values and reset conditions.

Table 2. SPI Register Overview

Read/Write Information	MSB			Bits				LSB
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Write	LINSL2	LINSL1	LIN-PU	HS3	HS2	HS1	MODE2	MODE1
Read	INTSRC (1)	LINWU or LINFAIL	VSOV	VSUV or BATFAIL (2)	VDDT	HSST	L2	L1
Write Reset Value	0	0	0	0	0	0	—	—
Write Reset Condition	POR, RESET	POR, RESET	POR	POR, RESET	POR, RESET	POR, RESET	—	—

Notes
1. D7 signals interrupt source. After interrupt occurs, if D7 is a logic [1] D6:D0 indicate the interrupt source. If D7 is a logic [0] no interrupt has occurred and D6:D0 report real-time status.
2. The first SPI read after a 33689 reset returns the BATFAIL status flag bit D4.

SPI Register: Write Control Bits

LINSL2 and LINSL1—LIN Baud Rate and Low-Power Mode Pre-Selection Bits

These bits select the LIN slew rate and requested low-power mode in accordance with Table 3. Reset clears the LINSL2:1 bits.

Table 3. LIN Slew Rate Control and Device Low Power Mode Pre-Selection Bits (D7 and D6)

LINSL2	LINSL1	Description
0	0	LIN slew rate normal (baud rate up to 20 kbps)
0	1	LIN slew rate slow (baud rate up to 10 kbps)
1	0	LIN slew rate fast (for program download, baud rate up to 100 kbps)
1	1	Low power mode (Sleep or Stop mode) request, no change in LIN slew rate

LIN-PU—LIN Pullup Enable Bit

This bit controls the LIN pullup resistor during Sleep and Stop modes in accordance with Table 4. Reset clears the LIN-PU bit.

Table 4. LIN Pullup Termination Control Bit (D5)

LIN-PU	Description
0	30 kΩ pullup connected in Sleep and Stop mode
1	30 kΩ pullup disconnected in Sleep and Stop mode

HS3:HS1—High-Side H3:HS1 Enable Bits

These bits enable the HS3:HS1 bits in accordance with Table 5. Reset clears the HSx bit.

Note If no PWM on HS1 and HS2 is required, the IN pin must be connected to the VDD pin.

Table 5. High-Side Switches Control Bits (D4, D3, and D2)

HS3	Description	HS2	Description	HS1	Description
0	HS3 OFF	0	HS2 OFF	0	HS1 OFF
1	HS3 ON	1	HS2 ON (if IN = 1)	1	HS1 ON (if IN = 1)

MODE2 and MODE1—Mode Section Bits

The MODE2 and MODE1 bits control the 33689 operating modes in accordance with Table 6.

Table 6. Mode Control Bits (D1 and D0)

MODE2	MODE1	Description
0	0	Sleep mode (3)
0	1	Stop mode
1	0	Normal mode + Watchdog clear (4)
1	1	Normal mode

Notes

3. Special SPI command and sequence is implemented in order to avoid going into Sleep or Stop mode with a single 8-bit SPI command. Refer to Tables 7 and 8.
4. When a logic [0] is written to MODE1 bit while MODE2 bit is written as a logic [1]. After the SPI command is completed, MODE1 bit is set to logic [1] and the 33689 stays in Normal mode. In order to set the 33689 in Sleep mode, both MODE1 and MODE2 bits must be written in the same 8-bit SPI command. The Watchdog clear on Normal Request mode (150 ms) has no window.

To safely enter Sleep or Stop mode and to ensure that these modes are not affected by noise issue during SPI transmission, the Sleep/Stop commands require two SPI transmissions.

Sleep Mode Sequence The Sleep command, as shown in Table 7, must be sent twice.

Table 7. Sleep Command Bits

LINSL2	LINSL1	LIN-PU	HS3	HS2	HS1	MODE2	MODE1
1	1	x	0	0	0	0	0

x = Don't care.

Stop Mode Sequence The Stop command, as shown in Table 8, must be sent twice.

Table 8. Stop Command Bits

LINSL2	LINSL1	LIN-PU	HS3	HS2	HS1	MODE2	MODE1
1	1	x	0	0	0	0	1

x = Don't care.

SPI Register: Read Control Bits

INTSCR—Register Content Flags or Interrupt Source

The INTSCR bit, as shown in Table 9, indicates if the register contents reflect the flags or an interrupt/wake-up source.

Table 9. Interrupt Status (D7)

INTSCR	Description
0	SPI word read reflects the flag state
1	SPI word read reflects the interrupt or wake-up source

LINWU/LINFAIL—LIN Bus Status Flag Bit

This bit indicates a LIN wake-up condition or a LIN overcurrent/overtemperature in accordance with Table 10.

Table 10. LIN Bus Status (D6)

LINWU/ LINFAIL	Description
0	No LIN bus wake-up **or** failure
1	LIN bus wake-up occurred or LIN overcurrent/ overtemperature

VSOV—Overvoltage Flag Bit, VSUV/BATFAIL—Undervoltage Flag Bit, VDDT—VDD Voltage Regulator Status Flag Bit, and HSST—High-Side Status Flag Bit

Table 11 indicates the register contents of the following flags:

- VSOV flag is set on an overvoltage condition.
- VSUV/BATFAIL flag is set on an undervoltage condition.
- VDDT flag is set as pre-warning in case of an overtemperature condition on the voltage regulator.
- HSST flag is set on overtemperature conditions on one of the high-side outputs.

Table 11. Over- and Undervoltage, VDD Voltage Regulator, and High-Side Status Flag Bits (D5, D4, D3, and D2)

VSOV	Description	VSUV/ BATFAIL	Description	VDDT	Description	HSST	Description
0	V_{SUP} below 19 V	0	V_{SUP} above 6.0 V	0	No overtemperature	0	HS No overtemperature
1	V_{SUP} above 18 V	1	V_{SUP} below 6.0 V	1	VDD overtemperature pre-warning	1	HS1, HS2, or HS3 OFF (overtemperature)

L2 and L1—Wake-Up Inputs L2 and L1 Status Flag Bit

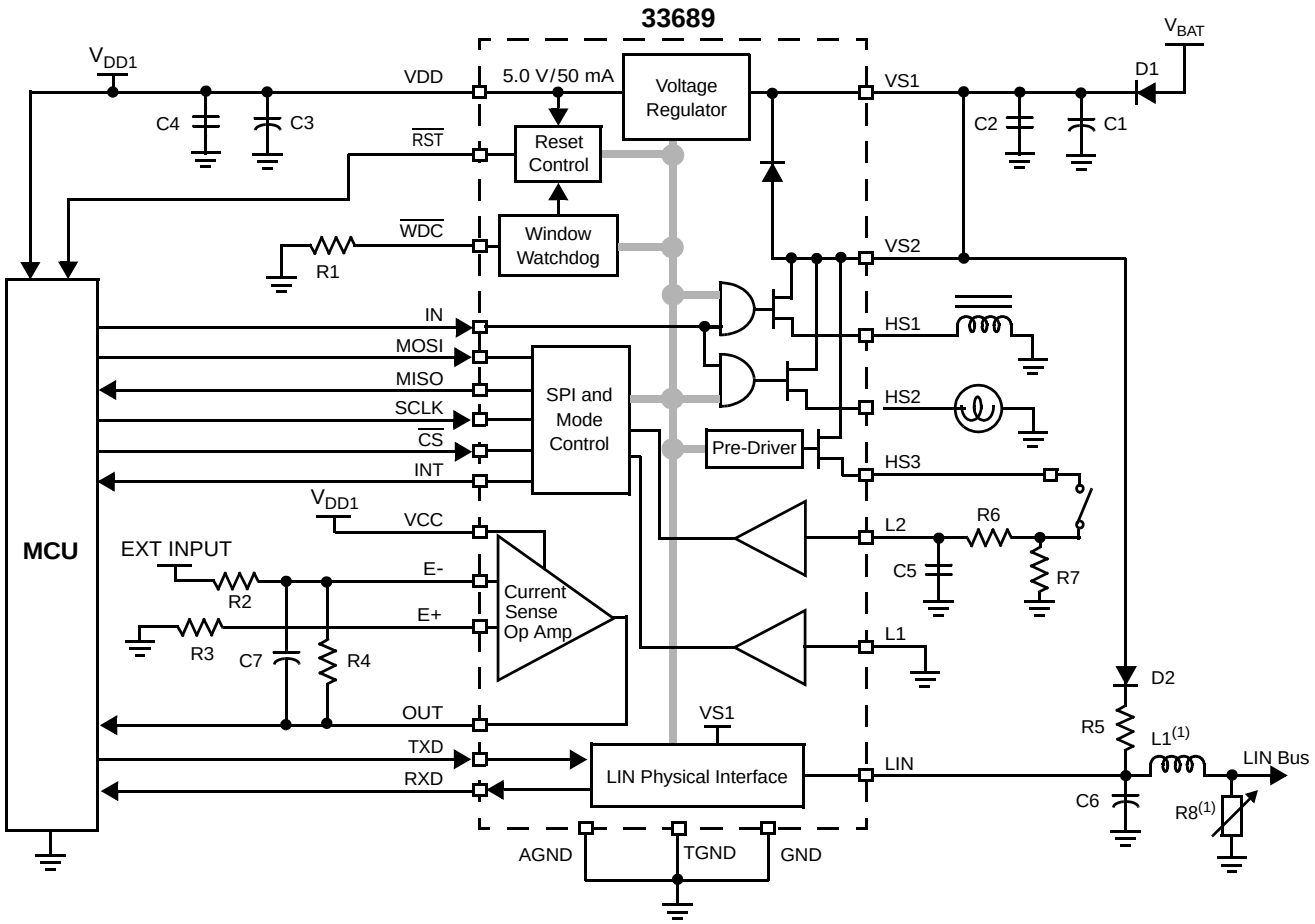
The L2 and L1 flags, as shown in Table 12, reflect the status of the L2 and L1 input pins and indicate the wake-up source.

Table 12. Switch Input Wake-Up and Real Time Status (D1 and D0)

L2	Description	L1	Description
0	L2 input LOW	0	L1 input LOW
1	L2 input HIGH or wake-up by L2 (first register read after wake-up)	1	L1 input HIGH or wake-up by L1 (first register read after wake-up)

TYPICAL APPLICATIONS

The 33689 can be configured in several applications. Figure 3 shows the 33689 in the typical master node application.



Component Values

C1=47 µF	R1=33 kΩ
C2=C4=C5=100 nF	R2 and R3 depend on the application
C3=10 µF	R4>5.0 kΩ
C6=220 pF	R5=1.0 kΩ
C7=4.7 nF	R6=10 kΩ
	R7=2.2 kΩ
	R8=Varistor type TDK AVR-M1608C270MBAAB(1)
	L1 = SMD Ferrite Bead-Type TDK MMZ2012Y202B(1)

Notes:

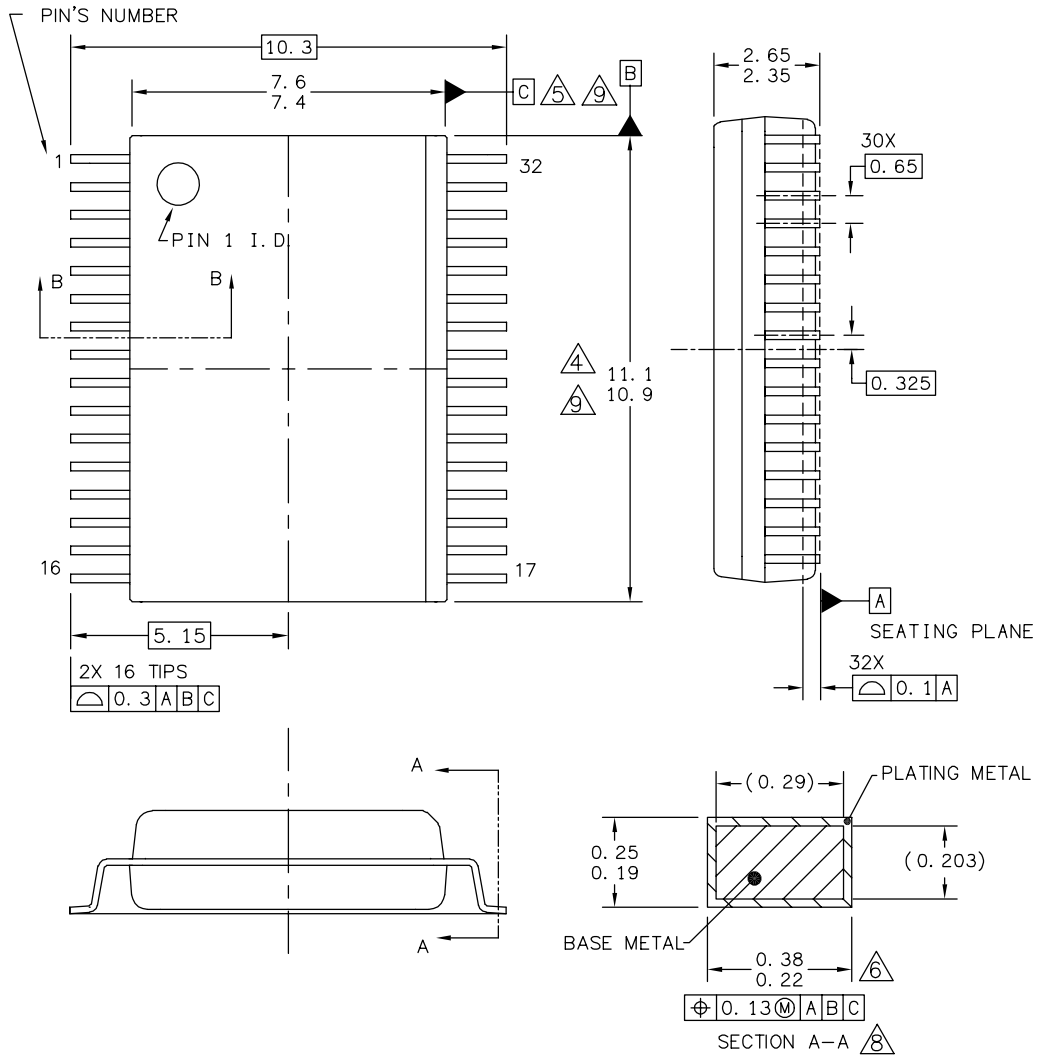
1. L1 and R8 are external components to improve EMC and ESD performances.
2. Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

Figure 3. 33689 in Typical Master Node Application

PACKAGING

PACKAGING DIMENSIONS

Important For the most current revision of the package, visit www.freescale.com and do a keyword search on the 98A drawing number below.



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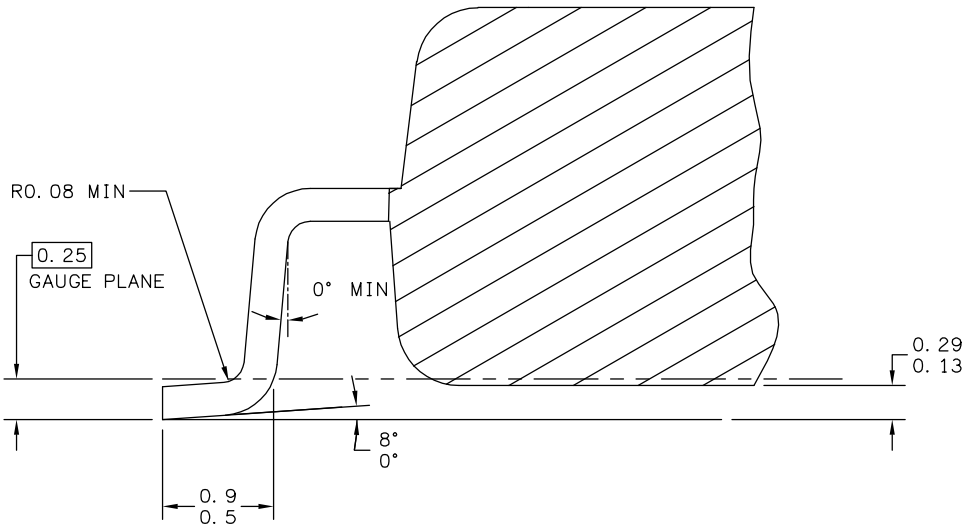
TITLE: 32LD SOIC W/B, 0.65 PITCH CASE OUTLINE	DOCUMENT NO: 98ARH99137A	REV: B
	CASE NUMBER: 1324–03	07 APR 2005
	STANDARD: FREESCALE	

DWB SUFFIX
EW SUFFIX (Pb-FREE)
32-PIN SOIC WIDE BODY
PLASTIC PACKAGE
98ARH99137A
ISSUE B

33689

PACKAGING DIMENSIONS (CONTINUED)



SECTION B–B

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	CASE NUMBER: 1324-03	07 APR 2005
	STANDARD: FREESCALE	

DWB SUFFIX
EW SUFFIX (Pb-FREE)
32-PIN SOIC WIDE BODY
PLASTIC PACKAGE
98ARH99137A
ISSUE B

33689

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
6.0	6/2006	• Implemented Revision History page • Updated Outline Drawing to Revision “B” • Eliminated all pages (pages 30 to 47) referring to the MC33689DWB/R2 device • Removed MC33689DWB/R2 from the orderable parts information • Updated to the prevailing form and style
7.0	8/2006	• Removed MC33689DEW/R2 and replaced with MCZ33689DEW/R2 in the Ordering Information block

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