

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# HD74LS83A

## 4-bit Binary Full Adder (with Fast Carry)

REJ03D0420-0200

Rev.2.00

Feb.18.2005

This improved full adder performs the addition of two 4-bit binary numbers. The sum ( $\Sigma$ ) outputs are provided for each bit and the resultant carry ( $C_4$ ) is obtained from the fourth bit. This adder features full internal look ahead across all four bit generating the carry term in ten nanoseconds typically. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

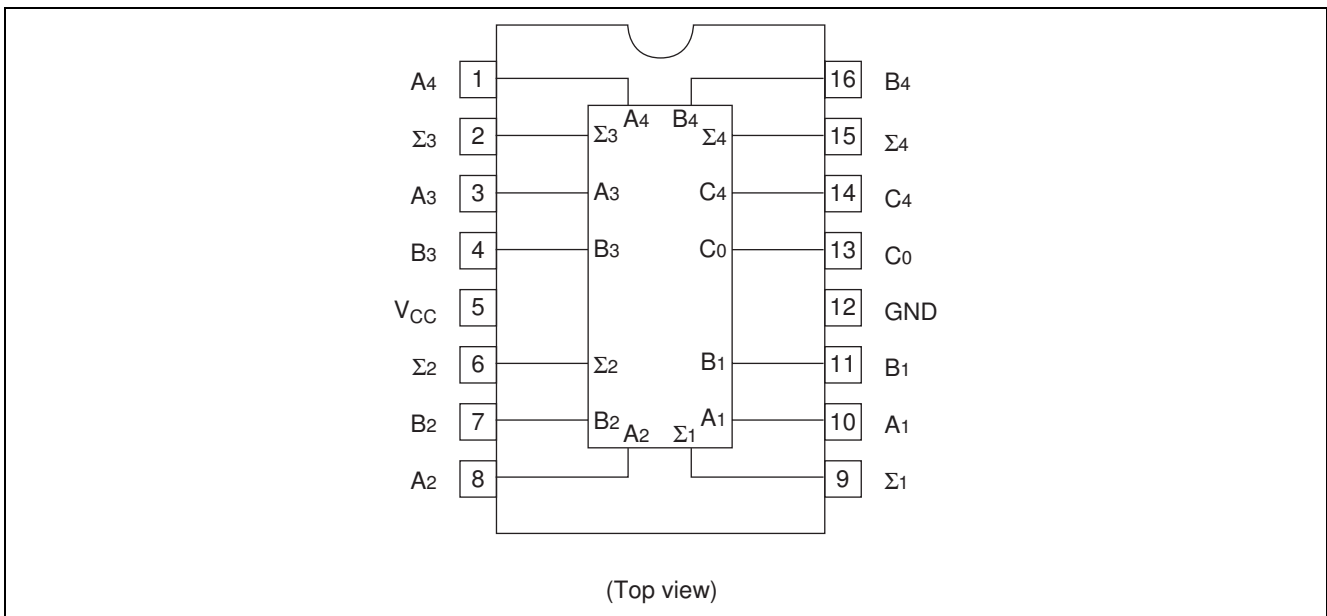
### Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS83AP	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—

Note: Please consult the sales office for the above package availability.

### Pin Arrangement



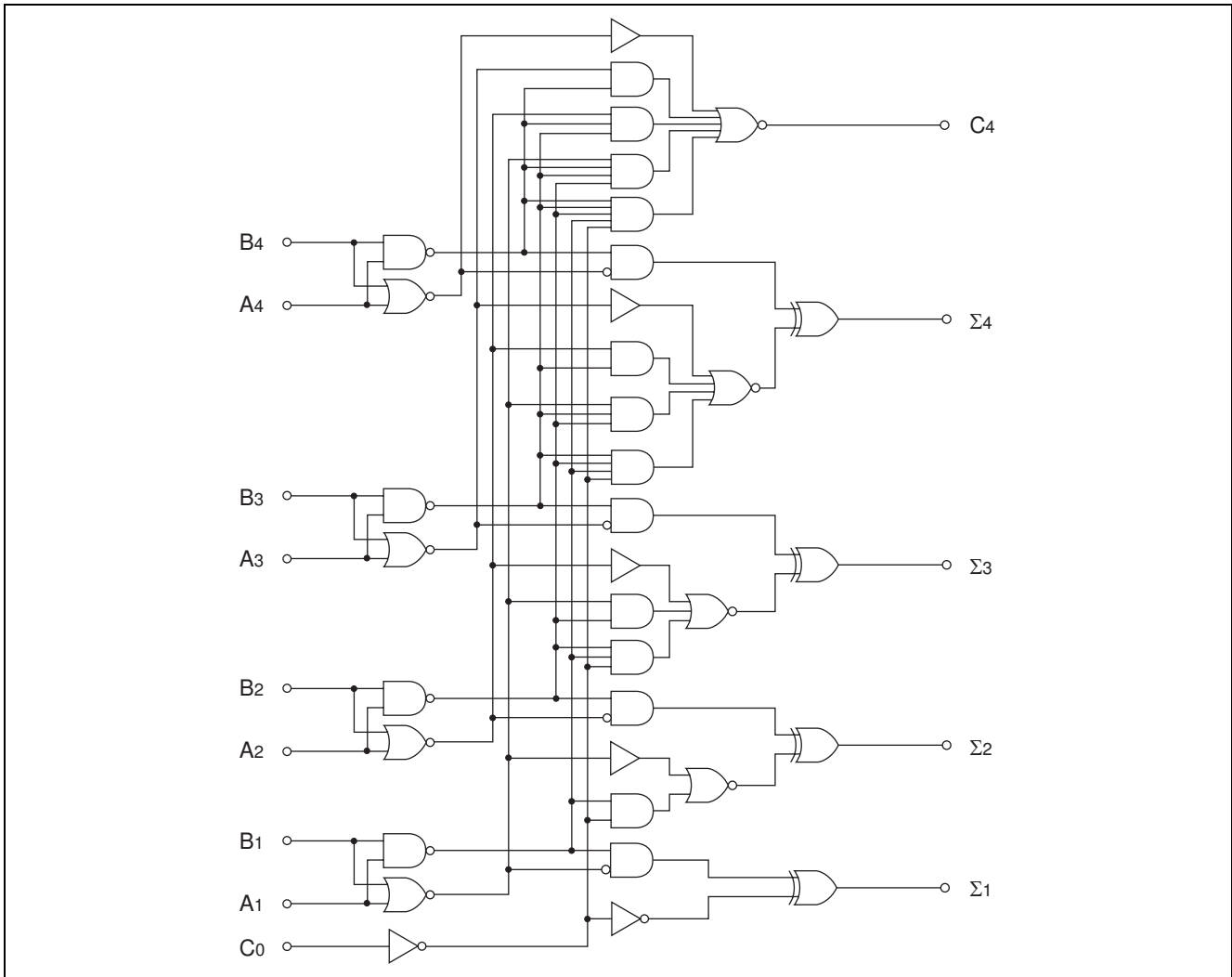
Function Table

Input				Output					
				When C <sub>0</sub> = L			When C <sub>0</sub> = H		
A <sub>1</sub>	B <sub>1</sub>	A <sub>2</sub>	B <sub>2</sub>	Σ <sub>1</sub>	Σ <sub>2</sub>	C <sub>2</sub>	Σ <sub>1</sub>	Σ <sub>2</sub>	C <sub>2</sub>
A <sub>3</sub>	B <sub>3</sub>	A <sub>4</sub>	B <sub>4</sub>	Σ <sub>3</sub>	Σ <sub>4</sub>	C <sub>4</sub>	Σ <sub>3</sub>	Σ <sub>4</sub>	C <sub>4</sub>
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H; high level, L; low level, X; irrelevant

Note: Input conditions at A<sub>1</sub>, B<sub>1</sub>, A<sub>2</sub>, B<sub>2</sub>, and C<sub>0</sub> are used to determine outputs Σ<sub>1</sub> and Σ<sub>2</sub> and the value of the internal carry C<sub>2</sub>. The value at C<sub>2</sub>, A<sub>3</sub>, B<sub>3</sub>, A<sub>4</sub>, and B<sub>4</sub> are then used to determine outputs Σ<sub>3</sub>, Σ<sub>4</sub> and C<sub>4</sub>.

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	7	V
Input voltage	$V_{IN}$	7	V
Power dissipation	$P_T$	400	mW
Storage temperature	$T_{stg}$	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.75	5.00	5.25	V
Output current	$I_{OH}$	—	—	-400	μA
	$I_{OL}$	—	—	8	mA
Operating temperature	$T_{opr}$	-20	25	75	°C

**Electrical Characteristics**

(Ta = -20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage	V <sub>IH</sub>	2.0	—	—	V		
	V <sub>IL</sub>	—	—	0.8	V		
Output voltage	V <sub>OH</sub>	2.7	—	—	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -400 μA	
	V <sub>OL</sub>	—	—	0.4	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V	
—		—	0.5				
Input current	except C <sub>0</sub>	—	—	40	μA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.7 V	
	C <sub>0</sub>			20			
	except C <sub>0</sub>	—	—	-0.8	mA		
	C <sub>0</sub>			-0.4			
except C <sub>0</sub>	—	—	0.2	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 7 V		
C <sub>0</sub>			0.1				
Short-circuit output current	I <sub>OS</sub>	-20	—	-100		mA	V <sub>CC</sub> = 5.25 V
Supply current	I <sub>CC</sub>	—	22	39		mA	All inputs = 0 V
		—	19	34	B input = 0.8 V, Other inputs 4.5 V		
		—	19	34	All inputs = 4.5 V		
						V <sub>CC</sub> = 5.25 V	
Input clamp voltage	V <sub>IR</sub>	—	—	-1.5	V	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA	

Note: \* V<sub>CC</sub> = 5 V, Ta = 25 °C

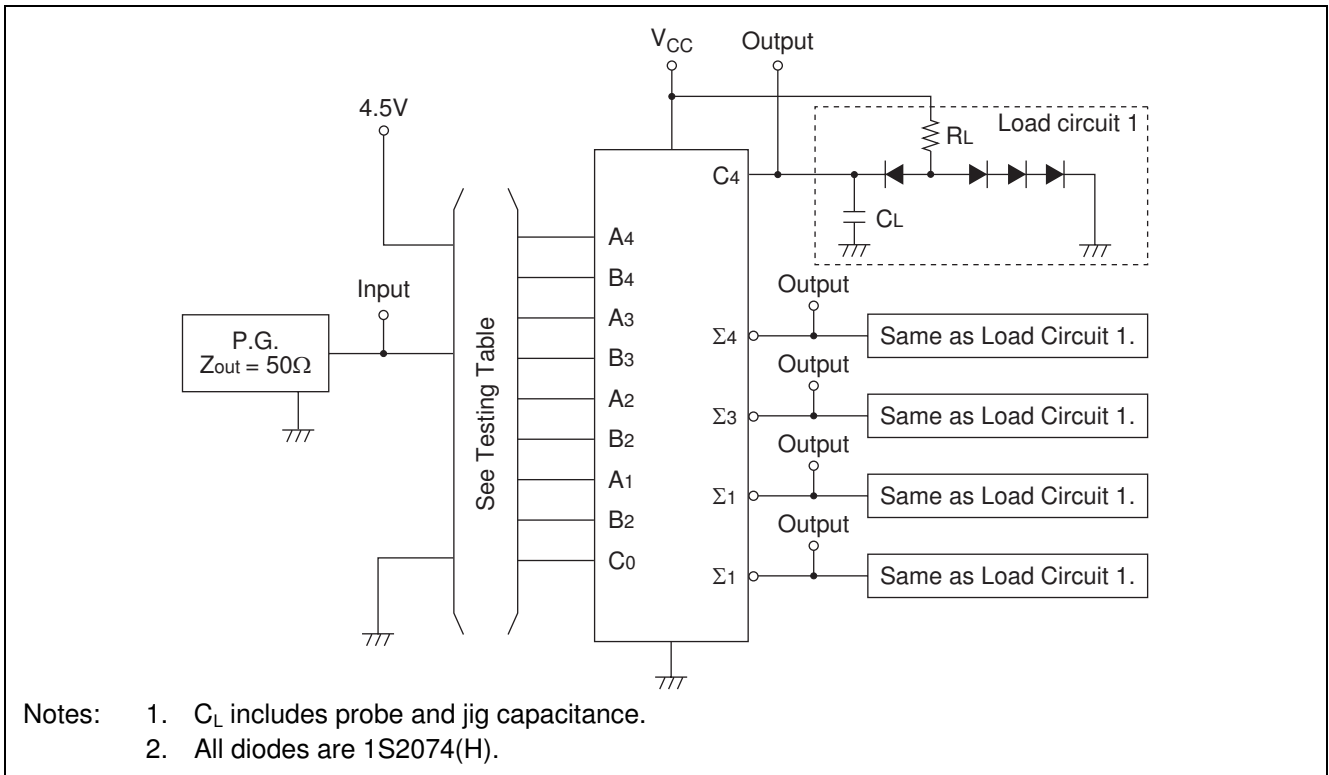
**Switching Characteristics**

(V<sub>CC</sub> = 5 V, Ta = 25 °C)

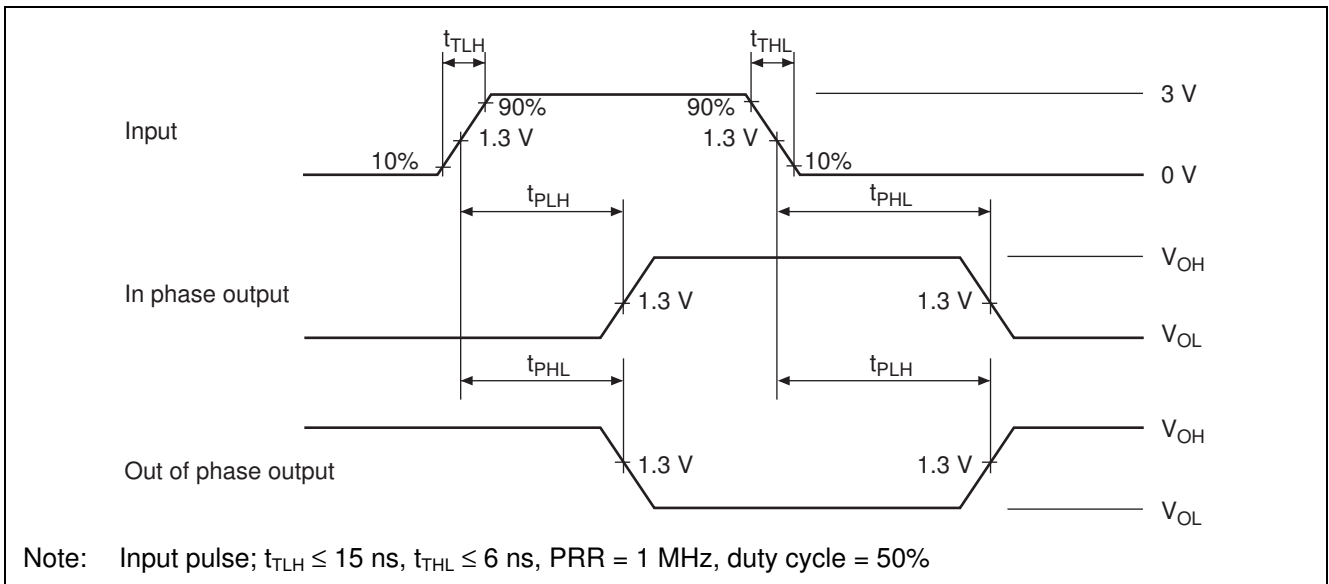
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Propagation delay time	t <sub>PLH</sub>	C <sub>0</sub>	Σ <sub>1</sub>	—	16	24	ns	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ
	t <sub>PHL</sub>			—	15	24		
	t <sub>PLH</sub>	A <sub>i</sub> , B <sub>i</sub>	Σ <sub>1</sub>	—	15	24		
	t <sub>PHL</sub>			—	15	24		
	t <sub>PLH</sub>	C <sub>0</sub>	C <sub>4</sub>	—	11	17		
	t <sub>PHL</sub>			—	15	22		
	t <sub>PLH</sub>	A <sub>i</sub> , B <sub>i</sub>	C <sub>4</sub>	—	11	17		
	t <sub>PHL</sub>			—	12	17		

## Testing Method

### Test Circuit



### Waveform

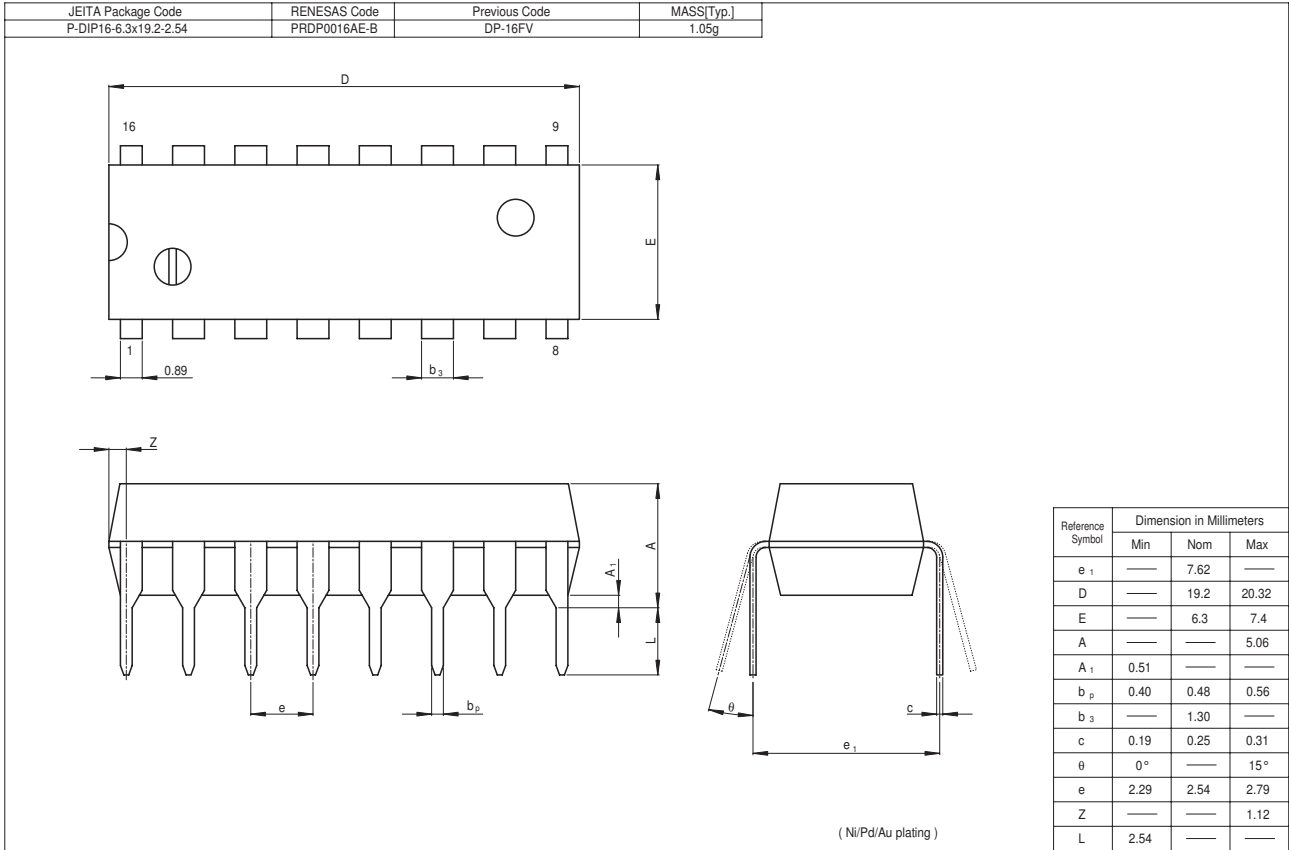


Testing Table

Item	From input to output	Input									Output							
		B <sub>4</sub>	A <sub>4</sub>	B <sub>3</sub>	A <sub>3</sub>	B <sub>2</sub>	A <sub>2</sub>	B <sub>1</sub>	A <sub>1</sub>	C <sub>0</sub>	C <sub>4</sub>	Σ <sub>4</sub>	Σ <sub>3</sub>	Σ <sub>2</sub>	Σ <sub>1</sub>			
t <sub>PLH</sub> t <sub>PHL</sub>	C <sub>0</sub> → Σ <sub>i</sub> or C <sub>4</sub>	GND	GND	GND	GND	GND	GND	GND	GND	GND	IN	—	—	—	—	OUT		
		GND	GND	GND	4.5 v	GND	4.5 v	GND	4.5 v	IN	IN	OUT	OUT	OUT	OUT	OUT		
	A <sub>i</sub> or B <sub>i</sub> → Σ <sub>i</sub> or C <sub>4</sub>	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	—	—	—	—	OUT	
																		GND
		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	—	—	—	OUT	—
		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	—	—	OUT	—	—
		GND	IN	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	—	OUT	—	—	—
		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	—	—	—	OUT	OUT
		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	—	—	OUT	OUT	—
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	—	OUT	OUT	—	—		
																	4.5 v	IN



Package Dimensions



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