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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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HD74LV07A

Hex Buffers / Drivers with Open Drain Outputs

REJ03D0231-0600

Rev.6.00

Dec 22, 2005

Description

The HD74LV07A has six buffers / drivers with open drain outputs in a 14-pin package.

Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- $V_{CC} = 2.0\text{ V}$ to 5.5 V operation
- All inputs V_{IH} (Max.) = 5.5 V (@ $V_{CC} = 0\text{ V}$ to 5.5 V)
- All outputs V_O (Max.) = 5.5 V (@ $V_{CC} = 0\text{ V}$)
- All outputs V_O (Max.) = 5.5 V (@ $V_{CC} = 2.0\text{ V}$ to 5.5 V , Output "Z" state)
- Typical V_{OL} ground bounce < 0.8 V (@ $V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Output current: $\pm 8\text{ mA}$ (@ $V_{CC} = 3.0\text{ V}$ to 3.6 V), $\pm 16\text{ mA}$ (@ $V_{CC} = 4.5\text{ V}$ to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV07AFPEL	SOP-14 pin(JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)
HD74LV07ARPEL	SOP-14 pin(JEDEC)	PRSP0014DE-A (FP-14DNV)	RP	EL (2,500 pcs/reel)
HD74LV07ATELL	TSSOP-14 pin	PTSP0014JA-B (TTP-14DV)	T	ELL (2,000 pcs/reel)

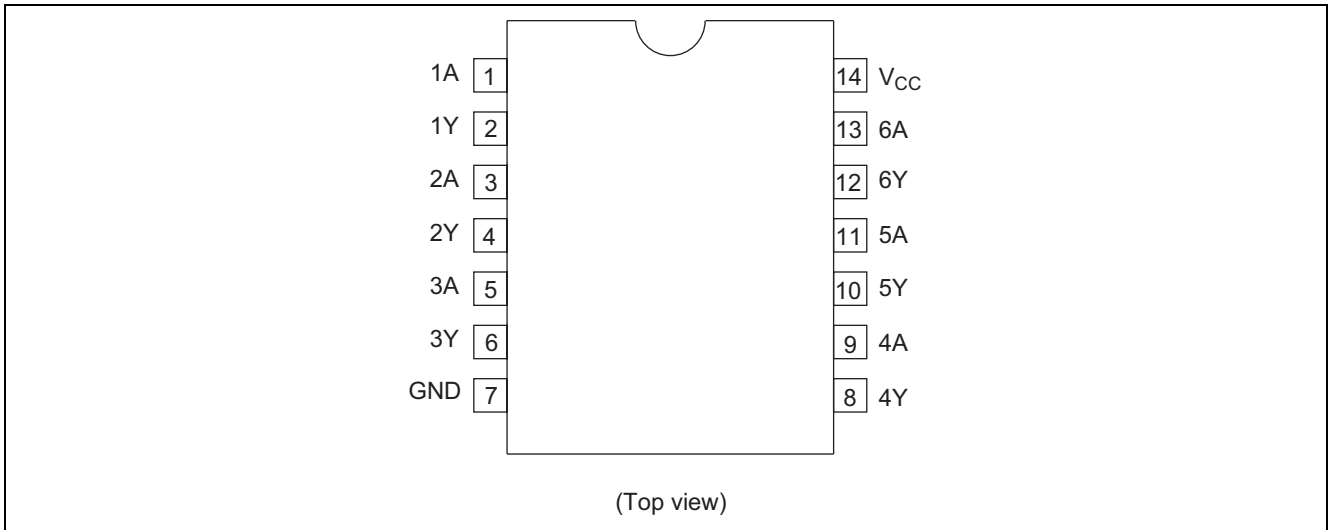
Note: Please consult the sales office for the above package availability.

Function Table

Input A	Output Y
L	L
H	Z

Note: H: High level
L: Low level
Z: High impedance

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range* ¹	V_I	-0.5 to 7.0	V	
Output voltage range* ^{1, 2}	V_O	-0.5 to $V_{CC} + 0.5$	V	Output: L
		-0.5 to 7.0		V_{CC} : OFF or Output: Z
Input clamp current	I_{IK}	-20	mA	$V_I < 0$
Output clamp current	I_{OK}	± 50	mA	$V_O < 0$
Continuous output current	I_O	± 35	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	± 50	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* ³	P_T	785	mW	SOP
		500		TSSOP
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

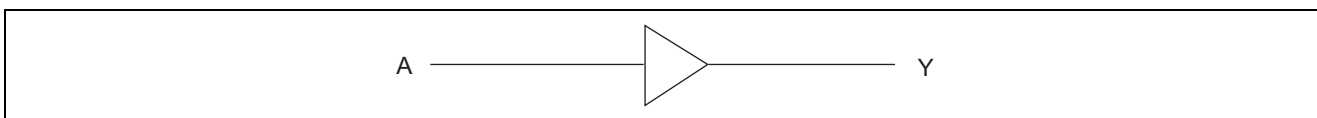
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 7.0 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150 $^\circ\text{C}$.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	5.5	V	
Output current	I_{OL}	—	50	μA	$V_{CC} = 2.0 \text{ V}$
		—	2	mA	$V_{CC} = 2.3 \text{ to } 2.7 \text{ V}$
		—	8		$V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$
		—	16		$V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3 \text{ to } 2.7 \text{ V}$
		0	100		$V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$
		0	20		$V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$
Operating free-air temperature	T_a	-40	85	$^{\circ}\text{C}$	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



DC Electrical Characteristics

$T_a = -40 \text{ to } 85^{\circ}\text{C}$

Item	Symbol	$V_{CC} \text{ (V)}^*$	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	$V_{CC} \times 0.7$	—	—		
		3.0 to 3.6	$V_{CC} \times 0.7$	—	—		
		4.5 to 5.5	$V_{CC} \times 0.7$	—	—		
	V_{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	$V_{CC} \times 0.3$		
		3.0 to 3.6	—	—	$V_{CC} \times 0.3$		
		4.5 to 5.5	—	—	$V_{CC} \times 0.3$		
Output voltage	V_{OL}	Min to Max	—	—	0.1	V	$I_{OL} = 50 \mu\text{A}$
		2.3	—	—	0.4		$I_{OL} = 2 \text{ mA}$
		3.0	—	—	0.44		$I_{OL} = 8 \text{ mA}$
		4.5	—	—	0.55		$I_{OL} = 16 \text{ mA}$
Input current	I_{IN}	0 to 5.5	—	—	± 1	μA	$V_{IN} = 5.5 \text{ V or GND}$
Off state output current	I_{OZ}	Min to Max	—	—	2.5	μA	$V_O = 5.5 \text{ V}$
Quiescent supply current	I_{CC}	5.5	—	—	20	μA	$V_{IN} = V_{CC} \text{ or GND, } I_O = 0$
Output leakage current	I_{OFF}	0	—	—	5	μA	$V_I \text{ or } V_O = 0 \text{ to } 5.5 \text{ V}$
Input capacitance	C_{IN}	3.3	—	2.3	—	pF	$V_I = V_{CC} \text{ or GND}$

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

$V_{CC} = 2.5 \pm 0.2 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	4.7	10.4	1.0	13.0	ns	C _L = 15 pF	A	Y
		—	9.5	15.2	1.0	18.0		C _L = 50 pF		
	t _{PHL}	—	5.4	10.4	1.0	13.0		C _L = 15 pF		
		—	7.9	15.2	1.0	18.0		C _L = 50 pF		

$V_{CC} = 3.3 \pm 0.3 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	4.0	7.1	1.0	8.5	ns	C _L = 15 pF	A	Y
		—	7.3	10.6	1.0	12.0		C _L = 50 pF		
	t _{PHL}	—	4.3	7.1	1.0	8.5		C _L = 15 pF		
		—	5.8	10.6	1.0	12.0		C _L = 50 pF		

$V_{CC} = 5.0 \pm 0.5 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	3.3	5.5	1.0	6.5	ns	C _L = 15 pF	A	Y
		—	5.6	7.5	1.0	8.5		C _L = 50 pF		
	t _{PHL}	—	3.4	5.5	1.0	6.5		C _L = 15 pF		
		—	4.1	7.5	1.0	8.5		C _L = 50 pF		

Operating Characteristics

$C_L = 50 \text{ pF}$

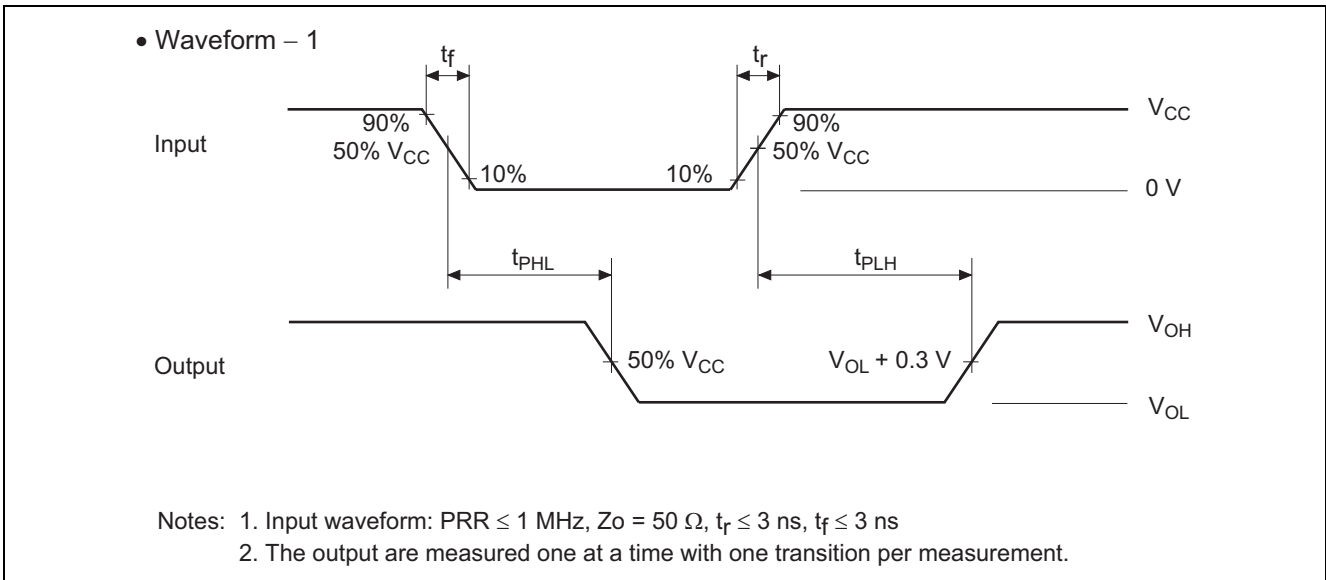
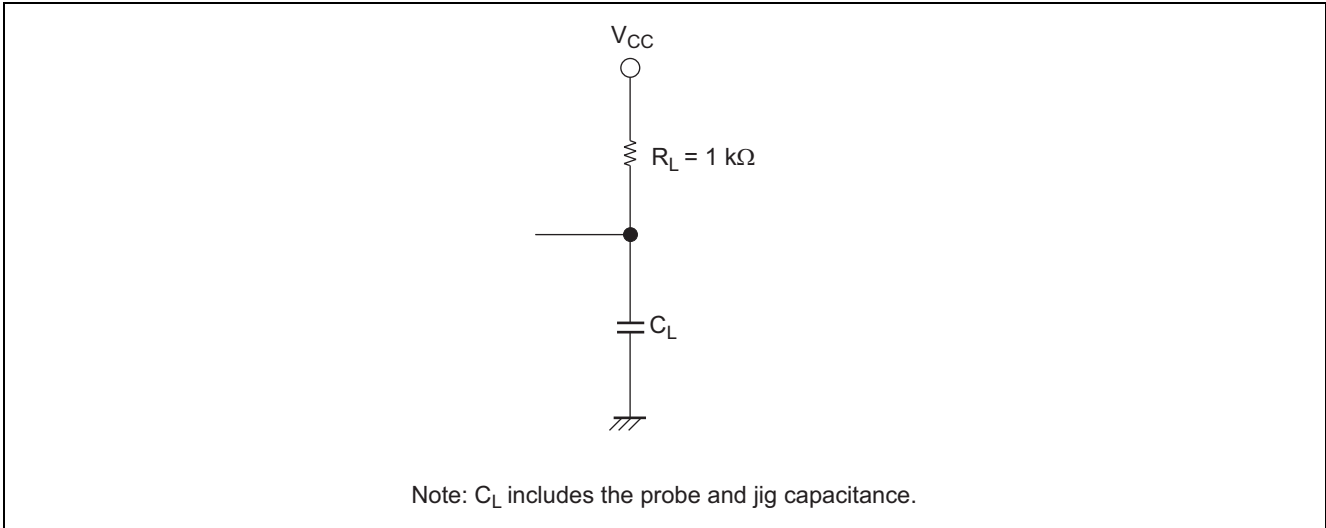
Item	Symbol	V _{CC} (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C _{PD}	3.3	—	9.6	—	pF	f = 10 MHz
		5.0	—	11.4	—		

Noise Characteristics

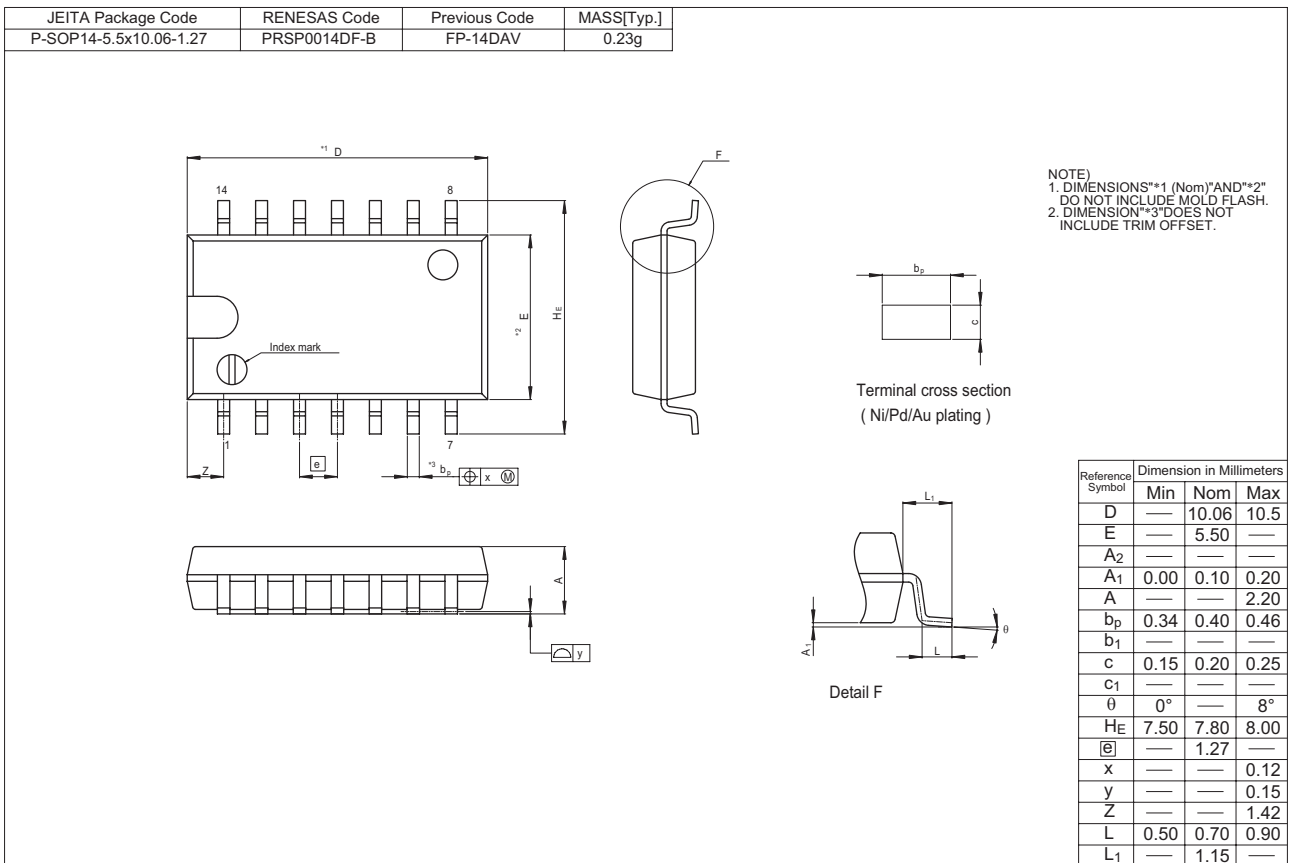
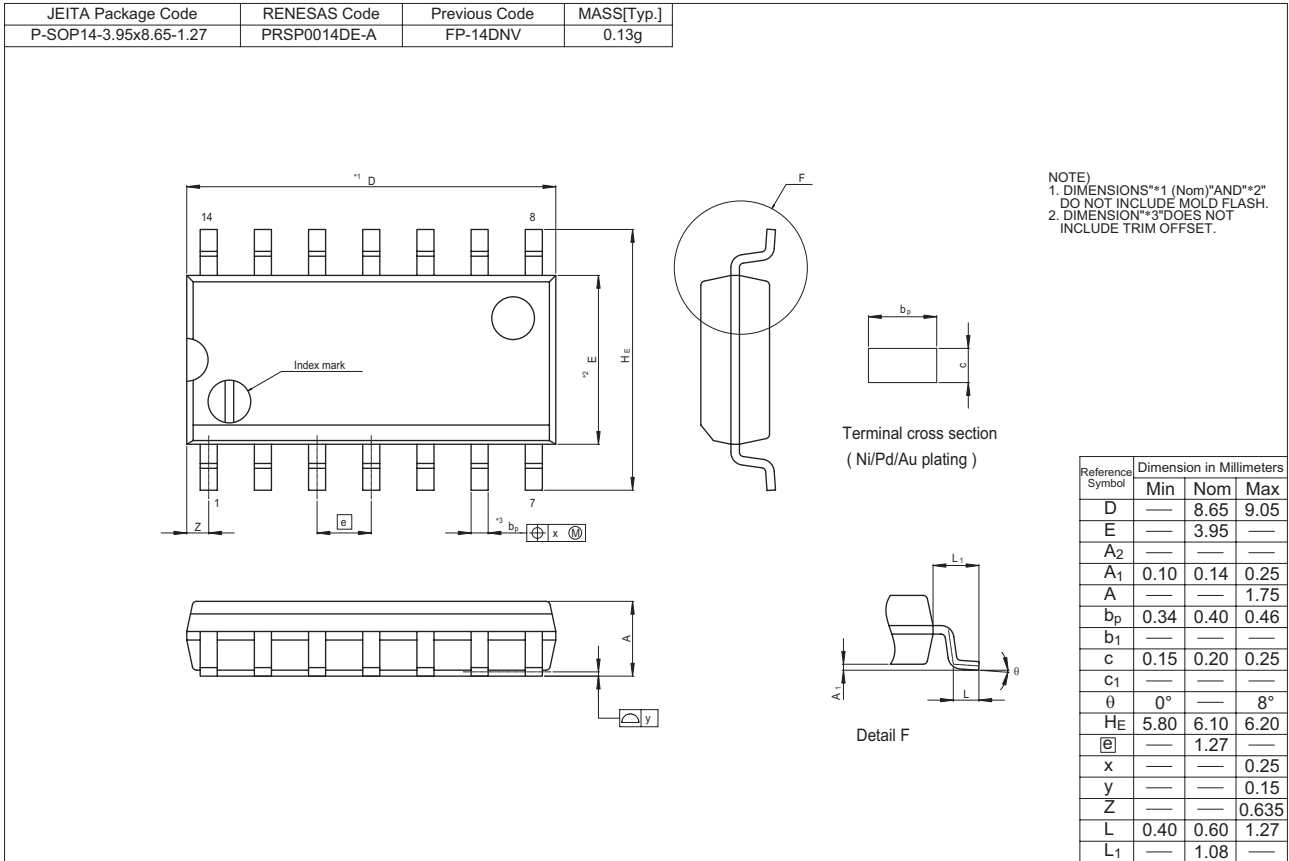
$C_L = 50 \text{ pF}$

Item	Symbol	V _{CC} (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic V _{OL}	V _{OL(P)}	3.3	—	0.3	0.8	V	
Quiet output, minimum dynamic V _{OL}	V _{OL(V)}	3.3	—	-0.1	-0.8	V	
High-level dynamic input voltage	V _{IH(D)}	3.3	2.31	—	—	V	
Low-level dynamic input voltage	V _{IL(D)}	3.3	—	—	0.99	V	

Test Circuit

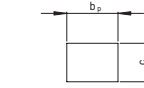
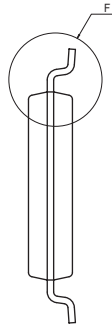
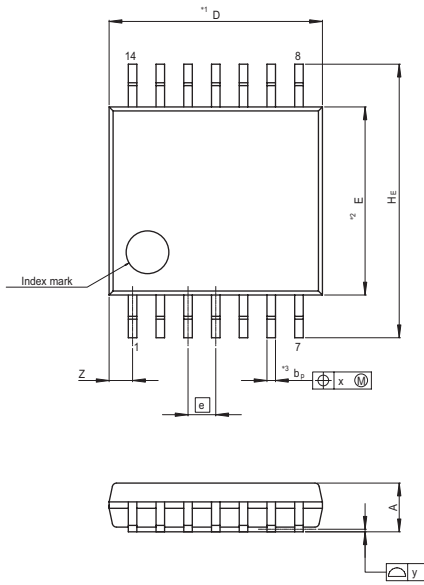


Package Dimensions

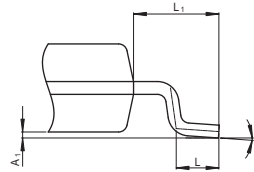


HD74LV07A

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP14-4.4x5-0.65	PTSP0014JA-B	TTP-14DV	0.05g



Terminal cross section
(Ni/Pd/Au plating)



Detail F

NOTE)
1. DIMENSIONS*1 (Nom)*AND*2*
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION*3*DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.00	5.30
E	—	4.40	—
A ₂	—	—	—
A ₁	0.03	0.07	0.10
A	—	—	1.10
b _p	0.15	0.20	0.25
d ₁	—	—	—
c	0.10	0.15	0.20
c ₁	—	—	—
θ	0°	—	8°
HE	6.20	6.40	6.60
⓪	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.83
L	0.4	0.5	0.6
L ₁	—	1.0	—

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