

HVD316

Variable Capacitance Diode for BS/CS tuner

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Rev.1.00
Jul 27, 2006

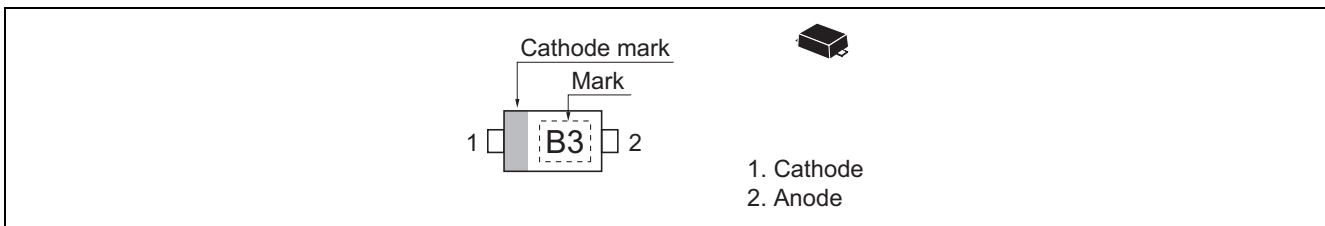
Features

- High capacitance ratio ($n = 9.0$ min)
- Low series resistance. ($r_s = 2.2 \Omega$ max)
- Super small Flat Lead Package (SFP) is suitable for surface mount design.

Ordering Information

Type No.	Laser Mark	Package Name	Package Code
HVD316	B3	SFP	PUSF0002ZB-A

Pin Arrangement



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Reverse voltage	V _R	30	V
Junction temperature	T _j	125	°C
Storage temperature	T _{stg}	-55 to +125	°C

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse current	I _{R1}	—	—	10	nA	V _R = 30 V
	I _{R2}	—	—	100		V _R = 30 V, Ta = 60°C
Capacitance	C ₁	5.16	—	7.22	pF	V _R = 1 V, f = 1 MHz
	C ₂₅	0.48	—	0.76		V _R = 25V, f = 1 MHz
Capacitance ratio	n	9.0	—	—	—	C ₁ / C ₂₅
Series resistance	r _s	—	—	2.20	Ω	V _R = 1 V, f = 470 MHz
Matching error	ΔC/C *1	—	—	6.00	%	V _R = 1 to 25 V, f = 1 MHz

Notes: 1. C.C system (Continuous Connected taping system) enable to make any 10 pcs of ΔC/C continuous in a reel, expect extention to another group.

Calculate Matching Error,

$$\Delta C/C = \frac{(C_{\max} - C_{\min})}{C_{\min}} \times 100 (\%)$$

2. For SFP package, the material of lead is exposed for cutting plane. There for, soldering nature of lead tip part is considered as unquestioned. Please kindly consider soldering nature.

Main Characteristic

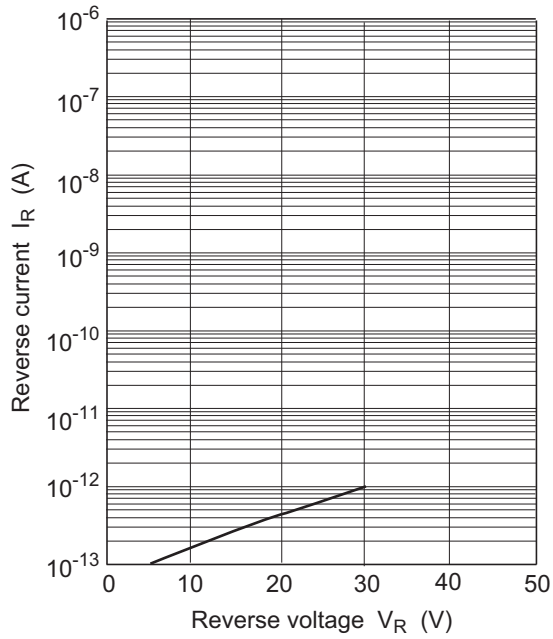


Fig.1 Reverse current vs. Reverse voltage

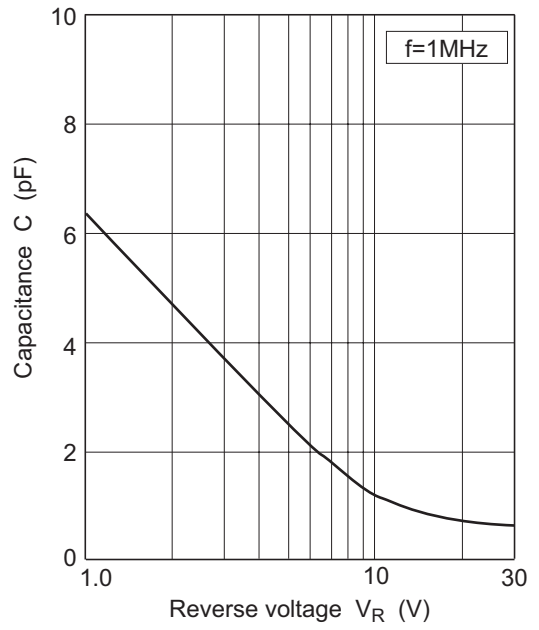


Fig.2 Capacitance vs. Reverse voltage

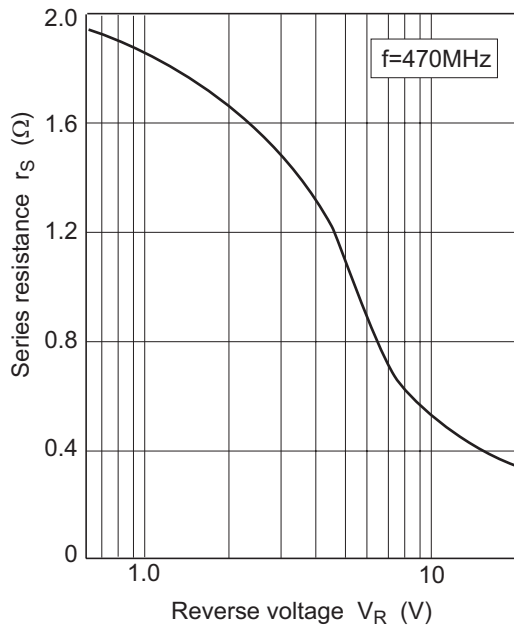
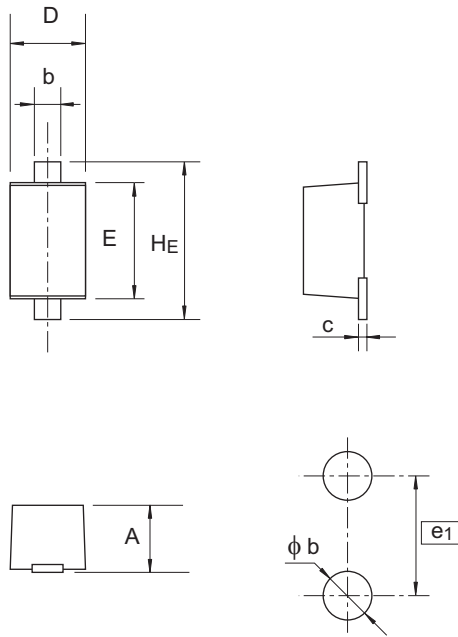


Fig.3 Series resistance vs. Reverse voltage

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SFP	—	PUSF0002ZB-A	SFP / SFPV	0.0010g



Pattern of terminal position areas

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	0.50	—	0.55
b	0.25	0.30	0.35
c	0.08	0.13	0.18
D	0.55	0.60	0.65
E	0.90	1.00	1.10
H_E	1.30	1.40	1.50
ϕb	—	0.50	—
e_1	—	1.40	—

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April 1st, 2010
Renesas Electronics Corporation

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