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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Not recommended
for new design

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HVD388C

Variable Capacitance Diode for VCO

REJ03G0362-0200
Rev.2.00
Mar 30, 2006

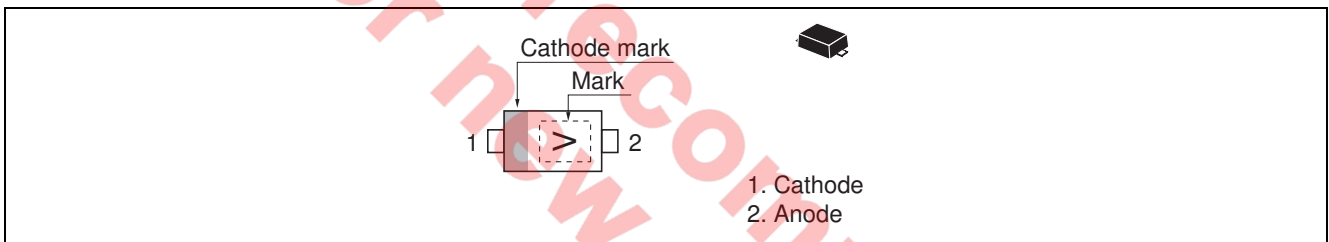
Features

- High capacitance ratio. ($n = 1.88$ min)
- Low series resistance. ($r_s = 0.75 \Omega$ max)
- Super small Flat Lead Package (SFP) is suitable for surface mount design.

Ordering Information

Type No.	Laser Mark	Package Name	Package Code
HVD388C	V	SFP	PUSF0002ZB-A

Pin Arrangement



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Reverse voltage	V _R	15	V
Junction temperature	T _j	125	°C
Storage temperature	T _{stg}	-55 to +125	°C

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse current	I _{R1}	—	—	10	nA	V _R = 15 V
	I _{R2}	—	—	50		V _R = 15 V, Ta = 60°C
Capacitance	C ₁	3.162	—	3.465	pF	V _R = 1 V, f = 1 MHz
	C ₃	1.570	—	1.720		V _R = 3 V, f = 1 MHz
Capacitance ratio	n	1.880	—	2.150	—	C ₁ / C ₃
Series resistance	r _s	—	—	0.75	Ω	V _R = 1 V, f = 470 MHz

Note: For SFP package, the material of lead is exposed for cutting plane. There for, soldering nature of lead tip part is considered as unquestioned. Please kindly consider soldering nature.

Main Characteristic

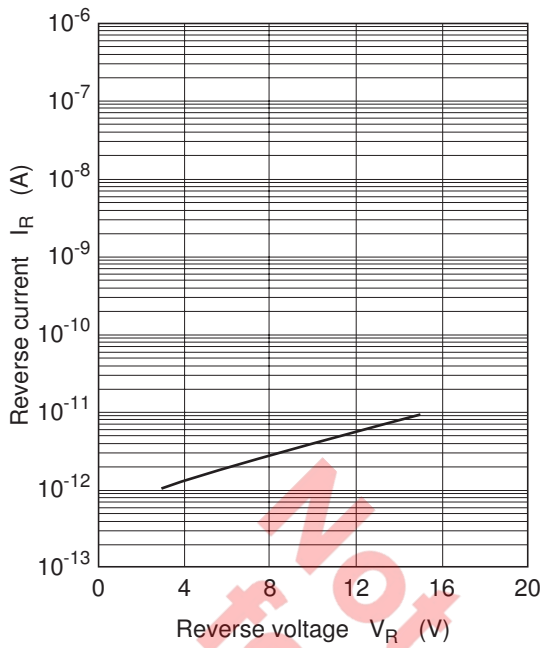


Fig.1 Reverse current vs. Reverse voltage

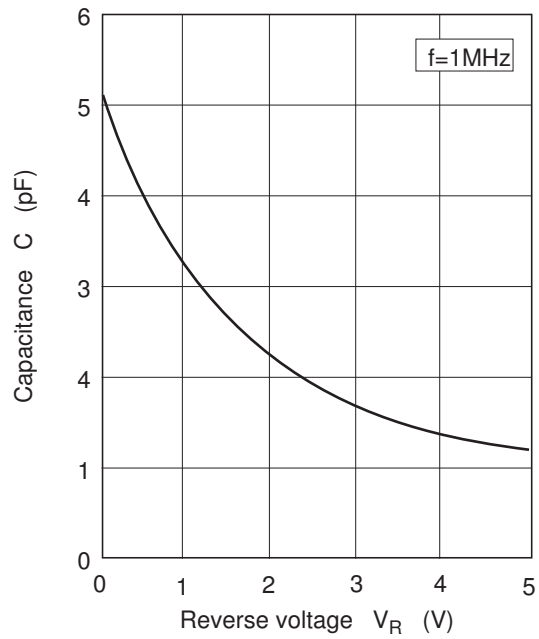


Fig.2 Capacitance vs. Reverse voltage

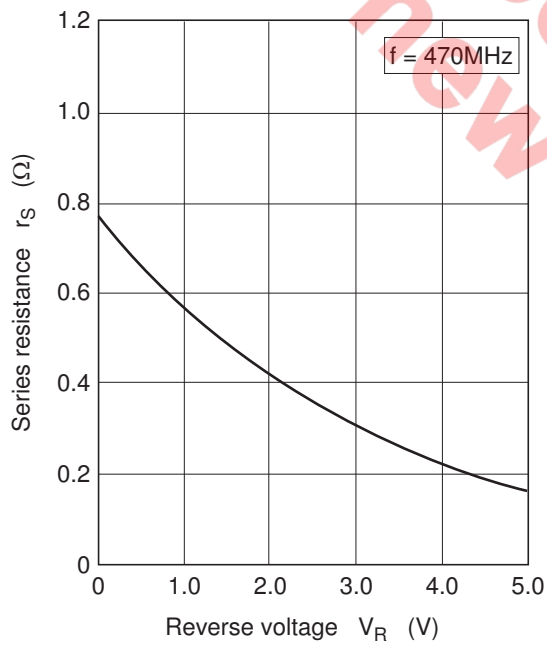


Fig.3 Series resistance vs. Reverse voltage

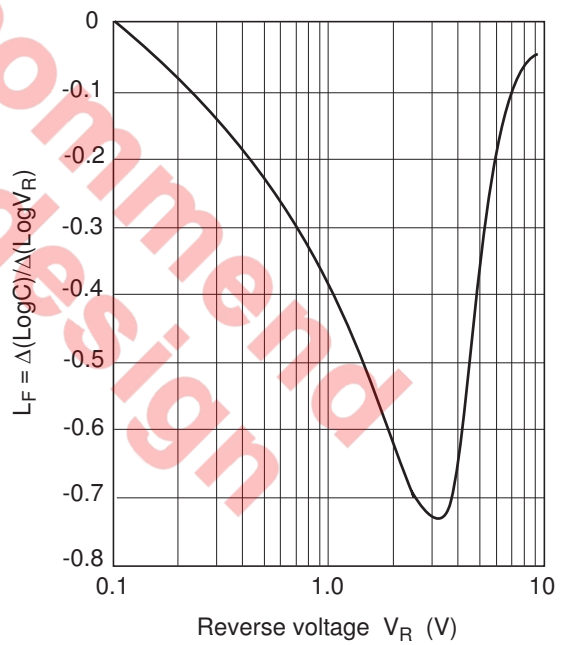
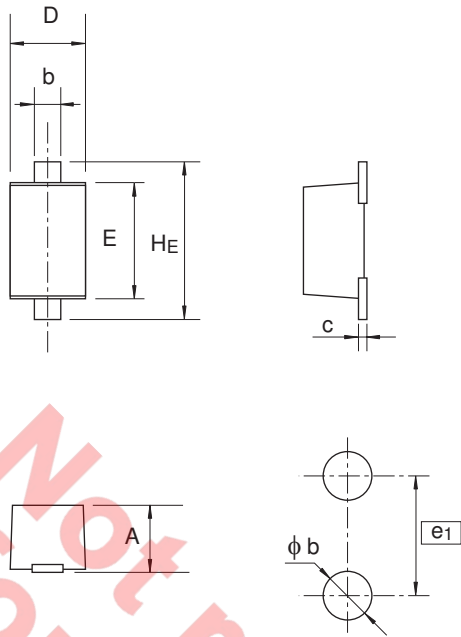


Fig.4 L_F vs. Reverse voltage

Package Dimensions

Package Name SFP	JEITA Package Code —	RENESAS Code PUSF0002ZB-A	Previous Code SFP / SFPV	MASS[Typ.] 0.0010g
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Pattern of terminal position areas

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	0.50	—	0.55
b	0.25	0.30	0.35
c	0.08	0.13	0.18
D	0.55	0.60	0.65
E	0.90	1.00	1.10
H_E	1.30	1.40	1.50
ϕb	—	0.50	—
e_1	—	1.40	—

Not recommend for new design

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