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# 8-bit 8ch D/A Converter

REJ03D0874-0301 Rev.3.01 Apr 15, 2008

### Description

The M62363FP is an integrated circuit semiconductor of CMOS structured with 8 channels of built-in 8-bit multiplication type D/A converters.

The input data is a easy-to-use 3-wire serial method and it is able to cascading serial use with D<sub>0</sub> terminal.

The device is suited for use in automatic adjustment combination of microcomputer.

### Features

- Digital data transfer method: 3-wire serial data transfer method
- D/A converter system Employment of the additional higher-order segment R-2R method doubled precision compared to the conventional R-2R method.
- Short setting time
- 4 quadrant multiplication

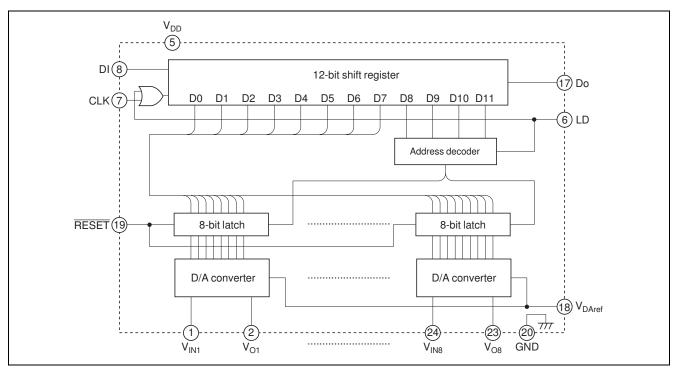
# Application

Conversion from digital control data to analog control data for home-use and industrial equipment.

Automatic adjustment by combination with EEPROM and microcomputer. (Replacement of conventional half-fixed resistor.)

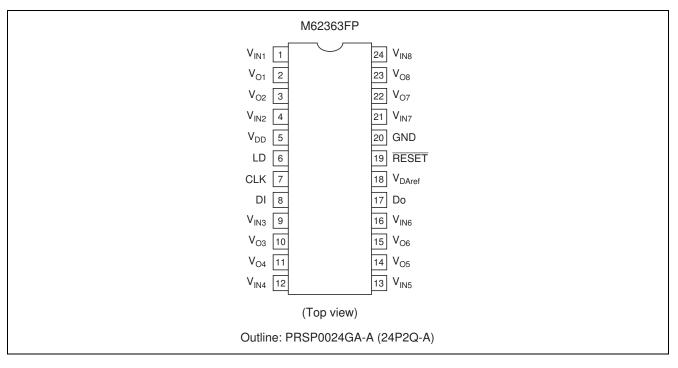
Signal gain control of display-monitor or CTV

# **Block Diagram**



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# **Pin Arrangement**



# **Pin Description**

| Pin No. | Pin Name           | Function  |
|---------|--------------------|---|
| 8       | DI                 | Serial data input terminal                                |
| 17      | Do                 | Serial data output terminal                               |
| 7       | CLK                | Serial clock input terminal                               |
| 6       | LD                 | LD terminal input high level then latch circuit data load |
| 19      | RESET              | Reset terminal  |
| 2       | V <sub>O1</sub>    | 8-bit resolution D/A output                               |
| 3       | V <sub>O2</sub>    |   |
| 10      | V <sub>O3</sub>    |   |
| 11      | V <sub>O4</sub>    |   |
| 14      | V <sub>O5</sub>    |   |
| 15      | V <sub>O6</sub>    |   |
| 22      | V <sub>07</sub>    |   |
| 23      | V <sub>O8</sub>    |   |
| 5       | V <sub>DD</sub>    | Power supply terminal                                     |
| 20      | GND                | GND terminal  |
| 1       | V <sub>IN1</sub>   | D/A converter input terminal                              |
| 4       | V <sub>IN2</sub>   |   |
| 9       | V <sub>IN3</sub>   |   |
| 12      | V <sub>IN4</sub>   |   |
| 13      | V <sub>IN5</sub>   |   |
| 16      | V <sub>IN6</sub>   |   |
| 21      | V <sub>IN7</sub>   |   |
| 24      | V <sub>IN8</sub>   |   |
| 18      | V <sub>DAref</sub> | D/A converter reference voltage input terminal            |
|         |                    | $V_{O} = (V_{IN} - V_{DAref}) \times n / 256 + V_{DAref}$ |

# **Absolute Maximum Ratings**

| Item                  | Symbol             | Ratings                       | Unit |
|-----------------------|--------------------|-------------------------------|------|
| Supply voltage        | V <sub>DD</sub>    | -0.3 to +7.0                  | V    |
| Input voltage         | V <sub>IND</sub>   | -0.3 to +7.0                  | V    |
| Input voltage         | V <sub>IN</sub>    | –0.3 to V <sub>DD</sub> + 0.3 | V    |
| Output voltage        | Vo                 | –0.3 to V <sub>DD</sub> + 0.3 | V    |
| D/A reference voltage | V <sub>DAref</sub> | –0.3 to V <sub>DD</sub> + 0.3 | V    |
| Operating temperature | Topr               | -20 to +75                    | °C   |
| Storage temperature   | Tstg               | -40 to +125                   | °C   |

# **Electrical Characteristics**

#### <Digital Part>

 $(V_{DD}, V_{IN} = +5 \text{ V} \pm 10\%, V_{DD} \ge V_{IN}, \text{GND} = V_{DAref} = 0 \text{ V}, \text{ Ta} = -20 \text{ to } +75^{\circ}\text{C}, \text{ unless otherwise noted.})$ 

|                     |                  | Limits              |     |                     |      |                           |
|---------------------|------------------|---------------------|-----|---------------------|------|---------------------------|
| Item                | Symbol           | Min                 | Тур | Max                 | Unit | Conditions                |
| Supply voltage      | V <sub>DD</sub>  | 4.5                 | 5.0 | 5.5                 | V    |                           |
| Input leak current  | I <sub>ILK</sub> | -10                 | —   | 10                  | μA   | $V_{IN} = 0$ to $V_{DD}$  |
| Input low voltage   | VIL              | —                   | —   | $0.2 V_{\text{DD}}$ | V    |                           |
| Input high voltage  | V <sub>IH</sub>  | 0.8 V <sub>DD</sub> | —   |                     | V    |                           |
| Output low voltage  | V <sub>OL</sub>  | —                   | —   | 0.4                 | V    | I <sub>OL</sub> = 2.5 mA  |
| Output high voltage | V <sub>OH</sub>  | $V_{\text{DD}}-0.4$ | _   |                     | V    | I <sub>OH</sub> = -400 μA |

#### <Analog Part>

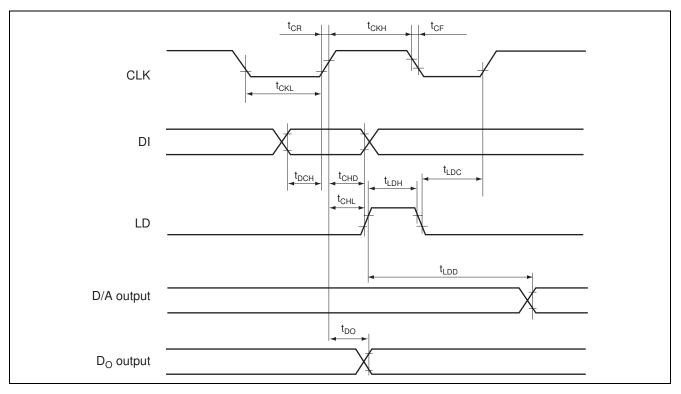
 $(V_{DD}, V_{IN} = +5 \text{ V} \pm 10\%, V_{DD} \ge V_{IN}, \text{GND} = V_{DAref} = 0 \text{ V}, \text{ Ta} = -20 \text{ to } +75^{\circ}\text{C}, \text{ unless otherwise noted.})$ 

|                             |                    |       | Limits |      |      |   |
|-----------------------------|--------------------|-------|--------|------|------|---|
| Item                        | Symbol             | Min   | Тур    | Max  | Unit | Conditions  |
| Input current               | l <sub>in</sub>    | _     | _      | 0.30 | mA   | $\label{eq:VIN} \begin{array}{l} V_{IN} = 5 \ V, \ V_{DAref} = 0 \ V \\ Proportional to Max. input current \\ condition \ (V_{IN} - V_{DAref}) \ and \ digital \\ data \ of each \ cannels \end{array}$ |
| D/A reference input current | I <sub>DAref</sub> | -2.40 | _      | _    | mA   | $V_{IN1}$ to $V_{IN8} = 5 V$ , $V_{DAref} = 0 V$<br>Proportional to Max. input current<br>condition ( $V_{IN} - V_{DAref}$ ) and digital<br>data of each channels                                       |
| Output impedance            | Ro                 | —     | _      | 50   | kΩ   | Constant for all D/A output mode  |
| Resolution                  | RES                | —     | 8      | —    | bit  |   |
| Differential nonlinearity   | DNL                | -1    | _      | 1    | LSB  |   |
| Nonlinearity                | NL                 | -1    | _      | 1    | LSB  |   |

# **AC Characteristics**

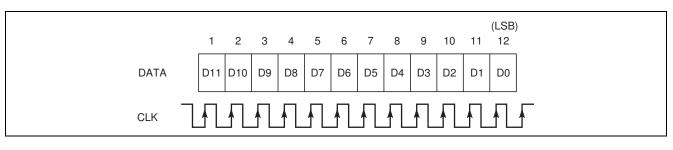
| $(V_{DD}, V_{IN} = +5 \text{ V} \pm 10\%, V_{DD} \ge V_{IN}, \text{GND} = V_{DAref} = 0 \text{ V}, \text{ Ta} = -20 \text{ to } +75^{\circ}\text{C}, \text{ unless otherwise noted.})$ |                  |     |        |     |      |                                  |
|--|------------------|-----|--------|-----|------|----------------------------------|
|  |                  |     | Limits |     |      |                                  |
| Item   | Symbol           | Min | Тур    | Max | Unit | Conditions                       |
| Clock "L" pulse width  | t <sub>CKL</sub> | 200 | —      | —   | ns   |                                  |
| Clock "H" pulse width  | tскн             | 200 | —      | _   | ns   |                                  |
| Clock rise time  | t <sub>CR</sub>  | —   | —      | 200 | ns   |                                  |
| Clock fall time  | t <sub>CF</sub>  | —   | —      | 200 | ns   |                                  |
| Data setup time  | tрсн             | 60  | —      | —   | ns   |                                  |
| Data hold time   | t <sub>CHD</sub> | 100 | —      | —   | ns   |                                  |
| LD setup time  | t <sub>CHL</sub> | 200 | —      | —   | ns   |                                  |
| LD hold time   | t <sub>LDC</sub> | 100 | —      | —   | ns   |                                  |
| LD "H" pulse width   | t <sub>LDH</sub> | 100 | —      | —   | ns   |                                  |
| Data output delay time   | t <sub>DO</sub>  | 70  | _      | 350 | ns   | Less than $C_L = 100 \text{ pF}$ |
| D/A output setting time  | t <sub>LDD</sub> | _   | —      | 5   | μs   | Without load                     |
| Input/output replay time   | —                | —   | —      | 5   | μs   | f = 10 kHz                       |

# **Timing Chart**

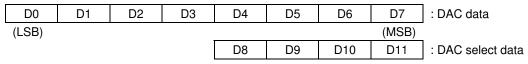


# **Digital Data Format**

#### 12-bit serial data



#### Data assignment



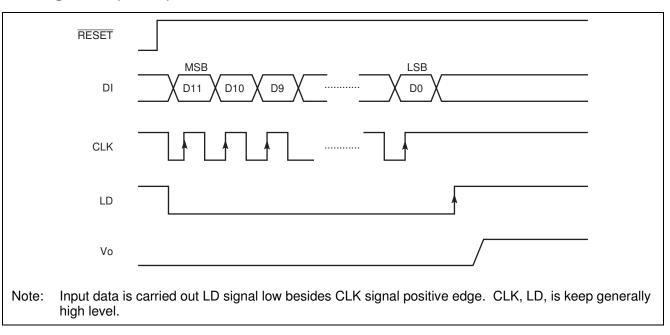
### DAC Data

| (LSB) |    |    |    |    |    |    | (MSB) |   |
|-------|----|----|----|----|----|----|-------|---|
| D0    | D1 | D2 | D3 | D4 | D5 | D6 | D7    | D/A Output  |
| 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0     | V <sub>DAref</sub>                                  |
| 1     | 0  | 0  | 0  | 0  | 0  | 0  | 0     | $(V_{IN} - V_{DAref}) / 256 \times 1 + V_{DAref}$   |
| 0     | 1  | 0  | 0  | 0  | 0  | 0  | 0     | $(V_{IN} - V_{DAref}) / 256 \times 2 + V_{DAref}$   |
| 1     | 1  | 0  | 0  | 0  | 0  | 0  | 0     | $(V_{IN} - V_{DAref}) / 256 \times 3 + V_{DAref}$   |
| :     | :  | :  | :  | :  | :  | :  | :     | :   |
| 1     | 1  | 1  | 1  | 1  | 1  | 1  | 1     | $(V_{IN} - V_{DAref}) / 256 \times 255 + V_{DAref}$ |

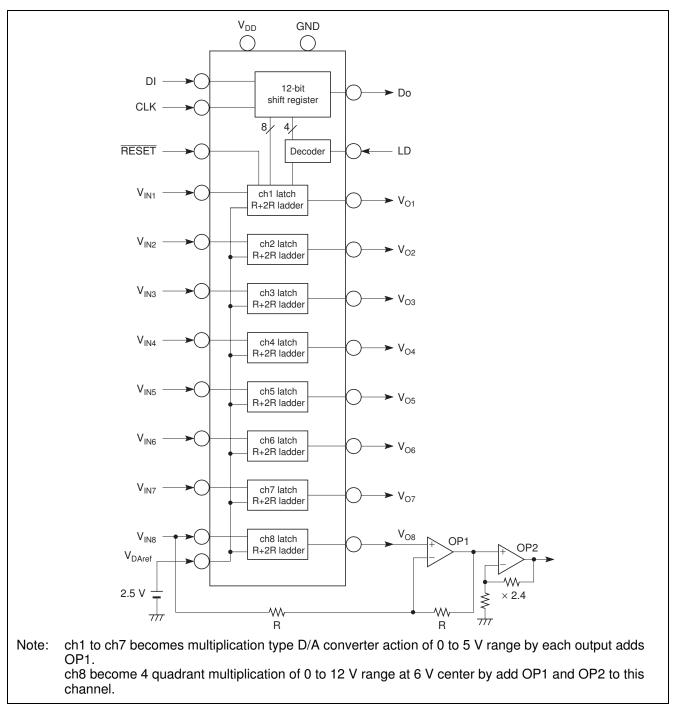
### **DAC Select Data**

| D8 | D9 | D10 | D11 | DAC Selection             |
|----|----|-----|-----|---------------------------|
| 0  | 0  | 0   | 0   | Don't care                |
| 0  | 0  | 0   | 1   | V <sub>01</sub> selection |
| 0  | 0  | 1   | 0   | V <sub>O2</sub> selection |
| 0  | 0  | 1   | 1   | V <sub>O3</sub> selection |
| 0  | 1  | 0   | 0   | V <sub>O4</sub> selection |
| 0  | 1  | 0   | 1   | V <sub>05</sub> selection |
| 0  | 1  | 1   | 0   | V <sub>O6</sub> selection |
| 0  | 1  | 1   | 1   | V <sub>07</sub> selection |
| 1  | 0  | 0   | 0   | V <sub>O8</sub> selection |
| 1  | 0  | 0   | 1   | Don't care                |
| 1  | 0  | 1   | 0   | Don't care                |
| 1  | 0  | 1   | 1   | Don't care                |
| 1  | 1  | 0   | 0   | Don't care                |
| 1  | 1  | 0   | 1   | Don't care                |
| 1  | 1  | 1   | 0   | Don't care                |
| 1  | 1  | 1   | 1   | Don't care                |

# **Timing Chart (Model)**



# **Operating Description**



1. The value of V<sub>0</sub> depend on output direct buffer.

$$V_{O} = (V_{IN} - V_{DAref}) \bullet \frac{n}{256} + V_{DAref} \dots (n = 0 \text{ to } 255) \dots (1)$$

| <v<sub>IN = 5 V&gt;</v<sub> |      |  |  |  |  |  |
|-----------------------------|------|--|--|--|--|--|
| n                           | Vo   |  |  |  |  |  |
| 0                           | 0    |  |  |  |  |  |
| 128                         | 3.75 |  |  |  |  |  |
| 255                         | 4.99 |  |  |  |  |  |

| <v<sub>IN = 0 V&gt;</v<sub> |  |  |  |  |  |  |
|-----------------------------|--|--|--|--|--|--|
| Vo                          |  |  |  |  |  |  |
| 2.5                         |  |  |  |  |  |  |
| 1.25                        |  |  |  |  |  |  |
| 0.01                        |  |  |  |  |  |  |
|                             |  |  |  |  |  |  |

2. The value of  $V_0$  depend on application of ch8.

$$V_{OP1} = (V_{IN} - V_{DAref}) \bullet (\frac{11}{128} - 1) + V_{DAref} \dots (n = 0 \text{ to } 255) \dots (2)$$

 $V_{\text{OP2}} = V_{\text{OP1}} \times 2.4 \ .... (3)$ 

 $< V_{IN} = 5 V >$ 

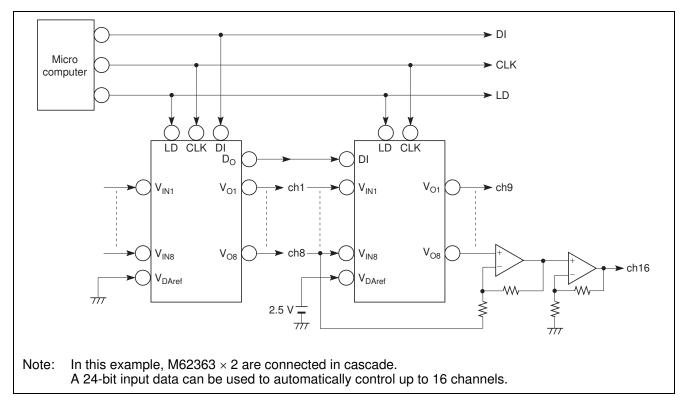
| n   | V <sub>OP1</sub> |
|-----|------------------|
| 0   | 0                |
| 128 | 2.50             |
| 255 | 4.98             |

| <v<sub>IN = 0 V&gt;</v<sub> |                  |  |  |  |  |  |  |
|-----------------------------|------------------|--|--|--|--|--|--|
| n                           | V <sub>OP1</sub> |  |  |  |  |  |  |
| 0                           | 5.00             |  |  |  |  |  |  |
| 128                         | 2.50             |  |  |  |  |  |  |
| 255                         | 0.02             |  |  |  |  |  |  |

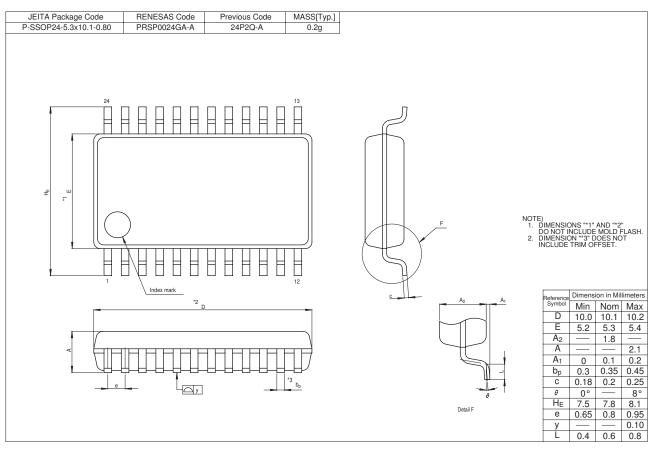
| n   | V <sub>OP1</sub> |
|-----|------------------|
| 0   | 0                |
| 128 | 6.00             |
| 255 | 11.95            |

| n   | V <sub>OP1</sub> |
|-----|------------------|
| 0   | 12.00            |
| 128 | 6.00             |
| 255 | 0.05             |

# **Application Example of Cascade Connection**



# **Package Dimensions**



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