To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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DATA SHEET

MOS FIELD EFFECT TRANSISTOR

NP32N055HDE, NP32N055IDE, NP32N055SDE

SWITCHING
N-CHANNEL POWER MOSFET

DESCRIPTION

These products are N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance
  $R_{DS(on)1}$ = 24 mΩ MAX. (V_{GS} = 10 V, I_D = 16 A)
  $R_{DS(on)2}$ = 29 mΩ MAX. (V_{GS} = 5.0 V, I_D = 16 A)
- Low C_{iss} : C_{iss} = 1300 pF TYP.

★ ORDERING INFORMATION

PART NUMBER	PACKAGE
NP32N055HDE	TO-251 (JEITA) / MP-3
NP32N055IDE Note	TO-252 (JEITA) / MP-3Z
NP32N055SDE	TO-252 (JEDEC) / MP-3ZK

Note Not for new design.

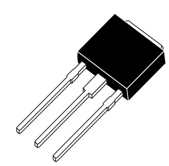
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	55	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±32	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±100	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	66	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Single Avalanche Current Note2	I_{AS}	28 / 21 / 8	A
Single Avalanche Energy Note2	E_{AS}	7.8 / 44 / 64	mJ

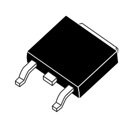
Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, R_G = 25 Ω , V_{GS} = 20 → 0 V

(TO-251)



(TO-252)



THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	2.27	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	125	°C/W

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Date Published July 2005 NS CP(K)
Printed in Japan

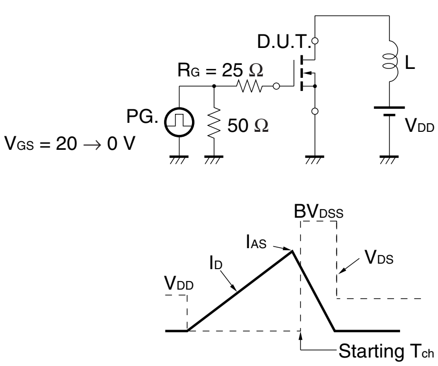
The mark ★ shows major revised points.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

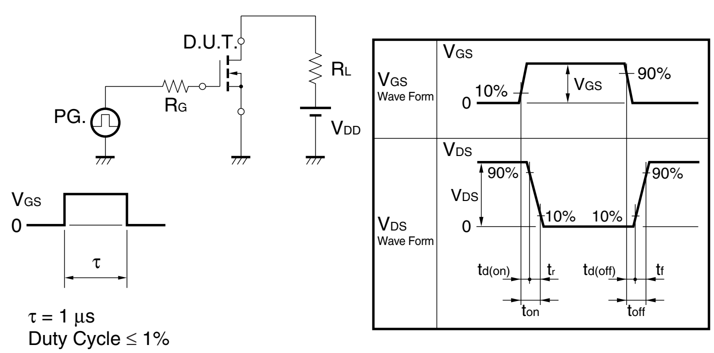
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 55 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.5	2	2.5	V
Forward Transfer Admittance Note	| y_{fs} |	V_{DS} = 10 V, I_D = 16 A	8	16		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 16 A		19	24	mΩ
	$R_{DS(on)2}$	V_{GS} = 5.0 V, I_D = 16 A		22	29	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.5 V, I_D = 16 A		24	33	mΩ
Input Capacitance	C_{iss}	V_{DS} = 25 V		1300	2000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		180	270	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		90	160	pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 28 V, I_D = 16 A		14	31	ns
Rise Time	t_r	V_{GS} = 10 V		8	20	ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 1 Ω		40	81	ns
Fall Time	t_f			7.4	19	ns
Total Gate Charge	Q_{G1}	V_{DD} = 44 V, V_{GS} = 10 V, I_D = 32 A		27	41	nC
	Q_{G2}	V_{DD} = 44 V		15	23	nC
Gate to Source Charge	Q_{GS}	V_{GS} = 5.0 V		5		nC
Gate to Drain Charge	Q_{GD}	I_D = 32 A		9		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 32 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 32 A, V_{GS} = 0 V		41		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		58		nC

Note Pulsed

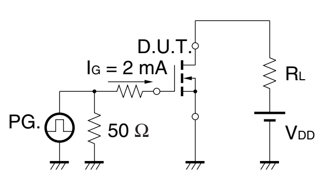
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS (T_A = 25°C)

Figure1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

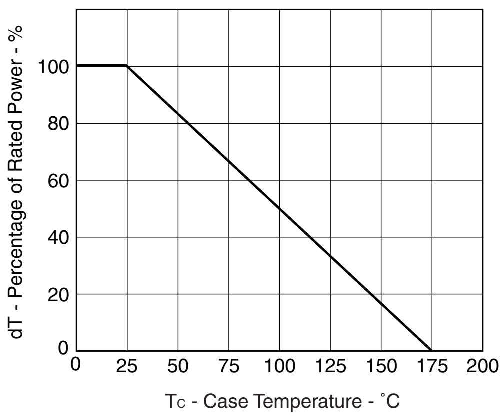


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

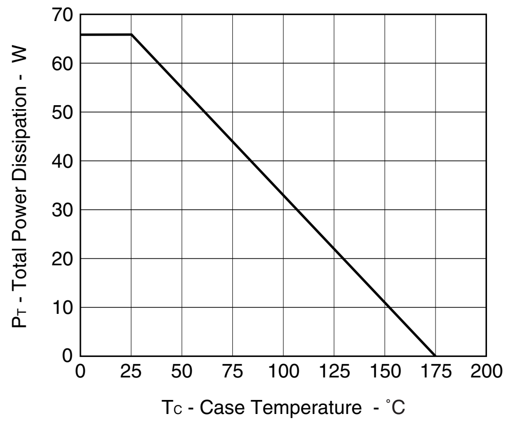


Figure3. FORWARD BIAS SAFE OPERATING AREA

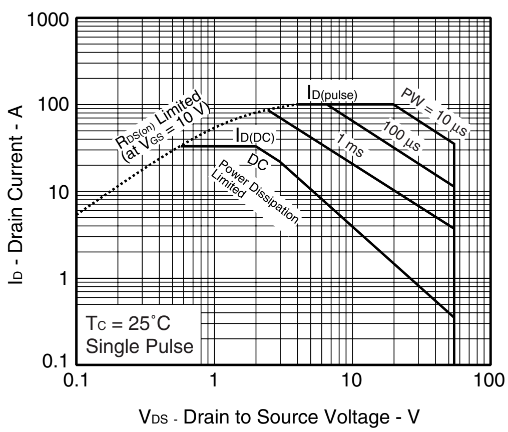


Figure4. SINGLE AVALANCHE ENERGY DERATING FACTOR

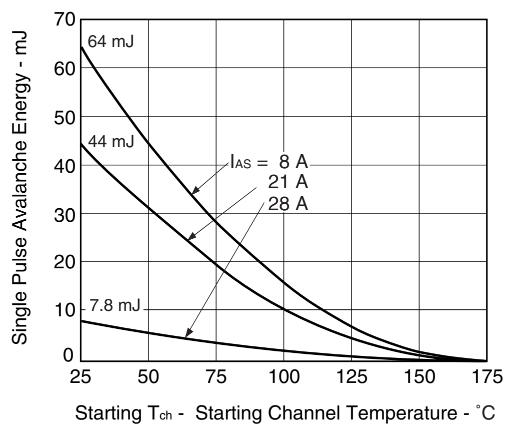


Figure5. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

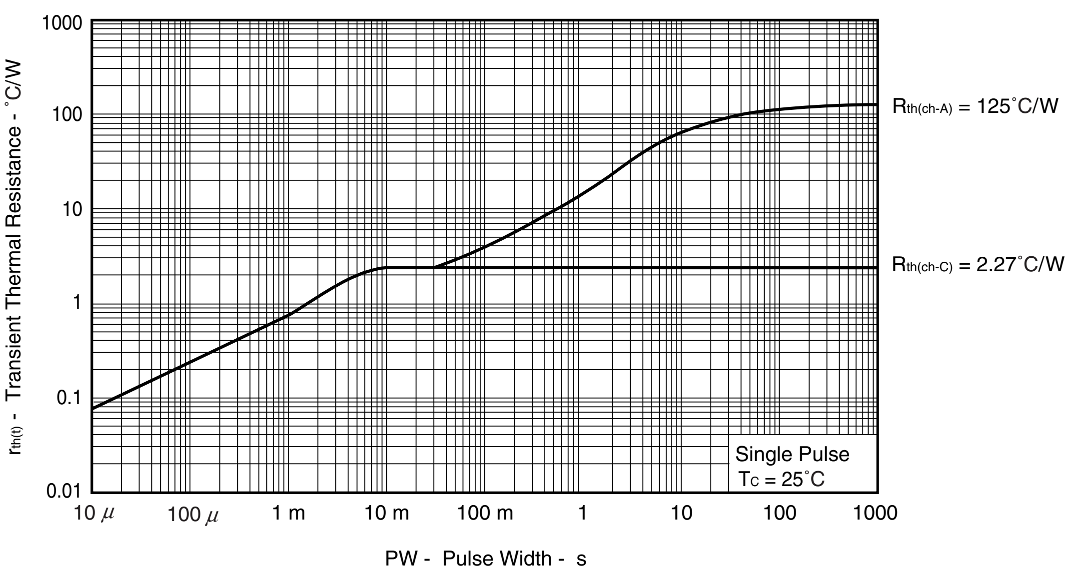


Figure6. FORWARD TRANSFER CHARACTERISTICS

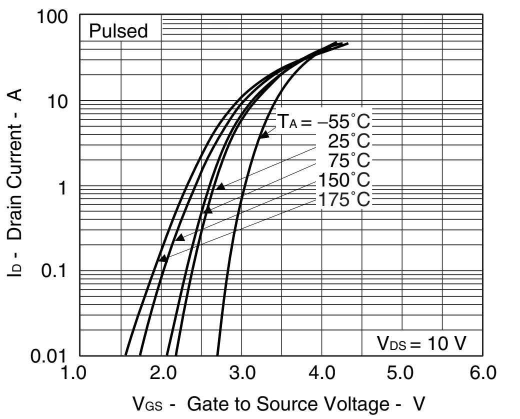


Figure7. DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

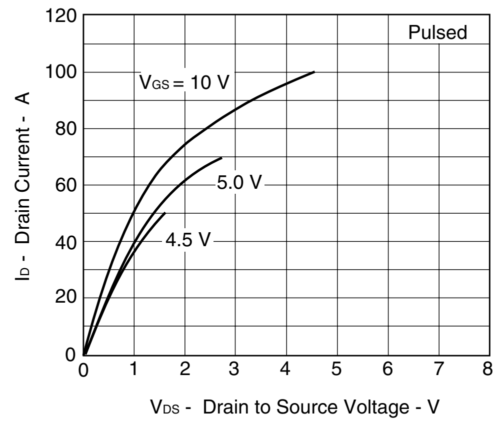


Figure8. FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT

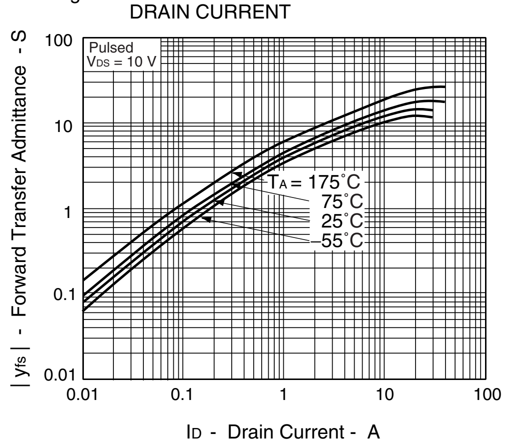


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE

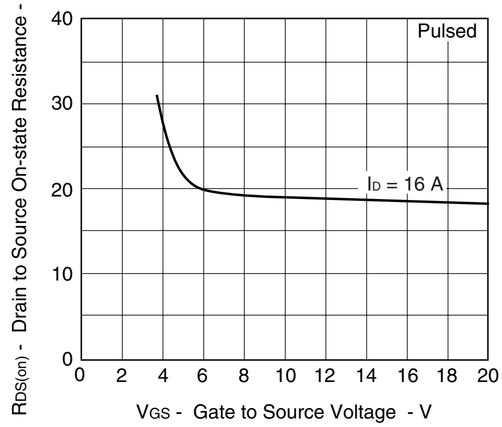


Figure10. DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT

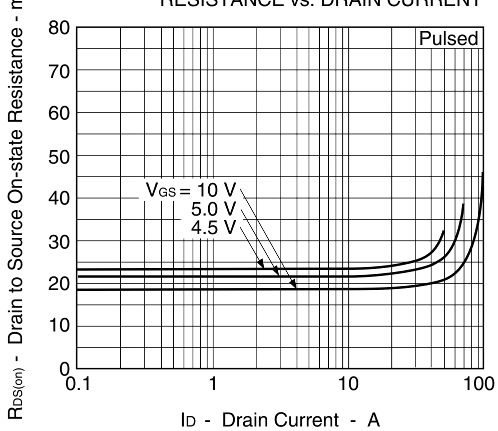


Figure11. GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE

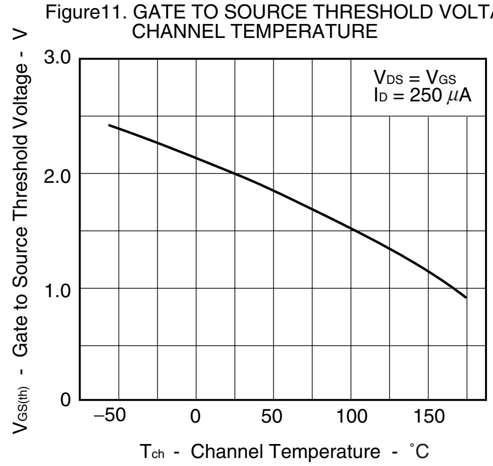


Figure12. DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

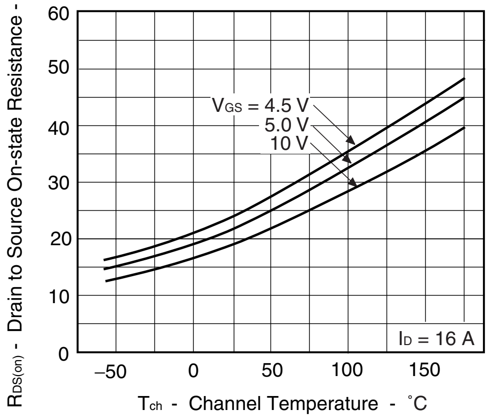


Figure13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

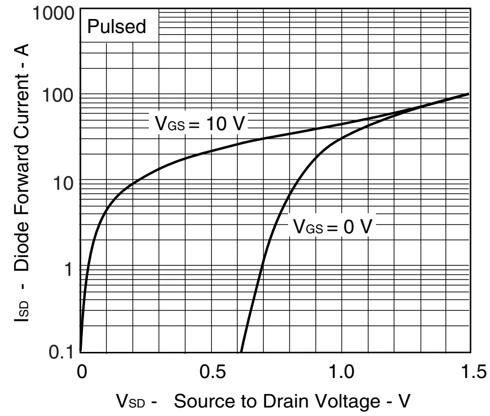


Figure14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

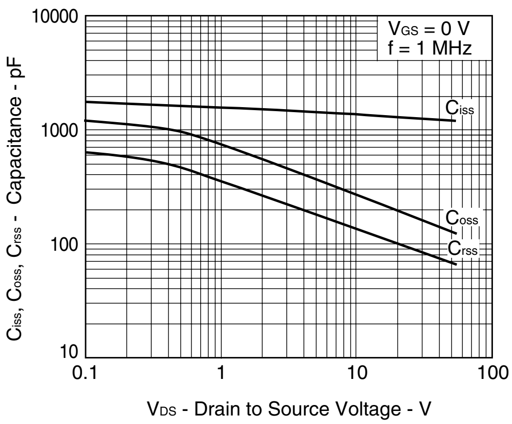


Figure15. SWITCHING CHARACTERISTICS

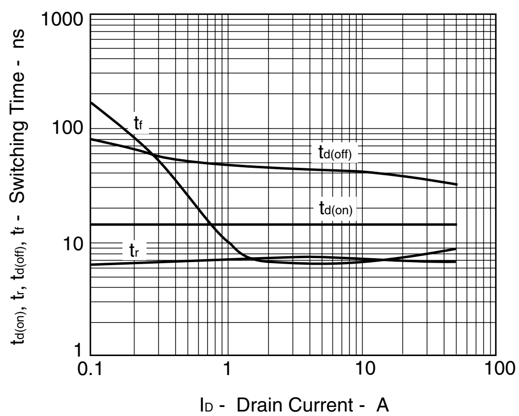


Figure16. REVERSE RECOVERY TIME vs. DRAIN CURRENT

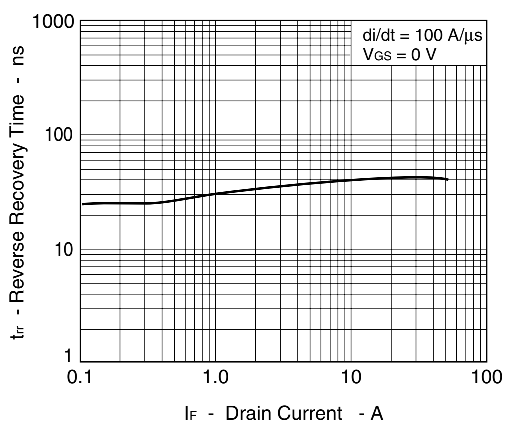
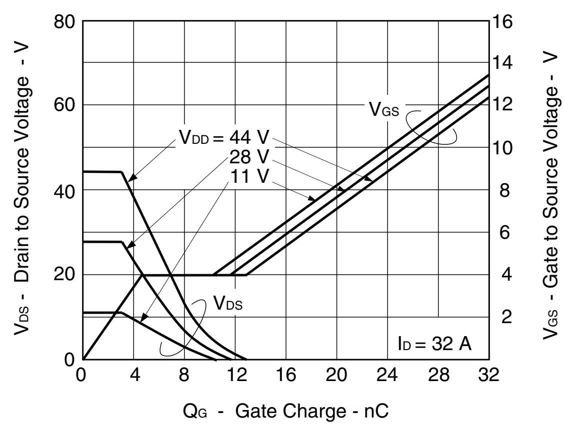
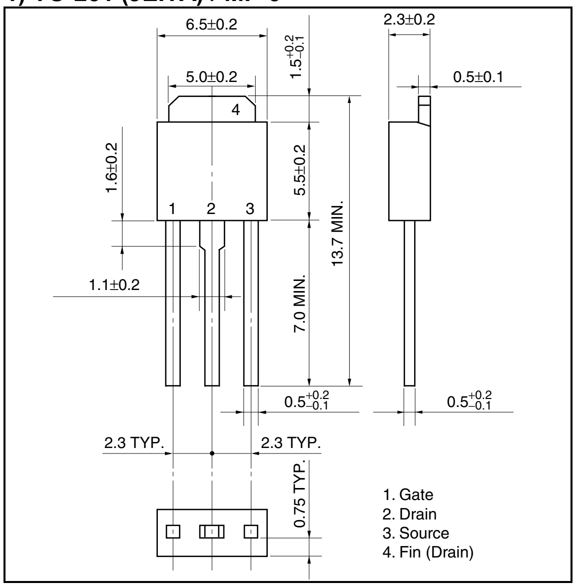


Figure17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

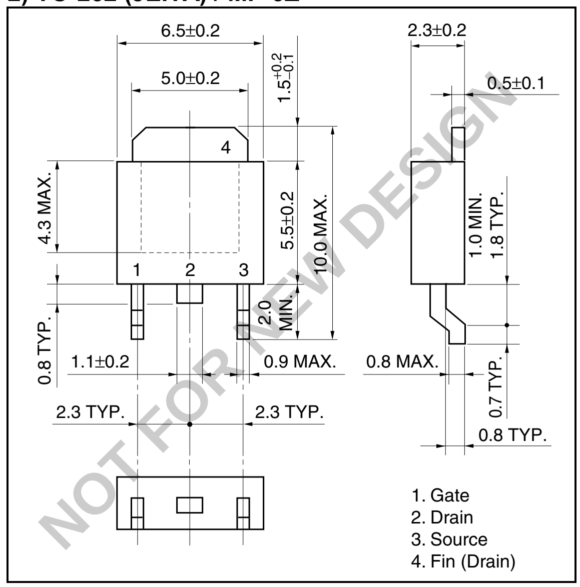


★ PACKAGE DRAWINGS (Unit: mm)

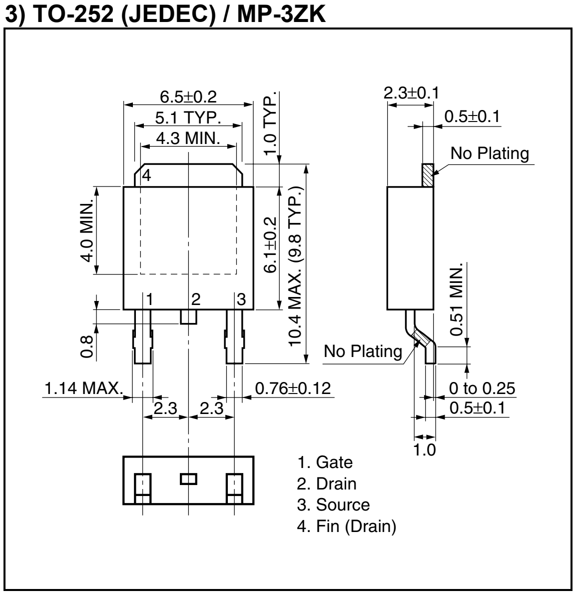
1) TO-251 (JEITA) / MP-3



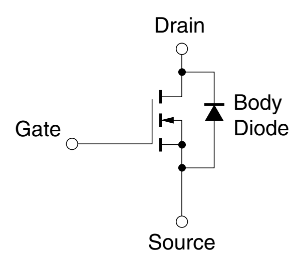
2) TO-252 (JEITA) / MP-3Z



3) TO-252 (JEDEC) / MP-3ZK



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.