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## 1. Overview

### 1.1 Features

The R8C/36T-A Group of single-chip microcontrollers (MCUs) incorporates the R8C CPU core, which provides sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, the CPU core is capable of executing instructions at high speed. In addition, it features a multiplier for high-speed arithmetic processing.

Power consumption is low, and additional power control is possible by selecting the operating mode. The R8C/36T-A Group is also designed to maximize EMI/EMS performance.

Integration of many peripheral functions, including multifunction timer and serial interface on the same chip, reduces the number of system components.

The R8C/36T-A Group integrates a touch sensor control unit, which enables detection of the floating capacitance of the electrostatic capacitive touch electrode.

This group also has on-chip data flash (1 KB × 4 blocks) with background operation (BGO) function.

#### 1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

## 1.1.2 Specifications

Tables 1.1 and 1.2 outline Specifications.

**Table 1.1 Specifications (1)**

| Item                           | Function                  | Description   |
|--------------------------------|---------------------------|---|
| CPU                            | Central processing unit   | R8C CPU core <ul style="list-style-type: none"> <li>Number of fundamental instructions: 89</li> <li>Minimum instruction execution time: <ul style="list-style-type: none"> <li>50 ns (CPU clock = 20 MHz, VCC = 2.7 V to 5.5 V)</li> <li>200 ns (CPU clock = 5 MHz, VCC = 1.8 V to 5.5 V)</li> </ul> </li> <li>Multiplier: 16 bits × 16 bits → 32 bits</li> <li>Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits</li> <li>Operating mode: Single-chip mode (address space: 1 Mbyte)</li> </ul>  |
| Memory                         | ROM, RAM, data flash      | Refer to <b>Table 1.3 Product List</b> .  |
| Voltage detection              | Voltage detection circuit | <ul style="list-style-type: none"> <li>Power-on reset</li> <li>Voltage detection with three check points (the detection levels for voltage detection 0 and voltage detection 1 can be selected.)</li> </ul>   |
| I/O ports                      | Programmable I/O ports    | <ul style="list-style-type: none"> <li>Input only: 1</li> <li>CMOS I/O: 59, selectable pull-up resistor</li> <li>High current drive ports: 59</li> </ul>  |
| Clock                          | Clock generation circuits | <ul style="list-style-type: none"> <li>4 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator</li> <li>Oscillation stop detection: XIN clock oscillation stop detection function</li> <li>Frequency divider circuit: Divided by 1, 2, 4, 8, or 16 can be selected</li> <li>Low-power mode: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode</li> </ul> |
| Interrupts                     |                           | <ul style="list-style-type: none"> <li>Number of interrupt vectors: 69</li> <li>External interrupt inputs: 9 (INT× 5, key input × 4)</li> <li>Priority levels: 7</li> </ul>   |
| Event link controller (ELC)    |                           | <ul style="list-style-type: none"> <li>Events output from peripheral functions can be linked to events input to different peripheral functions. (30 sources × 10 types of event link operations)</li> <li>Events can be handled independently from interrupt requests.</li> </ul>   |
| Watchdog timer                 |                           | <ul style="list-style-type: none"> <li>14 bits × 1</li> <li>Selectable reset start function</li> <li>Selectable low-speed on-chip oscillator for the watchdog timer</li> </ul>  |
| DTC (data transfer controller) |                           | <ul style="list-style-type: none"> <li>1 channel</li> <li>Activation sources: 27</li> <li>Transfer modes: 2 (normal mode, repeat mode)</li> </ul>   |
| Timer                          | Timers RJ_0               | 16 bits × 1: 1 circuit integrated on-chip<br>Timer mode (periodic timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode   |
|                                | Timer RB2_0               | 16 bits × 1: 1 circuit integrated on-chip<br>Timer mode (periodic timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode   |
|                                | Timers RC_0               | 16 bits (with 4 capture/compare registers) × 1: 1 circuit integrated on-chip<br>Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)  |
|                                | Timer RE2                 | 8 bits × 1<br>Compare match timer mode, real-time clock mode  |

**Table 1.2 Specifications (2)**

| Item   | Function                                     | Description  |
|--|--|--|
| Serial interface                             | UART0_0 and<br>UART0_1                       | 2 channels<br>Clock synchronous serial I/O mode, clock asynchronous serial I/O mode  |
|  | UART2  | 1 channel<br>Clock synchronous serial I/O mode, clock asynchronous serial I/O mode, I <sup>2</sup> C mode (I <sup>2</sup> C-bus), multiprocessor communication mode  |
| Clock Synchronous serial interface           | (SSU)<br>SSU_0                               | 1 channel (also used for the I <sup>2</sup> C bus)   |
|  | (I <sup>2</sup> C bus)<br>I <sup>2</sup> C_0 | 1 channel (also used for the SSU)  |
| LIN module                                   | HW-LIN_0                                     | Hardware LIN<br>1 channel (timer RJ_0, UART0_0, or UART0_1 used)   |
| A/D converter                                |  | Resolution: 10 bits × 12 channels, sample and hold function, sweep mode  |
| Comparator B                                 |  | 2 circuits   |
| Touch Sensor control unit (TSCU)             |  | System CH × 4, electrostatic capacitive touch detection × 28   |
| CRC calculator                               |  | CRC-CCITT ( $X^{16} + X^{12} + X^5 + 1$ ), CRC-16 ( $X^{16} + X^{15} + X^2 + 1$ ) compliant  |
| Flash memory                                 |  | <ul style="list-style-type: none"> <li>• Program/erase voltage: VCC = 2.7 V to 5.5 V</li> <li>• Program/erase endurance: 10,000 times (data flash)<br/>1,000 times (program ROM)</li> <li>• Program security: ROM codeprotect, ID code check</li> <li>• Debug functions: On-chip debug, on-board flash rewrite function</li> <li>• BGO (background operation) function (data flash)</li> </ul> |
| Operating frequency/<br>Power supply voltage |  | CPU clock = 20 MHz (VCC = 2.7 V to 5.5 V)<br>CPU clock = 5 MHz (VCC = 1.8 V to 5.5 V)  |
| Current consumption                          |  | Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz)<br>Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz)<br>Typ. 4.0 μA (VCC = 3.0 V, wait mode f(XCIN) = 32 kHz)<br>Typ. 2.2 μA (VCC = 3.0 V, stop mode)  |
| Operating ambient temperature                |  | -20°C to 85°C (N version)<br>-40°C to 85°C (D version) <sup>(1)</sup>  |
| Package                                      |  | 64-pin LQFP<br>Package code: PLQP0064KB-A (previous code: 64P6Q-A)<br>Package code: PLQP0064GA-A (previous code: 64P6U-A)  |

Note:

1. Specify the D version if it is to be used.

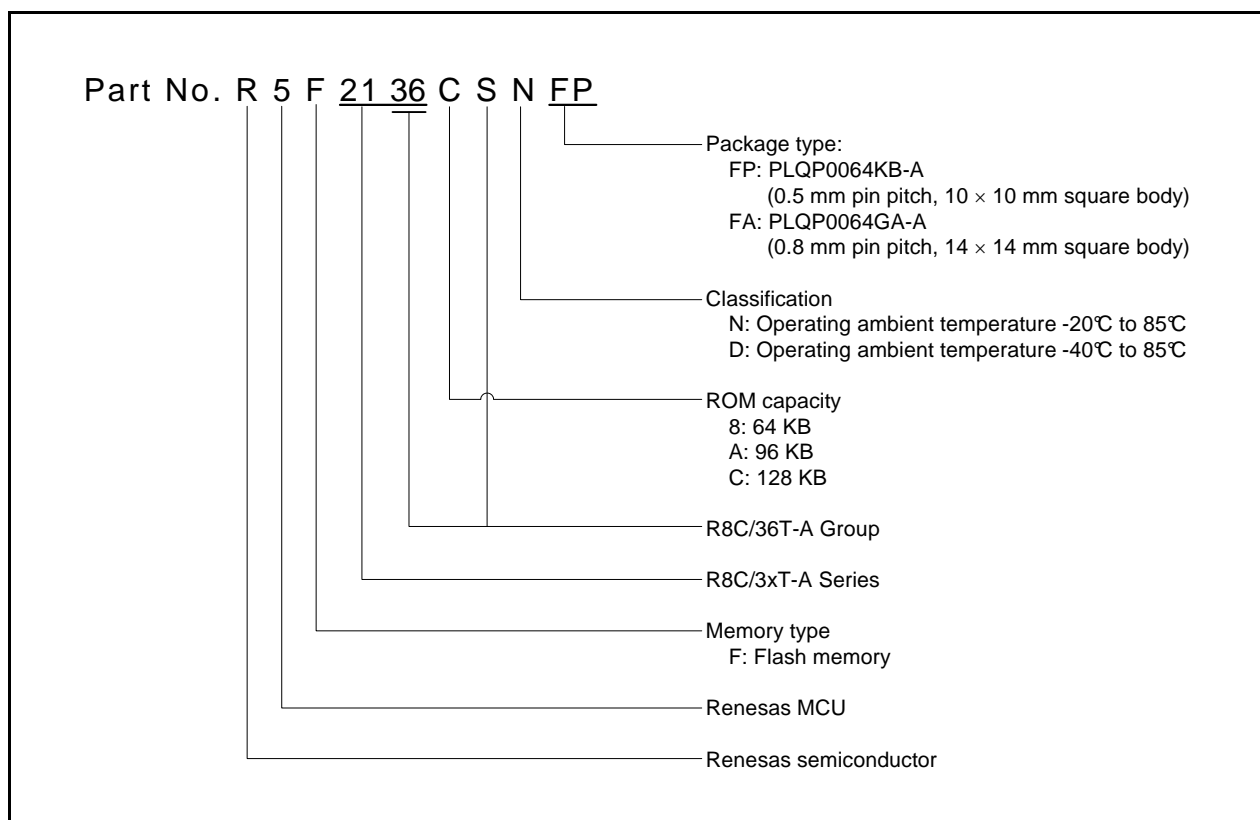
## 1.2 Product List

Table 1.3 lists product information. Figure 1.1 shows the Product Part Number Structure.

**Table 1.3 Product List**

**Current of Dec 2011**

| Part No.     | Internal ROM Capacity |             | Internal RAM Capacity | Package Type | Remarks   |
|--------------|-----------------------|-------------|-----------------------|--------------|-----------|
|              | Program ROM           | Data Flash  |                       |              |           |
| R5F21368SNFP | 64 Kbytes             | 1 Kbyte x 4 | 6 Kbytes              | PLQP0064KB-A | N version |
| R5F2136ASNFP | 96 Kbytes             |             | 8 Kbytes              |              |           |
| R5F2136CSNFP | 128 Kbytes            |             | 10 Kbytes             |              |           |
| R5F21368SNFA | 64 Kbytes             |             | 6 Kbytes              | PLQP0064GA-A |           |
| R5F2136ASNFA | 96 Kbytes             |             | 8 Kbytes              |              |           |
| R5F2136CSNFA | 128 Kbytes            |             | 10 Kbytes             |              |           |
| R5F21368SDFP | 64 Kbytes             |             | 6 Kbytes              | PLQP0064KB-A | D version |
| R5F2136ASDFP | 96 Kbytes             |             | 8 Kbytes              |              |           |
| R5F2136CSDFP | 128 Kbytes            |             | 10 Kbytes             |              |           |
| R5F21368SDFA | 64 Kbytes             |             | 6 Kbytes              | PLQP0064GA-A |           |
| R5F2136ASDFA | 96 Kbytes             |             | 8 Kbytes              |              |           |
| R5F2136CSDFA | 128 Kbytes            |             | 10 Kbytes             |              |           |



**Figure 1.1 Product Part Number Structure**

### 1.3 Block Diagram

Figure 1.2 shows the Block Diagram.

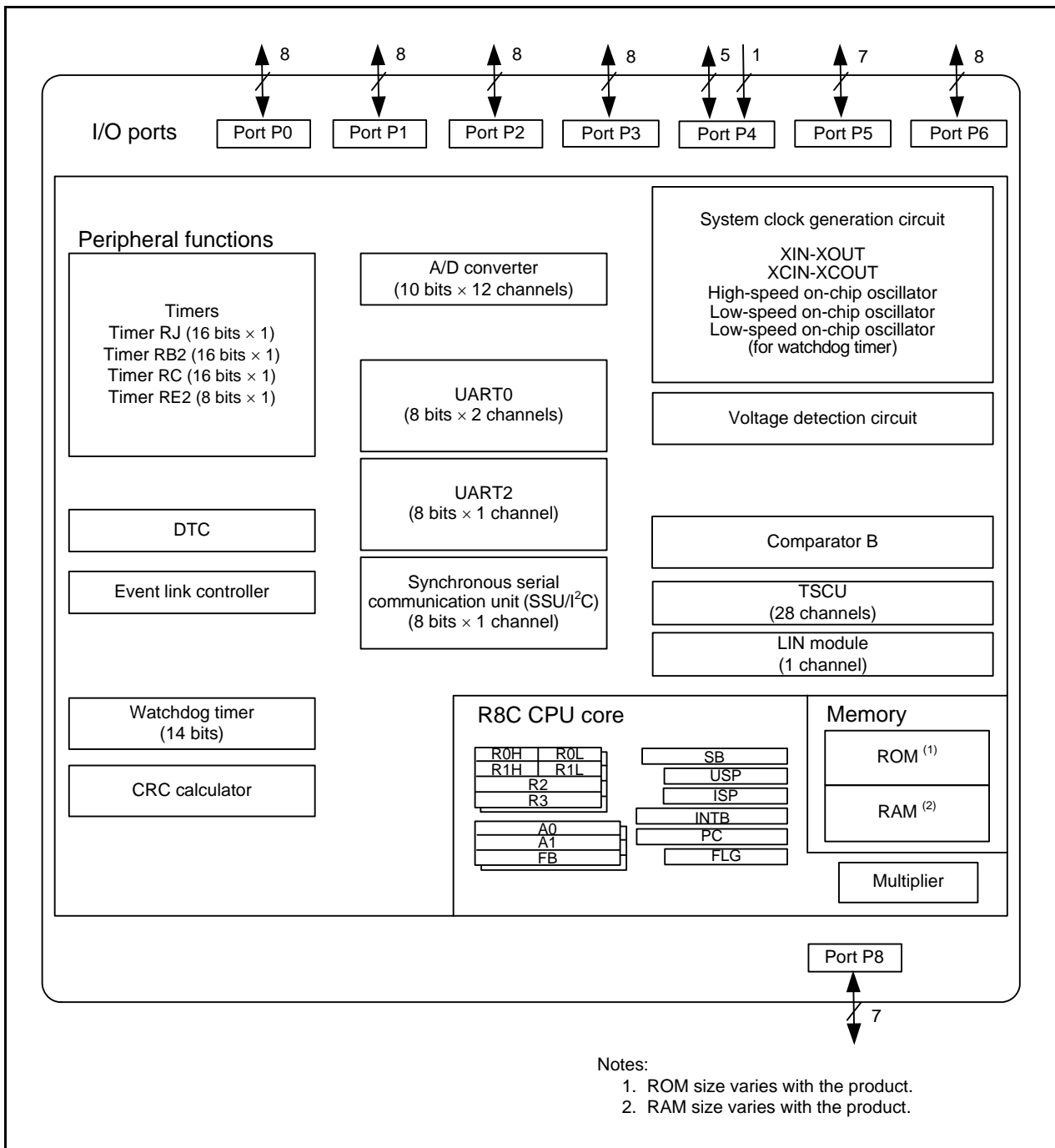


Figure 1.2 Block Diagram

### 1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Tables 1.4 to 1.6 list the Pin Name Information by Pin Number.

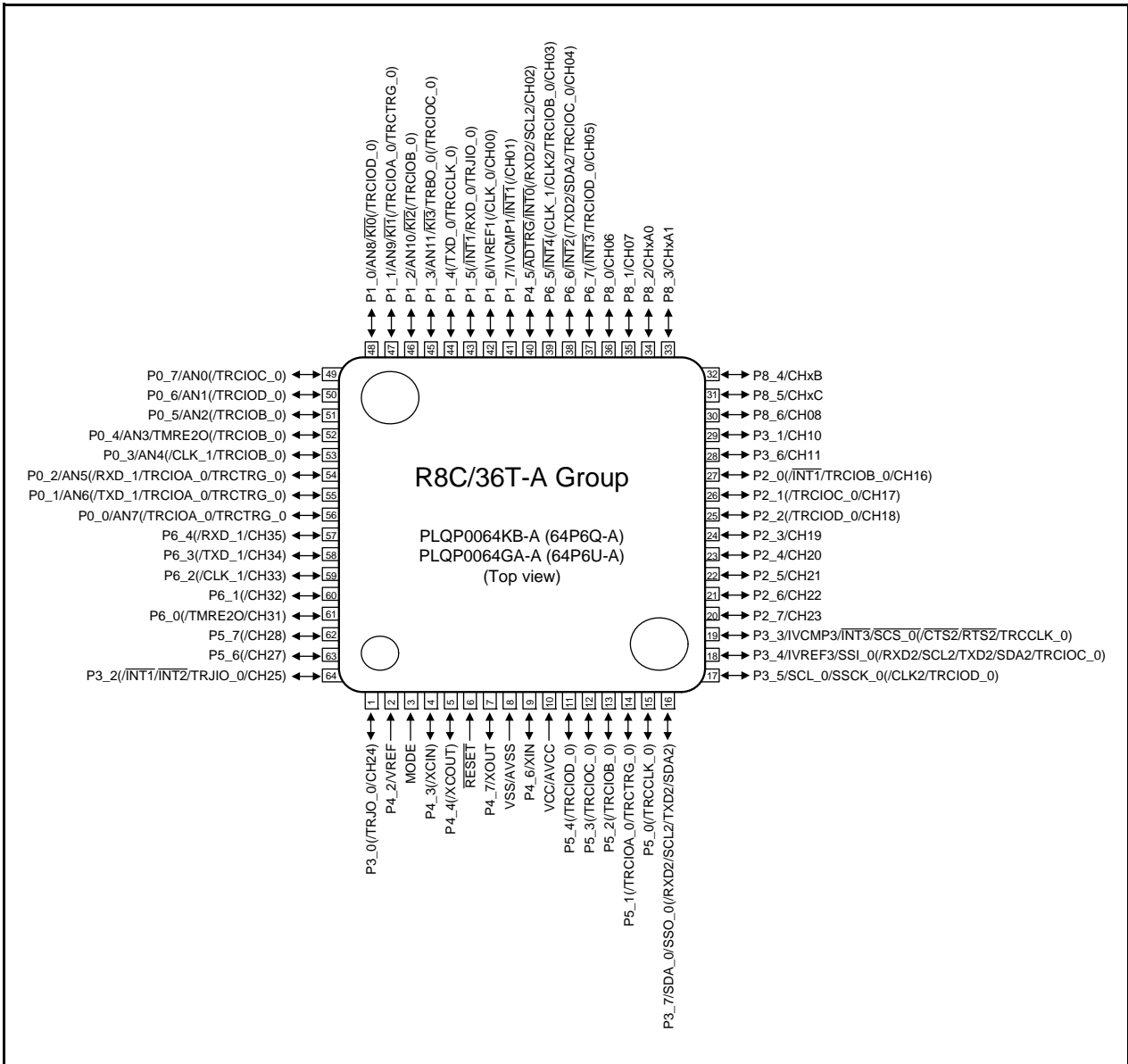


Figure 1.3 Pin Assignment (Top View)

**Table 1.4 Pin Name Information by Pin Number (INT, URAT0, and UART2)**

| Port | Pin No. | INT  |      |      |      | UART0 |       |       |       |       |       | UART2 |      |      |      |      |      |      |      |
|------|---------|------|------|------|------|-------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|
|      |         | INT0 | INT1 | INT2 | INT3 | INT4  | TXD_0 | TXD_1 | RXD_0 | RXD_1 | CLK_0 | CLK_1 | TXD2 | RXD2 | CTS2 | RTS2 | SDA2 | SCL2 | CLK2 |
| P0_0 | 56      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P0_1 | 55      |      |      |      |      |       |       | TXD_1 |       |       |       |       |      |      |      |      |      |      |      |
| P0_2 | 54      |      |      |      |      |       |       |       | RXD_1 |       |       |       |      |      |      |      |      |      |      |
| P0_3 | 53      |      |      |      |      |       |       |       |       |       | CLK_1 |       |      |      |      |      |      |      |      |
| P0_4 | 52      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P0_5 | 51      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P0_6 | 50      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P0_7 | 49      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P1_0 | 48      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P1_1 | 47      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P1_2 | 46      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P1_3 | 45      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P1_4 | 44      |      |      |      |      |       | TXD_0 |       |       |       |       |       |      |      |      |      |      |      |      |
| P1_5 | 43      |      | INT1 |      |      |       |       | RXD_0 |       |       |       |       |      |      |      |      |      |      |      |
| P1_6 | 42      |      |      |      |      |       |       |       |       | CLK_0 |       |       |      |      |      |      |      |      |      |
| P1_7 | 41      |      | INT1 |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P2_0 | 27      |      | INT1 |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P2_1 | 26      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P2_2 | 25      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P2_3 | 24      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P2_4 | 23      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P2_5 | 22      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P2_6 | 21      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P2_7 | 20      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P3_0 | 1       |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P3_1 | 29      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P3_2 | 64      |      | INT1 | INT2 |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P3_3 | 19      |      |      |      | INT3 |       |       |       |       |       |       |       |      | CTS2 | RTS2 |      |      |      |      |
| P3_4 | 18      |      |      |      |      |       |       |       |       |       |       | TXD2  | RXD2 |      |      | SDA2 | SCL2 |      |      |
| P3_5 | 17      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      | CLK2 |
| P3_6 | 28      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P3_7 | 16      |      |      |      |      |       |       |       |       |       |       | TXD2  | RXD2 |      |      | SDA2 | SCL2 |      |      |
| P4_2 | 2       |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P4_3 | 4       |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P4_4 | 5       |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P4_5 | 40      | INT0 |      |      |      |       |       |       |       |       |       |       | RXD2 |      |      |      | SCL2 |      |      |
| P4_6 | 9       |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P4_7 | 7       |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P5_0 | 15      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P5_1 | 14      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P5_2 | 13      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P5_3 | 12      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P5_4 | 11      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P5_6 | 63      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P5_7 | 62      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P6_0 | 61      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P6_1 | 60      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P6_2 | 59      |      |      |      |      |       |       |       |       |       | CLK_1 |       |      |      |      |      |      |      |      |
| P6_3 | 58      |      |      |      |      |       |       | TXD_1 |       |       |       |       |      |      |      |      |      |      |      |
| P6_4 | 57      |      |      |      |      |       |       |       | RXD_1 |       |       |       |      |      |      |      |      |      |      |
| P6_5 | 39      |      |      |      |      |       |       |       |       |       | CLK_1 |       |      |      |      |      |      |      | CLK2 |
| P6_6 | 38      |      |      | INT2 |      |       |       |       |       |       |       | TXD2  |      |      |      | SDA2 |      |      |      |
| P6_7 | 37      |      |      |      | INT3 |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P8_0 | 36      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P8_1 | 35      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P8_2 | 34      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P8_3 | 33      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P8_4 | 32      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P8_5 | 31      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |
| P8_6 | 30      |      |      |      |      |       |       |       |       |       |       |       |      |      |      |      |      |      |      |

**Table 1.5 Pin Name Information by Pin Number (SSU/I<sup>2</sup>C, Timer RJ, and Timer RB2)**

| Port | Pin No. | SSU/I <sup>2</sup> C |       |       |       |        |       | Timer RJ |        | Timer RB2 |
|------|---------|----------------------|-------|-------|-------|--------|-------|----------|--------|-----------|
|      |         | SCL_0                | SDA_0 | SSI_0 | SCS_0 | SSCK_0 | SSO_0 | TRJO_0   | TRJO_0 | TRBO_0    |
| P0_0 | 56      |                      |       |       |       |        |       |          |        |           |
| P0_1 | 55      |                      |       |       |       |        |       |          |        |           |
| P0_2 | 54      |                      |       |       |       |        |       |          |        |           |
| P0_3 | 53      |                      |       |       |       |        |       |          |        |           |
| P0_4 | 52      |                      |       |       |       |        |       |          |        |           |
| P0_5 | 51      |                      |       |       |       |        |       |          |        |           |
| P0_6 | 50      |                      |       |       |       |        |       |          |        |           |
| P0_7 | 49      |                      |       |       |       |        |       |          |        |           |
| P1_0 | 48      |                      |       |       |       |        |       |          |        |           |
| P1_1 | 47      |                      |       |       |       |        |       |          |        |           |
| P1_2 | 46      |                      |       |       |       |        |       |          |        |           |
| P1_3 | 45      |                      |       |       |       |        |       |          |        | TRBO_0    |
| P1_4 | 44      |                      |       |       |       |        |       |          |        |           |
| P1_5 | 43      |                      |       |       |       |        |       |          | TRJO_0 |           |
| P1_6 | 42      |                      |       |       |       |        |       |          |        |           |
| P1_7 | 41      |                      |       |       |       |        |       |          |        |           |
| P2_0 | 27      |                      |       |       |       |        |       |          |        |           |
| P2_1 | 26      |                      |       |       |       |        |       |          |        |           |
| P2_2 | 25      |                      |       |       |       |        |       |          |        |           |
| P2_3 | 24      |                      |       |       |       |        |       |          |        |           |
| P2_4 | 23      |                      |       |       |       |        |       |          |        |           |
| P2_5 | 22      |                      |       |       |       |        |       |          |        |           |
| P2_6 | 21      |                      |       |       |       |        |       |          |        |           |
| P2_7 | 20      |                      |       |       |       |        |       |          |        |           |
| P3_0 | 1       |                      |       |       |       |        |       | TRJO_0   |        |           |
| P3_1 | 29      |                      |       |       |       |        |       |          |        |           |
| P3_2 | 64      |                      |       |       |       |        |       |          | TRJO_0 |           |
| P3_3 | 19      |                      |       |       | SCS_0 |        |       |          |        |           |
| P3_4 | 18      |                      |       | SSI_0 |       |        |       |          |        |           |
| P3_5 | 17      | SCL_0                |       |       |       | SSCK_0 |       |          |        |           |
| P3_6 | 28      |                      |       |       |       |        |       |          |        |           |
| P3_7 | 16      |                      | SDA_0 |       |       |        | SSO_0 |          |        |           |
| P4_2 | 2       |                      |       |       |       |        |       |          |        |           |
| P4_3 | 4       |                      |       |       |       |        |       |          |        |           |
| P4_4 | 5       |                      |       |       |       |        |       |          |        |           |
| P4_5 | 40      |                      |       |       |       |        |       |          |        |           |
| P4_6 | 9       |                      |       |       |       |        |       |          |        |           |
| P4_7 | 7       |                      |       |       |       |        |       |          |        |           |
| P5_0 | 15      |                      |       |       |       |        |       |          |        |           |
| P5_1 | 14      |                      |       |       |       |        |       |          |        |           |
| P5_2 | 13      |                      |       |       |       |        |       |          |        |           |
| P5_3 | 12      |                      |       |       |       |        |       |          |        |           |
| P5_4 | 11      |                      |       |       |       |        |       |          |        |           |
| P5_6 | 63      |                      |       |       |       |        |       |          |        |           |
| P5_7 | 62      |                      |       |       |       |        |       |          |        |           |
| P6_0 | 61      |                      |       |       |       |        |       |          |        |           |
| P6_1 | 60      |                      |       |       |       |        |       |          |        |           |
| P6_2 | 59      |                      |       |       |       |        |       |          |        |           |
| P6_3 | 58      |                      |       |       |       |        |       |          |        |           |
| P6_4 | 57      |                      |       |       |       |        |       |          |        |           |
| P6_5 | 39      |                      |       |       |       |        |       |          |        |           |
| P6_6 | 38      |                      |       |       |       |        |       |          |        |           |
| P6_7 | 37      |                      |       |       |       |        |       |          |        |           |
| P8_0 | 36      |                      |       |       |       |        |       |          |        |           |
| P8_1 | 35      |                      |       |       |       |        |       |          |        |           |
| P8_2 | 34      |                      |       |       |       |        |       |          |        |           |
| P8_3 | 33      |                      |       |       |       |        |       |          |        |           |
| P8_4 | 32      |                      |       |       |       |        |       |          |        |           |
| P8_5 | 31      |                      |       |       |       |        |       |          |        |           |
| P8_6 | 30      |                      |       |       |       |        |       |          |        |           |



**Table 1.6 Pin Name Information by Pin Number (Timer RC, Timer RE2, and Others)**

| Port | Pin No. | Timer RC |          |          |          |          |          | Timer RE2 | Others |     |       |
|------|---------|----------|----------|----------|----------|----------|----------|-----------|--------|-----|-------|
|      |         | TRCCLK_0 | TRCIOA_0 | TRCIOB_0 | TRCIOC_0 | TRCIOD_0 | TRCTRG_0 | TMRE20    |        |     |       |
| P0_0 | 56      |          | TRCIOA_0 |          |          |          | TRCTRG_0 |           | AN7    |     |       |
| P0_1 | 55      |          | TRCIOA_0 |          |          |          | TRCTRG_0 |           | AN6    |     |       |
| P0_2 | 54      |          | TRCIOA_0 |          |          |          | TRCTRG_0 |           | AN5    |     |       |
| P0_3 | 53      |          |          | TRCIOB_0 |          |          |          |           | AN4    |     |       |
| P0_4 | 52      |          |          | TRCIOB_0 |          |          |          | TMRE20    | AN3    |     |       |
| P0_5 | 51      |          |          | TRCIOB_0 |          |          |          |           | AN2    |     |       |
| P0_6 | 50      |          |          |          |          | TRCIOD_0 |          |           | AN1    |     |       |
| P0_7 | 49      |          |          |          | TRCIOC_0 |          |          |           | AN0    |     |       |
| P1_0 | 48      |          |          |          |          | TRCIOD_0 |          |           | AN8    | K10 |       |
| P1_1 | 47      |          | TRCIOA_0 |          |          |          | TRCTRG_0 |           | AN9    | K11 |       |
| P1_2 | 46      |          |          | TRCIOB_0 |          |          |          |           | AN10   | K12 |       |
| P1_3 | 45      |          |          |          | TRCIOC_0 |          |          |           | AN11   | K13 |       |
| P1_4 | 44      | TRCCLK_0 |          |          |          |          |          |           |        |     |       |
| P1_5 | 43      |          |          |          |          |          |          |           |        |     |       |
| P1_6 | 42      |          |          |          |          |          |          |           | IVREF1 |     | CH00  |
| P1_7 | 41      |          |          |          |          |          |          |           | IVCMP1 |     | CH01  |
| P2_0 | 27      |          |          | TRCIOB_0 |          |          |          |           |        |     | CH16  |
| P2_1 | 26      |          |          |          | TRCIOC_0 |          |          |           |        |     | CH17  |
| P2_2 | 25      |          |          |          |          | TRCIOD_0 |          |           |        |     | CH18  |
| P2_3 | 24      |          |          |          |          |          |          |           |        |     | CH19  |
| P2_4 | 23      |          |          |          |          |          |          |           |        |     | CH20  |
| P2_5 | 22      |          |          |          |          |          |          |           |        |     | CH21  |
| P2_6 | 21      |          |          |          |          |          |          |           |        |     | CH22  |
| P2_7 | 20      |          |          |          |          |          |          |           |        |     | CH23  |
| P3_0 | 1       |          |          |          |          |          |          |           |        |     | CH24  |
| P3_1 | 29      |          |          |          |          |          |          |           |        |     | CH10  |
| P3_2 | 64      |          |          |          |          |          |          |           |        |     | CH25  |
| P3_3 | 19      | TRCCLK_0 |          |          |          |          |          |           | IVCMP3 |     |       |
| P3_4 | 18      |          |          |          | TRCIOC_0 |          |          |           | IVREF3 |     |       |
| P3_5 | 17      |          |          |          |          | TRCIOD_0 |          |           |        |     |       |
| P3_6 | 28      |          |          |          |          |          |          |           |        |     | CH11  |
| P3_7 | 16      |          |          |          |          |          |          |           |        |     |       |
| P4_2 | 2       |          |          |          |          |          |          |           | VREF   |     |       |
| P4_3 | 4       |          |          |          |          |          |          |           | XCIN   |     |       |
| P4_4 | 5       |          |          |          |          |          |          |           | XCOU   |     |       |
| P4_5 | 40      |          |          |          |          |          |          |           | ADTRG  |     | CH02  |
| P4_6 | 9       |          |          |          |          |          |          |           | XIN    |     |       |
| P4_7 | 7       |          |          |          |          |          |          |           | XOUT   |     |       |
| P5_0 | 15      | TRCCLK_0 |          |          |          |          |          |           |        |     |       |
| P5_1 | 14      |          | TRCIOA_0 |          |          |          | TRCTRG_0 |           |        |     |       |
| P5_2 | 13      |          |          | TRCIOB_0 |          |          |          |           |        |     |       |
| P5_3 | 12      |          |          |          | TRCIOC_0 |          |          |           |        |     |       |
| P5_4 | 11      |          |          |          |          | TRCIOD_0 |          |           |        |     |       |
| P5_6 | 63      |          |          |          |          |          |          |           |        |     | CH27  |
| P5_7 | 62      |          |          |          |          |          |          |           |        |     | CH28  |
| P6_0 | 61      |          |          |          |          |          |          | TMRE20    |        |     | CH31  |
| P6_1 | 60      |          |          |          |          |          |          |           |        |     | CH32  |
| P6_2 | 59      |          |          |          |          |          |          |           |        |     | CH33  |
| P6_3 | 58      |          |          |          |          |          |          |           |        |     | CH34  |
| P6_4 | 57      |          |          |          |          |          |          |           |        |     | CH35  |
| P6_5 | 39      |          |          | TRCIOB_0 |          |          |          |           |        |     | CH03  |
| P6_6 | 38      |          |          |          | TRCIOC_0 |          |          |           |        |     | CH04  |
| P6_7 | 37      |          |          |          |          | TRCIOD_0 |          |           |        |     | CH05  |
| P8_0 | 36      |          |          |          |          |          |          |           |        |     | CH06  |
| P8_1 | 35      |          |          |          |          |          |          |           |        |     | CH07  |
| P8_2 | 34      |          |          |          |          |          |          |           |        |     | CHxA0 |
| P8_3 | 33      |          |          |          |          |          |          |           |        |     | CHxA1 |
| P8_4 | 32      |          |          |          |          |          |          |           |        |     | CHxB  |
| P8_5 | 31      |          |          |          |          |          |          |           |        |     | CHxC  |
| P8_6 | 30      |          |          |          |          |          |          |           |        |     | CH08  |

## 1.5 Pin Functions

Tables 1.7 and 1.8 list Pin Functions.

**Table 1.7 Pin Functions (1)**

| Item  | Pin Name   | I/O | Description   |
|---|--|-----|---|
| Power supply input                            | VCC, VSS   | —   | Apply 1.8 V through 5.5 V to the VCC pin.<br>Apply 0 V to the VSS pin.  |
| Analog power supply input                     | AVCC, AVSS   | —   | Power supply input for the A/D converter.<br>Connect a capacitor between pins AVCC and AVSS.  |
| Reset input                                   | $\overline{\text{RESET}}$                            | I   | Applying a low level to this pin resets the MCU.  |
| MODE  | MODE   | I   | Connect this pin to the VCC pin via a resistor.   |
| XIN clock input                               | XIN  | I   | I/O for the XIN clock generation circuit.   |
| XIN clock output                              | XOUT   | I/O | Connect a ceramic resonator or a crystal oscillator between pins XIN and XOUT. <sup>(1)</sup><br>To use an external clock, input it to the XIN pin and leave the XOUT pin open. |
| XCIN clock input                              | XCIN   | I   | I/O for the XCIN clock generation circuit.  |
| XCIN clock output                             | XCOU   | I/O | Connect a crystal oscillator between pins XCIN and XCOU. <sup>(1)</sup><br>To use an external clock, input it to the XCOU pin and leave the XCIN pin open.                      |
| $\overline{\text{INT}}$ interrupt input       | $\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ | I   | $\overline{\text{INT}}$ interrupt input.  |
| Key input interrupt                           | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$   | I   | Key input interrupt input.  |
| Timer RJ_0                                    | TRJIO_0  | I/O | Input/output for timer RJ.  |
|   | TRJO_0   | O   | Output for timer RJ.  |
| Timer RB2_0                                   | TRBO_0   | O   | Output for timer RB2.   |
| Timer RC_0                                    | TRCLK_0  | I   | External clock input.   |
|   | TRCTRG_0   | I   | External trigger input.   |
|   | TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0               | I/O | Input/output for timer RC.  |
|   | TMRE2O   | O   | Divided clock output.   |
| Serial interface (UART0)                      | CLK_0, CLK_1   | I/O | Transfer clock input/output.  |
|   | RXD_0, RXD_1   | I   | Serial data input.  |
|   | TXD_0, TXD_1   | O   | Serial data output.   |
| Serial interface (UART2)                      | $\overline{\text{CTS2}}$                             | I   | Input for transmission control.   |
|   | $\overline{\text{RTS2}}$                             | O   | Output for reception control.   |
|   | SCL2   | I/O | I <sup>2</sup> C mode clock input/output.   |
|   | SDA2   | I/O | I <sup>2</sup> C mode data input/output.  |
|   | RXD2   | I   | Serial data input.  |
|   | TXD2   | O   | Serial data output.   |
|   | CLK2   | I/O | Transfer clock input/output.  |
| Synchronous serial communication unit (SSU_0) | SSI_0  | I/O | Data input/output.  |
|   | $\overline{\text{SCS}}_0$                            | I/O | Chip-select input/output.   |
|   | $\overline{\text{SSCK}}_0$                           | I/O | Clock input/output.   |
|   | SSO_0  | I/O | Data input/output.  |
| I <sup>2</sup> C bus (I <sup>2</sup> C_0)     | SCL_0  | I/O | Clock input/output.   |
|   | SDA_0  | I/O | Data input/output.  |
| Reference voltage input                       | VREF   | I   | Reference voltage input for the A/D converter.  |

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

**Table 1.8 Pin Functions (2)**

| Item                      | Pin Name   | I/O | Description  |
|---------------------------|--|-----|--|
| A/D converter             | AN0 to AN11  | I   | Analog input for the A/D converter.  |
|                           | ADTRG  | I   | External trigger input for the A/D converter.  |
| Comparator B              | IVCMP1, IVCMP3   | I   | Analog voltage input for comparator B.   |
|                           | IVREF1, IVREF3   | I   | Reference voltage input for comparator B.  |
| Touch sensor control unit | CHxA0, CHxA1, CHxB, CHxC   | I/O | Control pins for electrostatic capacitive touch detection.   |
|                           | CH00 to CH08, CH10, CH11, CH16 to CH25, CH27, CH28, CH31 to CH35   | I   | Electrostatic capacitive touch detection pins.   |
| I/O ports                 | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6_0 to P6_7, P8_0 to P8_6 | I/O | 8-bit CMOS input/output ports. Each port has an I/O select direction register, enabling switching input and output for each pin. For input ports, the presence or absence of a pull-up resistor can be selected by a program. All ports can be used as LED drive (high drive) ports. |
| Input port                | P4_2   | I   | Input-only port.   |

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the 13 CPU Registers. The registers R0, R1, R2, R3, A0, A1, and FB form a single register bank. The CPU has two register banks.

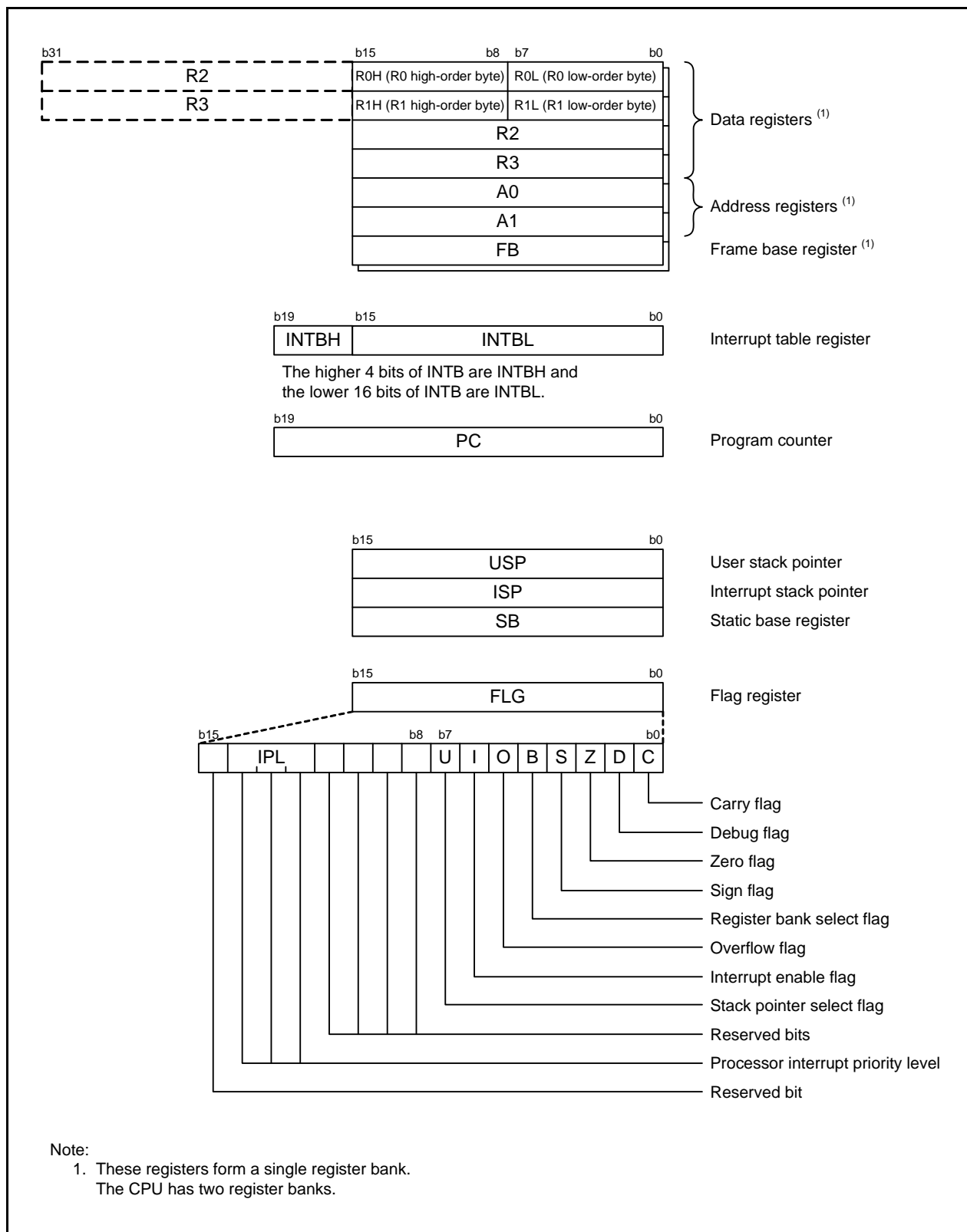


Figure 2.1 CPU Registers

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 through R3.

R0 can be split into high-order (R0H) and low-order (R0L) registers to be used separately as 8-bit data registers. The same applies to R1H and R1L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). Similarly, R3 and R1 can be used as a 32-bit data register.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 functions in the same manner as A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register used for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

## 2.5 Program Counter (PC)

PC is a 20-bit register that indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of the FLG register is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated in the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. It must only be set to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0. Otherwise it is set to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value. Otherwise it is set to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow. Otherwise it is set to 0.

### **2.8.7 Interrupt Enable Flag (I)**

The I flag enables maskable interrupts. Interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is set to 0 when an interrupt request is acknowledged.

### **2.8.8 Stack Pointer Select Flag (U)**

ISP is selected when the U flag is 0. USP is selected when the U flag is 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction for a software interrupt numbered from 0 to 31 is executed.

### **2.8.9 Processor Interrupt Priority Level (IPL)**

IPL is 3 bits wide and assigns eight processor interrupt priority levels from 0 to 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

### **2.8.10 Reserved Bit**

The write value must be 0. The read value is undefined.

## 3. Address Space

### 3.1 Memory Map

Figure 3.1 shows the Memory Map. The R8C/36T-A Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. Up to 32 Kbytes of the internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. The area in excess of 32 Kbytes is allocated at higher addresses, beginning with address 10000h. For example, a 64-Kbyte internal ROM is allocated at addresses 08000h to 17FFFh.

The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated at addresses 07000h to 07FFFh.

The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM is allocated at addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated at addresses 00000h to 02FFFh and addresses 06800h to 06FFFh.

Peripheral function control registers are allocated here. All unallocated locations within the SFRs are reserved and cannot be accessed by users.

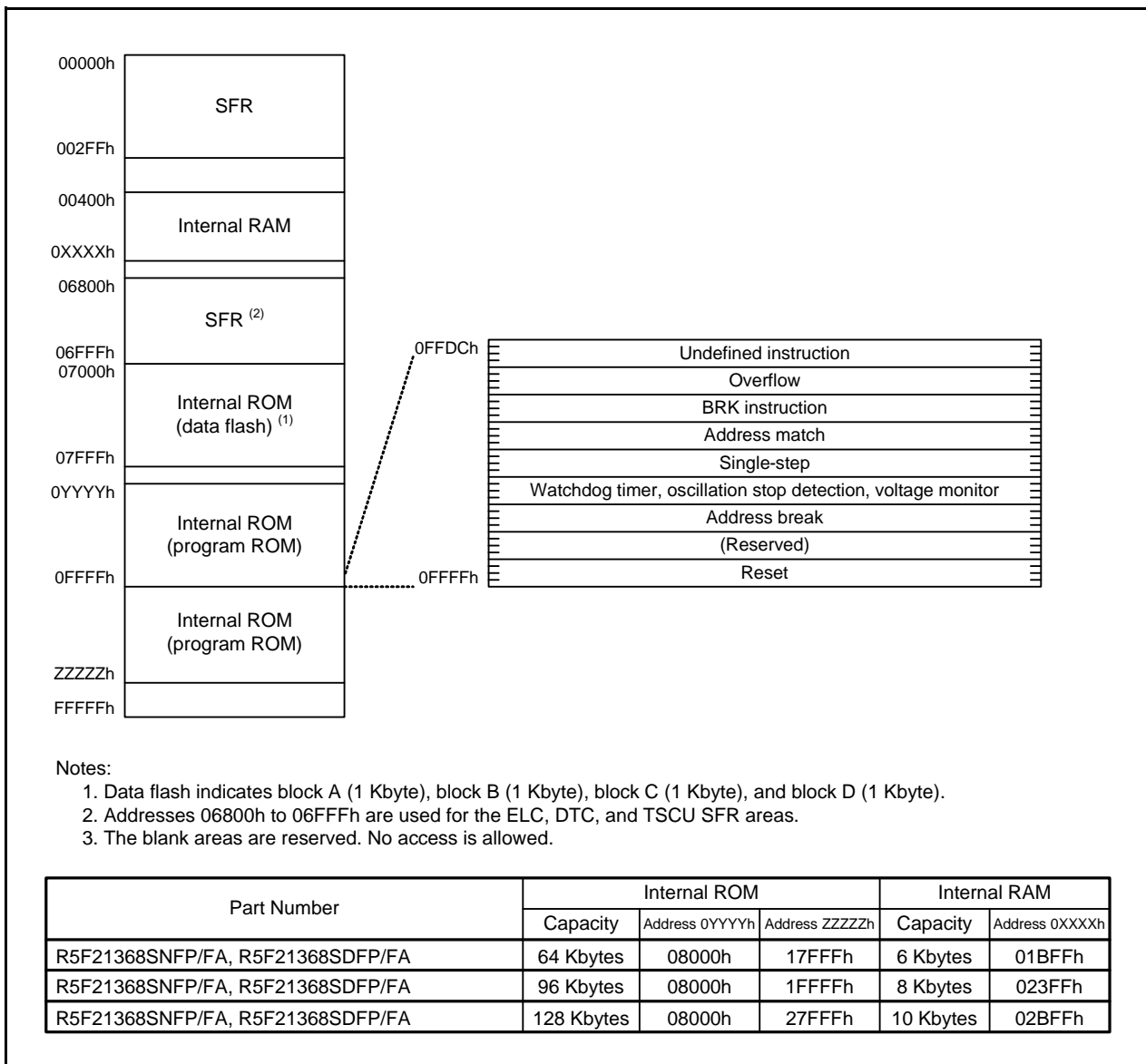


Figure 3.1 Memory Map

### 3.2 Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 3.1 to 3.16 list the SFR Information. Table 3.17 lists the ID code Area, Option Function Select Area.

**Table 3.1 SFR Information (1) (1)**

| Address | Symbol   | Register Name                                    | After Reset               | Remarks  |
|---------|----------|--|---------------------------|----------|
| 0000h   |          |  |                           |          |
| 0001h   |          |  |                           |          |
| 0002h   |          |  |                           |          |
| 0003h   |          |  |                           |          |
| 0004h   | PM0      | Processor Mode Register 0                        | 00h                       |          |
| 0005h   | PM1      | Processor Mode Register 1                        | 1000000b                  |          |
| 0006h   |          |  |                           |          |
| 0007h   | PRCR     | Protect Register                                 | 00h                       |          |
| 0008h   | CM0      | System Clock Control Register 0                  | 00101000b                 |          |
| 0009h   | CM1      | System Clock Control Register 1                  | 00100000b                 |          |
| 000Ah   | OCD      | Oscillation Stop Detection Register              | 00h                       |          |
| 000Bh   | CM3      | System Clock Control Register 3                  | 00h                       |          |
| 000Ch   | CM4      | System Clock Control Register 4                  | 00000001b                 |          |
| 000Dh   |          |  |                           |          |
| 000Eh   |          |  |                           |          |
| 000Fh   |          |  |                           |          |
| 0010h   | CPSRF    | Clock Prescaler Reset Flag                       | 00h                       |          |
| 0011h   |          |  |                           |          |
| 0012h   | FRA0     | High-Speed On-Chip Oscillator Control Register 0 | 00h                       |          |
| 0013h   |          |  |                           |          |
| 0014h   | FRA2     | High-Speed On-Chip Oscillator Control Register 2 | 00h                       |          |
| 0015h   |          |  |                           |          |
| 0016h   |          |  |                           |          |
| 0017h   |          |  |                           |          |
| 0018h   |          |  |                           |          |
| 0019h   |          |  |                           |          |
| 001Ah   |          |  |                           |          |
| 001Bh   |          |  |                           |          |
| 001Ch   |          |  |                           |          |
| 001Dh   |          |  |                           |          |
| 001Eh   |          |  |                           |          |
| 001Fh   |          |  |                           |          |
| 0020h   | RISR     | Reset Interrupt Select Register                  | 1000000b or<br>0000000b   | (Note 2) |
| 0021h   | WDTR     | Watchdog Timer Reset Register                    | FFh                       |          |
| 0022h   | WDTS     | Watchdog Timer Start Register                    | FFh                       |          |
| 0023h   | WDTC     | Watchdog Timer Control Register                  | 0111111b                  |          |
| 0024h   | CSPR     | Count Source Protection Mode Register            | 1000000b or<br>0000000b   | (Note 2) |
| 0025h   |          |  |                           |          |
| 0026h   |          |  |                           |          |
| 0027h   |          |  |                           |          |
| 0028h   | RSTFR    | Reset Source Determination Register              | 00XXXXXXb                 |          |
| 0029h   |          |  |                           |          |
| 002Ah   |          |  |                           |          |
| 002Bh   |          |  |                           |          |
| 002Ch   | SVDC     | STBY VDC Power Control Register                  | 00h                       |          |
| 002Dh   |          |  |                           |          |
| 002Eh   |          |  |                           |          |
| 002Fh   |          |  |                           |          |
| 0030h   | CMPA     | Voltage Monitor Circuit Control Register         | 00h                       |          |
| 0031h   | VCAC     | Voltage Monitor Circuit Edge Select Register     | 00h                       |          |
| 0032h   | OCVREFCR | On-Chip Reference Voltage Control Register       | 00h                       |          |
| 0033h   |          |  |                           |          |
| 0034h   | VCA2     | Voltage Detection Register 2                     | 0000000b or<br>00100000b  | (Note 3) |
| 0035h   |          |  |                           |          |
| 0036h   | VD1LS    | Voltage Detection 1 Level Select Register        | 00000111b                 |          |
| 0037h   |          |  |                           |          |
| 0038h   | VW0C     | Voltage Monitor 0 Circuit Control Register       | 1100XX10b or<br>1100XX11b | (Note 3) |
| 0039h   | VW1C     | Voltage Monitor 1 Circuit Control Register       | 10001010b                 |          |

X: Undefined

Notes:

1. The blank areas are reserved. No access is allowed.
2. Depends on the CSPROINI bit in the OFS register.
3. Depends on the LVDASI bit in the OFS register.



**Table 3.2 SFR Information (2) (1)**

| Address | Symbol          | Register Name                              | After Reset | Remarks |
|---------|-----------------|--|-------------|---------|
| 0003Ah  | VW2C            | Voltage Monitor 2 Circuit Control Register | 10001010b   |         |
| 0003Bh  |                 |  |             |         |
| 0003Ch  |                 |  |             |         |
| 0003Dh  |                 |  |             |         |
| 0003Eh  |                 |  |             |         |
| 0003Fh  |                 |  |             |         |
| 00040h  |                 |  |             |         |
| 00041h  | FMRDYIC         | Interrupt Control Register                 | 00h         |         |
| 00042h  |                 |  |             |         |
| 00043h  |                 |  |             |         |
| 00044h  |                 |  |             |         |
| 00045h  |                 |  |             |         |
| 00046h  | INT4IC          | Interrupt Control Register                 | 00h         |         |
| 00047h  | TRCIC_0         | Interrupt Control Register                 | 00h         |         |
| 00048h  |                 |  |             |         |
| 00049h  |                 |  |             |         |
| 0004Ah  | TRE2IC          | Interrupt Control Register                 | 00h         |         |
| 0004Bh  | U2TIC           | Interrupt Control Register                 | 00h         |         |
| 0004Ch  | U2RIC           | Interrupt Control Register                 | 00h         |         |
| 0004Dh  | KUPIC           | Interrupt Control Register                 | 00h         |         |
| 0004Eh  | ADIC            | Interrupt Control Register                 | 00h         |         |
| 0004Fh  | SSUIC_0/IICIC_0 | Interrupt Control Register                 | 00h         |         |
| 00050h  |                 |  |             |         |
| 00051h  | U0TIC_0         | Interrupt Control Register                 | 00h         |         |
| 00052h  | U0RIC_0         | Interrupt Control Register                 | 00h         |         |
| 00053h  | U0TIC_1         | Interrupt Control Register                 | 00h         |         |
| 00054h  | U0RIC_1         | Interrupt Control Register                 | 00h         |         |
| 00055h  | INT2IC          | Interrupt Control Register                 | 00h         |         |
| 00056h  | TRJIC_0         | Interrupt Control Register                 | 00h         |         |
| 00057h  |                 |  |             |         |
| 00058h  | TRB2IC_0        | Interrupt Control Register                 | 00h         |         |
| 00059h  | INT1IC          | Interrupt Control Register                 | 00h         |         |
| 0005Ah  | INT3IC          | Interrupt Control Register                 | 00h         |         |
| 0005Bh  |                 |  |             |         |
| 0005Ch  |                 |  |             |         |
| 0005Dh  | INT0IC          | Interrupt Control Register                 | 00h         |         |
| 0005Eh  | U2BCNIC         | Interrupt Control Register                 | 00h         |         |
| 0005Fh  |                 |  |             |         |
| 00060h  |                 |  |             |         |
| 00061h  |                 |  |             |         |
| 00062h  |                 |  |             |         |
| 00063h  |                 |  |             |         |
| 00064h  |                 |  |             |         |
| 00065h  |                 |  |             |         |
| 00066h  |                 |  |             |         |
| 00067h  |                 |  |             |         |
| 00068h  |                 |  |             |         |
| 00069h  |                 |  |             |         |
| 0006Ah  |                 |  |             |         |
| 0006Bh  |                 |  |             |         |
| 0006Ch  |                 |  |             |         |
| 0006Dh  |                 |  |             |         |
| 0006Eh  |                 |  |             |         |
| 0006Fh  |                 |  |             |         |
| 00070h  |                 |  |             |         |
| 00071h  |                 |  |             |         |
| 00072h  | VCMP1IC         | Interrupt Control Register                 | 00h         |         |
| 00073h  | VCMP2IC         | Interrupt Control Register                 | 00h         |         |
| 00074h  |                 |  |             |         |
| 00075h  | TSCUIC          | Interrupt Control Register                 | 00h         |         |
| 00076h  |                 |  |             |         |
| 00077h  |                 |  |             |         |
| 00078h  |                 |  |             |         |
| 00079h  |                 |  |             |         |

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.3 SFR Information (3) (1)**

| Address | Symbol   | Register Name                               | After Reset | Remarks |
|---------|----------|---|-------------|---------|
| 0007Ah  |          |   |             |         |
| 0007Bh  |          |   |             |         |
| 0007Ch  |          |   |             |         |
| 0007Dh  |          |   |             |         |
| 0007Eh  |          |   |             |         |
| 0007Fh  |          |   |             |         |
| 00080h  | U0MR_0   | UART0_0 Transmit/Receive Mode Register      | 00h         |         |
| 00081h  | U0BRG_0  | UART0_0 Bit Rate Register                   | XXh         |         |
| 00082h  | U0TB_0   | UART0_0 Transmit Buffer Register            | XXh         |         |
| 00083h  |          |   | XXh         |         |
| 00084h  | U0C0_0   | UART0_0 Transmit/Receive Control Register 0 | 00001000b   |         |
| 00085h  | U0C1_0   | UART0_0 Transmit/Receive Control Register 1 | 00000010b   |         |
| 00086h  | U0RB_0   | UART0_0 Receive Buffer Register             | XXXXh       |         |
| 00087h  |          |   |             |         |
| 00088h  | U0IR_0   | UART0_0 Interrupt Flag and Enable Register  | 00h         |         |
| 00089h  |          |   |             |         |
| 0008Ah  |          |   |             |         |
| 0008Bh  |          |   |             |         |
| 0008Ch  | LINCR2_0 | LIN_0 Special Function Register             | 00h         |         |
| 0008Dh  |          |   |             |         |
| 0008Eh  | LINCT_0  | LIN_0 Control Register                      | 00h         |         |
| 0008Fh  | LINST_0  | LIN_0 Status Register                       | 00h         |         |
| 00090h  | U0MR_1   | UART0_1 Transmit/Receive Mode Register      | 00h         |         |
| 00091h  | U0BRG_1  | UART0_1 Bit Rate Register                   | XXh         |         |
| 00092h  | U0TB_1   | UART0_1 Transmit Buffer Register            | XXh         |         |
| 00093h  |          |   | XXh         |         |
| 00094h  | U0C0_1   | UART0_1 Transmit/Receive Control Register 0 | 00001000b   |         |
| 00095h  | U0C1_1   | UART0_1 Transmit/Receive Control Register 1 | 00000010b   |         |
| 00096h  | U0RB_1   | UART0_1 Receive Buffer Register             | XXXXh       |         |
| 00097h  |          |   |             |         |
| 00098h  | U0IR_1   | UART0_1 Interrupt Flag and Enable Register  | 00h         |         |
| 00099h  |          |   |             |         |
| 0009Ah  |          |   |             |         |
| 0009Bh  |          |   |             |         |
| 0009Ch  |          |   |             |         |
| 0009Dh  |          |   |             |         |
| 0009Eh  |          |   |             |         |
| 0009Fh  |          |   |             |         |
| 000A0h  |          |   |             |         |
| 000A1h  |          |   |             |         |
| 000A2h  |          |   |             |         |
| 000A3h  |          |   |             |         |
| 000A4h  |          |   |             |         |
| 000A5h  |          |   |             |         |
| 000A8h  |          |   |             |         |
| 000A9h  |          |   |             |         |
| 000AAh  |          |   |             |         |
| 000ABh  |          |   |             |         |
| 000ACh  |          |   |             |         |
| 000ADh  |          |   |             |         |
| 000AEh  |          |   |             |         |
| 000AFh  |          |   |             |         |
| 000B0h  |          |   |             |         |
| 000B1h  |          |   |             |         |
| 000B4h  |          |   |             |         |
| 000B5h  |          |   |             |         |
| 000B8h  |          |   |             |         |
| 000B9h  |          |   |             |         |

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.4 SFR Information (4) (1)**

| Address | Symbol  | Register Name                                 | After Reset | Remarks |
|---------|---------|---|-------------|---------|
| 000BAh  |         |   |             |         |
| 000BBh  |         |   |             |         |
| 000BCh  |         |   |             |         |
| 000BDh  |         |   |             |         |
| 000BEh  |         |   |             |         |
| 000BFh  |         |   |             |         |
| 000C0h  | U2MR    | UART2 Transmit/Receive Mode Register          | 00h         |         |
| 000C1h  | U2BRG   | UART2 Bit Rate Register                       | 00h         |         |
| 000C2h  | U2TB    | UART2 Transmit Buffer Register                | 00h         |         |
| 000C3h  |         |   | 00h         |         |
| 000C4h  | U2C0    | UART2 Transmit/Receive Control Register 0     | 00001000b   |         |
| 000C5h  | U2C1    | UART2 Transmit/Receive Control Register 1     | 00000010b   |         |
| 000C6h  | U2RB    | UART2 Receive Buffer Register                 | 0000h       |         |
| 000C7h  |         |   |             |         |
| 000C8h  | U2RXDF  | UART2 Digital Filter Function Select Register | 00h         |         |
| 000C9h  |         |   |             |         |
| 000CAh  |         |   |             |         |
| 000CBh  |         |   |             |         |
| 000CCh  |         |   |             |         |
| 000CDh  |         |   |             |         |
| 000CEh  |         |   |             |         |
| 000CFh  |         |   |             |         |
| 000D0h  | U2SMR5  | UART2 Special Mode Register 5                 | 00h         |         |
| 000D1h  |         |   |             |         |
| 000D2h  |         |   |             |         |
| 000D3h  |         |   |             |         |
| 000D4h  | U2SMR4  | UART2 Special Mode Register 4                 | 00h         |         |
| 000D5h  | U2SMR3  | UART2 Special Mode Register 3                 | 00h         |         |
| 000D6h  | U2SMR2  | UART2 Special Mode Register 2                 | 00h         |         |
| 000D7h  | U2SMR   | UART2 Special Mode Register                   | 00h         |         |
| 000D8h  |         |   |             |         |
| 000D9h  |         |   |             |         |
| 000DAh  |         |   |             |         |
| 000DBh  |         |   |             |         |
| 000DCh  |         |   |             |         |
| 000DDh  |         |   |             |         |
| 000DEh  |         |   |             |         |
| 000DFh  |         |   |             |         |
| 000E0h  | IICCR_0 | I <sup>2</sup> C_0 Control Register           | 00001110b   |         |
| 000E1h  | SSBR_0  | SS_0 Bit Counter Register                     | 11111000b   |         |
| 000E2h  | SITDR_0 | SI_0 Transmit Data Register                   | FFh         |         |
| 000E3h  |         |   | FFh         |         |
| 000E4h  | SIRDR_0 | SI_0 Receive Data Register                    | FFh         |         |
| 000E5h  |         |   | FFh         |         |
| 000E6h  | SICR1_0 | SI_0 Control Register 1                       | 00h         |         |
| 000E7h  | SICR2_0 | SI_0 Control Register 2                       | 0111101b    |         |
| 000E8h  | SIMR1_0 | SI_0 Mode Register 1                          | 00010000b   |         |
| 000E9h  | SIER_0  | SI_0 Interrupt Enable Register                | 00h         |         |
| 000EAh  | SISR_0  | SI_0 Status Register                          | 00h         |         |
| 000EBh  | SIMR2_0 | SI_0 Mode Register 2                          | 00h         |         |
| 000ECh  |         |   |             |         |
| 000EDh  |         |   |             |         |
| 000EEh  |         |   |             |         |
| 000EFh  |         |   |             |         |
| 000F0h  |         |   |             |         |
| 000F1h  |         |   |             |         |
| 000F2h  |         |   |             |         |
| 000F3h  |         |   |             |         |
| 000F4h  |         |   |             |         |
| 000F5h  |         |   |             |         |
| 000F6h  |         |   |             |         |
| 000F7h  |         |   |             |         |
| 000F8h  |         |   |             |         |
| 000F9h  |         |   |             |         |

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.5 SFR Information (5) (1)**

| Address | Symbol    | Register Name                          | After Reset | Remarks |
|---------|-----------|--|-------------|---------|
| 000FAh  |           |  |             |         |
| 000FBh  |           |  |             |         |
| 000FCh  |           |  |             |         |
| 000FDh  |           |  |             |         |
| 000FEh  |           |  |             |         |
| 000FFh  |           |  |             |         |
| 00100h  |           |  |             |         |
| 00101h  |           |  |             |         |
| 00102h  |           |  |             |         |
| 00103h  |           |  |             |         |
| 00104h  |           |  |             |         |
| 00105h  |           |  |             |         |
| 00106h  |           |  |             |         |
| 00107h  |           |  |             |         |
| 00108h  |           |  |             |         |
| 00109h  |           |  |             |         |
| 0010Ah  |           |  |             |         |
| 0010Bh  |           |  |             |         |
| 0010Ch  |           |  |             |         |
| 0010Dh  |           |  |             |         |
| 0010Eh  |           |  |             |         |
| 0010Fh  |           |  |             |         |
| 00110h  | TRJ_0     | Timer RJ_0 Counter Register            | FFFFh       |         |
| 00111h  |           |  |             |         |
| 00112h  | TRJCR_0   | Timer RJ_0 Control Register            | 00h         |         |
| 00113h  | TRJIOC_0  | Timer RJ_0 I/O Control Register        | 00h         |         |
| 00114h  | TRJMR_0   | Timer RJ_0 Mode Register               | 00h         |         |
| 00115h  | TRJISR_0  | Timer RJ_0 Event Pin Select Register   | 00h         |         |
| 00116h  |           |  |             |         |
| 00117h  |           |  |             |         |
| 00118h  |           |  |             |         |
| 00119h  |           |  |             |         |
| 0011Ah  |           |  |             |         |
| 0011Bh  |           |  |             |         |
| 0011Ch  |           |  |             |         |
| 0011Dh  |           |  |             |         |
| 0011Eh  |           |  |             |         |
| 0011Fh  |           |  |             |         |
| 00120h  |           |  |             |         |
| 00121h  |           |  |             |         |
| 00122h  |           |  |             |         |
| 00123h  |           |  |             |         |
| 00124h  |           |  |             |         |
| 00125h  |           |  |             |         |
| 00126h  |           |  |             |         |
| 00127h  |           |  |             |         |
| 00128h  |           |  |             |         |
| 00129h  |           |  |             |         |
| 0012Ah  |           |  |             |         |
| 0012Bh  |           |  |             |         |
| 0012Ch  |           |  |             |         |
| 0012Dh  |           |  |             |         |
| 0012Eh  |           |  |             |         |
| 0012Fh  |           |  |             |         |
| 00130h  | TRBCR_0   | Timer RB2_0 Control Register           | 00h         |         |
| 00131h  | TRBOCR_0  | Timer RB2_0 One-Shot Control Register  | 00h         |         |
| 00132h  | TRBIOC_0  | Timer RB2_0 I/O Control Register       | 00h         |         |
| 00133h  | TRBMR_0   | Timer RB2_0 Mode Register              | 00h         |         |
| 00134h  | TRBPRES_0 | Timer RB2_0 Prescaler Register         | FFh         |         |
| 00135h  | TRBPR_0   | Timer RB2_0 Primary Register           | FFh         |         |
| 00136h  | TRBSC_0   | Timer RB2_0 Secondary Register         | FFh         |         |
| 00137h  | TRBIR_0   | Timer RB2_0 Interrupt Request Register | 00h         |         |
| 00138h  | TRCCNT_0  | Timer RC_0 Counter                     | 0000h       |         |
| 00139h  |           |  |             |         |

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.6 SFR Information (6) (1)**

| Address | Symbol     | Register Name                                      | After Reset | Remarks |
|---------|------------|--|-------------|---------|
| 0013Ah  | TRCGRA_0   | Timer RC_0 General Register A                      | FFFFh       |         |
| 0013Bh  |            |  |             |         |
| 0013Ch  | TRCGRB_0   | Timer RC_0 General Register B                      | FFFFh       |         |
| 0013Dh  |            |  |             |         |
| 0013Eh  | TRCGRC_0   | Timer RC_0 General Register C                      | FFFFh       |         |
| 0013Fh  |            |  |             |         |
| 00140h  | TRCGRD_0   | Timer RC_0 General Register D                      | FFFFh       |         |
| 00141h  |            |  |             |         |
| 00142h  | TRCMR_0    | Timer RC_0 Mode Register                           | 01001000b   |         |
| 00143h  | TRCCR1_0   | Timer RC_0 Control Register 1                      | 00h         |         |
| 00144h  | TRCIER_0   | Timer RC_0 Interrupt Enable Register               | 01110000b   |         |
| 00145h  | TRCSR_0    | Timer RC_0 Status Register                         | 01110000b   |         |
| 00146h  | TRCIOR0_0  | Timer RC_0 I/O Control Register 0                  | 10001000b   |         |
| 00147h  | TRCIOR1_0  | Timer RC_0 I/O Control Register 1                  | 10001000b   |         |
| 00148h  | TRCCR2_0   | Timer RC_0 Control Register 2                      | 00011000b   |         |
| 00149h  | TRCDF_0    | Timer RC_0 Digital Filter Function Select Register | 00h         |         |
| 0014Ah  | TRCOER_0   | Timer RC_0 Output Enable Register                  | 01111111b   |         |
| 0014Bh  | TRCADCR_0  | Timer RC_0 A/D Conversion Trigger Control Register | 11110000b   |         |
| 0014Ch  | TRCOPR_0   | Timer RC_0 Output Waveform Manipulation Register   | 00h         |         |
| 0014Dh  | TRCELCCR_0 | Timer RC_0 ELC Cooperation Control Register        | 00h         |         |
| 0014Eh  |            |  |             |         |
| 0014Fh  |            |  |             |         |
| 00150h  |            |  |             |         |
| 00151h  |            |  |             |         |
| 00152h  |            |  |             |         |
| 00153h  |            |  |             |         |
| 00154h  |            |  |             |         |
| 00155h  |            |  |             |         |
| 00156h  |            |  |             |         |
| 00157h  |            |  |             |         |
| 00158h  |            |  |             |         |
| 00159h  |            |  |             |         |
| 0015Ah  |            |  |             |         |
| 0015Bh  |            |  |             |         |
| 0015Ch  |            |  |             |         |
| 0015Dh  |            |  |             |         |
| 0015Eh  |            |  |             |         |
| 0015Fh  |            |  |             |         |
| 00160h  |            |  |             |         |
| 00161h  |            |  |             |         |
| 00162h  |            |  |             |         |
| 00163h  |            |  |             |         |
| 00164h  |            |  |             |         |
| 00165h  |            |  |             |         |
| 00166h  |            |  |             |         |
| 00167h  |            |  |             |         |
| 00168h  |            |  |             |         |
| 00169h  |            |  |             |         |
| 0016Ah  |            |  |             |         |
| 0016Bh  |            |  |             |         |
| 0016Ch  |            |  |             |         |
| 0016Dh  |            |  |             |         |
| 0016Eh  |            |  |             |         |
| 0016Fh  |            |  |             |         |
| 00170h  | TRESEC     | Timer RE2 Counter Data Register                    | 00h         |         |
|         |            | Timer RE2 Second Data Register                     |             |         |
| 00171h  | TREMINT    | Timer RE2 Compare Data Register                    | 00h         |         |
|         |            | Timer RE2 Minute Data Register                     |             |         |
| 00172h  | TREHR      | Timer RE2 Hour Data Register                       | 00h         |         |
| 00173h  | TREWK      | Timer RE2 Day-of-the-Week Data Register            | 00h         |         |
| 00174h  | TREDY      | Timer RE2 Day Data Register                        | 00000001b   |         |
| 00175h  | TREMON     | Timer RE2 Month Data Register                      | 00000001b   |         |
| 00176h  | TREYR      | Timer RE2 Year Data Register                       | 00h         |         |
| 00177h  | TRECR      | Timer RE2 Control Register                         | 00000100b   |         |
| 00178h  | TRECSR     | Timer RE2 Count Source Select Register             | 00001000b   |         |
| 00179h  | TREADJ     | Timer RE2 Clock Error Correction Register          | 00h         |         |

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.7 SFR Information (7) (1)**

| Address                | Symbol  | Register Name                            | After Reset | Remarks |
|------------------------|---------|--|-------------|---------|
| 0017Ah                 | TREIFR  | Timer RE2 Interrupt Flag Register        | 00h         |         |
| 0017Bh                 | TREIER  | Timer RE2 Interrupt Enable Register      | 00h         |         |
| 0017Ch                 | TREAMN  | Timer RE2 Alarm Minute Register          | 00h         |         |
| 0017Dh                 | TREAHR  | Timer RE2 Alarm Hour Register            | 00h         |         |
| 0017Eh                 | TREAWK  | Timer RE2 Alarm Day-of-the-Week Register | 00h         |         |
| 0017Fh                 | TREPRC  | Timer RE2 Protect Register               | 00h         |         |
| 00180h<br>to<br>001FFh |         |  |             |         |
| 00200h                 | AD0     | A/D Register 0                           | 00h         |         |
| 00201h                 |         |  | 00h         |         |
| 00202h                 | AD1     | A/D Register 1                           | 00h         |         |
| 00203h                 |         |  | 00h         |         |
| 00204h                 | AD2     | A/D Register 2                           | 00h         |         |
| 00205h                 |         |  | 00h         |         |
| 00206h                 | AD3     | A/D Register 3                           | 00h         |         |
| 00207h                 |         |  | 00h         |         |
| 00208h                 | AD4     | A/D Register 4                           | 00h         |         |
| 00209h                 |         |  | 00h         |         |
| 0020Ah                 | AD5     | A/D Register 5                           | 00h         |         |
| 0020Bh                 |         |  | 00h         |         |
| 0020Ch                 | AD6     | A/D Register 6                           | 00h         |         |
| 0020Dh                 |         |  | 00h         |         |
| 0020Eh                 | AD7     | A/D Register 7                           | 00h         |         |
| 0020Fh                 |         |  | 00h         |         |
| 00210h                 |         |  |             |         |
| 00211h                 |         |  |             |         |
| 00212h                 |         |  |             |         |
| 00213h                 |         |  |             |         |
| 00214h                 | ADMOD   | A/D Mode Register                        | 00h         |         |
| 00215h                 | ADINSEL | A/D Input Select Register                | 11000000b   |         |
| 00216h                 | ADCON0  | A/D Control Register 0                   | 00h         |         |
| 00217h                 | ADCON1  | A/D Control Register 1                   | 00h         |         |
| 00218h                 |         |  |             |         |
| 00219h                 |         |  |             |         |
| 0021Ah                 |         |  |             |         |
| 0021Bh                 |         |  |             |         |
| 0021Ch                 |         |  |             |         |
| 0021Dh                 |         |  |             |         |
| 0021Eh                 |         |  |             |         |
| 0021Fh                 |         |  |             |         |
| 00220h                 |         |  |             |         |
| 00221h                 |         |  |             |         |
| 00222h                 |         |  |             |         |
| 00223h                 |         |  |             |         |
| 00224h                 |         |  |             |         |
| 00225h                 |         |  |             |         |
| 00226h                 |         |  |             |         |
| 00227h                 |         |  |             |         |
| 00228h                 | INTCMP  | Comparator B Control Register 0          | 00h         |         |
| 00229h                 |         |  |             |         |
| 0022Ah                 |         |  |             |         |
| 0022Bh                 |         |  |             |         |
| 0022Ch                 |         |  |             |         |
| 0022Dh                 |         |  |             |         |
| 0022Eh                 |         |  |             |         |
| 0022Fh                 |         |  |             |         |
| 00230h                 | INTEN   | External Input Enable Register 0         | 00h         |         |
| 00231h                 | INTEN1  | External Input Enable Register 1         | 00h         |         |
| 00232h                 | INTF    | INT Input Filter Select Register 0       | 00h         |         |
| 00233h                 | INTF1   | INT Input Filter Select Register 1       | 00h         |         |
| 00234h                 | INTPOL  | INT Input Polarity Switch Register       | 00h         |         |
| 00235h                 |         |  |             |         |
| 00236h                 | KIEN    | Key Input Interrupt Enable Register      | 00h         |         |
| 00237h                 |         |  |             |         |
| 00238h                 | MSTCR0  | Module Standby Control Register 0        | 00h         |         |
| 00239h                 | MSTCR1  | Module Standby Control Register 1        | 00h         |         |

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.8 SFR Information (8) (1)**

| Address | Symbol  | Register Name                               | After Reset | Remarks |
|---------|---------|---|-------------|---------|
| 0023Ah  | MSTCR2  | Module Standby Control Register 2           | 00h         |         |
| 0023Bh  | MSTCR3  | Module Standby Control Register 3           | 00h         |         |
| 0023Ch  | MSTCR4  | Module Standby Control Register 4           | 00h         |         |
| 0023Dh  |         |   |             |         |
| 0023Eh  |         |   |             |         |
| 0023Fh  |         |   |             |         |
| 00240h  |         |   |             |         |
| 00241h  |         |   |             |         |
| 00242h  |         |   |             |         |
| 00243h  |         |   |             |         |
| 00244h  |         |   |             |         |
| 00245h  |         |   |             |         |
| 00246h  |         |   |             |         |
| 00247h  |         |   |             |         |
| 00248h  |         |   |             |         |
| 00249h  |         |   |             |         |
| 0024Ah  |         |   |             |         |
| 0024Bh  |         |   |             |         |
| 0024Ch  |         |   |             |         |
| 0024Dh  |         |   |             |         |
| 0024Eh  |         |   |             |         |
| 0024Fh  |         |   |             |         |
| 00250h  |         |   |             |         |
| 00251h  |         |   |             |         |
| 00252h  | FST     | Flash Memory Status Register                | 10000X00b   |         |
| 00253h  |         |   |             |         |
| 00254h  | FMR0    | Flash Memory Control Register 0             | 00h         |         |
| 00255h  | FMR1    | Flash Memory Control Register 1             | 00h         |         |
| 00256h  | FMR2    | Flash Memory Control Register 2             | 00h         |         |
| 00257h  |         |   |             |         |
| 00258h  |         |   |             |         |
| 00259h  |         |   |             |         |
| 0025Ah  |         |   |             |         |
| 0025Bh  |         |   |             |         |
| 0025Ch  |         |   |             |         |
| 0025Dh  |         |   |             |         |
| 0025Eh  |         |   |             |         |
| 0025Fh  |         |   |             |         |
| 00260h  | AIADR0L | Address Match Interrupt Address 0L Register | XXXXh       |         |
| 00261h  |         |   |             |         |
| 00262h  | AIADR0H | Address Match Interrupt Address 0H Register | 0000XXXXb   |         |
| 00263h  | AIEN0   | Address Match Interrupt Enable 0 Register   | 00h         |         |
| 00264h  | AIADR1L | Address Match Interrupt Address 1L Register | XXXXh       |         |
| 00265h  |         |   |             |         |
| 00266h  | AIADR1H | Address Match Interrupt Address 1H Register | 0000XXXXb   |         |
| 00267h  | AIEN1   | Address Match Interrupt Enable 1 Register   | 00h         |         |
| 00268h  |         |   |             |         |
| 00269h  |         |   |             |         |
| 0026Ah  |         |   |             |         |
| 0026Bh  |         |   |             |         |
| 0026Ch  |         |   |             |         |
| 0026Dh  |         |   |             |         |
| 0026Eh  |         |   |             |         |
| 0026Fh  |         |   |             |         |
| 00270h  |         |   |             |         |
| 00271h  |         |   |             |         |
| 00272h  |         |   |             |         |
| 00273h  |         |   |             |         |
| 00274h  |         |   |             |         |
| 00275h  |         |   |             |         |
| 00276h  |         |   |             |         |
| 00277h  |         |   |             |         |
| 00278h  |         |   |             |         |
| 00279h  |         |   |             |         |
| 0027Ah  |         |   |             |         |
| 0027Bh  |         |   |             |         |
| 0027Ch  |         |   |             |         |
| 0027Dh  |         |   |             |         |
| 0027Eh  |         |   |             |         |
| 0027Fh  |         |   |             |         |

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.9 SFR Information (9) (1)**

| Address | Symbol   | Register Name                             | After Reset | Remarks |
|---------|----------|---|-------------|---------|
| 00280h  | DTCTL    | DTC Activation Control Register           | 00h         |         |
| 00281h  |          |   |             |         |
| 00282h  |          |   |             |         |
| 00283h  |          |   |             |         |
| 00284h  |          |   |             |         |
| 00285h  |          |   |             |         |
| 00286h  |          |   |             |         |
| 00287h  |          |   |             |         |
| 00288h  | DTCEN0   | DTC Activation Enable Register 0          | 00h         |         |
| 00289h  | DTCEN1   | DTC Activation Enable Register 1          | 00h         |         |
| 0028Ah  | DTCEN2   | DTC Activation Enable Register 2          | 00h         |         |
| 0028Bh  | DTCEN3   | DTC Activation Enable Register 3          | 00h         |         |
| 0028Ch  |          |   |             |         |
| 0028Dh  | DTCEN5   | DTC Activation Enable Register 5          | 00h         |         |
| 0028Eh  | DTCEN6   | DTC Activation Enable Register 6          | 00h         |         |
| 0028Fh  |          |   |             |         |
| 00290h  | CRCSAR   | SFR Snoop Address Register                | 0000h       |         |
| 00291h  |          |   |             |         |
| 00292h  | CRCMR    | CRC Control Register                      | 00h         |         |
| 00293h  |          |   |             |         |
| 00294h  | CRCD     | CRC Data Register                         | 0000h       |         |
| 00295h  |          |   |             |         |
| 00296h  | CRCIN    | CRC Input Register                        | 00h         |         |
| 00297h  |          |   |             |         |
| 00298h  |          |   |             |         |
| 00299h  |          |   |             |         |
| 0029Ah  |          |   |             |         |
| 0029Bh  |          |   |             |         |
| 0029Ch  |          |   |             |         |
| 0029Dh  |          |   |             |         |
| 0029Eh  |          |   |             |         |
| 0029Fh  |          |   |             |         |
| 002A0h  | TRJ_0SR  | Timer RJ_0 Pin Select Register            | 08h         |         |
| 002A1h  |          |   |             |         |
| 002A2h  |          |   |             |         |
| 002A3h  |          |   |             |         |
| 002A4h  |          |   |             |         |
| 002A5h  | TRCLKSR  | Timer RCCLK Pin Select Register           | 00h         |         |
| 002A6h  | TRC_0SR0 | Timer RC_0 Pin Select Register 0          | 00h         |         |
| 002A7h  | TRC_0SR1 | Timer RC_0 Pin Select Register 1          | 00h         |         |
| 002A8h  |          |   |             |         |
| 002A9h  |          |   |             |         |
| 002AAh  |          |   |             |         |
| 002ABh  |          |   |             |         |
| 002ACh  |          |   |             |         |
| 002ADh  | TIMSR    | Timer Pin Select Register                 | 00h         |         |
| 002AEh  | U_0SR    | UART0_0 Pin Select Register               | 00h         |         |
| 002AFh  | U_1SR    | UART0_1 Pin Select Register               | 00h         |         |
| 002B0h  |          |   |             |         |
| 002B1h  |          |   |             |         |
| 002B2h  | U2SR0    | UART2 Pin Select Register 0               | 00h         |         |
| 002B3h  | U2SR1    | UART2 Pin Select Register 1               | 00h         |         |
| 002B4h  |          |   |             |         |
| 002B5h  |          |   |             |         |
| 002B6h  | INTSR0   | INT Interrupt Input Pin Select Register 0 | 00h         |         |
| 002B7h  |          |   |             |         |
| 002B8h  |          |   |             |         |
| 002B9h  | PINSR    | I/O Function Pin Select Register          | 00h         |         |
| 002BAh  |          |   |             |         |
| 002BBh  |          |   |             |         |
| 002BCh  |          |   |             |         |
| 002BDh  |          |   |             |         |
| 002BEh  | PMCSEL   | Pin Assignment Select Register            | 00h         |         |
| 002BFh  |          |   |             |         |

Note:

1. The blank areas are reserved. No access is allowed.



**Table 3.10 SFR Information (10) (1)**

| Address                | Symbol | Register Name                           | After Reset | Remarks |
|------------------------|--------|---|-------------|---------|
| 002C0h                 | PUR0   | Pull-Up Control Register 0              | 00h         |         |
| 002C1h                 | PUR1   | Pull-Up Control Register 1              | 00h         |         |
| 002C2h                 | PUR2   | Pull-Up Control Register 2              | 00h         |         |
| 002C3h                 |        |   |             |         |
| 002C4h                 |        |   |             |         |
| 002C5h                 |        |   |             |         |
| 002C6h                 |        |   |             |         |
| 002C7h                 |        |   |             |         |
| 002C8h                 | P1DRR  | Port P1 Drive Capacity Control Register | 00h         |         |
| 002C9h                 | P2DRR  | Port P2 Drive Capacity Control Register | 00h         |         |
| 002CAh                 |        |   |             |         |
| 002CBh                 |        |   |             |         |
| 002CCh                 | DRR0   | Drive Capacity Control Register 0       | 00h         |         |
| 002CDh                 | DRR1   | Drive Capacity Control Register 1       | 00h         |         |
| 002CEh                 | DRR2   | Drive Capacity Control Register 2       | 00h         |         |
| 002CFh                 |        |   |             |         |
| 002D0h                 | VLT0   | Input Threshold Control Register 0      | 00h         |         |
| 002D1h                 | VLT1   | Input Threshold Control Register 1      | 00h         |         |
| 002D2h                 | VLT2   | Input Threshold Control Register 2      | 00h         |         |
| 002D3h                 |        |   |             |         |
| 002D4h                 |        |   |             |         |
| 002D5h                 |        |   |             |         |
| 002D6h                 |        |   |             |         |
| 002D7h                 |        |   |             |         |
| 002D8h                 |        |   |             |         |
| 002D9h                 |        |   |             |         |
| 002DAh                 |        |   |             |         |
| 002DBh                 |        |   |             |         |
| 002DCh                 |        |   |             |         |
| 002DDh                 |        |   |             |         |
| 002DEh                 |        |   |             |         |
| 002DFh                 |        |   |             |         |
| 002E0h                 | PORT0  | Port P0 Register                        | XXh         |         |
| 002E1h                 | PORT1  | Port P1 Register                        | XXh         |         |
| 002E2h                 | PD0    | Port P0 Direction Register              | 00h         |         |
| 002E3h                 | PD1    | Port P1 Direction Register              | 00h         |         |
| 002E4h                 | PORT2  | Port P2 Register                        | XXh         |         |
| 002E5h                 | PORT3  | Port P3 Register                        | XXh         |         |
| 002E6h                 | PD2    | Port P2 Direction Register              | 00h         |         |
| 002E7h                 | PD3    | Port P3 Direction Register              | 00h         |         |
| 002E8h                 | PORT4  | Port P4 Register                        | XXh         |         |
| 002E9h                 | PORT5  | Port P5 Register                        | XXh         |         |
| 002EAh                 | PD4    | Port P4 Direction Register              | 00h         |         |
| 002EBh                 | PD5    | Port P5 Direction Register              | 00h         |         |
| 002ECh                 | PORT6  | Port P6 Register                        | XXh         |         |
| 002EDh                 |        |   |             |         |
| 002EEh                 | PD6    | Port P6 Direction Register              | 00h         |         |
| 002EFh                 |        |   |             |         |
| 002F0h                 | PORT8  | Port P8 Register                        | XXh         |         |
| 002F1h                 |        |   |             |         |
| 002F2h                 | PD8    | Port P8 Direction Register              | 00h         |         |
| 002F3h                 |        |   |             |         |
| 002F4h                 |        |   |             |         |
| 002F5h                 |        |   |             |         |
| 002F6h                 |        |   |             |         |
| 002F7h                 |        |   |             |         |
| 002F8h                 |        |   |             |         |
| 002F9h                 |        |   |             |         |
| 002FAh                 |        |   |             |         |
| 002FBh                 |        |   |             |         |
| 002FCh                 |        |   |             |         |
| 002FDh                 |        |   |             |         |
| 002FEh                 |        |   |             |         |
| 002FFh                 |        |   |             |         |
| 00300h<br>to<br>003FFh |        |   |             |         |

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.11 SFR Information (11) (1)**

| Address                | Symbol      | Register Name                               | After Reset | Remarks |
|------------------------|-------------|---|-------------|---------|
| 00400h<br>to<br>053FFh | On-chip RAM | On-chip RAM                                 |             |         |
| 05400h<br>to<br>069FFh |             |   |             |         |
| 06A00h                 | ELSELR0     | Event Output Destination Select Register 0  | 00h         |         |
| 06A01h                 | ELSELR1     | Event Output Destination Select Register 1  | 00h         |         |
| 06A02h                 | ELSELR2     | Event Output Destination Select Register 2  | 00h         |         |
| 06A03h                 | ELSELR3     | Event Output Destination Select Register 3  | 00h         |         |
| 06A04h                 | ELSELR4     | Event Output Destination Select Register 4  | 00h         |         |
| 06A05h                 |             |   |             |         |
| 06A06h                 |             |   |             |         |
| 06A07h                 |             |   |             |         |
| 06A08h                 | ELSELR8     | Event Output Destination Select Register 8  | 00h         |         |
| 06A09h                 | ELSELR9     | Event Output Destination Select Register 9  | 00h         |         |
| 06A0Ah                 |             |   |             |         |
| 06A0Bh                 | ELSELR11    | Event Output Destination Select Register 11 | 00h         |         |
| 06A0Ch                 | ELSELR12    | Event Output Destination Select Register 12 | 00h         |         |
| 06A0Dh                 | ELSELR13    | Event Output Destination Select Register 13 | 00h         |         |
| 06A0Eh                 | ELSELR14    | Event Output Destination Select Register 14 | 00h         |         |
| 06A0Fh                 | ELSELR15    | Event Output Destination Select Register 15 | 00h         |         |
| 06A10h                 | ELSELR16    | Event Output Destination Select Register 16 | 00h         |         |
| 06A11h                 |             |   |             |         |
| 06A12h                 |             |   |             |         |
| 06A13h                 |             |   |             |         |
| 06A14h                 |             |   |             |         |
| 06A15h                 |             |   |             |         |
| 06A16h                 |             |   |             |         |
| 06A17h                 |             |   |             |         |
| 06A18h                 |             |   |             |         |
| 06A19h                 |             |   |             |         |
| 06A1Ah                 |             |   |             |         |
| 06A1Bh                 |             |   |             |         |
| 06A1Ch                 |             |   |             |         |
| 06A1Dh                 |             |   |             |         |
| 06A1Eh                 |             |   |             |         |
| 06A1Fh                 |             |   |             |         |
| 06A20h                 |             |   |             |         |
| 06A21h                 |             |   |             |         |
| 06A22h                 |             |   |             |         |
| 06A23h                 |             |   |             |         |
| 06A24h                 |             |   |             |         |
| 06A25h                 |             |   |             |         |
| 06A26h                 |             |   |             |         |
| 06A27h                 |             |   |             |         |
| 06A28h                 |             |   |             |         |
| 06A29h                 |             |   |             |         |
| 06A2Ah                 |             |   |             |         |
| 06A2Bh                 |             |   |             |         |
| 06A2Ch                 |             |   |             |         |
| 06A2Dh                 |             |   |             |         |
| 06A2Eh                 |             |   |             |         |
| 06A2Fh                 |             |   |             |         |
| 06A30h                 |             |   |             |         |
| 06A31h<br>to<br>06AFFh |             |   |             |         |

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.12 SFR Information (12) (1)**

| Address                | Symbol   | Register Name                          | After Reset       | Remarks |
|------------------------|----------|--|-------------------|---------|
| 06B00h                 | TSCUCR0  | TSCU Control Register 0                | 0000h             |         |
| 06B01h                 |          |  |                   |         |
| 06B02h                 | TSCUCR1  | TSCU Control Register 1                | 000000000010000b  |         |
| 06B03h                 |          |  |                   |         |
| 06B04h                 | TSCUMR   | TSCU Mode Register                     | 000000001000000b  |         |
| 06B05h                 |          |  |                   |         |
| 06B06h                 | TSCUTCRA | TSCU Timing Control Register 0A        | 000000001111111b  |         |
| 06B07h                 |          |  |                   |         |
| 06B08h                 | TSCUTCRA | TSCU Timing Control Register 0B        | 000000001111111b  |         |
| 06B09h                 |          |  |                   |         |
| 06B0Ah                 | TSCUTCRA | TSCU Timing Control Register 1         | 0000000000000001b |         |
| 06B0Bh                 |          |  |                   |         |
| 06B0Ch                 | TSCUTCRA | TSCU Timing Control Register 2         | 0000h             |         |
| 06B0Dh                 |          |  |                   |         |
| 06B0Eh                 | TSCUTCRA | TSCU Timing Control Register 3         | 0000h             |         |
| 06B0Fh                 |          |  |                   |         |
| 06B10h                 | TSCUHC   | TSCU Channel Control Register          | 001111110000000b  |         |
| 06B11h                 |          |  |                   |         |
| 06B12h                 | TSCUFR   | TSCU Flag Register                     | 0000h             |         |
| 06B13h                 |          |  |                   |         |
| 06B14h                 | TSCUSTC  | TSCU Status Counter Register           | 0000h             |         |
| 06B15h                 |          |  |                   |         |
| 06B16h                 | TSCUSCS  | TSCU Secondary Counter Set Register    | 00000000010000b   |         |
| 06B17h                 |          |  |                   |         |
| 06B18h                 | TSCUSCC  | TSCU Secondary Counter                 | 00000000010000b   |         |
| 06B19h                 |          |  |                   |         |
| 06B1Ah                 | TSCUDBR  | TSCU Data Buffer Register              | 0000h             |         |
| 06B1Bh                 |          |  |                   |         |
| 06B1Ch                 | TSCUPRC  | TSCU Primary Counter                   | 0000h             |         |
| 06B1Dh                 |          |  |                   |         |
| 06B1Eh                 | TSCURVR0 | TSCU Random Value Store Register 0     | 0000h             |         |
| 06B1Fh                 |          |  |                   |         |
| 06B20h                 | TSCURVR1 | TSCU Random Value Store Register 1     | 0000h             |         |
| 06B21h                 |          |  |                   |         |
| 06B22h                 | TSCURVR2 | TSCU Random Value Store Register 2     | 0000h             |         |
| 06B23h                 |          |  |                   |         |
| 06B24h                 | TSCURVR3 | TSCU Random Value Store Register 3     | 0000h             |         |
| 06B25h                 |          |  |                   |         |
| 06B26h                 | TSIE0    | TSCU Input Enable Register 0           | 0000h             |         |
| 06B27h                 |          |  |                   |         |
| 06B28h                 | TSIE1    | TSCU Input Enable Register 1           | 0000h             |         |
| 06B29h                 |          |  |                   |         |
| 06B2Ah                 | TSIE2    | TSCU Input Enable Register 2           | 0000h             |         |
| 06B2Bh                 |          |  |                   |         |
| 06B2Ch                 | TSCHSEL0 | TSCUCHXA Select Register 0             | 0000h             |         |
| 06B2Dh                 |          |  |                   |         |
| 06B2Eh                 | TSCHSEL1 | TSCUCHXA Select Register 1             | 0000h             |         |
| 06B2Fh                 |          |  |                   |         |
| 06B30h                 | TSCHSEL2 | TSCUCHXA Select Register 2             | 0000h             |         |
| 06B31h                 |          |  |                   |         |
| 06B32h<br>to<br>06BFFh |          |  |                   |         |
| 06C00h                 |          | Area for storing DTC transfer vector 0 | XXh               |         |
| 06C01h                 |          | Area for storing DTC transfer vector 1 | XXh               |         |
| 06C02h                 |          | Area for storing DTC transfer vector 2 | XXh               |         |
| 06C03h                 |          | Area for storing DTC transfer vector 3 | XXh               |         |
| 06C04h                 |          | Area for storing DTC transfer vector 4 | XXh               |         |
| 06C05h                 |          |  |                   |         |
| 06C06h                 |          |  |                   |         |
| 06C07h                 |          |  |                   |         |
| 06C08h                 |          | Area for storing DTC transfer vector 8 | XXh               |         |
| 06C09h                 |          | Area for storing DTC transfer vector 9 | XXh               |         |

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.13 SFR Information (13) (1)**

| Address | Symbol | Register Name                           | After Reset | Remarks |
|---------|--------|---|-------------|---------|
| 06C0Ah  |        | Area for storing DTC transfer vector 10 | XXh         |         |
| 06C0Bh  |        | Area for storing DTC transfer vector 11 | XXh         |         |
| 06C0Ch  |        | Area for storing DTC transfer vector 12 | XXh         |         |
| 06C0Dh  |        | Area for storing DTC transfer vector 13 | XXh         |         |
| 06C0Eh  |        | Area for storing DTC transfer vector 14 | XXh         |         |
| 06C0Fh  |        | Area for storing DTC transfer vector 15 | XXh         |         |
| 06C10h  |        | Area for storing DTC transfer vector 16 | XXh         |         |
| 06C11h  |        | Area for storing DTC transfer vector 17 | XXh         |         |
| 06C12h  |        | Area for storing DTC transfer vector 18 | XXh         |         |
| 06C13h  |        | Area for storing DTC transfer vector 19 | XXh         |         |
| 06C14h  |        |   |             |         |
| 06C15h  |        |   |             |         |
| 06C16h  |        | Area for storing DTC transfer vector 22 | XXh         |         |
| 06C17h  |        | Area for storing DTC transfer vector 23 | XXh         |         |
| 06C18h  |        | Area for storing DTC transfer vector 24 | XXh         |         |
| 06C19h  |        | Area for storing DTC transfer vector 25 | XXh         |         |
| 06C1Ah  |        |   |             |         |
| 06C1Bh  |        |   |             |         |
| 06C1Ch  |        |   |             |         |
| 06C1Dh  |        |   |             |         |
| 06C1Eh  |        |   |             |         |
| 06C1Fh  |        |   |             |         |
| 06C20h  |        |   |             |         |
| 06C21h  |        |   |             |         |
| 06C22h  |        |   |             |         |
| 06C23h  |        |   |             |         |
| 06C24h  |        |   |             |         |
| 06C25h  |        |   |             |         |
| 06C26h  |        |   |             |         |
| 06C27h  |        |   |             |         |
| 06C28h  |        |   |             |         |
| 06C29h  |        |   |             |         |
| 06C2Ah  |        | Area for storing DTC transfer vector 42 | XXh         |         |
| 06C2Bh  |        |   |             |         |
| 06C2Ch  |        |   |             |         |
| 06C2Dh  |        |   |             |         |
| 06C2Eh  |        |   |             |         |
| 06C2Fh  |        |   |             |         |
| 06C30h  |        |   |             |         |
| 06C31h  |        | Area for storing DTC transfer vector 49 | XXh         |         |
| 06C32h  |        |   |             |         |
| 06C33h  |        | Area for storing DTC transfer vector 51 | XXh         |         |
| 06C34h  |        | Area for storing DTC transfer vector 52 | XXh         |         |
| 06C35h  |        | Area for storing DTC transfer vector 53 | XXh         |         |
| 06C36h  |        | Area for storing DTC transfer vector 54 | XXh         |         |
| 06C37h  |        |   |             |         |
| 06C38h  |        |   |             |         |
| 06C39h  |        |   |             |         |
| 06C3Ah  |        |   |             |         |
| 06C3Bh  |        |   |             |         |
| 06C3Ch  |        |   |             |         |
| 06C3Dh  |        |   |             |         |
| 06C3Eh  |        |   |             |         |
| 06C3Fh  |        |   |             |         |
| 06C40h  | DTCCR0 | DTC Control Register 0                  | XXh         |         |
| 06C41h  | DTBLS0 | DTC Block Size Register 0               | XXh         |         |
| 06C42h  | DTCC0  | DTC Transfer Count Register 0           | XXh         |         |
| 06C43h  | DTRL0  | DTC Transfer Count Reload Register 0    | XXh         |         |
| 06C44h  | DTSAR0 | DTC Source Address Register 0           | XXXXh       |         |
| 06C45h  |        |   |             |         |
| 06C46h  | DTDAR0 | DTC Destination Address Register 0      | XXXXh       |         |
| 06C47h  |        |   |             |         |
| 06C48h  | DTCCR1 | DTC Control Register 1                  | XXh         |         |
| 06C49h  | DTBLS1 | DTC Block Size Register 1               | XXh         |         |

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.14 SFR Information (14) (1)**

| Address | Symbol | Register Name                        | After Reset | Remarks |
|---------|--------|--------------------------------------|-------------|---------|
| 06C4Ah  | DTCCT1 | DTC Transfer Count Register 1        | XXh         |         |
| 06C4Bh  | DTRLD1 | DTC Transfer Count Reload Register 1 | XXh         |         |
| 06C4Ch  | DTSAR1 | DTC Source Address Register 1        | XXXXh       |         |
| 06C4Dh  |        |                                      |             |         |
| 06C4Eh  | DTDAR1 | DTC Destination Address Register 1   | XXXXh       |         |
| 06C4Fh  |        |                                      |             |         |
| 06C50h  | DTCCR2 | DTC Control Register 2               | XXh         |         |
| 06C51h  | DTBLS2 | DTC Block Size Register 2            | XXh         |         |
| 06C52h  | DTCCT2 | DTC Transfer Count Register 2        | XXh         |         |
| 06C53h  | DTRLD2 | DTC Transfer Count Reload Register 2 | XXh         |         |
| 06C54h  | DTSAR2 | DTC Source Address Register 2        | XXXXh       |         |
| 06C55h  |        |                                      |             |         |
| 06C56h  | DTDAR2 | DTC Destination Address Register 2   | XXXXh       |         |
| 06C57h  |        |                                      |             |         |
| 06C58h  | DTCCR3 | DTC Control Register 3               | XXh         |         |
| 06C59h  | DTBLS3 | DTC Block Size Register 3            | XXh         |         |
| 06C5Ah  | DTCCT3 | DTC Transfer Count Register 3        | XXh         |         |
| 06C5Bh  | DTRLD3 | DTC Transfer Count Reload Register 3 | XXh         |         |
| 06C5Ch  | DTSAR3 | DTC Source Address Register 3        | XXXXh       |         |
| 06C5Dh  |        |                                      |             |         |
| 06C5Eh  | DTDAR3 | DTC Destination Address Register 3   | XXXXh       |         |
| 06C5Fh  |        |                                      |             |         |
| 06C60h  | DTCCR4 | DTC Control Register 4               | XXh         |         |
| 06C61h  | DTBLS4 | DTC Block Size Register 4            | XXh         |         |
| 06C62h  | DTCCT4 | DTC Transfer Count Register 4        | XXh         |         |
| 06C63h  | DTRLD4 | DTC Transfer Count Reload Register 4 | XXh         |         |
| 06C64h  | DTSAR4 | DTC Source Address Register 4        | XXXXh       |         |
| 06C65h  |        |                                      |             |         |
| 06C66h  | DTDAR4 | DTC Destination Address Register 4   | XXXXh       |         |
| 06C67h  |        |                                      |             |         |
| 06C68h  | DTCCR5 | DTC Control Register 5               | XXh         |         |
| 06C69h  | DTBLS5 | DTC Block Size Register 5            | XXh         |         |
| 06C6Ah  | DTCCT5 | DTC Transfer Count Register 5        | XXh         |         |
| 06C6Bh  | DTRLD5 | DTC Transfer Count Reload Register 5 | XXh         |         |
| 06C6Ch  | DTSAR5 | DTC Source Address Register 5        | XXXXh       |         |
| 06C6Dh  |        |                                      |             |         |
| 06C6Eh  | DTDAR5 | DTC Destination Address Register 5   | XXXXh       |         |
| 06C6Fh  |        |                                      |             |         |
| 06C70h  | DTCCR6 | DTC Control Register 6               | XXh         |         |
| 06C71h  | DTBLS6 | DTC Block Size Register 6            | XXh         |         |
| 06C72h  | DTCCT6 | DTC Transfer Count Register 6        | XXh         |         |
| 06C73h  | DTRLD6 | DTC Transfer Count Reload Register 6 | XXh         |         |
| 06C74h  | DTSAR6 | DTC Source Address Register 6        | XXXXh       |         |
| 06C75h  |        |                                      |             |         |
| 06C76h  | DTDAR6 | DTC Destination Address Register 6   | XXXXh       |         |
| 06C77h  |        |                                      |             |         |
| 06C78h  | DTCCR7 | DTC Control Register 7               | XXh         |         |
| 06C79h  | DTBLS7 | DTC Block Size Register 7            | XXh         |         |
| 06C7Ah  | DTCCT7 | DTC Transfer Count Register 7        | XXh         |         |
| 06C7Bh  | DTRLD7 | DTC Transfer Count Reload Register 7 | XXh         |         |
| 06C7Ch  | DTSAR7 | DTC Source Address Register 7        | XXXXh       |         |
| 06C7Dh  |        |                                      |             |         |
| 06C7Eh  | DTDAR7 | DTC Destination Address Register 7   | XXXXh       |         |
| 06C7Fh  |        |                                      |             |         |
| 06C80h  | DTCCR8 | DTC Control Register 8               | XXh         |         |
| 06C81h  | DTBLS8 | DTC Block Size Register 8            | XXh         |         |
| 06C82h  | DTCCT8 | DTC Transfer Count Register 8        | XXh         |         |
| 06C83h  | DTRLD8 | DTC Transfer Count Reload Register 8 | XXh         |         |
| 06C84h  | DTSAR8 | DTC Source Address Register 8        | XXXXh       |         |
| 06C85h  |        |                                      |             |         |
| 06C86h  | DTDAR8 | DTC Destination Address Register 8   | XXXXh       |         |
| 06C87h  |        |                                      |             |         |
| 06C88h  | DTCCR9 | DTC Control Register 9               | XXh         |         |
| 06C89h  | DTBLS9 | DTC Block Size Register 9            | XXh         |         |
| 06C8Ah  | DTCCT9 | DTC Transfer Count Register 9        | XXh         |         |
| 06C8Bh  | DTRLD9 | DTC Transfer Count Reload Register 9 | XXh         |         |
| 06C8Ch  | DTSAR9 | DTC Source Address Register 9        | XXXXh       |         |
| 06C8Dh  |        |                                      |             |         |
| 06C8Eh  | DTDAR9 | DTC Destination Address Register 9   | XXXXh       |         |
| 06C8Fh  |        |                                      |             |         |

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.15 SFR Information (15) (1)**

| Address | Symbol  | Register Name                         | After Reset | Remarks |
|---------|---------|---------------------------------------|-------------|---------|
| 06C90h  | DTCCR10 | DTC Control Register 10               | XXh         |         |
| 06C91h  | DTBLS10 | DTC Block Size Register 10            | XXh         |         |
| 06C92h  | DTCCT10 | DTC Transfer Count Register 10        | XXh         |         |
| 06C93h  | DTRLD10 | DTC Transfer Count Reload Register 10 | XXh         |         |
| 06C94h  | DTSAR10 | DTC Source Address Register 10        | XXXXh       |         |
| 06C95h  |         |                                       |             |         |
| 06C96h  | DTDAR10 | DTC Destination Address Register 10   | XXXXh       |         |
| 06C97h  |         |                                       |             |         |
| 06C98h  | DTCCR11 | DTC Control Register 11               | XXh         |         |
| 06C99h  | DTBLS11 | DTC Block Size Register 11            | XXh         |         |
| 06CA0h  | DTCCT11 | DTC Transfer Count Register 11        | XXh         |         |
| 06C9Bh  | DTRLD11 | DTC Transfer Count Reload Register 11 | XXh         |         |
| 06C9Ch  | DTSAR11 | DTC Source Address Register 11        | XXXXh       |         |
| 06C9Dh  |         |                                       |             |         |
| 06C9Eh  | DTDAR11 | DTC Destination Address Register 11   | XXXXh       |         |
| 06C9Fh  |         |                                       |             |         |
| 06CA0h  | DTCCR12 | DTC Control Register 12               | XXh         |         |
| 06CA1h  | DTBLS12 | DTC Block Size Register 12            | XXh         |         |
| 06CA2h  | DTCCT12 | DTC Transfer Count Register 12        | XXh         |         |
| 06CA3h  | DTRLD12 | DTC Transfer Count Reload Register 12 | XXh         |         |
| 06CA4h  | DTSAR12 | DTC Source Address Register 12        | XXXXh       |         |
| 06CA5h  |         |                                       |             |         |
| 06CA6h  | DTDAR12 | DTC Destination Address Register 12   | XXXXh       |         |
| 06CA7h  |         |                                       |             |         |
| 06CA8h  | DTCCR13 | DTC Control Register 13               | XXh         |         |
| 06CA9h  | DTBLS13 | DTC Block Size Register 13            | XXh         |         |
| 06CAAh  | DTCCT13 | DTC Transfer Count Register 13        | XXh         |         |
| 06CABh  | DTRLD13 | DTC Transfer Count Reload Register 13 | XXh         |         |
| 06CACh  | DTSAR13 | DTC Source Address Register 13        | XXXXh       |         |
| 06CADh  |         |                                       |             |         |
| 06CAEh  | DTDAR13 | DTC Destination Address Register 13   | XXXXh       |         |
| 06CAFh  |         |                                       |             |         |
| 06CB0h  | DTCCR14 | DTC Control Register 14               | XXh         |         |
| 06CB1h  | DTBLS14 | DTC Block Size Register 14            | XXh         |         |
| 06CB2h  | DTCCT14 | DTC Transfer Count Register 14        | XXh         |         |
| 06CB3h  | DTRLD14 | DTC Transfer Count Reload Register 14 | XXh         |         |
| 06CB4h  | DTSAR14 | DTC Source Address Register 14        | XXXXh       |         |
| 06CB5h  |         |                                       |             |         |
| 06CB6h  | DTDAR14 | DTC Destination Address Register 14   | XXXXh       |         |
| 06CB7h  |         |                                       |             |         |
| 06CB8h  | DTCCR15 | DTC Control Register 15               | XXh         |         |
| 06CB9h  | DTBLS15 | DTC Block Size Register 15            | XXh         |         |
| 06CBAh  | DTCCT15 | DTC Transfer Count Register 15        | XXh         |         |
| 06CBBh  | DTRLD15 | DTC Transfer Count Reload Register 15 | XXh         |         |
| 06CBCh  | DTSAR15 | DTC Source Address Register 15        | XXXXh       |         |
| 06CBDh  |         |                                       |             |         |
| 06CBEh  | DTDAR15 | DTC Destination Address Register 15   | XXXXh       |         |
| 06CBFh  |         |                                       |             |         |
| 06CC0h  | DTCCR16 | DTC Control Register 16               | XXh         |         |
| 06CC1h  | DTBLS16 | DTC Block Size Register 16            | XXh         |         |
| 06CC2h  | DTCCT16 | DTC Transfer Count Register 16        | XXh         |         |
| 06CC3h  | DTRLD16 | DTC Transfer Count Reload Register 16 | XXh         |         |
| 06CC4h  | DTSAR16 | DTC Source Address Register 16        | XXXXh       |         |
| 06CC5h  |         |                                       |             |         |
| 06CC6h  | DTDAR16 | DTC Destination Address Register 16   | XXXXh       |         |
| 06CC7h  |         |                                       |             |         |
| 06CC8h  | DTCCR17 | DTC Control Register 17               | XXh         |         |
| 06CC9h  | DTBLS17 | DTC Block Size Register 17            | XXh         |         |
| 06CCAh  | DTCCT17 | DTC Transfer Count Register 17        | XXh         |         |
| 06CCBh  | DTRLD17 | DTC Transfer Count Reload Register 17 | XXh         |         |
| 06CCCh  | DTSAR17 | DTC Source Address Register 17        | XXXXh       |         |
| 06CCDh  |         |                                       |             |         |
| 06CCEh  | DTDAR17 | DTC Destination Address Register 17   | XXXXh       |         |
| 06CCFh  |         |                                       |             |         |

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.16 SFR Information (16) (1)**

| Address                | Symbol  | Register Name                         | After Reset | Remarks |
|------------------------|---------|---------------------------------------|-------------|---------|
| 06CD0h                 | DTCCR18 | DTC Control Register 18               | XXh         |         |
| 06CD1h                 | DTBLS18 | DTC Block Size Register 18            | XXh         |         |
| 06CD2h                 | DTCCT18 | DTC Transfer Count Register 18        | XXh         |         |
| 06CD3h                 | DTRLD18 | DTC Transfer Count Reload Register 18 | XXh         |         |
| 06CD4h                 | DTSAR18 | DTC Source Address Register 18        | XXXXh       |         |
| 06CD5h                 |         |                                       |             |         |
| 06CD6h                 | DTDAR18 | DTC Destination Address Register 18   | XXXXh       |         |
| 06CD7h                 |         |                                       |             |         |
| 06CD8h                 | DTCCR19 | DTC Control Register 19               | XXh         |         |
| 06CD9h                 | DTBLS19 | DTC Block Size Register 19            | XXh         |         |
| 06CDAh                 | DTCCT19 | DTC Transfer Count Register 19        | XXh         |         |
| 06CDBh                 | DTRLD19 | DTC Transfer Count Reload Register 19 | XXh         |         |
| 06CDC                  | DTSAR19 | DTC Source Address Register 19        | XXXXh       |         |
| 06CDDh                 |         |                                       |             |         |
| 06CDEh                 | DTDAR19 | DTC Destination Address Register 19   | XXXXh       |         |
| 06CDFh                 |         |                                       |             |         |
| 06CE0h                 | DTCCR20 | DTC Control Register 20               | XXh         |         |
| 06CE1h                 | DTBLS20 | DTC Block Size Register 20            | XXh         |         |
| 06CE2h                 | DTCCT20 | DTC Transfer Count Register 20        | XXh         |         |
| 06CE3h                 | DTRLD20 | DTC Transfer Count Reload Register 20 | XXh         |         |
| 06CE4h                 | DTSAR20 | DTC Source Address Register 20        | XXXXh       |         |
| 06CE5h                 |         |                                       |             |         |
| 06CE6h                 | DTDAR20 | DTC Destination Address Register 20   | XXXXh       |         |
| 06CE7h                 |         |                                       |             |         |
| 06CE8h                 | DTCCR21 | DTC Control Register 21               | XXh         |         |
| 06CE9h                 | DTBLS21 | DTC Block Size Register 21            | XXh         |         |
| 06CEAh                 | DTCCT21 | DTC Transfer Count Register 21        | XXh         |         |
| 06CEBh                 | DTRLD21 | DTC Transfer Count Reload Register 21 | XXh         |         |
| 06CECh                 | DTSAR21 | DTC Source Address Register 21        | XXXXh       |         |
| 06CEDh                 |         |                                       |             |         |
| 06CEEh                 | DTDAR21 | DTC Destination Address Register 21   | XXXXh       |         |
| 06CEFh                 |         |                                       |             |         |
| 06CF0h                 | DTCCR22 | DTC Control Register 22               | XXh         |         |
| 06CF1h                 | DTBLS22 | DTC Block Size Register 22            | XXh         |         |
| 06CF2h                 | DTCCT22 | DTC Transfer Count Register 22        | XXh         |         |
| 06CF3h                 | DTRLD22 | DTC Transfer Count Reload Register 22 | XXh         |         |
| 06CF4h                 | DTSAR22 | DTC Source Address Register 22        | XXXXh       |         |
| 06CF5h                 |         |                                       |             |         |
| 06CF6h                 | DTDAR22 | DTC Destination Address Register 22   | XXXXh       |         |
| 06CF7h                 |         |                                       |             |         |
| 06CF8h                 | DTCCR23 | DTC Control Register 23               | XXh         |         |
| 06CF9h                 | DTBLS23 | DTC Block Size Register 23            | XXh         |         |
| 06CFAh                 | DTCCT23 | DTC Transfer Count Register 23        | XXh         |         |
| 06CFBh                 | DTRLD23 | DTC Transfer Count Reload Register 23 | XXh         |         |
| 06CFCh                 | DTSAR23 | DTC Source Address Register 23        | XXXXh       |         |
| 06CFDh                 |         |                                       |             |         |
| 06CFEh                 | DTDAR23 | DTC Destination Address Register 23   | XXXXh       |         |
| 06CFFh                 |         |                                       |             |         |
| 06D00h<br>to<br>06FFFh |         |                                       |             |         |

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 3.17 ID code Area, Option Function Select Area**

| Address | Symbol | Area Name                         | After Reset | Address size |
|---------|--------|-----------------------------------|-------------|--------------|
| 0FFDBh  | OFS2   | Option Function Select Register 2 | (Note 1)    |              |
| 0FFDFh  | ID1    |                                   | (Note 2)    |              |
| 0FFE3h  | ID2    |                                   | (Note 2)    |              |
| 0FFEBh  | ID3    |                                   | (Note 2)    |              |
| 0FFEFh  | ID4    |                                   | (Note 2)    |              |
| 0FFF3h  | ID5    |                                   | (Note 2)    |              |
| 0FFF7h  | ID6    |                                   | (Note 2)    |              |
| 0FFFBh  | ID7    |                                   | (Note 2)    |              |
| 0FFFFh  | OFS    | Option Function Select Register   | (Note 1)    |              |

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the option function select area. Erasing the block including the option function select area sets the option function select area to FFh.
2. The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the ID code area. Erasing the block including the ID code area sets the ID code area to FFh.



## 4. Electrical Characteristics

### 4.1 Absolute Maximum Ratings

**Table 4.1 Absolute Maximum Ratings**

| Symbol  | Parameter                     | Condition                       | Rated Value                                     | Unit |
|---|-------------------------------|---------------------------------|---|------|
| V <sub>cc</sub> /A <sub>V</sub> cc<br>I <sub>CE</sub> V <sub>cc</sub> | Supply voltage                |                                 | -0.3 to 6.5                                     | V    |
| V <sub>i</sub>  | Input voltage                 |                                 | -0.3 to V <sub>cc</sub> + 0.3                   | V    |
| V <sub>o</sub>  | Output voltage                |                                 | -0.3 to V <sub>cc</sub> + 0.3                   | V    |
| P <sub>d</sub>  | Power dissipation             | -40°C ≤ T <sub>opr</sub> ≤ 85°C | 500   | mW   |
| T <sub>opr</sub>  | Operating ambient temperature |                                 | -20 to 85 (N version)/<br>-40 to 85 (D version) | °C   |
| T <sub>stg</sub>  | Storage temperature           |                                 | -65 to 150                                      | °C   |

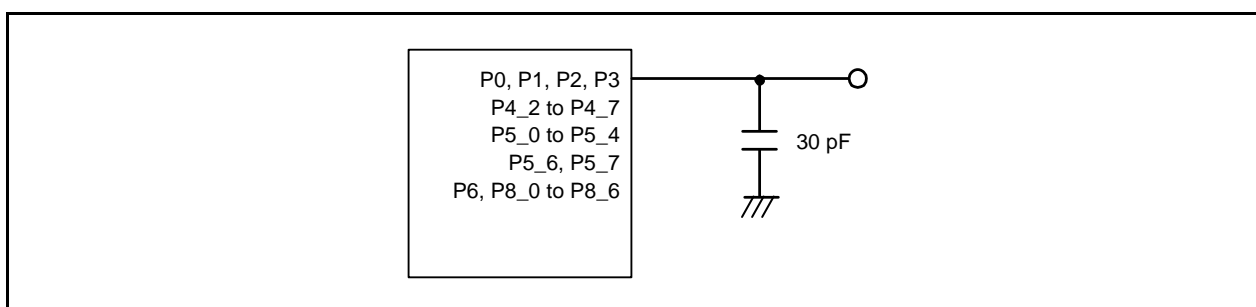
## 4.2 Recommended Operating Conditions

**Table 4.2 Recommended Operating Conditions (1)**  
( $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ ,  $T_{opr} = -20^\circ\text{C to } 85^\circ\text{C}$  (N version)/  $-40^\circ\text{C to } 85^\circ\text{C}$  (D version), unless otherwise specified)

| Symbol           | Parameter                              |  | Conditions                                     | Standard                                      |  |              | Unit        |             |   |
|------------------|--|--|--|---|--|--------------|-------------|-------------|---|
|                  |  |  |  | Min.  | Typ.   | Max.         |             |             |   |
| $V_{CC}/AV_{CC}$ | Supply voltage                         |  |  | 1.8   | —  | 5.5          | V           |             |   |
| $V_{SS}/AV_{SS}$ | Supply voltage                         |  |  | —   | 0  | —            | V           |             |   |
| $V_{IH}$         | Input high voltage                     | Other than CMOS input                          |  |   | $0.8V_{CC}$                                    | —            | $V_{CC}$    | V           |   |
|                  |  | CMOS input                                     | Input level switching function (I/O port)      | Input level selection:<br>0.35V <sub>CC</sub> | $4.0 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ | $0.5V_{CC}$  | —           | $V_{CC}$    | V |
|                  |  |  |  |   | $2.7 \text{ V} \leq V_{CC} < 4.0 \text{ V}$    | $0.55V_{CC}$ | —           | $V_{CC}$    | V |
|                  |  |  |  | Input level selection:<br>0.5V <sub>CC</sub>  | $1.8 \text{ V} \leq V_{CC} < 2.7 \text{ V}$    | $0.65V_{CC}$ | —           | $V_{CC}$    | V |
|                  |  |  |  |   | $4.0 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ | $0.65V_{CC}$ | —           | $V_{CC}$    | V |
|                  |  |  |  | Input level selection:<br>0.7V <sub>CC</sub>  | $2.7 \text{ V} \leq V_{CC} < 4.0 \text{ V}$    | $0.7V_{CC}$  | —           | $V_{CC}$    | V |
|                  |  |  |  |   | $1.8 \text{ V} \leq V_{CC} < 2.7 \text{ V}$    | $0.8V_{CC}$  | —           | $V_{CC}$    | V |
|                  |  | Input level selection:<br>0.7V <sub>CC</sub>   | $4.0 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ | $0.85V_{CC}$                                  | —  | $V_{CC}$     | V           |             |   |
|                  |  |  | $2.7 \text{ V} \leq V_{CC} < 4.0 \text{ V}$    | $0.85V_{CC}$                                  | —  | $V_{CC}$     | V           |             |   |
|                  |  | External clock input (XOUT)                    |  |   |  | 1.2          | —           | $V_{CC}$    | V |
| $V_{IL}$         | Input low voltage                      | Other than CMOS input                          |  |   | 0  | —            | $0.2V_{CC}$ | V           |   |
|                  |  | CMOS input                                     | Input level switching function (I/O port)      | Input level selection:<br>0.35V <sub>CC</sub> | $4.0 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ | 0            | —           | $0.2V_{CC}$ | V |
|                  |  |  |  |   | $2.7 \text{ V} \leq V_{CC} < 4.0 \text{ V}$    | 0            | —           | $0.2V_{CC}$ | V |
|                  |  |  |  | Input level selection:<br>0.5V <sub>CC</sub>  | $1.8 \text{ V} \leq V_{CC} < 2.7 \text{ V}$    | 0            | —           | $0.2V_{CC}$ | V |
|                  |  |  |  |   | $4.0 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ | 0            | —           | $0.4V_{CC}$ | V |
|                  |  |  |  | Input level selection:<br>0.7V <sub>CC</sub>  | $2.7 \text{ V} \leq V_{CC} < 4.0 \text{ V}$    | 0            | —           | $0.3V_{CC}$ | V |
|                  |  |  |  |   | $1.8 \text{ V} \leq V_{CC} < 2.7 \text{ V}$    | 0            | —           | $0.2V_{CC}$ | V |
|                  |  | Input level selection:<br>0.7V <sub>CC</sub>   | $4.0 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ | 0   | —  | $0.55V_{CC}$ | V           |             |   |
|                  |  |  | $2.7 \text{ V} \leq V_{CC} < 4.0 \text{ V}$    | 0   | —  | $0.45V_{CC}$ | V           |             |   |
|                  |  | External clock input (XOUT)                    |  |   |  | 0            | —           | 0.4         | V |
| $I_{OH(sum)}$    | Peak sum output high current           | Sum of all pins $I_{OH(peak)}$                 |  | —   | —  | -80          | mA          |             |   |
| $I_{OH(sum)}$    | Average sum output high current        | Sum of all pins $I_{OH(avg)}$                  |  | —   | —  | -40          | mA          |             |   |
| $I_{OH(peak)}$   | Peak output high current               | When drive capacity is low                     |  | —   | —  | -10          | mA          |             |   |
|                  |  | When drive capacity is high                    |  | —   | —  | -40          | mA          |             |   |
| $I_{OH(avg)}$    | Average output high current            | When drive capacity is low                     |  | —   | —  | -5           | mA          |             |   |
|                  |  | When drive capacity is high                    |  | —   | —  | -20          | mA          |             |   |
| $I_{OL(sum)}$    | Peak sum output low current            | Sum of all pins $I_{OL(peak)}$                 |  | —   | —  | 80           | mA          |             |   |
| $I_{OL(sum)}$    | Average sum output low current         | Sum of all pins $I_{OL(avg)}$                  |  | —   | —  | 40           | mA          |             |   |
| $I_{OL(peak)}$   | Peak output low current                | When drive capacity is low                     |  | —   | —  | 10           | mA          |             |   |
|                  |  | When drive capacity is high                    |  | —   | —  | 40           | mA          |             |   |
| $I_{OL(avg)}$    | Average output low current             | When drive capacity is low                     |  | —   | —  | 5            | mA          |             |   |
|                  |  | When drive capacity is high                    |  | —   | —  | 20           | mA          |             |   |
| $f_{(XIN)}$      | XIN clock input oscillation frequency  | $2.7 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ |  | —   | —  | 20           | MHz         |             |   |
|                  |  | $1.8 \text{ V} \leq V_{CC} < 2.7 \text{ V}$    |  | —   | —  | 5            | MHz         |             |   |
| $f_{(XCIN)}$     | XCIN clock input oscillation frequency | $1.8 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ |  | —   | 32.768   | 50           | kHz         |             |   |
| $f_{HOCO}$       | Count source for timer RC              | $2.7 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ |  | 32  | —  | 40           | MHz         |             |   |
| $f_{HOCO-F}$     | fHOCO-F frequency                      | $2.7 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ |  | —   | —  | 20           | MHz         |             |   |
|                  |  | $1.8 \text{ V} \leq V_{CC} < 2.7 \text{ V}$    |  | —   | —  | 5            | MHz         |             |   |
| —                | System clock frequency                 | $2.7 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ |  | —   | —  | 20           | MHz         |             |   |
|                  |  | $1.8 \text{ V} \leq V_{CC} < 2.7 \text{ V}$    |  | —   | —  | 5            | MHz         |             |   |
| $f_{(BCLK)}$     | CPU clock frequency                    | $2.7 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ |  | —   | —  | 20           | MHz         |             |   |
|                  |  | $1.8 \text{ V} \leq V_{CC} < 2.7 \text{ V}$    |  | —   | —  | 5            | MHz         |             |   |

Note:

1. The average output current indicates the average value of current measured during 100 ms.



**Figure 4.1** Timing Measurement Circuit for Ports P0, P1, P2, P3, P4\_2 to P4\_7, P5\_0 to P5\_4, P5\_6, P5\_7, P6, and P8\_0 to P8\_6

### 4.3 Peripheral Function Characteristics

**Table 4.3 A/D Converter Characteristics**  
( $V_{CC}/AV_{CC} = V_{ref} = 2.2\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_{opr} = -20^{\circ}\text{C to }85^{\circ}\text{C}$  (N version)/  
 $-40^{\circ}\text{C to }85^{\circ}\text{C}$  (D version), unless otherwise specified)

| Symbol      | Parameter                 |  | Conditions   | Standard |         |           | Unit          |
|-------------|---------------------------|--|--|----------|---------|-----------|---------------|
|             |                           |  |  | Min.     | Typ.    | Max.      |               |
| —           | Resolution                |  | $V_{ref} = AV_{CC}$  | —        | —       | 10        | Bit           |
| —           | Absolute accuracy         | 10-bit mode  | $V_{ref} = AV_{CC} = 5.0\text{ V}$ AN0 to AN11 input             | —        | —       | $\pm 3$   | LSB           |
|             |                           |  | $V_{ref} = AV_{CC} = 3.3\text{ V}$ AN0 to AN11 input             | —        | —       | $\pm 5$   | LSB           |
|             |                           |  | $V_{ref} = AV_{CC} = 3.0\text{ V}$ AN0 to AN11 input             | —        | —       | $\pm 5$   | LSB           |
|             |                           |  | $V_{ref} = AV_{CC} = 2.2\text{ V}$ AN0 to AN11 input             | —        | —       | $\pm 5$   | LSB           |
|             | 8-bit mode                | $V_{ref} = AV_{CC} = 5.0\text{ V}$ AN0 to AN11 input | —  | —        | $\pm 2$ | LSB       |               |
|             |                           | $V_{ref} = AV_{CC} = 3.3\text{ V}$ AN0 to AN11 input | —  | —        | $\pm 2$ | LSB       |               |
|             |                           | $V_{ref} = AV_{CC} = 3.0\text{ V}$ AN0 to AN11 input | —  | —        | $\pm 2$ | LSB       |               |
|             |                           | $V_{ref} = AV_{CC} = 2.2\text{ V}$ AN0 to AN11 input | —  | —        | $\pm 2$ | LSB       |               |
| $\phi_{AD}$ | A/D conversion clock      |  | $4.0\text{ V} \leq V_{ref} = AV_{CC} \leq 5.5\text{ V}$ (1)      | 2        | —       | 20        | MHz           |
|             |                           |  | $3.2\text{ V} \leq V_{ref} = AV_{CC} \leq 5.5\text{ V}$ (1)      | 2        | —       | 16        | MHz           |
|             |                           |  | $2.7\text{ V} \leq V_{ref} = AV_{CC} \leq 5.5\text{ V}$ (1)      | 2        | —       | 10        | MHz           |
|             |                           |  | $2.2\text{ V} \leq V_{ref} = AV_{CC} \leq 5.5\text{ V}$ (1)      | 2        | —       | 5         | MHz           |
| —           | Tolerance level impedance |  |  | —        | 3       | —         | k $\Omega$    |
| $I_{Vref}$  | Vref current              |  | $V_{CC} = 5\text{ V}$ , $XIN = f1 = fAD = 20\text{ MHz}$         | —        | 45      | —         | $\mu\text{A}$ |
| $t_{CONV}$  | Conversion time           | 10-bit mode  | $V_{ref} = AV_{CC} = 5.0\text{ V}$ , $\phi_{AD} = 20\text{ MHz}$ | 2.2      | —       | —         | $\mu\text{s}$ |
|             |                           | 8-bit mode   | $V_{ref} = AV_{CC} = 5.0\text{ V}$ , $\phi_{AD} = 20\text{ MHz}$ | 2.2      | —       | —         | $\mu\text{s}$ |
| $t_{SAMP}$  | Sampling time             |  | $\phi_{AD} = 20\text{ MHz}$                                      | 0.8      | —       | —         | $\mu\text{s}$ |
| $V_{ref}$   | Reference voltage         |  |  | 2.2      | —       | $AV_{CC}$ | V             |
| $V_{IA}$    | Analog input voltage (2)  |  |  | 0        | —       | $V_{ref}$ | V             |
| OCVREF      | On-chip reference voltage |  | $2\text{ MHz} \leq \phi_{AD} \leq 4\text{ MHz}$                  | 1.19     | 1.34    | 1.49      | V             |

Notes:

1. If the CPU and the flash memory stop, the A/D conversion result will be undefined.
2. When the analog input voltage exceeds the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

**Table 4.4 Comparator B Characteristics**  
( $V_{CC}/AV_{CC} = 2.2\text{ V to }5.5\text{ V}$ ,  $T_{opr} = -20^{\circ}\text{C to }85^{\circ}\text{C}$  (N version)/  $-40^{\circ}\text{C to }85^{\circ}\text{C}$  (D version),  
unless otherwise specified)

| Symbol    | Parameter                              |  | Conditions                        | Standard |      |                | Unit          |
|-----------|--|--|-----------------------------------|----------|------|----------------|---------------|
|           |  |  |                                   | Min.     | Typ. | Max.           |               |
| $V_{ref}$ | IVREF1, IVREF3 input reference voltage |  |                                   | 0        | —    | $V_{CC} - 1.4$ | V             |
| $V_I$     | IVCMP1, IVCMP3 input voltage           |  |                                   | -0.3     | —    | $V_{CC} + 0.3$ | V             |
| —         | Offset                                 |  |                                   | —        | 5    | 100            | mV            |
| $t_d$     | Comparator output delay time (1)       |  | $V_I = V_{ref} \pm 100\text{ mV}$ | —        | 0.1  | —              | $\mu\text{s}$ |
| $I_{CMP}$ | Comparator operating current           |  | $V_{CC} = 5.0\text{ V}$           | —        | 17.5 | —              | $\mu\text{A}$ |

Note:

1. When the digital filter is not selected.

**Table 4.5 Flash Memory (Program ROM) Characteristics**  
**(V<sub>cc</sub> = 2.7 V to 5.5 V, T<sub>opr</sub> = -20°C to 85°C (N version)/ -40°C to 85°C (D version),**  
**unless otherwise specified)**

| Symbol                        | Parameter  | Conditions  | Standard                     |      |                             | Unit  |
|-------------------------------|--|---|------------------------------|------|-----------------------------|-------|
|                               |  |   | Min.                         | Typ. | Max.                        |       |
| —                             | Program/erase endurance <sup>(1)</sup>                                 |   | 1,000 <sup>(2)</sup>         | —    | —                           | times |
| —                             | Byte program time<br>(Program and erase endurance ≤ 100 times)         |   | —                            | —    | —                           | μs    |
| —                             | Byte program time<br>(Program and erase endurance ≤ 1,000 times)       |   | —                            | —    | —                           | μs    |
| —                             | Word program time<br>(Program and erase endurance ≤ 100 times)         | T <sub>opr</sub> = 25°C,<br>V <sub>cc</sub> = 5.0 V | —                            | 100  | 200                         | μs    |
| —                             | Word program time<br>(Program and erase endurance ≤ 100 times)         |   | —                            | 100  | 400                         | μs    |
| —                             | Word program time<br>(Program and erase endurance ≤ 1,000 times)       |   | —                            | 100  | 650                         | μs    |
| —                             | Block erase time   |   | —                            | 0.3  | 4                           | s     |
| t <sub>d</sub> (SR-SUS)       | Time delay from suspend request until suspend                          |   | —                            | —    | 5 + CPU clock<br>× 3 cycles | ms    |
| —                             | Interval from erase start/restart until following suspend request      |   | 0                            | —    | —                           | μs    |
| —                             | Time from suspend until erase restart                                  |   | —                            | —    | 30 + CPU clock<br>× 1 cycle | μs    |
| t <sub>d</sub> (CMDRST-READY) | Time from when command is forcibly terminated until reading is enabled |   | —                            | —    | 30 + CPU clock<br>× 1 cycle | μs    |
| —                             | Program, erase voltage   |   | 2.7                          | —    | 5.5                         | V     |
| —                             | Read voltage   |   | 1.8                          | —    | 5.5                         | V     |
| —                             | Program, erase temperature   |   | -20 (N ver.)<br>-40 (D ver.) | —    | 85                          | °C    |
| —                             | Data hold time <sup>(6)</sup>  | Ambient temperature<br>= 55°C <sup>(7)</sup>        | 20                           | —    | —                           | year  |

## Notes:

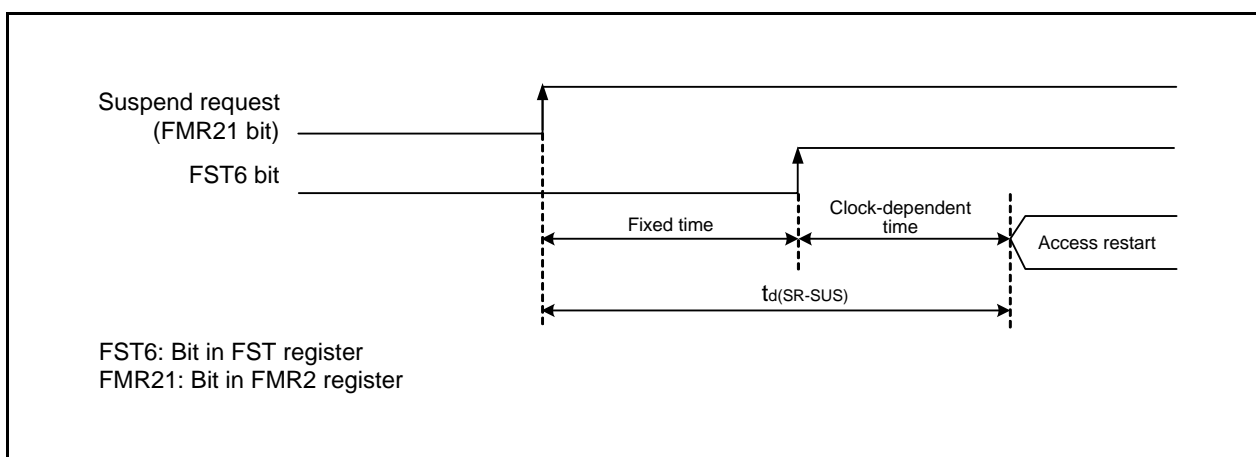
- Definition of programming/erasure endurance  
The programming and erasure endurance is defined on a per-block basis.  
If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.  
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- The data hold time includes time that the power supply is off or the clock is not supplied.
- The data hold time includes 7,000 hours under an environment of ambient temperature 85°C.

**Table 4.6 Flash Memory (Data flash Block A to Block D) Characteristics**  
**(V<sub>cc</sub> = 2.7 V to 5.5 V, T<sub>opr</sub> = -20°C to 85°C (N version)/ -40°C to 85°C (D version),**  
**unless otherwise specified)**

| Symbol                        | Parameter  | Conditions                                | Standard                     |      |                             | Unit  |
|-------------------------------|--|---|------------------------------|------|-----------------------------|-------|
|                               |  |   | Min.                         | Typ. | Max.                        |       |
| —                             | Program/erase endurance <sup>(1)</sup>                                 |   | 10,000 <sup>(2)</sup>        | —    | —                           | times |
| —                             | Byte program time<br>(Program and erase endurance ≤ 1,000 times)       |   | —                            | 160  | 950                         | μs    |
| —                             | Byte program time<br>(Program and erase endurance > 1,000 times)       |   | —                            | 300  | 950                         | μs    |
| —                             | Block erase time<br>(Program and erase endurance ≤ 1,000 times)        |   | —                            | 0.2  | 1                           | s     |
| —                             | Block erase time<br>(Program and erase endurance > 1,000 times)        |   | —                            | 0.3  | 1                           | s     |
| t <sub>d</sub> (SR-SUS)       | Time delay from suspend request until suspend                          |   | —                            | —    | 3 + CPU clock<br>× 3 cycles | ms    |
| —                             | Interval from erase start/restart until following suspend request      |   | 0                            | —    | —                           | μs    |
| —                             | Time from suspend until erase restart                                  |   | —                            | —    | 30 + CPU clock<br>× 1 cycle | μs    |
| t <sub>d</sub> (CMDRST-READY) | Time from when command is forcibly terminated until reading is enabled |   | —                            | —    | 30 + CPU clock<br>× 1 cycle | μs    |
| —                             | Program, erase voltage   |   | 2.7                          | —    | 5.5                         | V     |
| —                             | Read voltage   |   | 1.8                          | —    | 5.5                         | V     |
| —                             | Program, erase temperature   |   | -20 (N ver.)<br>-40 (D ver.) | —    | 85                          | °C    |
| —                             | Data hold time <sup>(6)</sup>  | Ambient temperature = 55°C <sup>(7)</sup> | 20                           | —    | —                           | year  |

## Notes:

- Definition of programming/erasure endurance  
The programming and erasure endurance is defined on a per-block basis.  
If the programming and erasure endurance is n (n = 100, 1,000 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.  
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- The data hold time includes time that the power supply is off or the clock is not supplied.
- The data hold time includes 7,000 hours under an environment of ambient temperature 85°C.



**Figure 4.2** Time Delay from Suspend Request until Suspend

**Table 4.7** Voltage Detection 0 Circuit Characteristics  
(Measurement conditions:  $V_{CC} = 1.8\text{ V to }5.5\text{ V}$ ,  $T_{opr} = -20^{\circ}\text{C to }85^{\circ}\text{C}$  (N version)/  
 $-40^{\circ}\text{C to }85^{\circ}\text{C}$  (D version))

| Symbol              | Parameter   | Conditions  | Standard |      |      | Unit |
|---------------------|---|---|----------|------|------|------|
|                     |   |   | Min.     | Typ. | Max. |      |
| V <sub>det0</sub>   | Voltage detection level V <sub>det0_0</sub> (1)                   | When V <sub>CC</sub> falls  | 1.80     | 1.90 | 2.05 | V    |
|                     | Voltage detection level V <sub>det0_1</sub> (1)                   | When V <sub>CC</sub> falls  | 2.15     | 2.35 | 2.55 | V    |
|                     | Voltage detection level V <sub>det0_2</sub> (1)                   | When V <sub>CC</sub> falls  | 2.70     | 2.85 | 3.05 | V    |
|                     | Voltage detection level V <sub>det0_3</sub> (1)                   | When V <sub>CC</sub> falls  | 3.55     | 3.80 | 4.05 | V    |
| —                   | Voltage detection 0 circuit response time (2)                     | At the falling of V <sub>CC</sub> from 5 V to (V <sub>det0</sub> - 0.1) V | —        | 6    | 150  | μs   |
| —                   | Voltage detection circuit self power consumption                  | VCA25 = 1, V <sub>CC</sub> = 5.0 V  | —        | 1.5  | —    | μA   |
| t <sub>d(E-A)</sub> | Waiting time until voltage detection circuit operation starts (3) |   | —        | —    | 100  | μs   |

Notes:

1. The voltage detection level must be selected with bits VDSEL0 and VDSEL1 in the OFS register.
2. Time until the voltage monitor 0 reset is generated after the voltage passes V<sub>det0</sub>.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

**Table 4.8 Voltage Detection 1 Circuit Characteristics**  
**(Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = -20°C to 85°C (N version)/**  
**-40°C to 85°C (D version))**

| Symbol                              | Parameter  | Conditions  | Standard |      |      | Unit |
|-------------------------------------|--|---|----------|------|------|------|
|                                     |  |   | Min.     | Typ. | Max. |      |
| Vdet1                               | Voltage detection level Vdet1_0 (1)                                  | When Vcc falls                                    | 2.00     | 2.20 | 2.40 | V    |
|                                     | Voltage detection level Vdet1_1 (1)                                  | When Vcc falls                                    | 2.15     | 2.35 | 2.55 | V    |
|                                     | Voltage detection level Vdet1_2 (1)                                  | When Vcc falls                                    | 2.30     | 2.50 | 2.70 | V    |
|                                     | Voltage detection level Vdet1_3 (1)                                  | When Vcc falls                                    | 2.45     | 2.65 | 2.85 | V    |
|                                     | Voltage detection level Vdet1_4 (1)                                  | When Vcc falls                                    | 2.60     | 2.80 | 3.00 | V    |
|                                     | Voltage detection level Vdet1_5 (1)                                  | When Vcc falls                                    | 2.75     | 2.95 | 3.15 | V    |
|                                     | Voltage detection level Vdet1_6 (1)                                  | When Vcc falls                                    | 2.80     | 3.10 | 3.40 | V    |
|                                     | Voltage detection level Vdet1_7 (1)                                  | When Vcc falls                                    | 2.95     | 3.25 | 3.55 | V    |
|                                     | Voltage detection level Vdet1_8 (1)                                  | When Vcc falls                                    | 3.10     | 3.40 | 3.70 | V    |
|                                     | Voltage detection level Vdet1_9 (1)                                  | When Vcc falls                                    | 3.25     | 3.55 | 3.85 | V    |
|                                     | Voltage detection level Vdet1_A (1)                                  | When Vcc falls                                    | 3.40     | 3.70 | 4.00 | V    |
|                                     | Voltage detection level Vdet1_B (1)                                  | When Vcc falls                                    | 3.55     | 3.85 | 4.15 | V    |
|                                     | Voltage detection level Vdet1_C (1)                                  | When Vcc falls                                    | 3.70     | 4.00 | 4.30 | V    |
|                                     | Voltage detection level Vdet1_D (1)                                  | When Vcc falls                                    | 3.85     | 4.15 | 4.45 | V    |
|                                     | Voltage detection level Vdet1_E (1)                                  | When Vcc falls                                    | 4.00     | 4.30 | 4.60 | V    |
| Voltage detection level Vdet1_F (1) | When Vcc falls   | 4.15  | 4.45     | 4.75 | V    |      |
| —                                   | Hysteresis width at the rising of Vcc in voltage detection 1 circuit | Vdet1_0 to Vdet1_5 selected                       | —        | 0.07 | —    | V    |
|                                     |  | Vdet1_6 to Vdet1_F selected                       | —        | 0.10 | —    | V    |
| —                                   | Voltage detection 1 circuit response time (2)                        | At the falling of Vcc from 5 V to (Vdet1 - 0.1) V | —        | 60   | 150  | μs   |
| —                                   | Voltage detection circuit self power consumption                     | VCA26 = 1, Vcc = 5.0 V                            | —        | 1.7  | —    | μA   |
| td(E-A)                             | Waiting time until voltage detection circuit operation starts (3)    |   | —        | —    | 100  | μs   |

Notes:

1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

**Table 4.9 Voltage Detection 2 Circuit Characteristics**  
**(Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = -20°C to 85°C (N version)/**  
**-40°C to 85°C (D version))**

| Symbol  | Parameter  | Conditions  | Standard |      |      | Unit |
|---------|--|---|----------|------|------|------|
|         |  |   | Min.     | Typ. | Max. |      |
| Vdet2   | Voltage detection level Vdet2_0                                      | When Vcc falls                                      | 3.70     | 4.00 | 4.30 | V    |
| —       | Hysteresis width at the rising of Vcc in voltage detection 2 circuit |   | —        | 0.1  | —    | μs   |
| —       | Voltage detection 2 circuit response time (1)                        | At the falling of Vcc from 5 V to (Vdet2_0 - 0.1) V | —        | 20   | 150  | μs   |
| —       | Voltage detection circuit self power consumption                     | VCA27 = 1, Vcc = 5.0 V                              | —        | 1.7  | —    | μA   |
| td(E-A) | Waiting time until voltage detection circuit operation starts (2)    |   | —        | —    | 100  | μs   |

Notes:

1. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

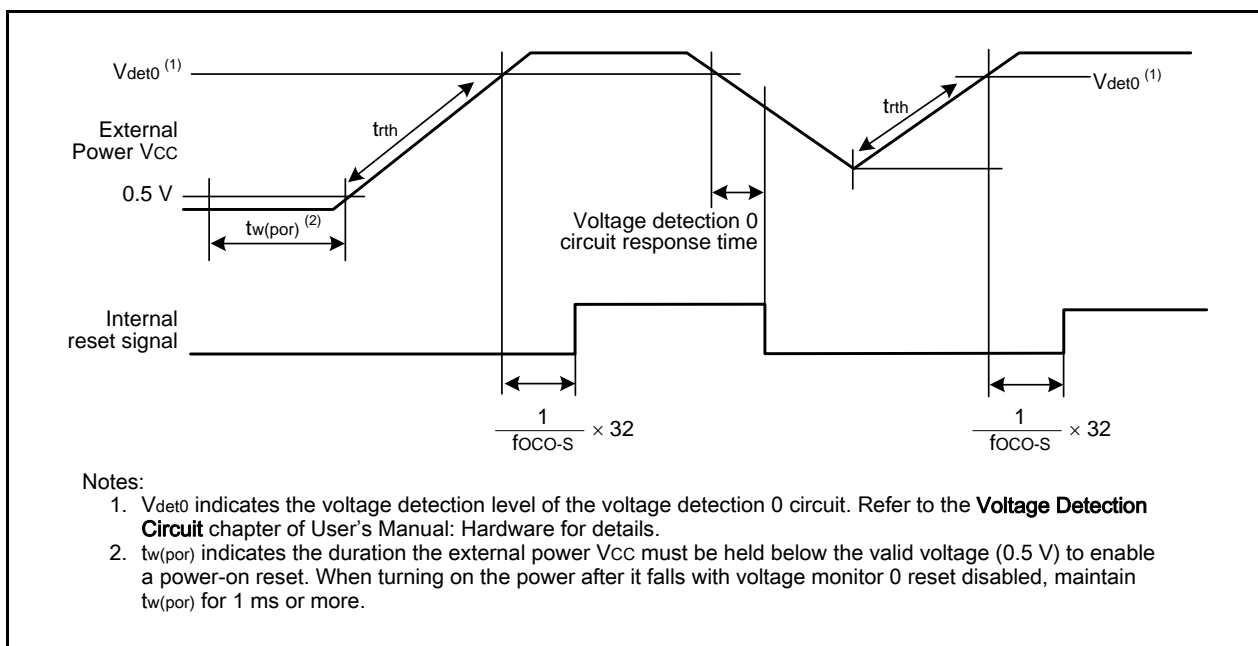


**Table 4.10 Power-On Reset Circuit Characteristics (1)**  
**(Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = -20°C to 85°C (N version)/**  
**-40°C to 85°C (D version))**

| Symbol | Parameter                        | Conditions | Standard |      |        | Unit    |
|--------|----------------------------------|------------|----------|------|--------|---------|
|        |                                  |            | Min.     | Typ. | Max.   |         |
| trth   | External power VCC rise gradient |            | 0        | —    | 50,000 | mV/msec |

Note:

- To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



**Figure 4.3 Power-on Reset Circuit Characteristics**

**Table 4.11 High-Speed On-Chip Oscillator Circuit Characteristics**

| Symbol | Parameter   | Conditions  | Standard |        |      | Unit |
|--------|---|---|----------|--------|------|------|
|        |   |   | Min.     | Typ.   | Max. |      |
| —      | High-speed on-chip oscillator frequency after reset   | V <sub>cc</sub> = 1.8 V to 5.5 V, -20°C ≤ Topr ≤ 85°C | —        | 40     | —    | MHz  |
| —      | High-speed on-chip oscillator frequency when 01b or 10b is written to bits FRA25 and FRA24 in the FRA2 register (1) | (N version)<br>-40°C ≤ Topr ≤ 85°C<br>(D version)     | —        | 36.864 | —    | MHz  |
| —      | High-speed on-chip oscillator frequency when 10b is written to bits FRA25 and FRA24 in the FRA2 register            |   | —        | 32     | —    | MHz  |
| —      | High-speed on-chip oscillator frequency dependence on temperature and power supply voltage (2)                      |   | -1.5     | —      | 1.5  | %    |
| —      | Oscillation stability time  | V <sub>cc</sub> = 5.0 V, Topr = 25°C                  | —        | 250    | —    | μs   |
| —      | Self power consumption at oscillation   | V <sub>cc</sub> = 5.0 V, Topr = 25°C                  | —        | 500    | —    | μA   |

Notes:

- This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.
- This indicates the precision error for the oscillation frequency of the high-speed on-chip oscillator.

**Table 4.12 Low-Speed On-Chip Oscillator Circuit Characteristics**  
**(Measurement conditions:  $V_{CC} = 1.8\text{ V to }5.5\text{ V}$ ,  $T_{opr} = -20^{\circ}\text{C to }85^{\circ}\text{C}$  (N version)/  
 $-40^{\circ}\text{C to }85^{\circ}\text{C}$  (D version))**

| Symbol             | Parameter                              | Conditions   | Standard |      |      | Unit          |
|--------------------|--|--|----------|------|------|---------------|
|                    |  |  | Min.     | Typ. | Max. |               |
| f <sub>L</sub> OCO | Low-speed on-chip oscillator frequency |  | 60       | 125  | 250  | kHz           |
| —                  | Oscillation stability time             | $V_{CC} = 5.0\text{ V}$ , $T_{opr} = 25^{\circ}\text{C}$ | —        | 30   | 100  | $\mu\text{s}$ |
| —                  | Self power consumption at oscillation  | $V_{CC} = 5.0\text{ V}$ , $T_{opr} = 25^{\circ}\text{C}$ | —        | 3    | —    | $\mu\text{A}$ |

**Table 4.13 Power Supply Circuit Characteristics**  
**(Measurement conditions:  $V_{CC} = 1.8\text{ V to }5.5\text{ V}$ ,  $T_{opr} = -20^{\circ}\text{C to }85^{\circ}\text{C}$  (N version)/  
 $-40^{\circ}\text{C to }85^{\circ}\text{C}$  (D version))**

| Symbol               | Parameter   | Conditions | Standard |      |       | Unit          |
|----------------------|---|------------|----------|------|-------|---------------|
|                      |   |            | Min.     | Typ. | Max.  |               |
| t <sub>d</sub> (P-R) | Time for internal power supply stabilization during power-on <sup>(1)</sup> |            | —        | —    | 2,000 | $\mu\text{s}$ |

Note:

1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

## 4.4 DC Characteristics

**Table 4.14 DC Characteristics (1) [4.2 V ≤ V<sub>CC</sub> ≤ 5.5 V]**  
**(Measurement conditions: V<sub>CC</sub> = 1.8 V to 5.5 V, Topr = -20°C to 85°C (N version)/**  
**-40°C to 85°C (D version))**

| Symbol              | Parameter           |   | Conditions               |                         | Standard              |                 |                 | Unit |
|---------------------|---------------------|---|--------------------------|-------------------------|-----------------------|-----------------|-----------------|------|
|                     |                     |   |                          |                         | Min.                  | Typ.            | Max.            |      |
| VOH                 | Output high voltage | Other than XOUT   | Drive capacity is high   | IOH = -20 mA            | V <sub>CC</sub> - 2.0 | —               | V <sub>CC</sub> | V    |
|                     |                     |   |                          | IOH = -5 mA             | V <sub>CC</sub> - 2.0 | —               | V <sub>CC</sub> | V    |
|                     |                     |   | IOH = -200 μA            | V <sub>CC</sub> - 0.3   | —                     | V <sub>CC</sub> | V               |      |
|                     |                     | XOUT  | IOH = -200 μA            | 1.0                     | —                     | V <sub>CC</sub> | V               |      |
| VOL                 | Output low voltage  | Other than XOUT   | Drive capacity is high   | IO <sub>L</sub> = 20 mA | —                     | —               | 2.0             | V    |
|                     |                     |   |                          | IO <sub>L</sub> = 5 mA  | —                     | —               | 2.0             | V    |
|                     |                     |   | IO <sub>L</sub> = 200 μA | —                       | —                     | 0.45            | V               |      |
|                     |                     | XOUT  | IO <sub>L</sub> = 200 μA | —                       | —                     | 0.5             | V               |      |
| VT+·VT-             | Hysteresis          | INT0 to INT4, KI0 to KI3,<br>TRJIO_0, TRCCLK_0,<br>TRCTRG_0, TRCIOA_0,<br>TRCIOB_0, TRCIOC_0,<br>TRCIOD_0,<br>CLK_0, CLK_1,<br>RXD_0, RXD_1, CTS2,<br>SCL2, SDA2, CLK2, RXD2,<br>SCL_0, SDA_0, SSI_0,<br>SCS_0, SSCK_0, SSO_0 |                          |                         | 0.1                   | 1.2             | —               | V    |
|                     |                     | RESET   | V <sub>CC</sub> = 5.0 V  |                         | 0.1                   | 1.2             | —               | V    |
| I <sub>IH</sub>     | Input high current  |   | V <sub>I</sub> = 5.0 V   |                         | —                     | —               | 1.0             | μA   |
| I <sub>IL</sub>     | Input low current   |   | V <sub>I</sub> = 0 V     |                         | —                     | —               | -1.0            | μA   |
| R <sub>PULLUP</sub> | Pull-up resistance  |   | V <sub>I</sub> = 0 V     |                         | 25                    | 50              | 100             | kΩ   |
| R <sub>IXIN</sub>   | Feedback resistance | XIN   |                          |                         | —                     | 0.3             | —               | MΩ   |
| R <sub>IXCIN</sub>  | Feedback resistance | XCIN  |                          |                         | —                     | 8               | —               | MΩ   |
| V <sub>RAM</sub>    | RAM hold voltage    |   | During stop mode         |                         | 1.8                   | —               | —               | V    |

**Table 4.15 DC Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V]  
(Topr = -20°C to 85°C (N version)/ -40°C to 85°C (D version), unless otherwise specified)**

| Symbol | Parameter                |                                    | Conditions  |        |                    |   |                                     |   |  | Standard (4) |      |      | Unit |
|--------|--------------------------|------------------------------------|-------------|--------|--------------------|---|-------------------------------------|---|--|--------------|------|------|------|
|        |                          |                                    | Oscillation |        | On-Chip Oscillator |   | CPU Clock                           | Low-Power-Consumption Setting                   | Other  | Min.         | Typ. | Max. |      |
|        |                          |                                    | XIN (2)     | XCIN   | High-Speed         | Low-Speed                                       |                                     |   |  |              |      |      |      |
| Icc    | Power supply current (1) | High-speed clock mode              | 20 MHz      | Off    | Off                | 125 kHz   | No division                         | —   |  | —            | 6.5  | 15   | mA   |
|        |                          |                                    | 16 MHz      | Off    | Off                | 125 kHz   | No division                         | —   |  | —            | 5.3  | 12.5 | mA   |
|        |                          |                                    | 10 MHz      | Off    | Off                | 125 kHz   | No division                         | —   |  | —            | 3.6  | —    | mA   |
|        |                          |                                    | 20 MHz      | Off    | Off                | 125 kHz   | Divide-by-8                         | —   |  | —            | 3.0  | —    | mA   |
|        |                          |                                    | 16 MHz      | Off    | Off                | 125 kHz   | Divide-by-8                         | —   |  | —            | 2.2  | —    | mA   |
|        |                          |                                    | 10 MHz      | Off    | Off                | 125 kHz   | Divide-by-8                         | —   |  | —            | 1.5  | —    | mA   |
|        |                          | High-speed on-chip oscillator mode | Off         | Off    | 20 MHz (3)         | 125 kHz   | No division                         | —   |  | —            | 7.0  | 15   | mA   |
|        |                          |                                    | Off         | Off    | 20 MHz (3)         | 125 kHz   | Divide-by-8                         | —   |  | —            | 3.0  | —    | mA   |
|        |                          |                                    | Off         | Off    | 4 MHz (3)          | 125 kHz   | Divide-by-16                        | MSTIIC = 1<br>MSTTRC = 1                        |  | —            | 1    | —    | mA   |
|        |                          | Low-speed on-chip oscillator mode  | Off         | Off    | Off                | 125 kHz   | Divide-by-8                         | FMR27 = 1<br>SVC0 = 0                           |  | —            | 90   | 400  | μA   |
|        |                          | Low-speed clock mode               | Off         | 32 kHz | Off                | Off   | —                                   | FMR27 = 1<br>SVC0 = 0                           |  | —            | 85   | 400  | μA   |
|        |                          |                                    | Off         | 32 kHz | Off                | Off   | —                                   | FMSTP = 1<br>SVC0 = 0                           | Program operation on RAM<br>Flash memory off                       | —            | 47   | —    | μA   |
|        |                          | Wait mode                          | Off         | Off    | Off                | 125 kHz   | —                                   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>SVC0 = 1 | While a WAIT instruction is executed<br>Peripheral clock operation | —            | 15   | 100  | μA   |
|        |                          |                                    | Off         | Off    | Off                | 125 kHz   | —                                   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>SVC0 = 1 | While a WAIT instruction is executed<br>Peripheral clock off       | —            | 4    | 90   | μA   |
|        |                          |                                    | Off         | 32 kHz | Off                | Off   | —                                   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>SVC0 = 1 | While a WAIT instruction is executed<br>Peripheral clock off       | —            | 3.5  | —    | μA   |
|        |                          | Stop mode                          | Off         | Off    | Off                | Off   | —                                   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1 | Topr = 25°C<br>Peripheral clock off                                | —            | 2.2  | 6.0  | μA   |
| Off    | Off                      |                                    | Off         | Off    | —                  | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1 | Topr = 85°C<br>Peripheral clock off | —   | 30   | —            | μA   |      |      |

## Notes:

- Vcc = 3.3 V to 5.5 V, single-chip mode, output pins are open, and other pins are Vss.
- XIN is set to square wave input.
- fHOCO-F
- The typical value (Typ.) indicates the current value when the CPU and the memory operate.  
The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

**Table 4.16 DC Characteristics (3) [2.7 V ≤ V<sub>CC</sub> < 4.2 V]**  
**(Measurement conditions: V<sub>CC</sub> = 1.8 V to 5.5 V, Topr = -20°C to 85°C (N version)/**  
**-40°C to 85°C (D version))**

| Symbol                           | Parameter           |  | Conditions              |                           | Standard              |      |                 | Unit |
|----------------------------------|---------------------|--|-------------------------|---------------------------|-----------------------|------|-----------------|------|
|                                  |                     |  |                         |                           | Min.                  | Typ. | Max.            |      |
| V <sub>OH</sub>                  | Output high voltage | Other than XOUT  | Drive capacity is high  | I <sub>OH</sub> = -5 mA   | V <sub>CC</sub> - 0.5 | —    | V <sub>CC</sub> | V    |
|                                  |                     |  | Drive capacity is low   | I <sub>OH</sub> = -1 mA   | V <sub>CC</sub> - 0.5 | —    | V <sub>CC</sub> | V    |
|                                  |                     | XOUT   |                         | I <sub>OH</sub> = -200 μA | 1.0                   | —    | V <sub>CC</sub> | V    |
| V <sub>OL</sub>                  | Output low voltage  | Other than XOUT  | Drive capacity is high  | I <sub>OL</sub> = 5 mA    | —                     | —    | 0.5             | V    |
|                                  |                     |  | Drive capacity is low   | I <sub>OL</sub> = 1 mA    | —                     | —    | 0.5             | V    |
|                                  |                     | XOUT   |                         | I <sub>OL</sub> = 200 μA  | —                     | —    | 0.5             | V    |
| V <sub>T+</sub> -V <sub>T-</sub> | Hysteresis          | INT0 to INT4, K10 to K13, TRJIO_0, TRCCLK_0, TRCTRG_0, TRCIOA_0, TRCIOB_0, TRCIOA_0, TRCIOD_0, CLK_0, CLK_1, RXD_0, RXD_1, CTS2, SCL2, SDA2, CLK2, RXD2, SCL_0, SDA_0, SSI_0, SCS_0, SSCK_0, SSO_0 |                         |                           | 0.1                   | 0.4  | —               | V    |
|                                  |                     | RESET  | V <sub>CC</sub> = 3.0 V |                           | 0.1                   | 0.5  | —               | V    |
| I <sub>IH</sub>                  | Input high current  |  | V <sub>I</sub> = 3.0 V  |                           | —                     | —    | 1.0             | μA   |
| I <sub>IL</sub>                  | Input low current   |  | V <sub>I</sub> = 0 V    |                           | —                     | —    | -1.0            | μA   |
| R <sub>PULLUP</sub>              | Pull-up resistance  |  | V <sub>I</sub> = 0 V    |                           | 42                    | 84   | 168             | kΩ   |
| R <sub>FXIN</sub>                | Feedback resistance | XIN  |                         |                           | —                     | 0.3  | —               | MΩ   |
| R <sub>FXCIN</sub>               | Feedback resistance | XCIN   |                         |                           | —                     | 8    | —               | MΩ   |
| V <sub>RAM</sub>                 | RAM hold voltage    |  | During stop mode        |                           | 1.8                   | —    | —               | V    |

**Table 4.17 DC Characteristics (4) [2.7 V ≤ Vcc < 3.3 V]  
(Topr = -20°C to 85°C (N version)/ -40°C to 85°C (D version), unless otherwise specified))**

| Symbol    | Parameter                |                                    | Conditions  |        |                    |   |                                     |   |  | Standard (4) |      |      | Unit |
|-----------|--------------------------|------------------------------------|-------------|--------|--------------------|---|-------------------------------------|---|--|--------------|------|------|------|
|           |                          |                                    | Oscillation |        | On-Chip Oscillator |   | CPU Clock                           | Low-Power-Consumption Setting                   | Other  | Min.         | Typ. | Max. |      |
|           |                          |                                    | XIN (2)     | XCIN   | High-Speed         | Low-Speed                                       |                                     |   |  |              |      |      |      |
| Icc       | Power supply current (1) | High-speed clock mode              | 10 MHz      | Off    | Off                | 125 kHz   | No division                         | —   |  | —            | 3.5  | 10   | mA   |
|           |                          |                                    | 10 MHz      | Off    | Off                | 125 kHz   | Divide-by-8                         | —   |  | —            | 1.5  | 7.5  | mA   |
|           |                          | High-speed on-chip oscillator mode | Off         | Off    | 20 MHz (3)         | 125 kHz   | No division                         | —   |  | —            | 7.0  | 15   | mA   |
|           |                          |                                    | Off         | Off    | 20 MHz (3)         | 125 kHz   | Divide-by-8                         | —   |  | —            | 3.0  | —    | mA   |
|           |                          |                                    | Off         | Off    | 10 MHz (3)         | 125 kHz   | No division                         | —   |  | —            | 4.0  | —    | mA   |
|           |                          |                                    | Off         | Off    | 10 MHz (3)         | 125 kHz   | Divide-by-8                         | —   |  | —            | 1.5  | —    | mA   |
|           |                          |                                    | Off         | Off    | 4 MHz (3)          | 125 kHz   | Divide-by-16                        | MSTIIC = 1<br>MSTTRC = 1                        |  | —            | 1    | —    | mA   |
|           |                          | Low-speed on-chip oscillator mode  | Off         | Off    | Off                | 125 kHz   | Divide-by-8                         | FMR27 = 1<br>SVC0 = 0                           |  | —            | 90   | 390  | μA   |
|           |                          |                                    | Off         | 32 kHz | Off                | Off   | No division                         | FMR27 = 1<br>SVC0 = 0                           |  | —            | 80   | 400  | μA   |
|           |                          | Low-speed clock mode               | Off         | 32 kHz | Off                | Off   | No division                         | FMSTP = 1<br>SVC0 = 0                           | Program operation on RAM<br>Flash memory off                       | —            | 40   | —    | μA   |
|           |                          |                                    | Off         | Off    | Off                | 125 kHz   | —                                   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>SVC0 = 1 | While a WAIT instruction is executed<br>Peripheral clock operation | —            | 15   | 90   | μA   |
|           |                          | Wait mode                          | Off         | Off    | Off                | 125 kHz   | —                                   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>SVC0 = 1 | While a WAIT instruction is executed<br>Peripheral clock off       | —            | 4    | 80   | μA   |
|           |                          |                                    | Off         | 32 kHz | Off                | Off   | —                                   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>SVC0 = 1 | While a WAIT instruction is executed<br>Peripheral clock off       | —            | 3.5  | —    | μA   |
|           |                          |                                    | Off         | Off    | Off                | Off   | —                                   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1 | Topr = 25°C<br>Peripheral clock off                                | —            | 2.2  | 6.0  | μA   |
| Stop mode | Off                      | Off                                | Off         | Off    | —                  | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1 | Topr = 85°C<br>Peripheral clock off | —   | 30   | —            | μA   |      |      |

## Notes:

1. Vcc = 2.7 V to 3.3 V, single-chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.  
The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

**Table 4.18 DC Characteristics (5) [1.8 V ≤ V<sub>CC</sub> < 2.7 V]**  
**(Measurement conditions: V<sub>CC</sub> = 1.8 V to 5.5 V, Topr = -20°C to 85°C (N version)/**  
**-40°C to 85°C (D version))**

| Symbol                           | Parameter           |   | Conditions              |                           | Standard              |      |                 | Unit |
|----------------------------------|---------------------|---|-------------------------|---------------------------|-----------------------|------|-----------------|------|
|                                  |                     |   |                         |                           | Min.                  | Typ. | Max.            |      |
| V <sub>OH</sub>                  | Output high voltage | Other than XOUT   | Drive capacity is high  | I <sub>OH</sub> = -2 mA   | V <sub>CC</sub> - 0.5 | —    | V <sub>CC</sub> | V    |
|                                  |                     |   | Drive capacity is low   | I <sub>OH</sub> = -1 mA   | V <sub>CC</sub> - 0.5 | —    | V <sub>CC</sub> | V    |
|                                  |                     | XOUT  |                         | I <sub>OH</sub> = -200 μA | 1.0                   | —    | V <sub>CC</sub> | V    |
| V <sub>OL</sub>                  | Output low voltage  | Other than XOUT   | Drive capacity is high  | I <sub>OL</sub> = 2 mA    | —                     | —    | 0.5             | V    |
|                                  |                     |   | Drive capacity is low   | I <sub>OL</sub> = 1 mA    | —                     | —    | 0.5             | V    |
|                                  |                     | XOUT  |                         | I <sub>OL</sub> = 200 μA  | —                     | —    | 0.5             | V    |
| V <sub>T+</sub> -V <sub>T-</sub> | Hysteresis          | INT0 to INT4, KI0 to KI3, TRJIO_0, TRCCLK_0, TRCTRG_0, TRCIOA_0, TRCIOB_0, TRCIOA_0, TRCIOD_0, CLK_0, CLK_1, RXD_0, RXD_1,CTS2, SCL2, SDA2, CLK2, RXD2, SCL_0, SDA_0,SSI_0, SCS_0, SSCK_0,SSO_0 |                         |                           | 0.05                  | 0.2  | —               | V    |
|                                  |                     | RESET   | V <sub>CC</sub> = 2.2 V |                           | 0.05                  | 0.2  | —               | V    |
| I <sub>IH</sub>                  | Input high current  |   | V <sub>I</sub> = 2.2 V  |                           | —                     | —    | 1.0             | μA   |
| I <sub>IL</sub>                  | Input low current   |   | V <sub>I</sub> = 0 V    |                           | —                     | —    | -1.0            | μA   |
| R <sub>PULLUP</sub>              | Pull-up resistance  |   | V <sub>I</sub> = 0 V    |                           | 100                   | 200  | 400             | kΩ   |
| R <sub>FXIN</sub>                | Feedback resistance | XIN   |                         |                           | —                     | 0.3  | —               | MΩ   |
| R <sub>FXCIN</sub>               | Feedback resistance | XCIN  |                         |                           | —                     | 8    | —               | MΩ   |
| V <sub>RAM</sub>                 | RAM hold voltage    |   | During stop mode        |                           | 1.8                   | —    | —               | V    |

**Table 4.19 DC Characteristics (6) [1.8 V ≤ V<sub>CC</sub> < 2.7 V]  
(Topr = −20°C to 85°C (N version)/ −40°C to 85°C (D version), unless otherwise specified)**

| Symbol          | Parameter                |                                    | Conditions  |        |                    |           |              |   |  | Standard (4) |      |      | Unit |
|-----------------|--------------------------|------------------------------------|-------------|--------|--------------------|-----------|--------------|---|--|--------------|------|------|------|
|                 |                          |                                    | Oscillation |        | On-Chip Oscillator |           | CPU Clock    | Low-Power-Consumption Setting                   | Other  | Min.         | Typ. | Max. |      |
|                 |                          |                                    | XIN (2)     | XCIN   | High-Speed         | Low-Speed |              |   |  |              |      |      |      |
| I <sub>CC</sub> | Power supply current (1) | High-speed clock mode              | 5 MHz       | Off    | Off                | 125 kHz   | No division  | —   |  | —            | 2.2  | —    | mA   |
|                 |                          |                                    | 5 MHz       | Off    | Off                | 125 kHz   | Divide-by-8  | —   |  | —            | 0.8  | —    | mA   |
|                 |                          | High-speed on-chip oscillator mode | Off         | Off    | 5 MHz (3)          | 125 kHz   | No division  | —   |  | —            | 2.5  | 10   | mA   |
|                 |                          |                                    | Off         | Off    | 5 MHz (3)          | 125 kHz   | Divide-by-8  | —   |  | —            | 1.7  | —    | mA   |
|                 |                          |                                    | Off         | Off    | 4 MHz (3)          | 125 kHz   | Divide-by-16 | MSTIIC = 1<br>MSTTRC = 1                        |  | —            | 1    | —    | mA   |
|                 |                          | Low-speed on-chip oscillator mode  | Off         | Off    | Off                | 125 kHz   | Divide-by-8  | FMR27 = 1<br>SVC0 = 0                           |  | —            | 90   | 300  | μA   |
|                 |                          | Low-speed clock mode               | Off         | 32 kHz | Off                | Off       | No division  | FMR27 = 1<br>SVC0 = 0                           |  | —            | 80   | 350  | μA   |
|                 |                          | Wait mode                          | Off         | Off    | Off                | 125 kHz   | —            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>SVC0 = 1 | While a WAIT instruction is executed<br>Peripheral clock operation | —            | 15   | 90   | μA   |
|                 |                          |                                    | Off         | Off    | Off                | 125 kHz   | —            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>SVC0 = 1 | While a WAIT instruction is executed<br>Peripheral clock off       | —            | 4    | 80   | μA   |
|                 |                          |                                    | Off         | 32 kHz | Off                | Off       | —            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>SVC0 = 1 | While a WAIT instruction is executed<br>Peripheral clock off       | —            | 3.5  | —    | μA   |
|                 |                          | Stop mode                          | Off         | Off    | Off                | Off       | —            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1 | Topr = 25°C<br>Peripheral clock off                                | —            | 2.2  | 6    | μA   |
|                 |                          |                                    | Off         | Off    | Off                | Off       | —            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1 | Topr = 85°C<br>Peripheral clock off                                | —            | 30   | —    | μA   |

## Notes:

1. V<sub>CC</sub> = 1.8 V to 2.7 V, single-chip mode, output pins are open, and other pins are V<sub>SS</sub>.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.  
The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.



## 4.5 AC Characteristics

**Table 4.20 Timing Requirements of Clock Synchronous Serial I/O with Chip Select  
(during Master Operation)  
(Measurement conditions:  $V_{CC} = 1.8\text{ V}$  to  $5.5\text{ V}$ ,  $T_{opr} = -20^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  (N version)/  
 $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  (D version))**

| Symbol | Parameter                                       | Conditions                                   | Standard                            |      |       | Unit     |
|--------|---|--|-------------------------------------|------|-------|----------|
|        |   |  | Min.                                | Typ. | Max.  |          |
| tsucyc | SSCK clock cycle time                           |  | 4.00                                | —    | —     | tcyc (1) |
| tHI    | SSCK clock high width                           |  | 0.40                                | —    | 0.60  | tsucyc   |
| tLO    | SSCK clock low width                            |  | 0.40                                | —    | 0.60  | tsucyc   |
| tRISE  | SSCK clock rising time                          | $2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | —                                   | —    | 0.50  | tcyc (1) |
|        |   | $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$    | —                                   | —    | 1.00  | tcyc (1) |
| tFALL  | SSCK clock falling time                         | $2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | —                                   | —    | 0.50  | tcyc (1) |
|        |   | $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$    | —                                   | —    | 1.00  | tcyc (1) |
| tsu    | SSI, SSO data input setup time                  | $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | 60                                  | —    | —     | ns       |
|        |   | $2.7\text{ V} \leq V_{CC} < 4.5\text{ V}$    | 70                                  | —    | —     | ns       |
|        |   | $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$    | 100                                 | —    | —     | ns       |
| tH     | SSI, SSO data input hold time                   | $2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | 2.00                                | —    | —     | tcyc (1) |
|        |   | $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$    | 2.00                                | —    | —     | tcyc (1) |
| tLEAD  | $\overline{\text{SCS}}$ -SCK output delay time  |  | $0.5\text{ tsucyc} - 1\text{ tcyc}$ | —    | —     | ns       |
| tLAG   | SCK - $\overline{\text{SCS}}$ output valid time |  | $0.5\text{ tsucyc} - 1\text{ tcyc}$ | —    | —     | ns       |
| tOD    | SSO data output delay time                      | $2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | —                                   | —    | 30.00 | ns       |
|        |   | $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$    | —                                   | —    | 1.00  | tcyc (1) |

Note:

1.  $1\text{tcyc} = 1/f_1$  (s)

**Table 4.21 Timing Requirements of Clock Synchronous Serial I/O with Chip Select  
(during Slave Operation)  
(Measurement conditions:  $V_{cc} = 1.8\text{ V to }5.5\text{ V}$ ,  $T_{opr} = -20^{\circ}\text{C to }85^{\circ}\text{C}$  (N version)/  
 $-40^{\circ}\text{C to }85^{\circ}\text{C}$  (D version))**

| Symbol | Parameter                          | Conditions                                   | Standard   |      |               | Unit                |
|--------|------------------------------------|--|------------|------|---------------|---------------------|
|        |                                    |  | Min.       | Typ. | Max.          |                     |
| tsucyc | SSCK clock cycle time              |  | 4.00       | —    | —             | tcyc <sup>(1)</sup> |
| tHI    | SSCK clock high width              |  | 0.40       | —    | 0.60          | tsucyc              |
| tLO    | SSCK clock low width               |  | 0.40       | —    | 0.60          | tsucyc              |
| tRISE  | SSCK clock rising time             |  | —          | —    | 1.00          | μs                  |
| tFALL  | SSCK clock falling time            |  | —          | —    | 1.00          | μs                  |
| tsu    | SSO data input setup time          |  | 10.00      | —    | —             | ns                  |
| tH     | SSO data input hold time           |  | 2.00       | —    | —             | tcyc <sup>(1)</sup> |
| tLEAD  | $\overline{\text{SCS}}$ setup time |  | 1tcyc + 50 | —    | —             | ns                  |
| tLAG   | $\overline{\text{SCS}}$ hold time  |  | 1tcyc + 50 | —    | —             | ns                  |
| tOD    | SSI, SSO data output delay time    | $4.5\text{ V} \leq V_{cc} \leq 5.5\text{ V}$ | —          | —    | 60            | ns                  |
|        |                                    | $2.7\text{ V} \leq V_{cc} < 4.5\text{ V}$    | —          | —    | 70            | ns                  |
|        |                                    | $1.8\text{ V} \leq V_{cc} < 2.7\text{ V}$    | —          | —    | 100.00        | ns                  |
| tsa    | SSI slave access time              | $2.7\text{ V} \leq V_{cc} \leq 5.5\text{ V}$ | —          | —    | 1.5tcyc + 100 | ns                  |
|        |                                    | $1.8\text{ V} \leq V_{cc} < 2.7\text{ V}$    | —          | —    | 1.5tcyc + 200 | ns                  |
| tor    | SSI slave out open time            | $2.7\text{ V} \leq V_{cc} \leq 5.5\text{ V}$ | —          | —    | 1.5tcyc + 100 | ns                  |
|        |                                    | $1.8\text{ V} \leq V_{cc} < 2.7\text{ V}$    | —          | —    | 1.5tcyc + 200 | ns                  |

Note:

1. 1tcyc = 1/f1 (s)

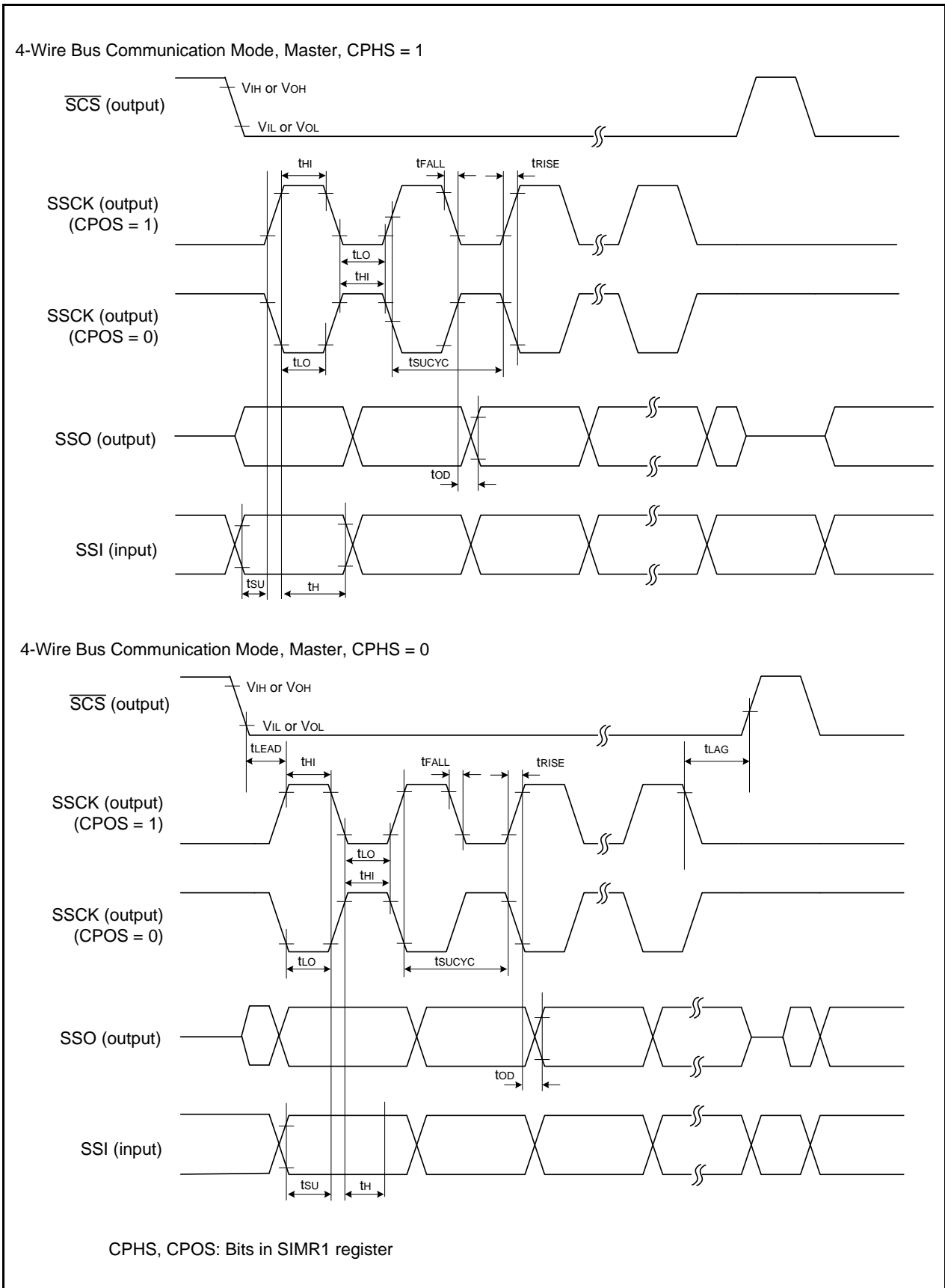


Figure 4.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

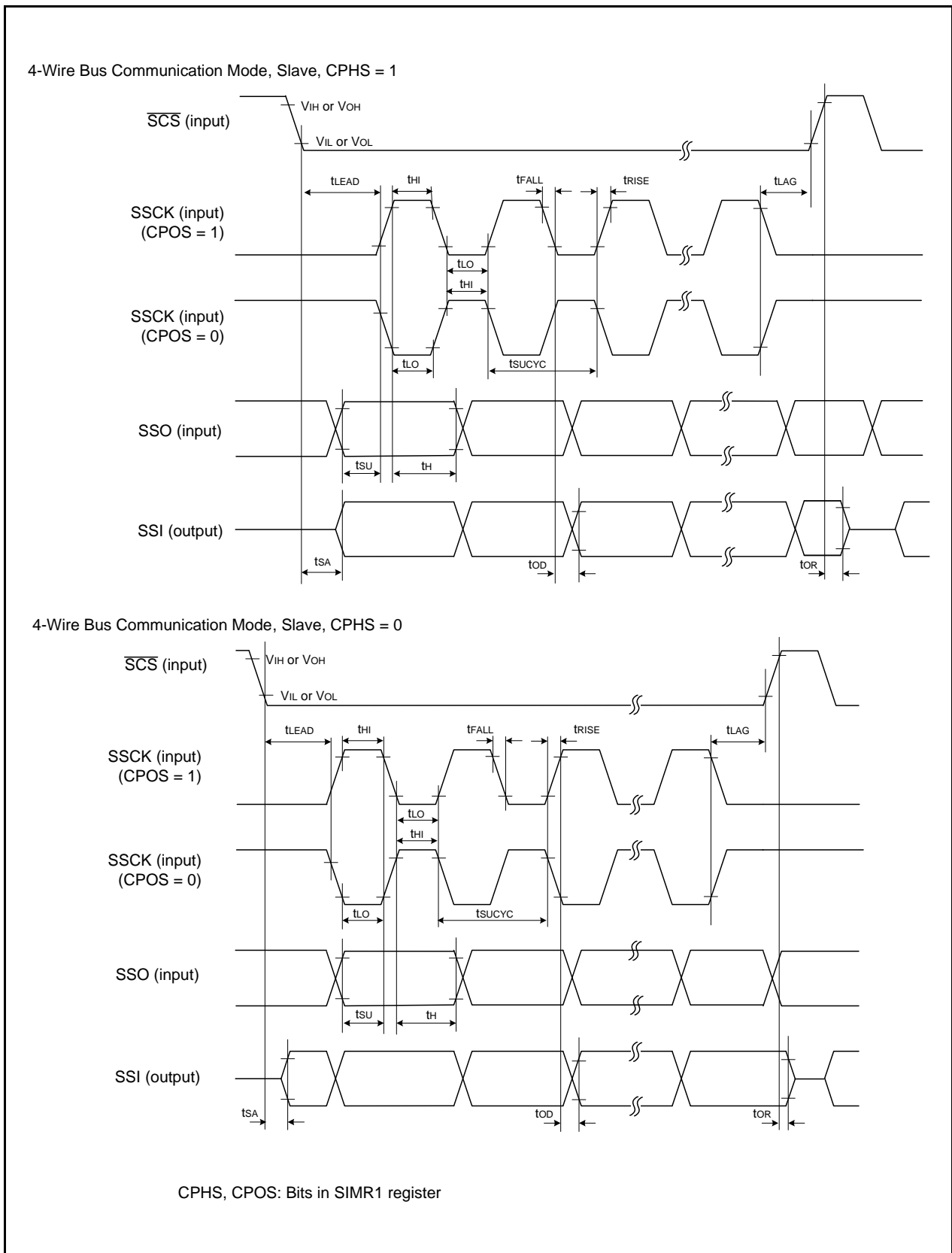
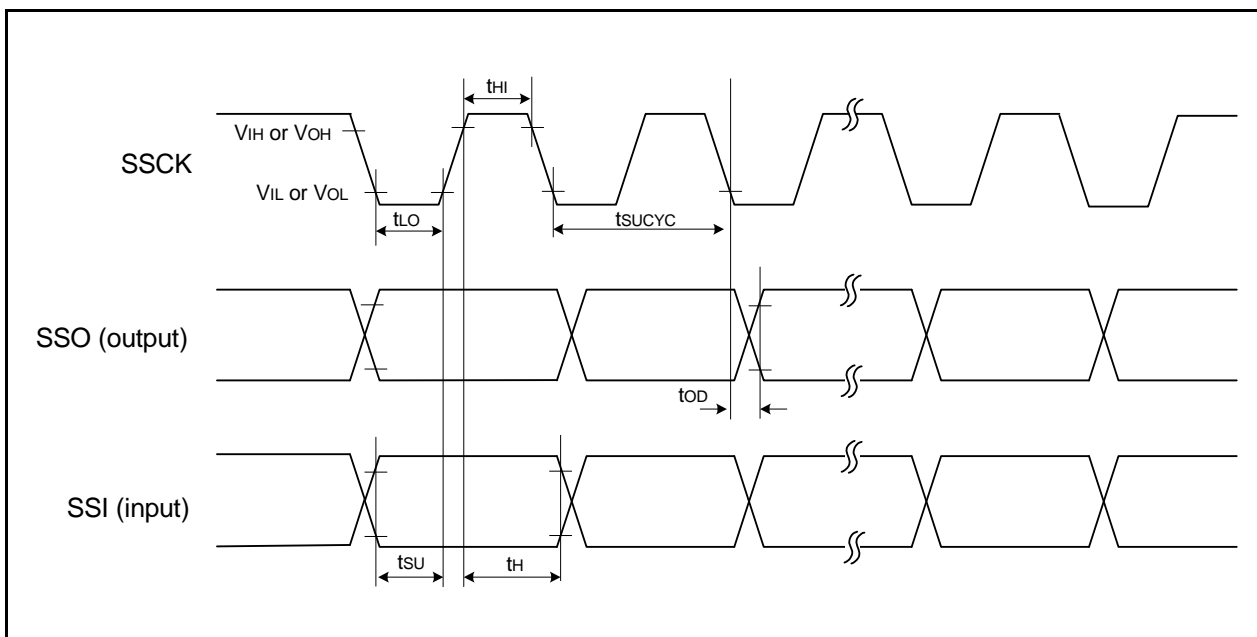


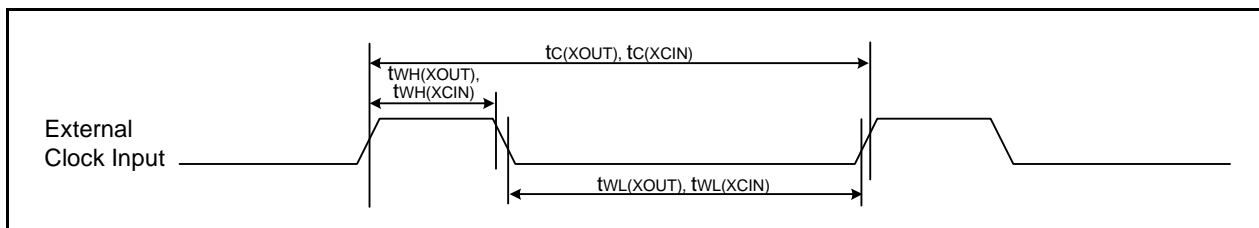
Figure 4.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)



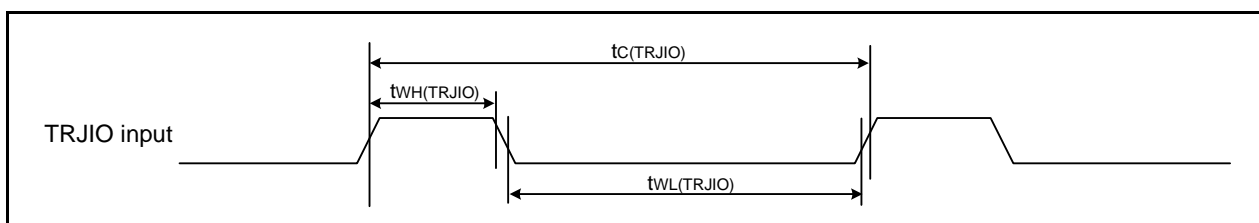
**Figure 4.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)**

**Table 4.22 External Clock Input (XOUT, XCIN)**

| Symbol                 | Parameter             | Standard                             |      |                                    |      |                                    |      | Unit |
|------------------------|-----------------------|--------------------------------------|------|------------------------------------|------|------------------------------------|------|------|
|                        |                       | V <sub>CC</sub> = 2.2 V, Topr = 25°C |      | V <sub>CC</sub> = 3 V, Topr = 25°C |      | V <sub>CC</sub> = 5 V, Topr = 25°C |      |      |
|                        |                       | Min.                                 | Max. | Min.                               | Max. | Min.                               | Max. |      |
| t <sub>c</sub> (XOUT)  | XOUT input cycle time | 200                                  | —    | 50                                 | —    | 50                                 | —    | ns   |
| t <sub>WH</sub> (XOUT) | XOUT input high width | 90                                   | —    | 24                                 | —    | 24                                 | —    | ns   |
| t <sub>WL</sub> (XOUT) | XOUT input low width  | 90                                   | —    | 24                                 | —    | 24                                 | —    | ns   |
| t <sub>c</sub> (XCIN)  | XCIN input cycle time | 14                                   | —    | 14                                 | —    | 14                                 | —    | μs   |
| t <sub>WH</sub> (XCIN) | XCIN input high width | 7                                    | —    | 7                                  | —    | 7                                  | —    | μs   |
| t <sub>WL</sub> (XCIN) | XCIN input low width  | 7                                    | —    | 7                                  | —    | 7                                  | —    | μs   |

**Figure 4.7 External Clock Input Timing Diagram****Table 4.23 Timing Requirements of TRJIO**

| Symbol                  | Parameter              | Standard                             |      |                                    |      |                                    |      | Unit |
|-------------------------|------------------------|--------------------------------------|------|------------------------------------|------|------------------------------------|------|------|
|                         |                        | V <sub>CC</sub> = 2.2 V, Topr = 25°C |      | V <sub>CC</sub> = 3 V, Topr = 25°C |      | V <sub>CC</sub> = 5 V, Topr = 25°C |      |      |
|                         |                        | Min.                                 | Max. | Min.                               | Max. | Min.                               | Max. |      |
| t <sub>c</sub> (TRJIO)  | TRJIO input cycle time | 500                                  | —    | 300                                | —    | 100                                | —    | ns   |
| t <sub>WH</sub> (TRJIO) | TRJIO input high width | 200                                  | —    | 120                                | —    | 40                                 | —    | ns   |
| t <sub>WL</sub> (TRJIO) | TRJIO input low width  | 200                                  | —    | 120                                | —    | 40                                 | —    | ns   |

**Figure 4.8 Input Timing of TRJIO**

**Table 4.24 Timing Requirements of Serial Interface  
(Internal clock selected as transfer clock (master communication))**

| Symbol               | Parameter                            | Standard                             |      |                                    |      |                                    |      | Unit |
|----------------------|--------------------------------------|--------------------------------------|------|------------------------------------|------|------------------------------------|------|------|
|                      |                                      | V <sub>CC</sub> = 2.2 V, Topr = 25°C |      | V <sub>CC</sub> = 3 V, Topr = 25°C |      | V <sub>CC</sub> = 5 V, Topr = 25°C |      |      |
|                      |                                      | Min.                                 | Max. | Min.                               | Max. | Min.                               | Max. |      |
| t <sub>d(C-Q)</sub>  | TXDi output delay time               | —                                    | 200  | —                                  | 30   | —                                  | 10   | ns   |
| t <sub>su(D-C)</sub> | RXDi input setup time <sup>(1)</sup> | 150                                  | —    | 120                                | —    | 90                                 | —    | ns   |
| t <sub>h(C-D)</sub>  | RXDi input hold time                 | 90                                   | —    | 90                                 | —    | 90                                 | —    | ns   |

i = 0 or 1

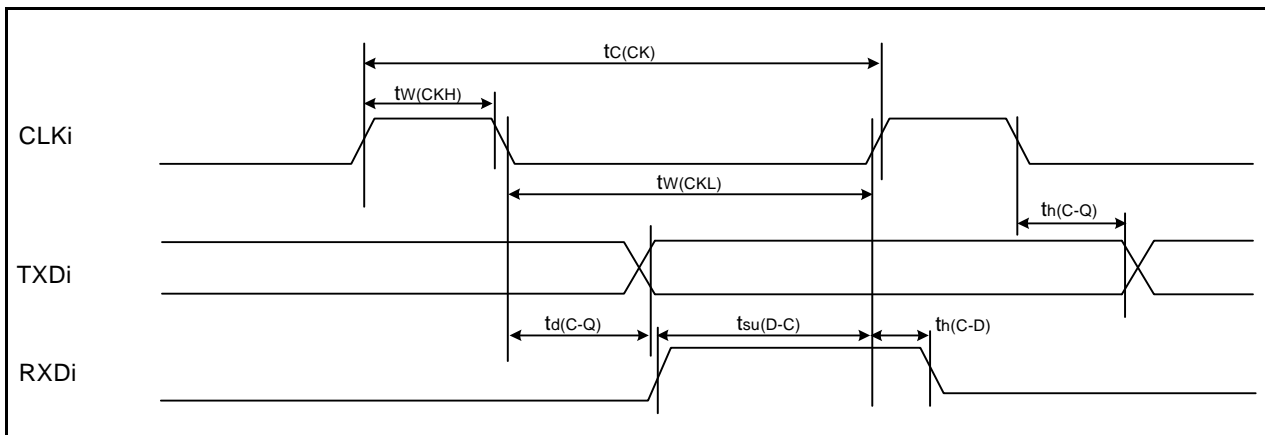
Note:

- External pin load condition CL = 30 pF

**Table 4.25 Timing Requirements of Serial Interface  
(External clock selected as transfer clock (slave communication))**

| Symbol               | Parameter              | Standard                             |      |                                    |      |                                    |      | Unit |
|----------------------|------------------------|--------------------------------------|------|------------------------------------|------|------------------------------------|------|------|
|                      |                        | V <sub>CC</sub> = 2.2 V, Topr = 25°C |      | V <sub>CC</sub> = 3 V, Topr = 25°C |      | V <sub>CC</sub> = 5 V, Topr = 25°C |      |      |
|                      |                        | Min.                                 | Max. | Min.                               | Max. | Min.                               | Max. |      |
| t <sub>c(CK)</sub>   | CLKi input cycle time  | 800                                  | —    | 300                                | —    | 200                                | —    | ns   |
| t <sub>w(CKH)</sub>  | CLKi input high width  | 400                                  | —    | 150                                | —    | 100                                | —    | ns   |
| t <sub>w(CKL)</sub>  | CLKi input low width   | 400                                  | —    | 150                                | —    | 100                                | —    | ns   |
| t <sub>d(C-Q)</sub>  | TXDi output delay time | —                                    | 200  | —                                  | 120  | —                                  | 90   | ns   |
| t <sub>su(D-C)</sub> | RXDi input setup time  | 150                                  | —    | 30                                 | —    | 10                                 | —    | ns   |
| t <sub>h(C-D)</sub>  | RXDi input hold time   | 90                                   | —    | 90                                 | —    | 90                                 | —    | ns   |

i = 0 or 1

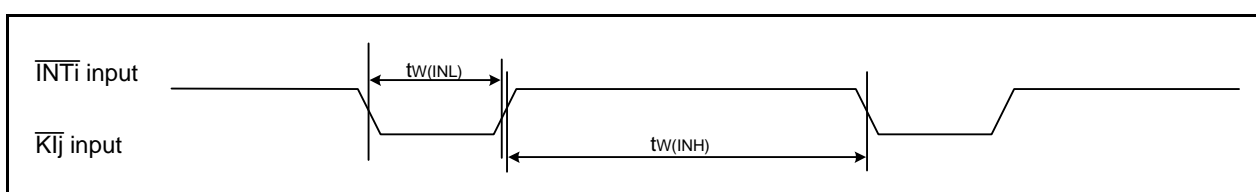
**Figure 4.9 Input and Output Timing of Serial Interface (i = 0 or 1)**

**Table 4.26 Timing Requirements of External Interrupt  $\overline{INTi}$  (i = 0 to 4) and Key Input Interrupt  $\overline{KIj}$  (j = 0 to 3)**

| Symbol       | Parameter  | Standard                 |      |                        |      |                        |      | Unit |
|--------------|--|--------------------------|------|------------------------|------|------------------------|------|------|
|              |  | Vcc = 2.2 V, Topr = 25°C |      | Vcc = 3 V, Topr = 25°C |      | Vcc = 5 V, Topr = 25°C |      |      |
|              |  | Min.                     | Max. | Min.                   | Max. | Min.                   | Max. |      |
| $t_{W(INH)}$ | $\overline{INTi}$ input high width,<br>$\overline{KIj}$ input high width | 1000 (1)                 | —    | 380 (1)                | —    | 250 (1)                | —    | ns   |
| $t_{W(INL)}$ | $\overline{INTi}$ input low width,<br>$\overline{KIj}$ input low width   | 1000 (2)                 | —    | 380 (2)                | —    | 250 (2)                | —    | ns   |

Notes:

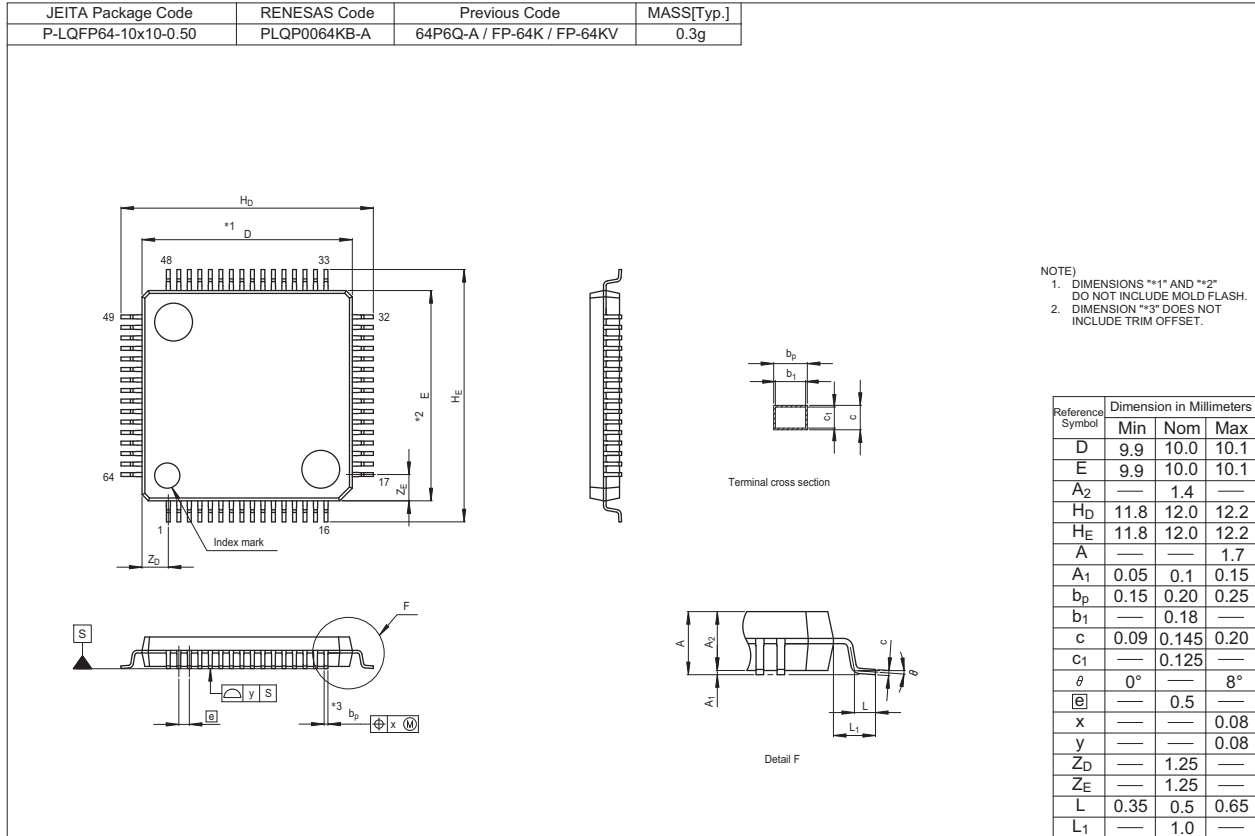
1. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input high pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input low pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.

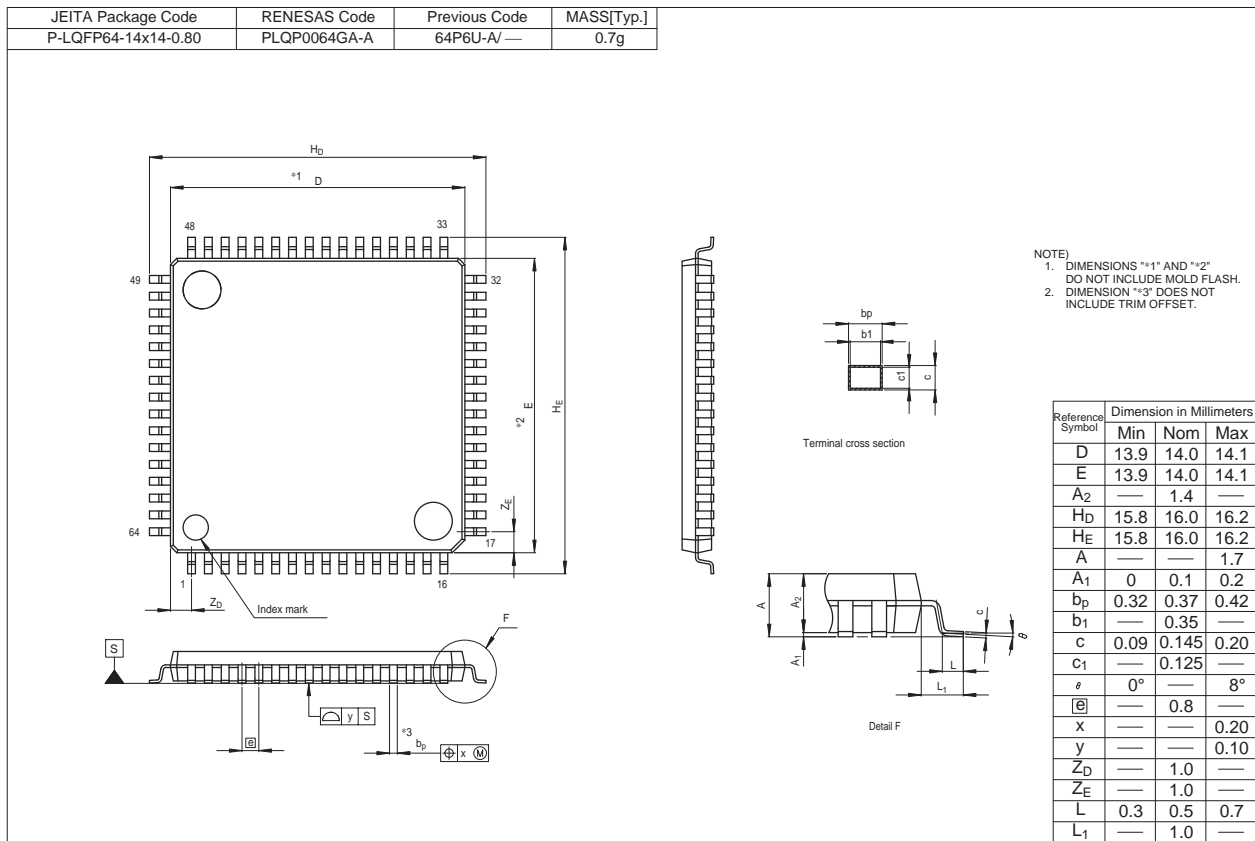
**Figure 4.10 Input Timing of External Interrupt  $\overline{INTi}$  and Key Input Interrupt  $\overline{KIj}$  (i = 0 to 4; j = 0 to 3)**



## Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.





REVISION HISTORY

R8C/36T-A Group Datasheet

| Rev. | Date         | Description                      |  |
|------|--------------|----------------------------------|--|
|      |              | Page                             | Summary  |
| 0.01 | Feb 23, 2011 | —                                | First Edition issued   |
| 1.00 | Dec 09, 2011 | All pages                        | "Preliminary", "Under development" deleted,<br>"sensor control unit" → "touch sensor control unit" |
|      |              | 2, 3                             | Tables 1.1 and 1.2 revised   |
|      |              | 6                                | Figure 1.3 "P3_10/CH10" → "P3_1/CH10"  |
|      |              | 11                               | Table 1.8 "Touch sensor control unit" added  |
|      |              | 13                               | 2.1 revised  |
|      |              | 16, 17,<br>19 to 22,<br>24 to 28 | Tables 3.1, 3.2, 3.4 to 3.7, 3.9 to 3.13   |
|      |              | 32                               | Table 3.17 revised, Note 2 added   |
|      |              | 33 to 56                         | "4. Electrical Characteristics" added  |

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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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