Single-Lead, Heart-Rate Monitor Analog Front End

Preliminary Technical Data

AD8232

FEATURES

Single lead ECG
2 or 3 electrodes
2-pole adjustable high pass filter with fast restore capability
3-pole adjustable low pass filter
Leads off detection: AC or DC options
Integrated right-leg drive (RLD) amplifier
Adjustable gain
Internal RFI filter
Shutdown Pin
20-lead 4x4mm LFCSP package

KEY SPECIFICATIONS

20µVp-p (typ) noise (0.5 Hz to 40 Hz)
CMRR: 80 dB (DC to 60 Hz)
Low supply current: 180 µA (typ)
±300 mV differential input range
Rail to rail output
2.0V to 3.5 supply voltage

APPLICATIONS

Fitness and Activity Heart Rate Monitoring
Portable ECG
Biopotential signal acquisition

FUNCTIONAL BLOCK DIAGRAM

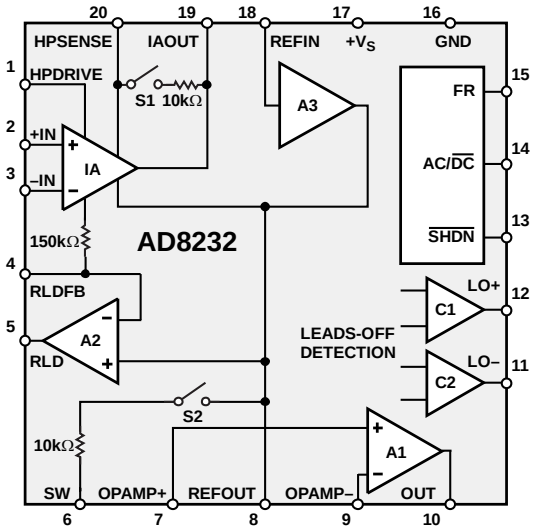

Figure 1.

GENERAL DESCRIPTION

The AD8232 is an integrated signal-conditioning block for ECG and other biopotential measurement applications. It is designed to convert the tiny, noisy signal from the electrodes into a large, filtered signal that can be easily read by a low resolution ADC.

The AD8232 can implement a two-pole high pass filter for eliminating motion artifacts and the electrode half-cell potential. This filter is tightly coupled with the instrumentation amplifier's architecture to allow both large gain and high pass filtering in a single stage, saving space and cost. Additionally, an uncommitted operational amplifier enables the AD8232 to create a three-pole low pass filter to remove line noise and other interference signals. The user can select the frequency cutoff of all filters to suit different types of applications.

The AD8232 includes a fast restore function that reduces the duration of otherwise long settling tails of the high-pass filters. After an abrupt change that rails the amplifier (such as a leads-off condition), the AD8232 automatically adjusts to higher filter cutoff. This functionality allows the AD8232 to recover quickly, and therefore take valid measurements soon after the leads are connected to the subject.

The AD8232 is available in a 4 x 4 mm 20 pin LFCSP package. Performance is specified from 0°C to +70°C and is operational from -40°C to 85°C.

Rev. PrD

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SPECIFICATIONS

$+V_S$ = +3V, $-V_S$ = 0V, V_{REF} = 1.5V, V_{IN+}=V_{IN-}=1.5V, T_A = 25°C, specifications referred to input, unless otherwise noted

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
IN AMP					
CMRR	DC to 60 Hz, V_{CM} = 0.5 V to 2.5V, V_{DIFF} = 0V		80		dB
PSRR	V_{DIFF} = 0V		80		dB
Gain			100		V/V
Gain Error	V_{DIFF} = –300mV to +300mV		3		%
Gain Drift	T_A = 0 to +70°C		50		ppm/°C
Input Range	T_A = 0 to +70°C				
DC Differential Input Operating Voltage		–300		300	mV
Input Operating Voltage (+IN, -IN)		$-V_S$ + 0.2		$+V_S$	V
Bias Current			100		pA
	T_A = 0 to +70°C				
Offset Current			100		pA
	T_A = 0 to +70°C				
Input Impedance					
Differential			100||5		MΩ||pF
Common Mode			100||5		MΩ||pF
Input Referred Voltage Noise	f=0.1 to 10 Hz				µV p-p
	f= 0.5 to 40 Hz		20		µV p-p
Output					
Output Swing	R_L= 50 kΩ to opposite supply rail, T_A = 0 to +70°C	$-V_S$ + 0.1		$+V_S$ – 0.1	V
Short Circuit Current					mA
Bandwidth			2		kHz
Slew Rate			0.05		V/µs
RFI Filter Cutoff			1		MHz
DC LEADS OFF COMPARATORS					
DC Leads Off Comparators					
Threshold Voltage		$+V_S$ – 0.6		$+V_S$ – 0.4	V
Hysteresis			50		mV
Propagation Delay	5 mV overdrive		10		µs
AC LEADS OFF					
Square Wave Frequency		50	100	175	kHz
Square Wave Amplitude			200		nA p-p
Impedance Threshold	Between +IN and –IN pins at 60 kHz	0.5	1	2	MΩ
FAST RESTORE CIRCUIT					
On Resistance	Between RC and IA OUT, Between REF and OP AMP+				
Normal Operation			1		GΩ
During Fast Recovery		8	10	13	kΩ
Comparator Window (Fast Restore Off)		$-V_S$ + 0.1		$+V_S$ – 0.1	V
Propagation Delay	5 mV overdrive		10		µs
RIGHT LEG DRIVE					
Output Swing	R_L= 50 kΩ to opposite supply rail	$-V_S$ + 0.1		$+V_S$ – 0.1	V
Short Circuit Current					
Sourcing			100		µA
Sinking			100		µA
Integrator Resistor		80	100	120	kΩ
Gain Bandwidth Product			100		kHz
REFERENCE BUFFER					
Input Bias Current				100	pA

Parameter	Conditions	Min	Typ	Max	Unit
Gain Error	R_L > 20 kΩ			0.5	%
Voltage Range	R_L = 20 kΩ to opposite supply rail	$-V_S$ + 0.1		$+V_S$ – 0.7	V
OP AMP					
Offset Voltage			TBD		µV
	T=0 to 70°C		TBD		µV
Input Bias Current			100		pA
	T=0 to 70°C				pA
Input Offset Current			100		pA
	T=0 to 70°C				
Input Voltage Range					V
Common Mode Rejection Ratio			100		dB
Power Supply Rejection Ratio					dB
Large Signal Voltage Gain					dB
Output Voltage Range	50 k Ω to opposite supply rail	–Vs+0.1		+Vs – 0.1	V
Short Circuit Current Limit					mA
Gain Bandwidth Product					kHz
Slew Rate					V/µs
Input Referred Voltage Noise	f=0.1 Hz to 10 Hz				µV p-p
	f=0.5 Hz to 40 Hz				µV p-p
SYSTEM SPECIFICATIONS					
Quiescent Supply Current					
Standard Operation			180		µA
	T=0 to 70°C				
Shutdown	T=0 to 70°C		1		µA
Supply Range		2.0		3.5	V
Specified Temperature Range		0		70	°C
Operational Temperature Range		–40		85	°C

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	+3.6V
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage at any input[1]	+Vs + 0.3V
Minimum Voltage at any input[1]	–0.3V
Storage Temperature Range	−40°C to +125°C
Max Junction Temperature	+150°C
θ_{JA} Thermal Impedance [2]	47°C/W
θ_{JC} Thermal Impedance	4.4°C/W
ESD	
Human Body Model	TBD
Charge Device Model	TBD
Machine Model	TBD

[1] If input voltages beyond the specified minimum or maximum voltages are expected, place resistors in series with the inputs to limit the current to less than 5 mA.

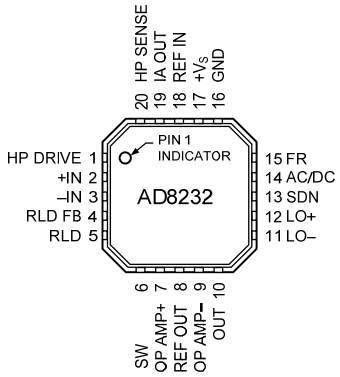
[2] θ_{JA} is specified for a device in free air on 4 layer JEDEC board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



TOP VIEW(Not to Scale)

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	HP DRIVE	Connect to capacitor in first high pass filter. AD8232 drives this pin to keep HP SENSE at the same level as the reference voltage.
2	+IN	Positive input terminal of instrumentation amplifier. Connect electrode (typically left arm) to this pin.
3	–IN	Negative input terminal of instrumentation amplifier. Connect electrode (typically right arm) to this pin.
4	RLD FB	Feedback terminal for right leg drive circuit.
5	RLD	Right leg drive output terminal. Connect driven electrode (typically right leg) to this pin.
6	SW	Fast restore switch for second high pass filter. Connect this pin to output of second high pass filter.
7	OP AMP+	Non-inverting input terminal of signal conditioning op amp.
8	REF OUT	Output of reference buffer. Connect to any point in the circuit that needs a reference voltage.
9	OP AMP–	Inverting terminal of signal conditioning op amp
10	OUT	Output of signal conditioning op amp. This output should have the fully conditioned heart rate signal. This terminal can be connected to the input of an analog to digital converter.
11	LO-	Leads-off comparator output In DC leads-off detection mode: high when electrode to –IN is disconnected. Low when connected. In AC leads-off detection mode: always low.
12	LO+	Leads-off comparator output In DC leads-off detection mode: high when +IN electrode is disconnected. Low when connected. In AC leads-off detection mode: high when either –IN or +IN electrode is disconnected. Low when both electrodes are connected.
13	$\overline{\text{SDN}}$	Shutdown control pin. Drive this pin low to enter the low-power shut down mode.
14	AC/$\overline{\text{DC}}$	Leads-off mode control pin. Drive this pin low for DC leads off mode. Drive this pin high for AC leads off mode.
15	FR	Fast recovery control pin. Drive this pin high enable fast recovery mode. Otherwise, drive it low.
16	GND	Ground
17	$+V_S$	Supply voltage
18	REF IN	Input to reference buffer.
19	IA OUT	Instrumentation amplifier output terminal.
20	HP SENSE	High pass sense terminal for instrumentation amplifier. Connect to junction of R and C that set AD8232's first high pass filter.
Exposed Pad		Connect to GND or leave unconnected

THEORY OF OPERATION

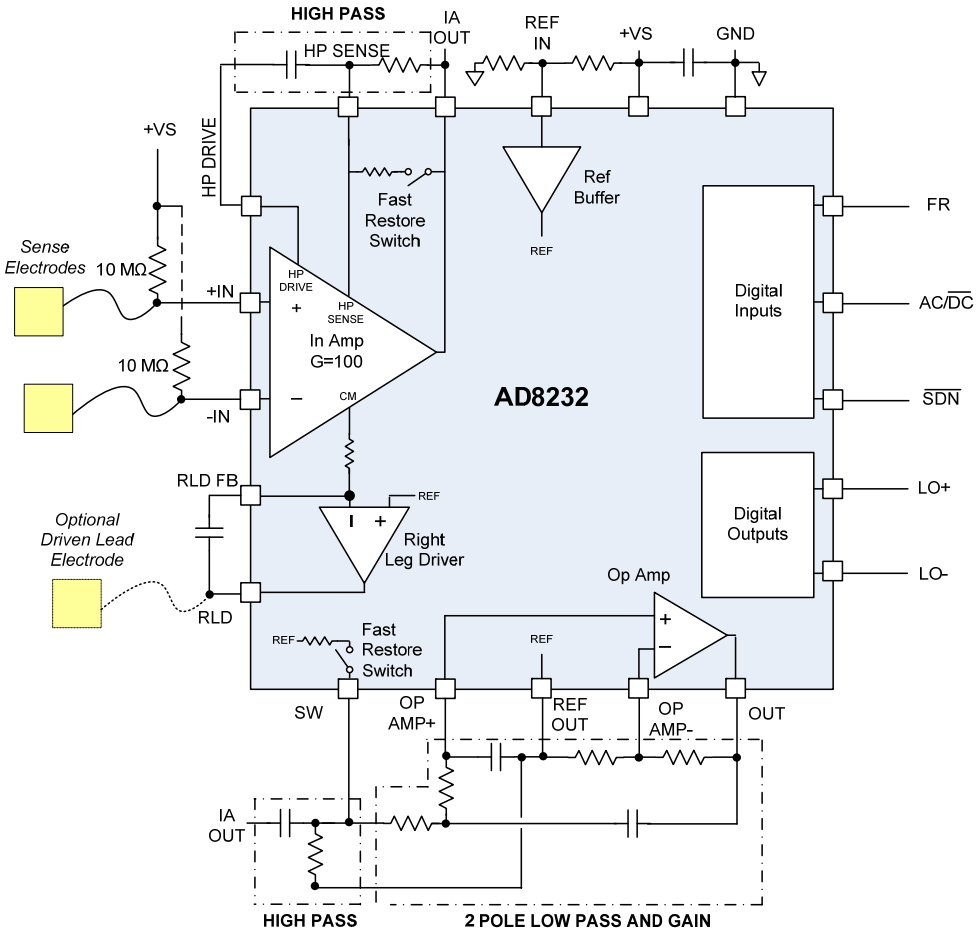


Figure 3. AD8232 Typical Application Schematic

ARCHITECTURE OVERVIEW

The AD8232 consists of four amplifiers:

- A custom instrumentation amplifier specifically designed to amplify ECG signals. Unlike traditional in amps, high pass filtering is built into the in amp's architecture, allowing it to apply a gain of 100 to the ECG signal, while rejecting DC offsets from the electrodes.
- A general-purpose op-amp. This is typically used for low pass filtering and additional gain
- A right-leg drive amplifier. This amplifier injects a small current into the patient to counteract common mode voltage variations between the AD8232 and the patient – improving common mode rejection.
- Reference buffer. This buffer generates a virtual ground at mid-supply, typically required by ac-coupled, single-supply applications.

The following sections describe in more detail the features of the AD8232.

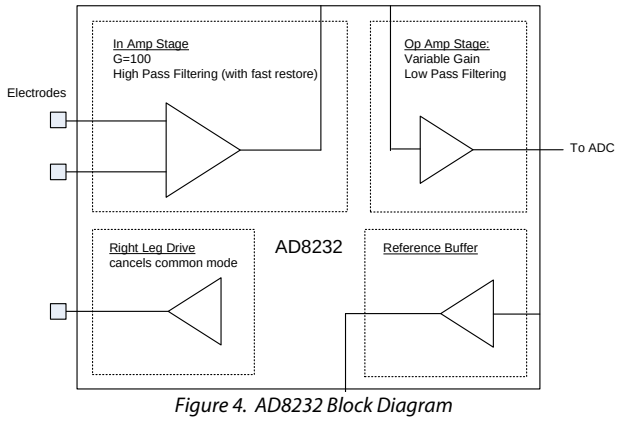


Figure 4. AD8232 Block Diagram

HIGH PASS FILTERING

The instrumentation amplifier in the AD8232 is designed to apply gain and high pass filtering simultaneously. This capability allows it to amplify a small ECG signal by 100 while rejecting electrode offsets as large as ±300 mV. The AD8232 can implement a high pass filter with up to two poles. A higher filter order will yield better artifact rejection at the cost of more passive components on the PCB board.

Single-pole high pass filter

For applications where the subject will remain relatively motionless during the ECG measurement, a signal pole filter can be used to minimize component count.

The cutoff frequency of the filter is:

$$f_c = 100/(2 \pi R_1 C_1)$$

Note that the filter cutoff is 100 times higher than would be typically expected from a single pole filter. Because of the feedback architecture of the instrumentation amplifier, the typical filter cutoff equation is modified by the instrumentation amplifier's gain.

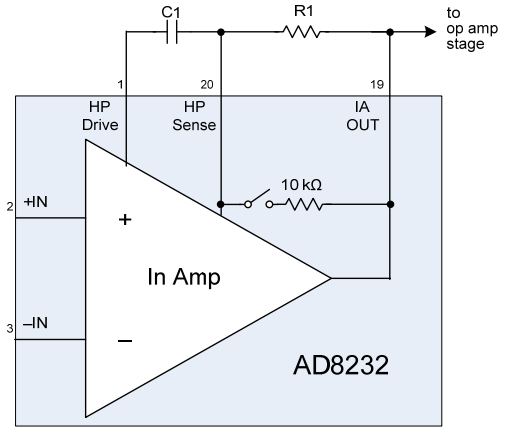


Figure 5. Schematic for one pole high pass filter

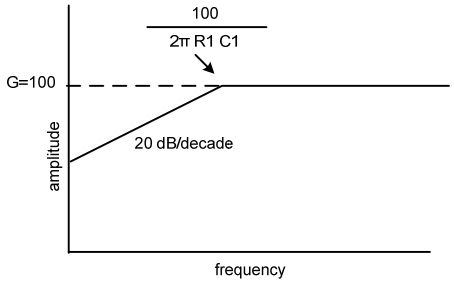


Figure 6. Frequency response of one pole filter

Two-pole high pass filter

A two-pole architecture can be implemented by adding a simple ac coupling RC at the output of the instrumentation amplifier. Keep in mind that if this passive network is not buffered, it will exhibit higher output impedance at the input of a subsequent low pass filter, such as a Sallen Key architecture. Careful component selection can yield good results without a buffer.

Fast Restore

Because of the low cutoff frequency used in low-pass filters in ECG applications, signals may require several seconds to settle. This settling time can result in a frustrating delay for the user after a step response: for example, when the leads are first connected.

The AD8232 includes a "fast restore" functionality to prevent these long delays. When the AD8232 detects a saturation condition at the output of the instrumentation amplifier, it switches in 10 kΩ resistors in parallel with the filter resistors. The lower resistance shifts the pole to a higher frequency, resulting in a quicker settling time. Once the AD8232 senses the instrumentation amplifier output is no longer saturated, it opens the switches and the AD8232 returns to normal operation. To disable this functionality, drive the FR pin low or tie it permanently to GND.

The fast restore settling time depends on how quickly the AD8232's internal 10 k Ω resistors can drain the capacitors in the high pass circuit. Smaller capacitor values will result in a shorter settling time.

The AD8232 contains two switch and resistor pairs for fast restore. One pair is placed between HP SENSE and IA OUT. The second is connected between SW and REF OUT.

LOW PASS FILTERING AND GAIN

The AD8232 includes an uncommitted op amp that can be used for extra gain and filtering. In most of the applications circuits in this datasheet, it is used to build a two-pole low pass filter with gain, using a Sallen-Key configuration.

For a two-pole low-pass filter, use the circuit in Figure 7 and the following design equations:

$f_C = 1/(2\pi\sqrt{(R4\ C4\ R5\ C5)})$

Gain = 1 + R5/R6

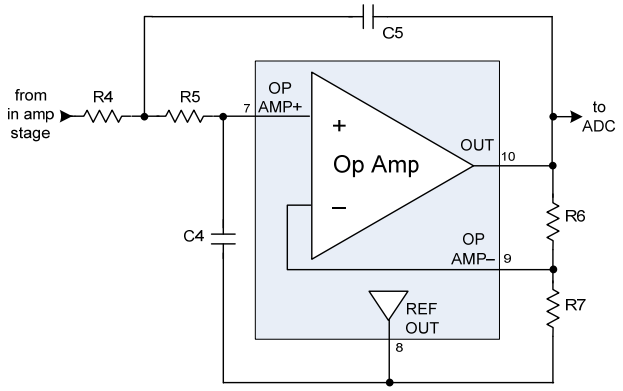


Figure 7. Schematic for a two-pole low-pass filter

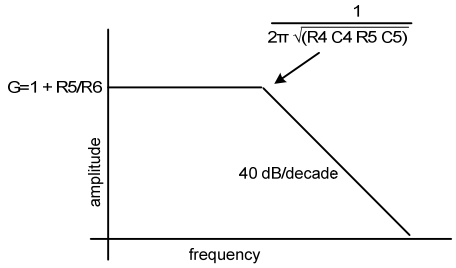


Figure 8. Frequency response for a two-pole low-pass filter

DRIVEN ELECTRODE

The AD8232 includes a right-leg drive (RLD) amplifier. The AD8232 senses the common mode voltage at its inputs and can drive an opposing signal into the patient. This driven electrode functionality maintains the voltage between the patient and the AD8232 constant, greatly improving the common mode rejection ratio.

As a safety measure, place a resistor between the RLD pin and the electrode connected to the subject, to ensure that current flow never exceeds 10μA. Calculate the value of this resistor should be calculated equal to the supply voltage across the AD8232 divided by 10μA.

The AD8232 uses an integrator formed by an internal 150kΩ resistor and an external capacitor to drive the reference electrode. Choice of the integrator capacitor is a tradeoff between line rejection capability and stability. The capacitor should be small to maintain as much loop gain as possible around 50 and 60 Hz, which are typical line frequencies. For stability, the gain of the integrator should be less than unity at the frequency of any other poles in the loop, such as those formed by the patient's capacitance and the safety resistor. The application circuits use a 1nF capacitor, which results in a loop gain of about 20 at line frequencies, with a crossover frequency of about 1 kHz.

In a two-lead configuration, the RLD pin can be used to drive the bias current resistors on the inputs. While not as effective as a true driven electrode, this configuration can provide some common mode rejection improvement if the sense electrode impedance is small and well matched.

LEADS OFF DETECTION

The AD8232 includes leads off detection. It provides modes optimized for either two or three-electrode configurations.

DC Leads-Off Detection

To use this mode, connect the AC/$\overline{\text{DC}}$ pin to ground. This mode works by sensing when either input goes high. This sets two requirements on the circuit configuration:
1) The system must be a three-electrode configuration - RLD output terminal must be connected to a driven electrode.
2) Each input must have a pull-up resistor connected to the supply.

In DC leads-off mode, the AD8232 checks each input individually, and is therefore able to indicate which electrode is disconnected. The AD8232 indicates which electrode is disconnected by setting the corresponding LO- or LO+ pin high.

AC Leads-Off Detection

This mode is useful when using only two electrodes (no separate driven electrode.) The AD8232 detects when an electrode is disconnected by sourcing a small 100 kHz current into the electrodes. As opposed to the DC detection mode, the ADC8232 is only able to determine that an electrode has lost its connection – not which one. During such event, the LO+ pin goes high. In this mode, the LO- pin is not used.

To use this mode, tie the AC/$\overline{\text{DC}}$ pin to the positive supply rail. To maintain the inputs inside the common-mode range of the amplifier, provide a bias return path for each input with a 10MΩ to REF OUT.

REFERENCE BUFFER

The AD8232 has been designed to operate from a single supply. To simplify the design of single-supply applications, the AD8232 includes a reference buffer to create a "virtual ground" in between the two supplies. The AD8232 amplifies the signals around this voltage. If there is zero differential input voltage, the output voltage will be this reference voltage.

The reference voltage level is set at the REF IN pin. It can be set with a voltage divider or by driving the REF IN pin from some other point in the circuit (for example the ADC reference). The voltage is available at the REF OUT pin for the filtering circuits or for an ADC reference.

OUTLINE DIMENSIONS

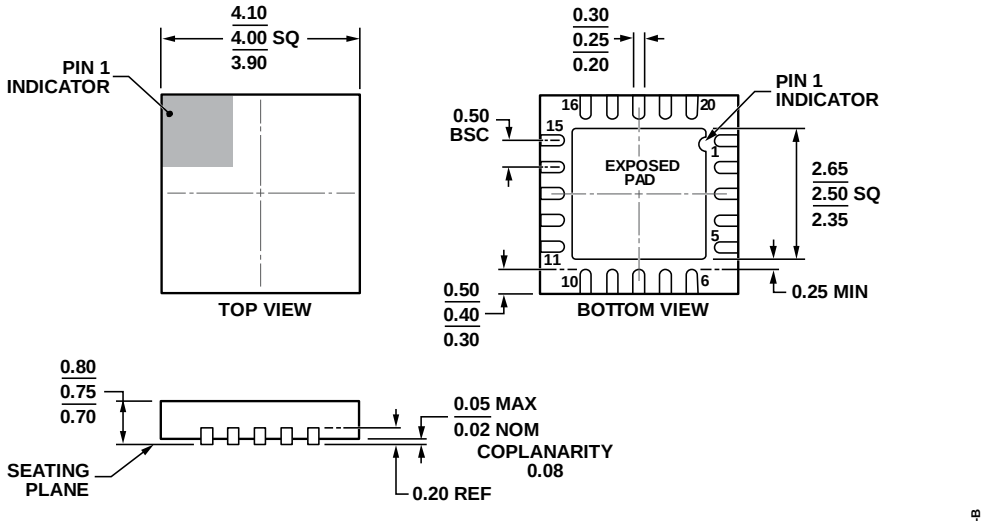


Figure 9. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 x 4 mm Body, Very Very Thin Quad (CP-20-10)
Dimensions shown in millimeters

PR10866-0-7/112(PrD)