

October 1989 Revised October 2000

# 74F164A

# Serial-In, Parallel-Out Shift Register

#### **General Description**

The 74F164A is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock. The 74F164A is a faster version of the 74F164.

#### **Features**

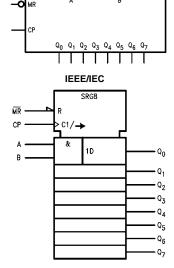
- Typical shift frequency of 90 MHz
- Asynchronous Master Reset
- Gated serial data input
- Fully synchronous data transfers
- 74F164A is a faster version of the 74F164

## **Ordering Code:**

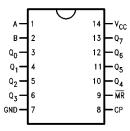
Order Number	Package Number	Package Description
74F164ASC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74F164ASJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F164APC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## **Logic Symbols**



### **Connection Diagram**



# **Unit Loading/Fan Out**

Pin Names	Description	U.L.	Input I <sub>IH</sub> /I <sub>IL</sub>		
Pin Names	Description	HIGH/LOW	Output I <sub>OH</sub> /I <sub>OL</sub>		
A, B	Data Inputs	1.0/1.0	20 μA/–0.6 mA		
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/–0.6 mA		
MR	Master Reset Input (Active LOW)	1.0/1.0	20 μA/–0.6 mA		
Q <sub>0</sub> –Q <sub>7</sub>	Outputs	50/33.3	−1 mA/20 mA		

#### **Functional Description**

The 74F164A is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q<sub>0</sub> the logical AND of the two data inputs (A ullet B) that existed before the rising clock edge. A LOW level on the Master Reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

#### **Mode Select Table**

Operating		nputs	5	Outputs		
Mode	MR	Α	В	$Q_0$	Q <sub>1</sub> –Q <sub>7</sub>	
Reset (Clear)	L	Х	Χ	L	L-L	
	Н	ı	ı	L	q <sub>0</sub> -q <sub>6</sub>	
Shift	Н	- 1	h	L	q <sub>0</sub> -q <sub>6</sub>	
	Н	h	- 1	L	$q_0 - q_6$	
	Н	h	h	Н	q <sub>0</sub> -q <sub>6</sub>	

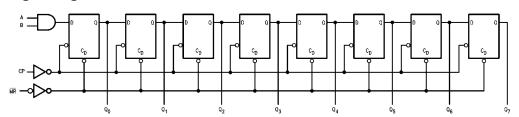
H(h) = HIGH Voltage Levels

L(I) = LOW Voltage Levels

X = Immaterial

 $\mathbf{q}_{\mathrm{n}} = \mathbf{Lower}$  case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

# **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## **Absolute Maximum Ratings**(Note 1)

-65°C to +150°C

 $\begin{array}{ll} \mbox{Ambient Temperature under Bias} & -55\mbox{°C to } +125\mbox{°C} \\ \mbox{Junction Temperature under Bias} & -55\mbox{°C to } +150\mbox{°C} \\ \end{array}$ 

 $\begin{array}{lll} \mbox{V}_{CC} \mbox{ Pin Potential to Ground Pin} & -0.5 \mbox{V to } +7.0 \mbox{V} \\ \mbox{Input Voltage (Note 1)} & -0.5 \mbox{V to } +7.0 \mbox{V} \\ \mbox{Input Current (Note 1)} & -30 \mbox{ mA to } +5.0 \mbox{ mA} \\ \end{array}$ 

Voltage Applied to Output

Storage Temperature

in HIGH State (with  $V_{CC} = 0V$ )

 $\begin{array}{ll} \text{Standard Output} & -0.5 \text{V to V}_{\text{CC}} \\ \text{3-STATE Output} & -0.5 \text{V to +5.5 V} \end{array}$ 

Current Applied to Output

# Recommended Operating Conditions

Free Air Ambient Temperature  $0^{\circ}\text{C to } +70^{\circ}\text{C}$ Supply Voltage +4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

# **DC Electrical Characteristics**

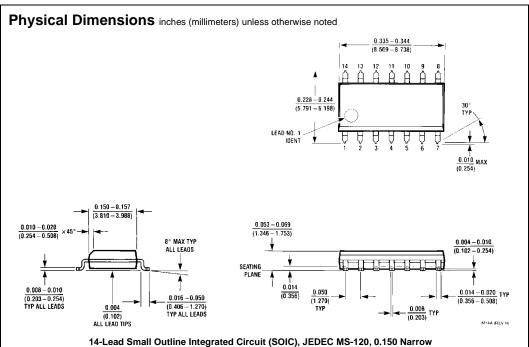
Symbol	Paramete	r	Min	Тур	Max	Units	v <sub>cc</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltag	е			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH	10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = -1 mA
	Voltage	5% V <sub>CC</sub>	2.7			V	IVIIII	$I_{OH} = -1 \text{ mA}$
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH				5.0	μА	Max	V <sub>IN</sub> = 2.7V
	Current				3.0	μΛ	IVIAX	V IN - 2.7 V
I <sub>BVI</sub>	Input HIGH Current				7.0	μА	Max	V <sub>IN</sub> = 7.0V
	Breakdown Test				7.0	μΛ	IVIAX	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH				50	μА	Max	V <sub>OUT</sub> = V <sub>CC</sub>
	Leakage Current				00	μιτ	IVICA	*001 - *CC
V <sub>ID</sub>	Input Leakage		4.75			V	0.0	$I_{ID} = 1.9  \mu A$
	Test		4.73			V	0.0	All other pins grounded
I <sub>OD</sub>	Output Leakage				3.75	μА	0.0	V <sub>IOD</sub> = 150 mV
	Circuit Current				3.73	μΛ	0.0	All other pins grounded
I <sub>IL</sub>	Input LOW Current				-0.6	mA	Max	V <sub>IN</sub> = 0.5V
los	Output Short-Circuit Curre	ent	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current			35	55	mA	Max	CP = HIGH
								$\overline{MR} = GND, A, B = GND$

# **AC Electrical Characteristics**

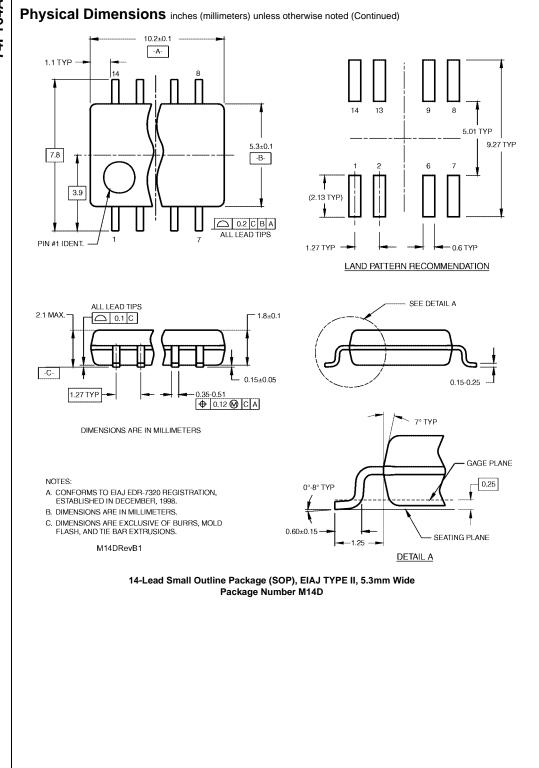
Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			$T_{A} = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V$ $C_{L} = 50 \text{ pF}$		$T_A = 0$ °C to +70°C $V_{CC} = 5.0$ V $C_L = 50$ pF		Units
		Min	Тур	Max	Min	Max	Min	Max	1
f <sub>MAX</sub>	Maximum Clock Frequency	80	120		60		80		MHz
t <sub>PLH</sub>	Propagation Delay	3.0	4.8	7.5	2.5	9.0	3.0	7.5	no
$t_{PHL}$	CP to Q <sub>n</sub>	3.5	5.0	8.0	3.0	8.5	3.5	8.0	ns
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>n</sub>	5.0	7.0	10.0	4.0	12.5	5.0	10.5	ns

# **AC Operating Requirements**

		$T_A = +25$ °C $V_{CC} = +5.0V$		$T_A = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V$		$T_A = 0$ °C to +70°C $V_{CC} = 5.0V$		Units
Symbol	Parameter							
		Min	Max	Min	Max	Min	Max	
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	4.5		5.5		4.5		
t <sub>S</sub> (L)	A or B to CP	4.0		4.0		4.0		no
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	1.0		1.0		1.0		ns
t <sub>H</sub> (L)	A or B to CP	1.0		1.0		1.0		
t <sub>W</sub> (H)	CP Pulse Width	4.0		4.0		4.0		20
$t_W(L)$	HIGH or LOW	7.0		7.0		7.0		ns
t <sub>W</sub> (L)	MR Pulse Width, LOW	4.0		5.0		4.0		ns
t <sub>REC</sub>	Recovery Time MR to CP	5.0		6.5		5.0		ns



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A



#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770(18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 0.250 ± 0.010 PIN NO. 1 IDENT PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\overline{(7.620 - 8.128)}$ 0.065 $\frac{0.145 - 0.200}{(3.683 - 5.080)}$ 0.060 4° TYP Optional (1.524) (1.651) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 $0.075 \pm 0.015$ $\overline{(3.175 - 3.810)}$ 0.280 (1.905 ± 0.381) (7.112) MIN 0.014 - 0.0230.100 ± 0.010 (2.540 ± 0.254) TYP (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)}$ TYP

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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 $0.325 + 0.040 \\ -0.015 \\ \hline (8.255 + 1.016) \\ -0.381)$ 

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N14A (REV F)