RF7411

3V WCDMA BAND 1 LINEAR PA MODULE

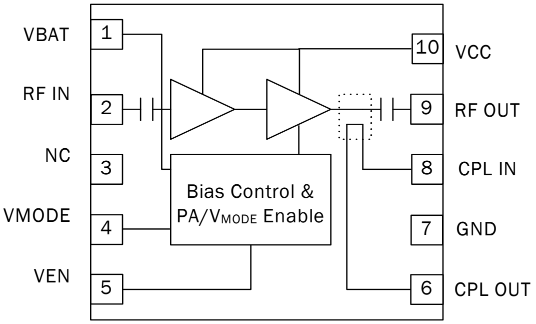
Package Style: Module, 10-Pin, 3mm x 3mm x 1.0mm

Features

- HSDPA/HSUPA/HSPA+/ LTE
- High Efficiency WCDMA Operation : 42.5% at P_{OUT} = +28dBm
- Low Voltage Positive Bias Supply (3.0V to 4.2V)
- Internal Voltage Regulator - No External (V_{REF}) Required
- Two Mode Power/Gain Stages with Digital Control Interface
- Integrated Power Coupler
- Integrated Blocking and Decoupling Capacitors

Applications

- WCDMA/HSPA+/LTE Wireless Data Cards
- WCDMA/HSPA+/LTE Handsets



Functional Block Diagram

Product Description

The RF7411 is a high-power, high-efficiency, linear power amplifier designed for use as the final RF amplifier in 3V, 50Ω WCDMA mobile cellular equipment and spread-spectrum systems. This PA is developed for UMTS Band 1 which operates in the 1920MHz to 1980MHz frequency band. The RF7411 has a digital control pin which enables a low power mode to reduce amplifier gain at lower power levels. The part also has an integrated directional coupler which eliminates the need for an external discrete coupler at the output. The RF7411 (Band 1) meets the spectral linearity requirements of High Speed Downlink Packet Access (HSDPA), High Speed Uplink Packet Access (HSUPA), and Long Term Evolution (LTE) data transmission. The RF7411 is assembled in a 10-pin, 3mm x 3mm module.

Ordering Information

RF7411	3V WCDMA Band 1 Linear PA Module
RF7411PCBA-410	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☐ GaAs HBT
☐ GaAs MESFET
☑ InGaP HBT
☐ SiGe BiCMOS
☐ Si BiCMOS
☐ SiGe HBT
☐ GaAs pHEMT
☐ Si CMOS
☐ Si BJT
☐ GaN HEMT
☐ BiFET HBT
☐ LDMOS

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage in Standby Mode	6.0	V
Supply Voltage in Idle Mode	6.0	V
Supply Voltage in Operating Mode, 50Ω Load	6.0	V
Supply Voltage, V_{BAT}	6.0	V
Control Voltage, V^{MODE}	3.7	V
Control Voltage, V_{EN}	3.7	V
RF - Input Power	+10	dBm
RF - Output Power	+30	dBm
Operating Ambient Temperature	-30 to +110	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Recommended Operating Conditions					
Operating Frequency Range	1920		1980	MHz	
V_{BAT}	+3.0	+3.2	+4.2	V	
V_{CC}	+3.0[1]	+3.2	+4.2	V	
V_{CC} (used with DC-DC)	0.5		+4.2	V	PA used with DC-DC converter to reduce current drain at back-off and lower output powers
V_{EN}	0		0.5	V	PA disabled.
	1.35	1.80	3.10	V	PA enabled.
V_{MODE}	0		0.5	V	Logic “low”.
	1.35	1.80	3.10	V	Logic “high”.
P_{OUT}					
Maximum Linear Output (HPM)	28.0[1,2]			dBm	High Power Mode (HPM)
Maximum Linear Output (LPM)	16[1,2]			dBm	Low Power Mode (LPM)
Ambient Temperature	-20	+25	+85	°C	

Notes:

[1] For operation at V_{CC} = +3.0V, derate P_{OUT} by 0.5dB.

[2] P_{OUT} is specified for 3GPP (Voice) modulation. For HSDPA and HSPA+ operation, derate P_{OUT} by 2dB:
HSDPA Configuration: βc=12, βd=15, βhs=24
HSPA+ Configuration: 3GPP Rel7 Subtest 1

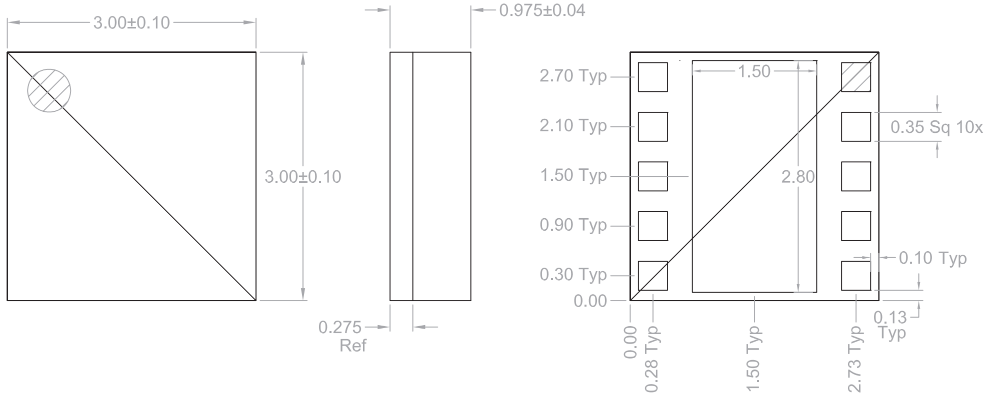
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Electrical Specifications					T = +25°C, $V_{CC} = V_{BAT} = +3.2V$, $V_{EN} = +1.8V$, 50Ω system, WCDMA Rel 99 Modulation unless otherwise specified.
Gain		28		dB	HPM, $P_{OUT} = 28.0dBm$
		15.5		dB	LPM, $P_{OUT} \leq 16.0dBm$
ACLR - 5MHz Offset		-40	-36	dBc	HPM, $P_{OUT} = 28.0dBm$
		-44	-38	dBc	LPM, $P_{OUT} = 16.0dBm$
ACLR - 10MHz Offset		-52	-48	dBc	HPM, $P_{OUT} = 28.0dBm$
		-60	-48	dBc	LPM, $P_{OUT} = 16.0dBm$
PAE	39	42.5		%	HPM, $P_{OUT} = 28.0dBm$
		10		%	LPM, $P_{OUT} = 16.0dBm$
Current Drain		435		mA	HPM, $P_{OUT} = 28.0dBm$
		116		mA	LPM, $P_{OUT} = 16.0dBm$
Quiescent Current		50		mA	HPM, DC only
Enable Current		0.03		mA	Source or sink current. $V_{EN} = 1.8V$.
Mode Current (I_{MODE})		0.01		mA	Source or sink current. $V_{MODE} = 1.8V$.
Leakage Current		2.1	10.0	µA	DC only. $V_{CC} = V_{BAT} = 4.2V$, $V_{EN} = V_{MODE} = 0.5V$.
Noise Power in Receive Band		-137		dBm/Hz	All power modes, measured at duplex offset frequency (F_{TX} + 190MHz). Rx: 2110MHz to 2170MHz, $P_{OUT} \leq 28.0dBm$
Input Impedance		1.8:1		VSWR	No ext. matching, $P_{OUT} \leq 28dBm$, all modes.
Harmonic, 2FO		-20	-7	dBm	$P_{OUT} \leq 28.0dBm$, all power modes.
Harmonic, 3FO		-23	-14	dBm	$P_{OUT} \leq 28.0dBm$, all power modes.
Spurious Output Level			-60	dBc	All spurious, $P_{OUT} \leq 28dBm$, all conditions, load VSWR ≤ 6:1, all phase angles.
Insertion Phase Shift	-30	9.8	+30	°	Phase shift at 16dBm when switching from HPM to LPM.
DC Enable Time			10	µS	DC only. Time from V_{EN} = high to stable idle current (90% of steady state value).
RF Rise/Fall Time			6	µS	$P_{OUT} \leq 28.0dBm$, all modes. 90% of target, DC settled prior to RF.
Ruggedness			10:1	VSWR	HPM, $P_{OUT} = 28.0dBm$, all phases.
Coupling Factor		-20		dB	$P_{OUT} \leq 28.0dBm$, all modes.
Daisy Chain Insertion Loss		0.25		dB	CPL_IN to CPL_OUT port, $V_{EN} = 0.5V$
Coupling Directivity		20		dB	

Pin	Function	Description
1	VBAT	Supply voltage for bias circuitry.
2	RF IN	RF input internally matched to 50Ω and DC blocked. The RF input matching circuit has a shunt inductor to ground which would short any DC voltage placed on this pin.
3	NC	No connection.
4	VMODE	Digital control input for power mode selection (see Operating Modes truth table).
5	VEN	Digital control input for PA enable and disable (see Operating Modes truth table).
6	CPL_OUT	Coupler output.
7	GND	This pin must be grounded.
8	CPL_IN	Coupler input used for cascading couplers in series. Terminate this pin with a 50Ω resistor if not connected to another coupler.
9	RF OUT	RF output internally matched to 50Ω and DC blocked.
10	VCC	Supply voltage for the first and second stage amplifiers, which can be connected to battery supply or output of DC-DC converter.
Pkg Base	GND	Ground connection. The package backside should be soldered to a topside ground pad connecting to the PCB ground plane with multiple ground vias. The pad should have a low thermal resistance and low electrical impedance to the ground plane.

Operating Mode Truth Table

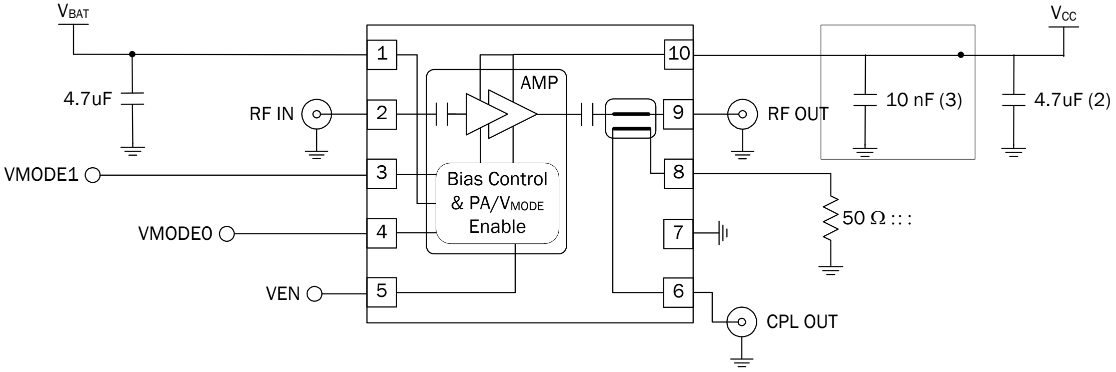
V_{EN}	V_{MODE}	V_{BAT}	V_{CC}	Conditions/Comments
Low	Low	3.0V to 4.2V	3.0V to 4.2V	Power down mode
Low	X	3.0V to 4.2V	3.0V to 4.2V	Standby Mode
High	Low	3.0V to 4.2V	3.0V to 4.2V	High power mode
High	High	3.0V to 4.2V	3.0V to 4.2V	Low power mode

Package Drawing



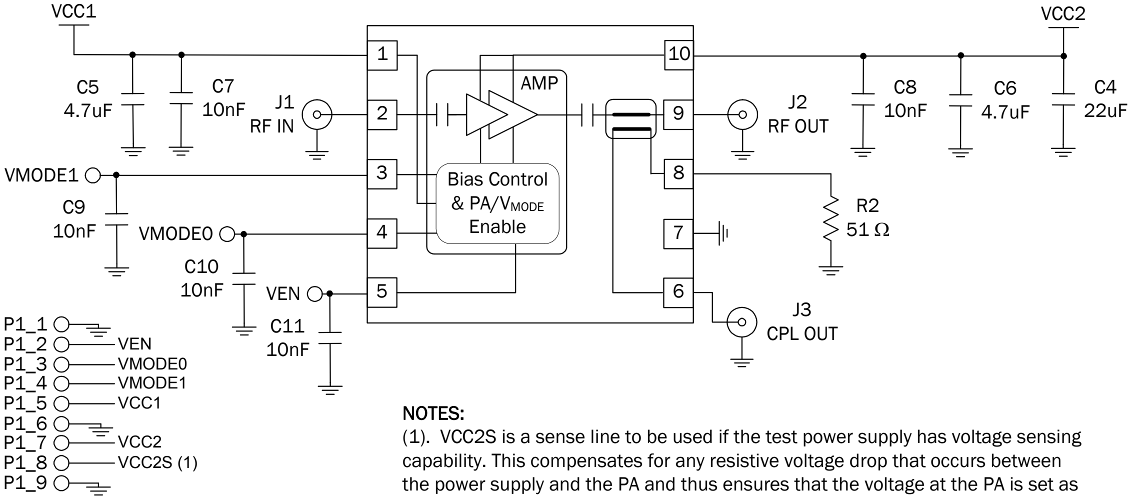
Notes:
1. Shaded area represents Pin 1 location
2. Defining I/O Pad Center:
   To define center of the I/O pad oepning, draw a right triangle
   in one corner of the I/O pad
   Then take the center of the hypotenuse to determine center
   of I/O pad

Application Schematic



NOTES:
(1). The 50 Ω resistor should be removed if pin 8 is connected to another coupler for daisy chaining multiple couplers.
(2). This capacitance value can be reduced for multi-PA with DC to DC converter applications where a total maximum capacitive load is required to be met. Keeping at least a 1uF capacitor close to the PA Vcc pin is recommended.
(3). A capacitor of at least 10 nF should be placed closed to the PA VCC pin (pin10) for optimum decoupling.

Evaluation Board Schematic



NOTES:
(1). VCC2S is a sense line to be used if the test power supply has voltage sensing capability. This compensates for any resistive voltage drop that occurs between the power supply and the PA and thus ensures that the voltage at the PA is set as expected.

PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land Pattern

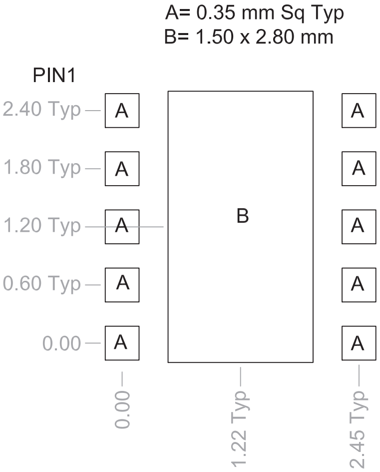


Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

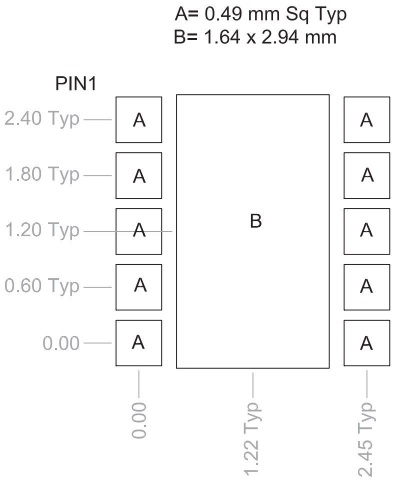


Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.