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RF3928

280W GaN WIDEBAND PULSED POWER AMPLIFIER

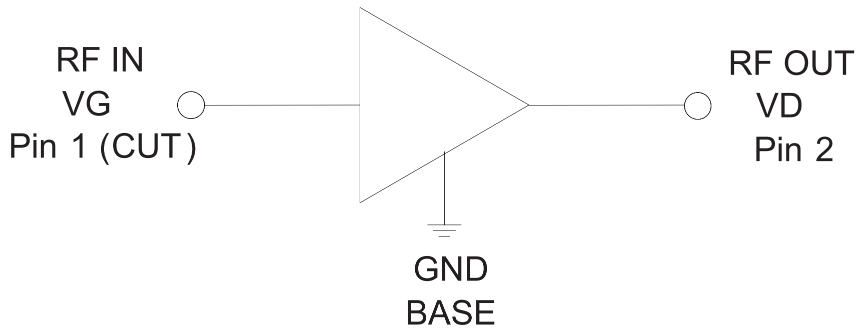
Package: Hermetic 2-Pin, Flanged Ceramic

Features

- Wideband Operation 2.8GHz to 3.4GHz
- Advanced GaN HEMT Technology
- Advanced Heat-Sink Technology
- Supports Multiple Pulse Conditions
  - 10% to 20% Duty Cycle
  - 100µs to 500µs Pulse Width
- Integrated Matching Components for High Terminal Impedances
- 50V Operation Typical Performance
  - Pulsed Output Power 280W
  - Small Signal Gain 12dB
  - Drain Efficiency 52%
  - -40°C to 85°C Operating Temperature

Applications

- Radar
- Air Traffic Control and Surveillance
- General Purpose Broadband Amplifiers



Functional Block Diagram

Product Description

The RF3928 is a 50V 280W high power discrete amplifier designed for S-Band pulsed radar, Air Traffic Control and Surveillance and general purpose broadband amplifier applications. Using an advanced high power density Gallium Nitride (GaN) semiconductor process, these high-performance amplifiers achieve high output power, high efficiency and flat gain over a broad frequency range in a single package. The RF3928 is a matched GaN transistor packaged in a hermetic, flanged ceramic package. This package provides excellent thermal stability through the use of advanced heat sink and power dissipation technologies. Ease of integration is accomplished through the incorporation of simple, optimized matching networks external to the package that provide wide band gain and power performance in a single amplifier.

Ordering Information

RF3928S2	2-Piece sample bag
RF3928SB	5-Piece bag
RF3928SQ	25-Piece bag
RF3928SR	50 Pieces on 7” short reel
RF3928TR13	250 Pieces on 13” reel
RF3928PCBA-410	Fully assembled evaluation board 2.8GHz to 3.4GHz; 50V operation

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☑ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ BiFET HBT
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Source Voltage	150	V
Gate Source Voltage	-8 to +2	V
Gate Current (I_G)	155	mA
Operational Voltage	50	V
Ruggedness (VSWR)	3:1	
Storage Temperature Range	-55 to +125	°C
Operating Temperature Range (T_L)	-40 to +85	°C
Operating Junction Temperature (T_J)	250	°C
Human Body Model	Class 1A	
MTTF (T_J < 200°C) MTTF (T_J < 250°C)	3.0E + 06 1.4E + 05	Hours
Thermal Resistance, Rth (junction to case) T_C = 85°C, DC bias only T_C = 85°C, 100µs pulse, 10% duty cycle T_C = 85°C, 500µs pulse, 10% duty cycle	 0.90 0.18 0.25	°C/W

Caution! ESD sensitive device.

* MTTF – median time to failure for wear-out failure mode (30% Idss degradation) which is determined by the technology process reliability. Refer to product qualification report for FIT (random) failure rate.
Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page two.
Bias Conditions should also satisfy the following expression: $P_{DISS} < (T_J - T_C)/R_{TH}$ J - C and $T_C = T_{CASE}$

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Recommended Operating Condition					
Drain Voltage (V_{DSQ})			50	V	
Gate Voltage (V_{GSQ})	-8	-3	-2	V	
Drain Bias Current		440		mA	
Frequency of Operation	2800		3400	MHz	
DC Functional Test					
$I_{G (OFF)}$ – Gate Leakage			2	mA	V_G = -8V, V_D = 0V
$I_{D (OFF)}$ – Drain Leakage			2	mA	V_G = -8V, V_D = 50V
$V_{GS (TH)}$ (th) – Threshold Voltage		-3.4		V	V_D = 50V, I_D = 20mA
V_{DS} – Drain Voltage at high current		0.22		V	V_G = 0V, I_D = 1.5A
RF Functional Test					[1,2]
Small Signal Gain		13.6		dB	F = 2800MHz, Pin =30dBm
Power Gain	10	10.5		dB	F = 2800MHz, Pin = 44dBm
Input Return Loss			-5.5	dB	F = 2800MHz, Pin = 30dBm

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Output Power	54	54.6		dBm	F = 2800MHz, Pin = 44dBm
Drain Efficiency	45	50		%	
Small Signal Gain		14.2		dB	F = 3100MHz, Pin = 30dBm
Power Gain	10	10.5		dB	F = 3100MHz, Pin = 44dBm
Input Return Loss			-5.5	dB	F = 3100MHz, Pin = 30dBm
Output Power	54	54.5		dBm	F = 3100MHz, Pin = 44dBm
Drain Efficiency	45	52		%	
Small Signal Gain		12.7		dB	F = 3400MHz, Pin = 30dBm
Power Gain	10	10.5		dB	F = 3400MHz, Pin = 44dBm
Input Return Loss			-5.5	dB	F = 3400MHz, Pin = 30dBm
Output Power	54	54.3		dBm	F = 3400MHz, Pin = 44dBm
Drain Efficiency	45	56		%	
RF Typical Performance					[1,2]
Frequency Range	2800		3400	MHz	
Small Signal Gain		12		dB	F = 3100MHz, Pin = 30dBm
Power Gain		10		dB	P_{OUT} = 54dBm
Gain Variation with Temperature			-0.015	dB/°C	At peak output power
Output Power (P_{SAT})		54.5		dBm	Peak output power
		280		W	Peak output power
Drain Efficiency		52		%	At peak output power

[1] Test Conditions: Pulsed Operation, PW = 100μs, DC = 10%, V_{DS} = 50V, I_{DQ} = 440mA, T = 25ºC
[2] Performance in a standard tuned test fixture

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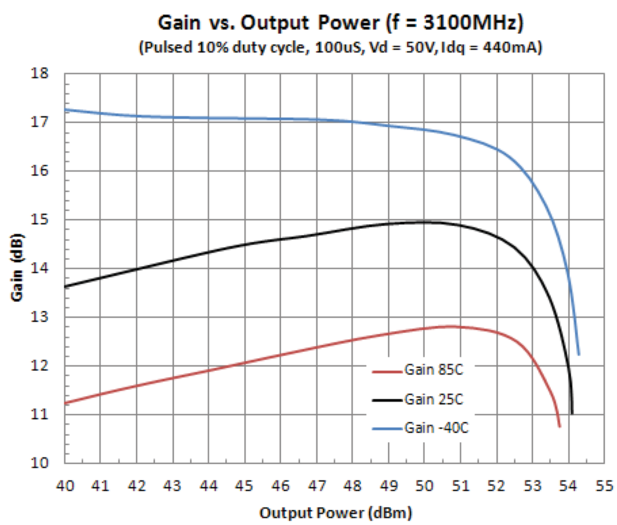
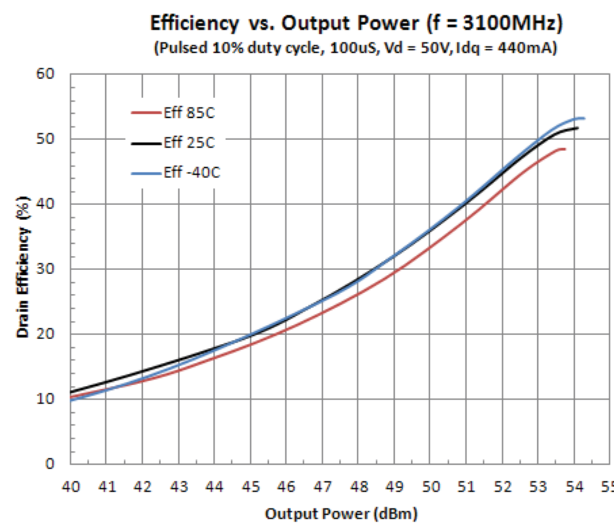
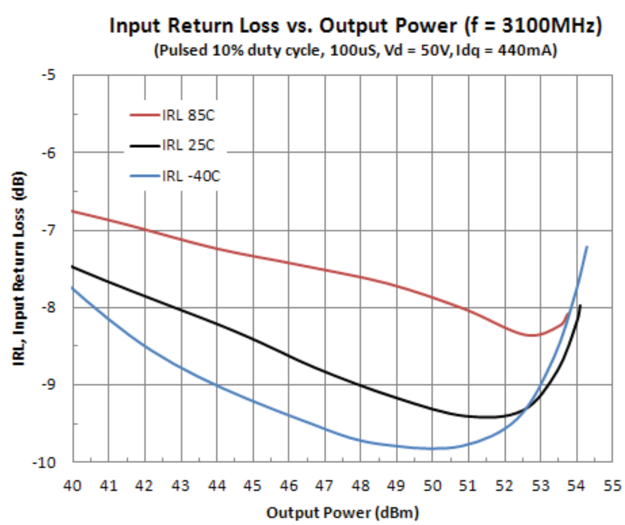
Typical Performance in Standard Fixed Tuned Test Fixture over Temperature (Pulsed at Center Band Frequency)







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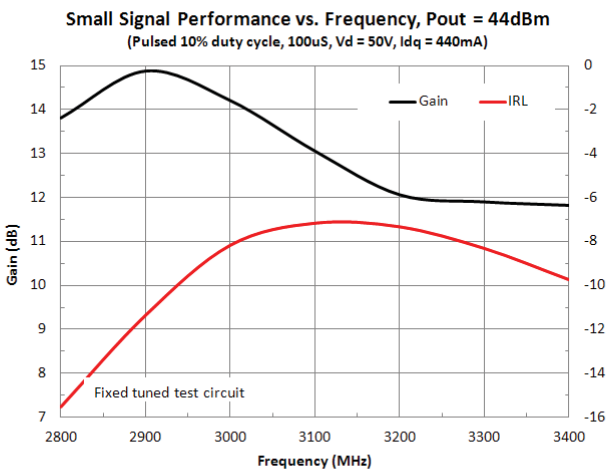
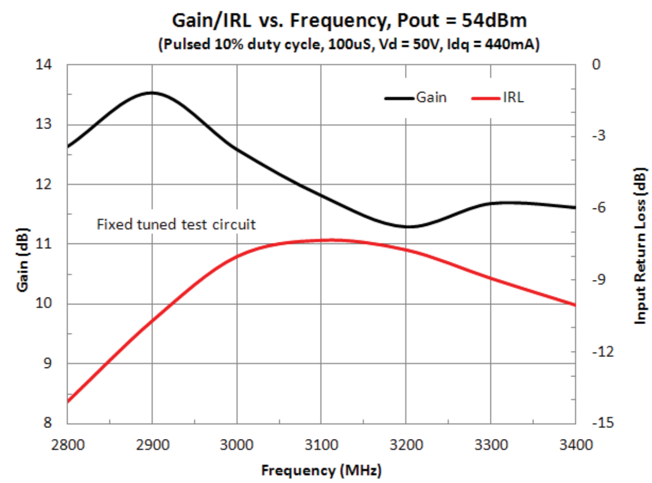
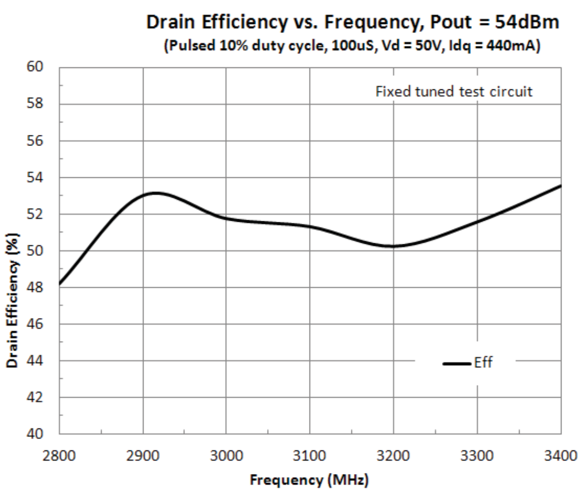
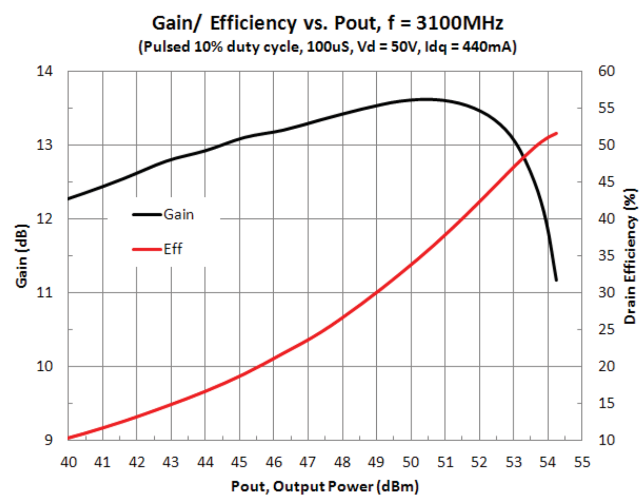
Typical Performance in Standard Fixed-tuned Test Fixture (T = 25°C, Unless Noted)









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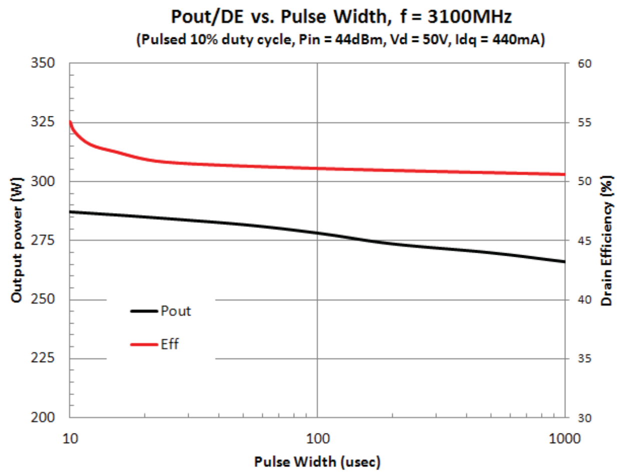
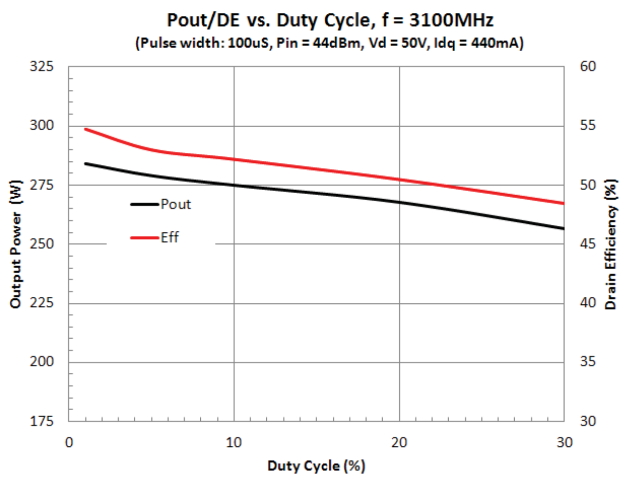
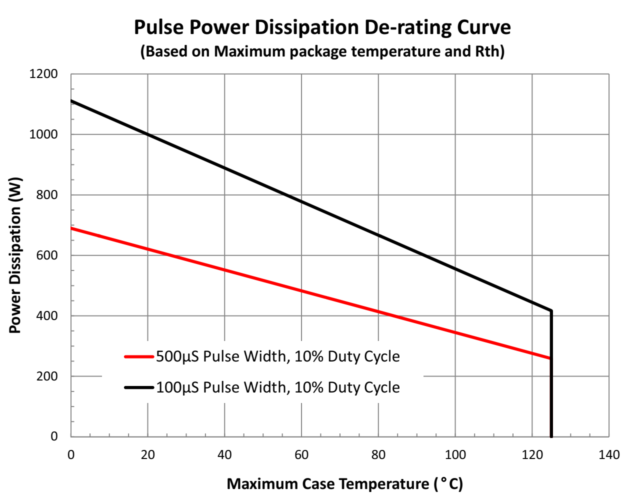
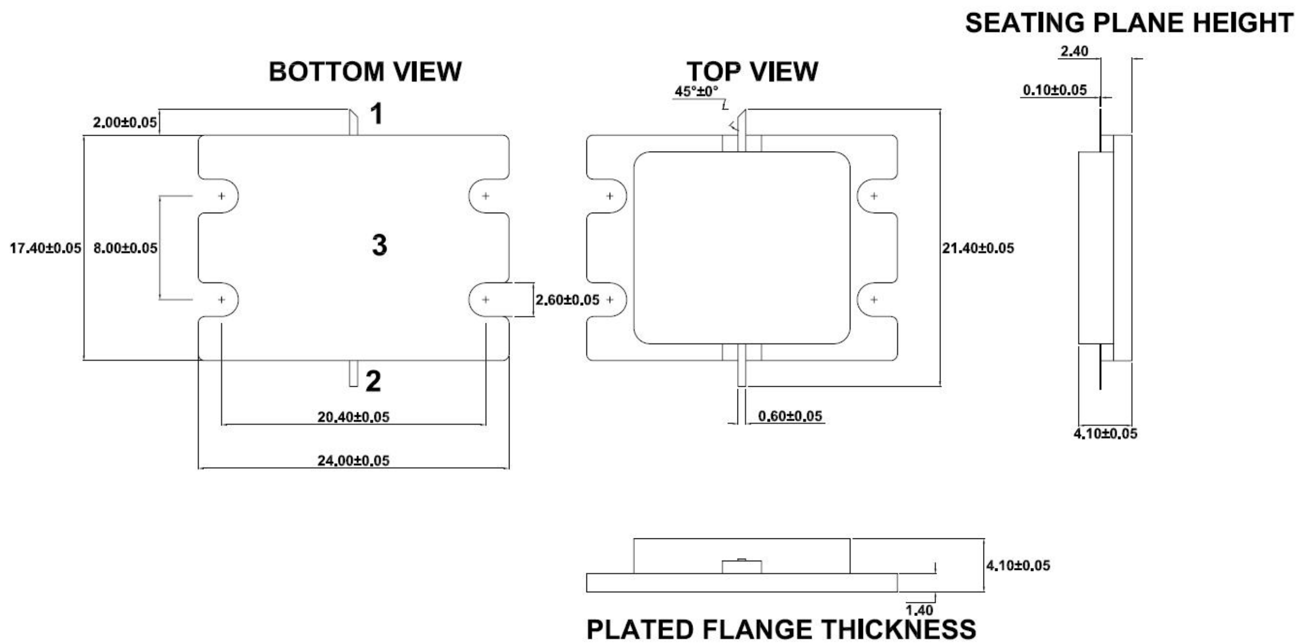

Pout/DE vs. Pulse Width, f = 3100MHz
(Pulsed 10% duty cycle, Pin = 44dBm, Vd = 50V, Idq = 440mA)
Output power (W)
Drain Efficiency (%)
Pulse Width (usec)
Pout
Eff
350
325
300
275
250
225
200
60
55
50
45
40
35
30
10
100
1000


Pout/DE vs. Duty Cycle, f = 3100MHz
(Pulse width: 100uS, Pin = 44dBm, Vd = 50V, Idq = 440mA)
Output Power (W)
Drain Efficiency (%)
Duty Cycle (%)
Pout
Eff
325
300
275
250
225
200
175
60
55
50
45
40
35
30
0
10
20
30


Pulse Power Dissipation De-rating Curve
(Based on Maximum package temperature and Rth)
Power Dissipation (W)
Maximum Case Temperature (°C)
500µS Pulse Width, 10% Duty Cycle
100µS Pulse Width, 10% Duty Cycle
1200
1000
800
600
400
200
0
0
20
40
60
80
100
120
140

Package Drawing

(All Dimensions in mm)



Pin Names and Descriptions

Pin	Name	Description
1	VG	Gate – VG RF Input
2	VD	Drain – VD RF Output
3	GND	Source – Ground Base

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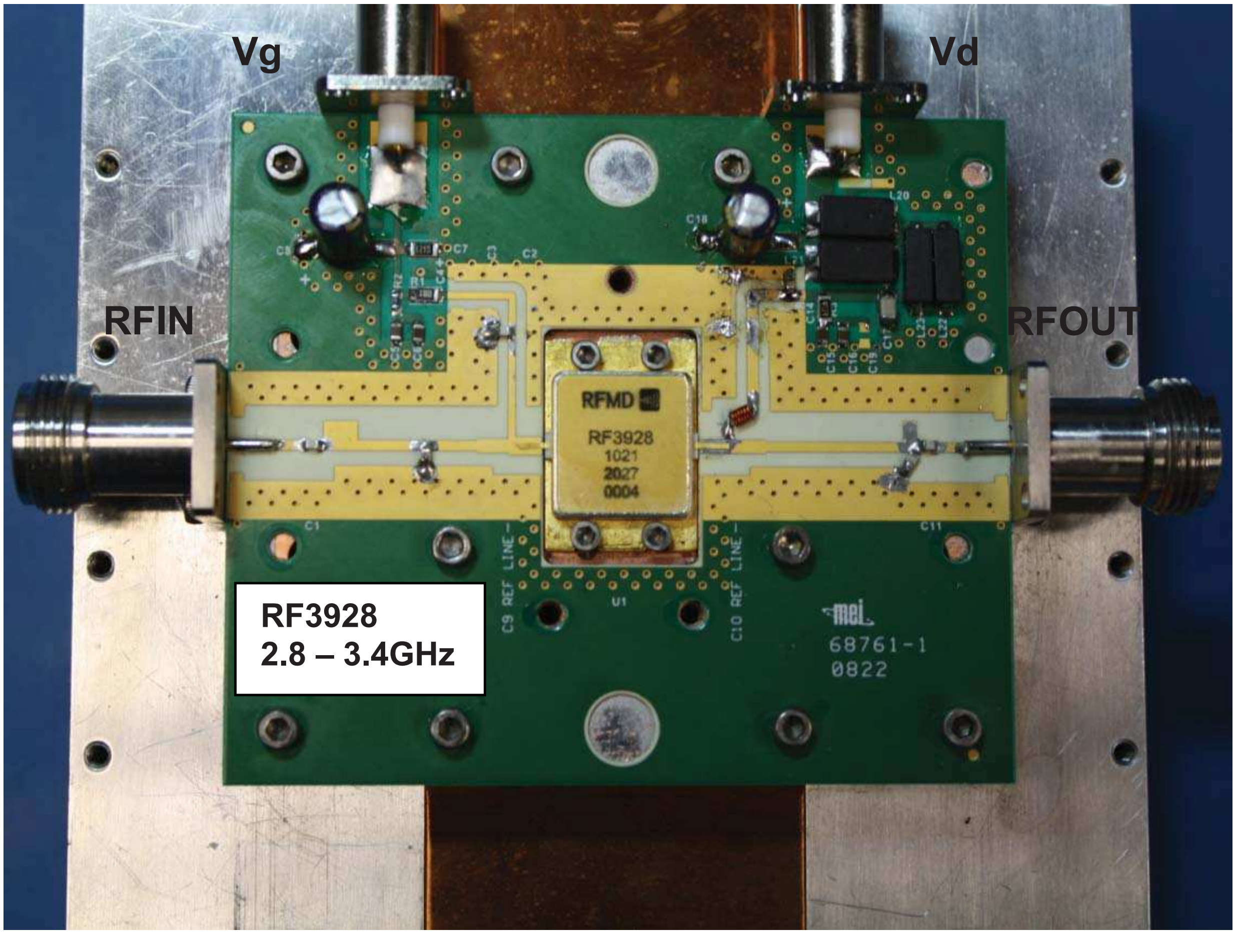
Bias Instruction for RF3928 Evaluation Board

ESD Sensitive Material. Please use proper ESD precautions when handling devices of evaluation board. Evaluation board requires additional external fan cooling. Connect all supplies before powering evaluation board.

1. Connect RF cables at RFIN and RFOUT.
2. Connect ground to the ground supply terminal, and ensure that both the VG and VD grounds are also connected to this ground terminal.
3. Apply -6V to VG.
4. Apply 50V to VD.
5. Increase V_G until drain current reaches 440mA or desired bias point.
6. Turn on the RF input.

IMPORTANT NOTE: Depletion mode device, when biasing the device V_G must be applied BEFORE V_D. When removing bias V_D must be removed BEFORE V_G is removed. Failure to follow sequencing will cause the device to fail.

NOTE: For optimal RF performance, consistent and optimal heat removal from the base of the package is required. A thin layer of thermal grease should be applied to the interface between the base of the package and the equipment chassis. It is recommended a small amount of thermal grease is applied to the underside of the device package. Even application and removal of excess thermal grease can be achieved by spreading the thermal grease using a razor blade. The package should then be bolted to the chassis and input and output leads soldered to the circuit board.



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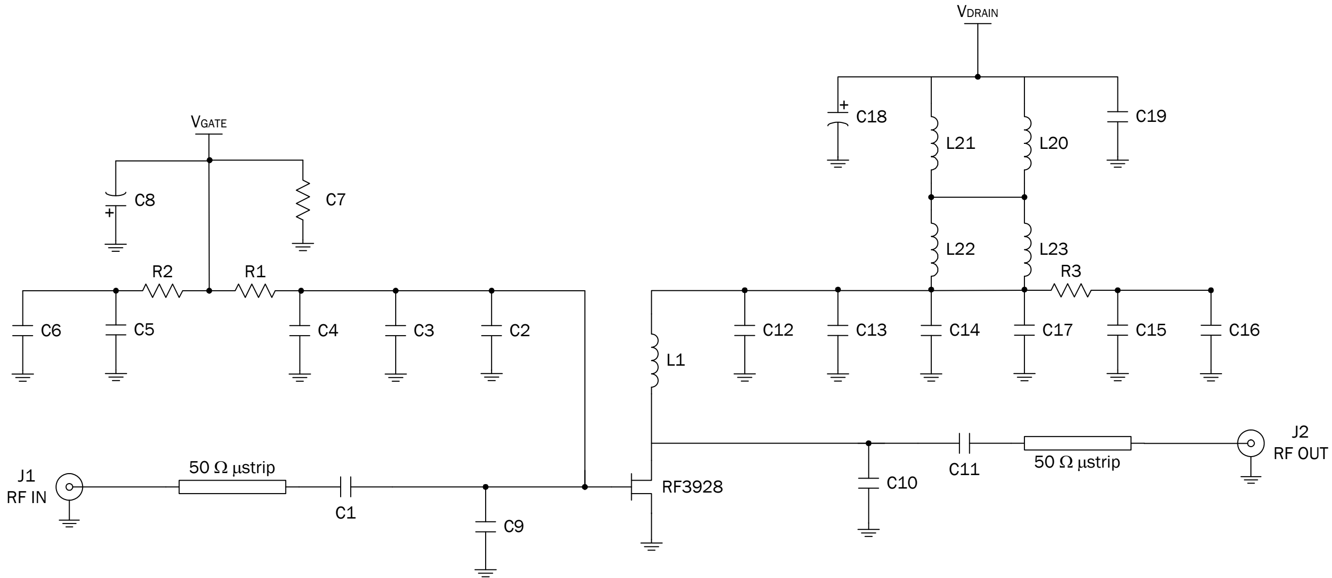
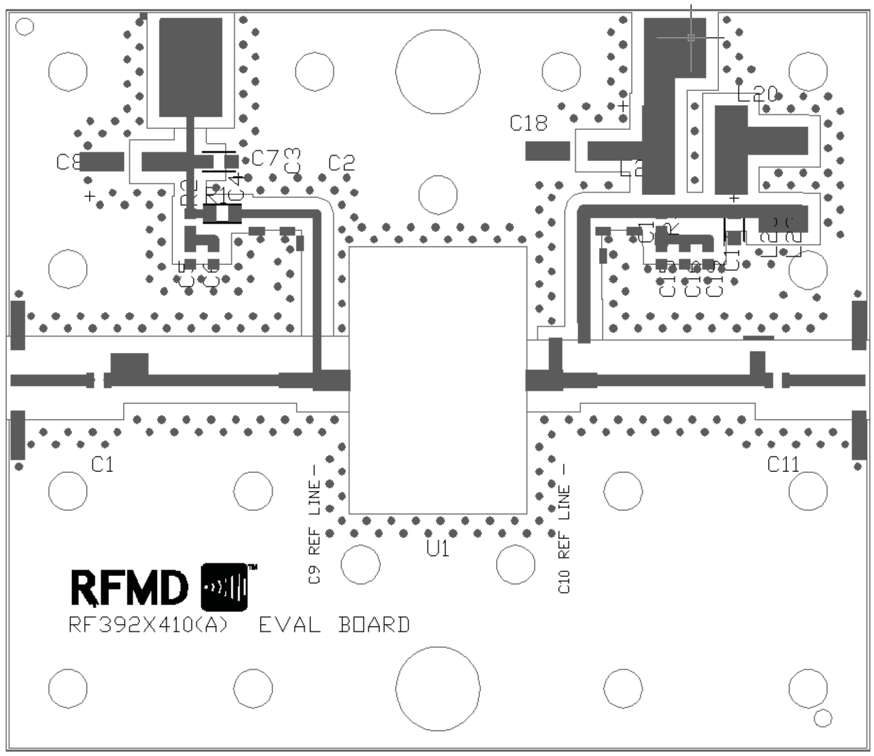
Evaluation Board Schematic



Evaluation Board Bill of Materials

Component	Value	Manufacturer	Part Number
R1	10Ω	Panasonic	ERJ-8GEYJ100V
R2	0Ω	Panasonic	ERJ-3GEY0R00
R3	51Ω	Panasonic	ERJ-8GEYJ510
C1,C11	22pF	ATC	ATC100A220JT
C2, C14	12pF	ATC	ATC100A120JT
C5, C16	1000pF	Novacap	0805G102M101NT
C6, C15	10000pF	TDK	C2012X7R2A103M
C7	120Ω	Panasonic	ERJ-6GEYJ120V
C8, C18	10µF	Panasonic	EEA-FC1E100
C9	0.7pF	ATC	ATC100A0R7BT
C10	0.2pF	ATC	ATC100A0R2BT
C17	62pF	ATC	ATC100B620JT
L1	22nH	Coilcraft	0807SQ-22N_LC
L20, L21	115Ω, 10A	Steward	28F0181-1SR-10
L22, L23	75Ω, 10A	Steward	35F0121-1SR-10
C19	330µF	Illinois Capacitor	9337CKE100M
C3, C4, C7, C12, C13	NOT POPULATED		

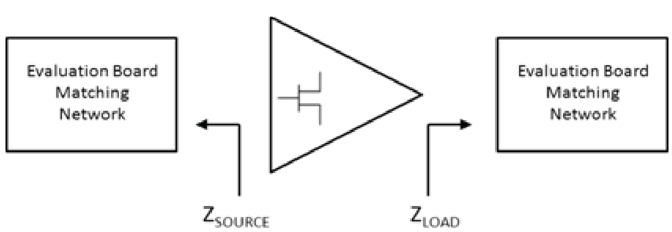
Evaluation Board Layout



Device Impedances

Frequency (MHz)	Z Source (Ω)	Z Load (Ω)
2800	60.4 – j0.5	42.1 – j30.5
3000	51.9 – j13.5	33.8 – j25.7
3200	44.1 – j16.5	29.5 – j8.9
3400	38.3 – j16.7	17.0 – j9.0

NOTE: Device impedances reported are the measured evaluation board impedances chosen for a trade off of peak power, peak efficiency and gain performance across the entire frequency bandwidth.



Device Handling/Environmental Conditions

GaN HEMT devices are ESD sensitive materials. Please use proper ESD precautions when handling devices or evaluation boards.

GaN HEMT Capacitances

The physical structure of the GaN HEMT results in three terminal capacitors similar to other FET technologies. These capacitances exist across all three terminals of the device. The physical manufactured characteristics of the device determine the value of the C_{DS} (drain to source), C_{GS} (gate to source) and C_{GD} (gate to drain). These capacitances change value as the terminal voltages are varied. RFMD presents the three terminal capacitances measured with the gate pinched off (V_{GS} = -8V) and zero volts applied to the drain. During the measurement process, the parasitic capacitances of the package that holds the amplifier is removed through a calibration step. Any internal matching is included in the terminal capacitance measurements. The capacitance values presented in the typical characteristics table of the device represent the measured input (C_{ISS}), output (C_{OSS}), and reverse (C_{RSS}) capacitance at the stated bias voltages. The relationship to three terminal capacitances is as follows:

$$C_{ISS} = C_{GD} + C_{GS}$$

$$C_{OSS} = C_{GD} + C_{DS}$$

$$C_{RSS} = C_{GD}$$

DC Bias

The GaN HEMT device is a depletion mode high electron mobility transistor (HEMT). At zero volts V_{GS} the drain of the device is saturated and uncontrolled drain current will destroy the transistor. The gate voltage must be taken to a potential lower than the source voltage to pinch off the device prior to applying the drain voltage, taking care not to exceed the gate voltage maximum limits. RFMD recommends applying V_{GS} = -5V before applying any V_{DS}.

RF Power transistor performance capabilities are determined by the applied quiescent drain current. This drain current can be adjusted to trade off power, linearity, and efficiency characteristics of the device. The recommended quiescent drain current (I_{DQ}) shown in the RF typical performance table is chosen to best represent the operational characteristics for this device, considering manufacturing variations and expected performance. The user may choose alternate conditions for biasing this device based on performance trade off.

Mounting and Thermal Considerations

The thermal resistance provided as R_{TH} (junction to case) represents only the packaged device thermal characteristics. This is measured using IR microscopy capturing the device under test temperature at the hottest spot of the die. At the same time, the package temperature is measured using a thermocouple touching the backside of the die embedded in the device heatsink but sized to prevent the measurement system from impacting the results. Knowing the dissipated power at the time of the measurement, the thermal resistance is calculated.

In order to achieve the advertised MTTF, proper heat removal must be considered to maintain the junction at or below the maximum of 200°C. Proper thermal design includes consideration of ambient temperature and the thermal resistance from ambient to the back of the package including heatsinking systems and air flow mechanisms. Incorporating the dissipated DC power, it is possible to calculate the junction temperature of the device.