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RFFM6901

2.8V TO 4.2V, 915MHZ ISM BAND TRANSMIT/ RECEIVE MODULE WITH DIVERSITY SWITCH

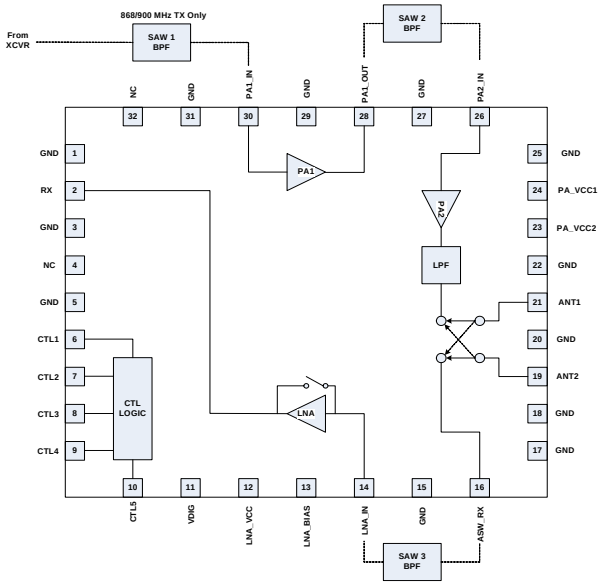
Package Style: LGA, 32-Pin, 6mm x 6mm

Features

- Tx Output Power: 30dBm
- Separate Rx/Tx 50Ω Transceiver Interface
- Antenna Diversity Switch
- LNA with Bypass mode

Applications

- Wireless Automated Metering
- Wireless Alarm Systems
- Portable Battery Powered Equipment
- Smart Energy
- 868MHz/915MHz ISM Band Application
- Single Chip RF Front End Module



Functional Block Diagram

Product Description

The RFFM6901 is a single-chip front end module (FEM) for application in the 915MHz ISM Band. The RFFM6901 addresses the need for aggressive size reduction for typical portable equipment RF front end designs and greatly reduces the number of components outside of the core chipset thus minimizing the footprint and assembly cost of the overall solution. The RFFM6901 contains an integrated 1W PA, dual port diversity antenna switch, LNA with bypass mode, and matching components. The RFFM6901 is packaged in a 32-pin, 6.0mm x 6.0mm x 1.2mm over-molded laminate package.

Ordering Information

RFFM6901	ISM Band Tx/Rx Module with Diversity Antenna Switch
RFFM6901SB	5-Piece Bag
RFFM6901SQ	25-Piece Bag
RFFM6901SR	Standard 100-Piece Reel
RFFM6901TR7	Standard 750-Piece Reel
RFFM6901TR13	Standard 2500-Piece Reel
RFFM6901PCK-410	Fully Assembled Evaluation Board and 5-Piece Bag

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☑ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ BiFET HBT
☑ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ SOI

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Absolute Maximum Ratings

Parameter	Rating	Unit
Voltage	5.25	V_{DC}
Storage Temperature Range	-40 to +150	°C
Operating Temperature Range	-40 to +85	°C
Maximum Input Power to PA, pin 30, 2 (no damage)	+5	dBm
Maximum Input Power to PA, pin 26(no damage)	+23	dBm
Maximum Input Power to LNA, pin 19, 21 (no damage)	+10	dBm
Moisture Sensitivity Level	MSL3	

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS (Restriction of Hazardous Substances): Compliant per EU Directive 2002/95/EC.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					
Active Frequency	868	902 to 928		MHz	PA and LNA
RF Port Impedance		50		Ω	
ESD, Human Body Model	500			V	RF Pins
	500			V	All Other Pins
ESD, Charge Device Model	500			V	RF Pins
	500			V	All Other Pins
PA Section					
Transmit Mode 4V (High Voltage)					TXRX_SEL Logic = LOW, P_{IN} = 0dBm at pin 30, V_{CC} DIG and Logic signals may be applied in any order
Power Supply Operation Voltage-High	3.8	4	4.2	V	PA V_{CC}
Input Power		0	5	dBm	Pin 30
CW Output Power-near saturation (ANT1) at 4.0V	31	31.5		dBm	
CW Output Power-near saturation (ANT2) at 4.0V	31	31.5		dBm	
Output Power (ANT1) at 4.0V	30	30.5		dBm	
Output Power (ANT2) at 4.0V	30	30.5		dBm	
Thermal Resistance	39.83			C°/W	V_{CC} = V_{DIG} = 4.0V, $LNAV_{CC}$ = GND, CTL1 = CTL4 = CTL5 = 3.8V, CTL2 = CTL3 = 0V, P_{OUT} = 30.1dBm, Modulation = CW, Freq = 902MHz, DC = 100%, T = 85°C
1W Current (ANT1) at 4.0V at P_{OUT} = 30dBm		600	700	mA	
1W Current (ANT2) at 4.0V at P_{OUT} = 30dBm		600	700	mA	
1/2W Current (ANT1) at 4.0V at P_{OUT} = 27dBm	415	450	490	mA	
1/2W Current (ANT2) at 4.0V at P_{OUT} = 27dBm	415	450	490	mA	
1/4W Current (ANT1) at 4.0V at P_{OUT} = 24dBm	310	340	370	mA	
1/4W Current (ANT2) at 4.0V at P_{OUT} = 24dBm	310	340	370	mA	
Large Signal Gain Overall High Bias (ANT1) at 4.0V	27	30	33	dB	

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
PA Section (continued)					
Large Signal Gain Overall High Bias (ANT2) at 4.0V	27	30	33	dB	
Large Signal Gain Overall Low Bias (ANT1) at 4.0V	22	25	28	dB	
Large Signal Gain Overall Low Bias (ANT2) at 4.0V	22	25	28	dB	
Transmit Mode 3V (Low Voltage)					
Power Supply Operation Voltage-Low	2.8	3	3.2	V	PA V_{CC}
Input Power			5	dBm	
CW Output Power-near saturation (ANT1) at 3.0V	27.5	28		dBm	
CW Output Power-near saturation (ANT2) at 3.0V	27.5	28		dBm	
Output Power (ANT1) at 3.0V	26.5	27		dBm	V_{CC} = 3.0V, P_{OUT} at ANT1
Output Power (ANT2) at 3.0V	26.5	27		dBm	V_{CC} = 3.0V, P_{OUT} at ANT2
1/2W Current (ANT1) at 3.0V at P_{OUT} = 27dBm	400	450	500	mA	
1/2W Current (ANT2) at 3.0V at P_{OUT} = 27dBm	400	450	500	mA	
1/4W Current (ANT1) at 3.0V at P_{OUT} = 24dBm	300	340	375	mA	
1/4W Current (ANT2) at 3.0V at P_{OUT} = 24dBm	300	340	375	mA	
2nd Harmonic (ANT1) High Voltage (4.0V) 30dBm P_{OUT}			-32	dBc	
3rd to 10th Harmonic (ANT1) High Voltage (4.0V) 30dBm P_{OUT}			-71	dBc	
2nd Harmonic (ANT2) High Voltage (4.0V) 30dBm P_{OUT}			-32	dBc	
3rd to 10th Harmonic (ANT2) High Voltage (4.0V) 30dBm P_{OUT}			-71	dBc	
2nd Harmonic (ANT1) Low Voltage (3.0V) 30dBm P_{OUT}			-32	dBc	
3rd to 10th Harmonic (ANT1) Low Voltage (3.0V) 30dBm P_{OUT}			-71	dBc	
2nd Harmonic (ANT2) Low Voltage (3.0V) 30dBm P_{OUT}			-32	dBc	
3rd to 10th Harmonic (ANT2) Low Voltage (3.0V) 30dBm P_{OUT}			-71	dBc	
Input Return Loss (PA1-ANT1)High Voltage (4.0V)		-10		dB	Measured at PA-IN Port at Pin 30
Input Return Loss (PA1-ANT2)High Voltage (4.0V)		-10		dB	Measured at PA-IN Port at Pin 30
Input Return Loss (PA1-ANT1)Low Voltage (3.0V)		-10		dB	Measured at PA-IN Port at Pin 30
Input Return Loss (PA1-ANT2)Low Voltage (3.0V)		-10		dB	Measured at PA-IN Port at Pin 30
PA Leakage Current		0.5	5	µA	PA V_{CC} = 4.2V, PD SEL Logic = 0.0V
Noise Power at ANT ½ -Electric only at -8MHz Offset from carrier		-132		dBm/Hz	PA_V_{CC} voltage of 4.2V and P_{OUT} = +28dBm, PA2 only zero noise contribution from PA1

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Rx Section					
High Bias Rx Mode					TXRX_SEL Logic = High, LNA_SEL Logic = High V_{CC}_DIG and Logic signals may be applied in any order; pin 13 floating
Operating Voltage	2.7	4	4.2	V	LNA_V_{CC}
Gain at High Bias (HB) PI = -40 to -10dBm 4.2V	15	17		dB	LNA_V_{CC} = 3.3V to 4.4V; LNA Bias = High Bias
Gain at High Bias (HB) PI = -40 to -10dBm 4.0V	15	17		dB	LNA_V_{CC} = 3.3V to 4.4V; LNA Bias = High Bias
Gain at High Bias (HB) PI = -40 to -10dBm 3.6V	15	17		dB	LNA_V_{CC} = 3.3V to 4.4V; LNA Bias = High Bias
Gain at High Bias (HB) PI = -40 to -10dBm 3.3V	15	17		dB	LNA_V_{CC} = 3.3V to 4.4V; LNA Bias = High Bias
Gain at High Bias (HB) PI = -40 to -10dBm 2.7V	13	15		dB	LNA_V_{CC} = 2.7V LNA Bias = High Bias
Noise Figure at HB		1.5	2	dB	LNA_VCC = 3.3 V to 4.2V; LNA Bias = High Bias
		1.5	2	dB	LNA_V_{CC} = 2.7V LNA Bias = High Bias
Input IP3 at HB	3	5		dBm	LNA_VCC = 4.2V; LNA Bias = High Bias
	2	5		dBm	LNA_V_{CC} = 2.7V LNA Bias = High Bias
Input Return Loss	10			dB	Measured at LNA-IN Port at Pin 14
Output Return Loss	10			dB	Measured at RF_{IO} 900 Pin 2
Power Supply Current	6	8	10	mA	LNA_V_{CC}
Low Bias Rx Mode					TXRX_SEL Logic = High, LNA_SEL Logic = HIGH V_{CC}_DIG and Logic signals may be applied in any order; 51KΩ resistor pull-down from pin 13 to ground.
Gain at Low Bias (LB)	13	15		dB	LNA_V_{CC} = 3.3V to 4.2V; LNA Bias = Low Bias
Gain at LB	9	12		dB	LNA_V_{CC} = 2.7V; LNA Bias = Low Bias
Noise Figure at LB		2.5	3.5	dB	LNA_V_{CC} = 3.3V to 4.2V; LNA Bias = Low Bias
		3	4	dB	LNA_V_{CC} = 2.7V; LNA Bias = Low Bias

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
LNA Section (LNA-IN Pin 14 to RFIO Pin 2)					
Input IP3 at LB	-1	1		dBm	LNA_V_{CC} = 3.3V to 4.2V; LNA Bias = Low Bias
Input IP3 at LB		-5		dBm	LNA_V_{CC} = 2.7V; LNA Bias = Low Bias
Power Supply Current	3	3	4	mA	LNA_V_{CC} = 3.6V
Rx LNA Bypass Mode					TXRX_SEL Logic = HIGH, LNA_SEL Logic = LOW, V_{CC}_DIG and Logic signals may be applied in any order.
Operating Voltage	2.7	4	4.2	V	LNA_V_{CC}
Gain	-3	-2.5	-2	dB	
Input Ip3	12	18		dBm	
Input Return Loss	10			dB	
Output Return Loss	10			dB	
Power Supply Current		1	2	mA	
LNA Leakage Current		0.5	5	µA	LNA_V_{CC} = 4.2, PD_SEL = LOW
Antenna Switch Section					
Insertion Loss TX-ANT1		0.8	1	dB	
Insertion Loss TX-ANT2		0.8	1	dB	
Insertion Loss ANT1-ASWRX		1	1.25	dB	
Insertion Loss ANT2-ASWRX		1	1.25	dB	
Isolation	20			dB	
Tx Return Loss	10	15		dB	

Operating Mode	CTL1	CTL2	CTL3	CTL4	CTL5
Tx to ANT1 LOW	1	0	0	1	0
Tx to ANT2 LOW	0	0	0	1	0
Rx from ANT1	1	1	1	1	0
Rx from ANT2	0	1	1	1	0
Rx from ANT1 LNA Bypass	1	1	0	1	0
Rx from ANT2 LNA Bypass	0	1	0	1	0
Tx ANT1 HI BIAS	1	0	0	1	1
Tx ANT2 HI BIAS	0	0	0	1	1

Pin Descriptions

Pin	Name	Description
1	GND	Ground.
2	RX	868MHz/900MHz Receive, Internally DC Blocked.
3	GND	Ground.
4	NC	Not Connected in FEM.
5	GND	Ground.
6	CTL1	ANT Select.
7	CTL2	TxRx Select.
8	CTL3	LNA Select.
9	CTL4	PD Select.
10	CTL5	PA_Low Bias.
11	VDIG	Digital V_{CC}.
12	LNA_Vcc	LNA V_{CC}.
13	LNA_Bias	LNA linearity bias (Place SMD Resistor to GND to Lower LNA I_{DD}).
14	LNA_IN	LNA Signal Input, Internally DC Blocked.
15	GND	Ground.
16	ASW_RX	Antenna Switch Receive Output, Internally DC Blocked.
17	GND	Ground.
18	GND	Ground.
19	ANT2	Antenna 2 Output/Input, Internally DC Blocked.
20	GND	Ground.
21	ANT1	Antenna 1 Output/Input, Internally DC Blocked.
22	GND	Ground.
23	PA VCC2	PA Battery Bias for Second Stage.
24	PA VCC1	PA Battery Bias for First Stage.
25	GND	Ground.
26	PA2_IN	Power Amplifier 2nd Stage Signal Input Port.
27	GND	Ground.
28	PA1_OUT	Power Amplifier 1st Stage Signal Output Port, Internally DC Blocked.
29	GND	Ground.
30	PA1_IN	Power Amplifier 1st Stage Signal Input Port, Internally DC Blocked.
31	GND	Ground.
32	NC	Not connected in FEM.

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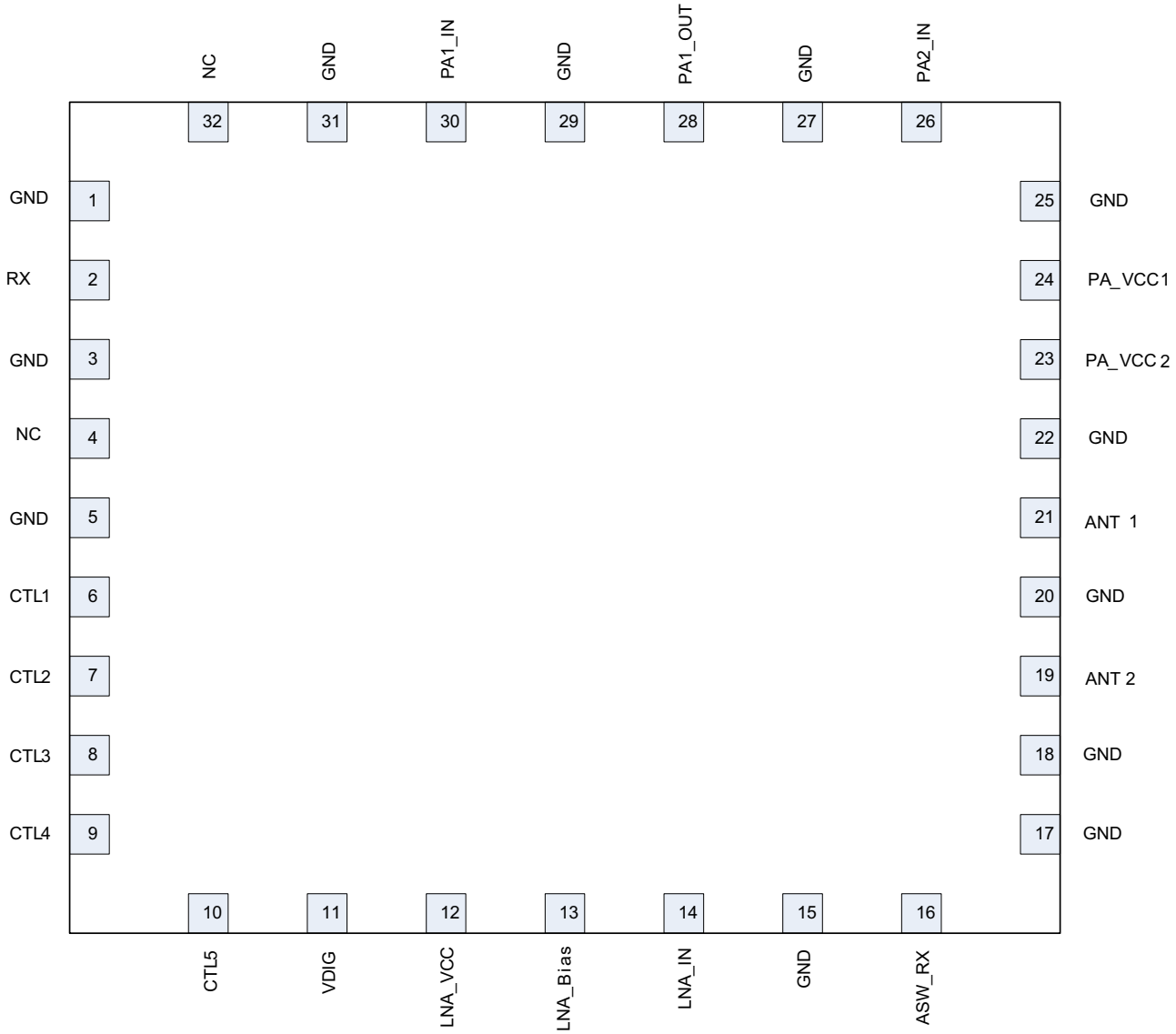
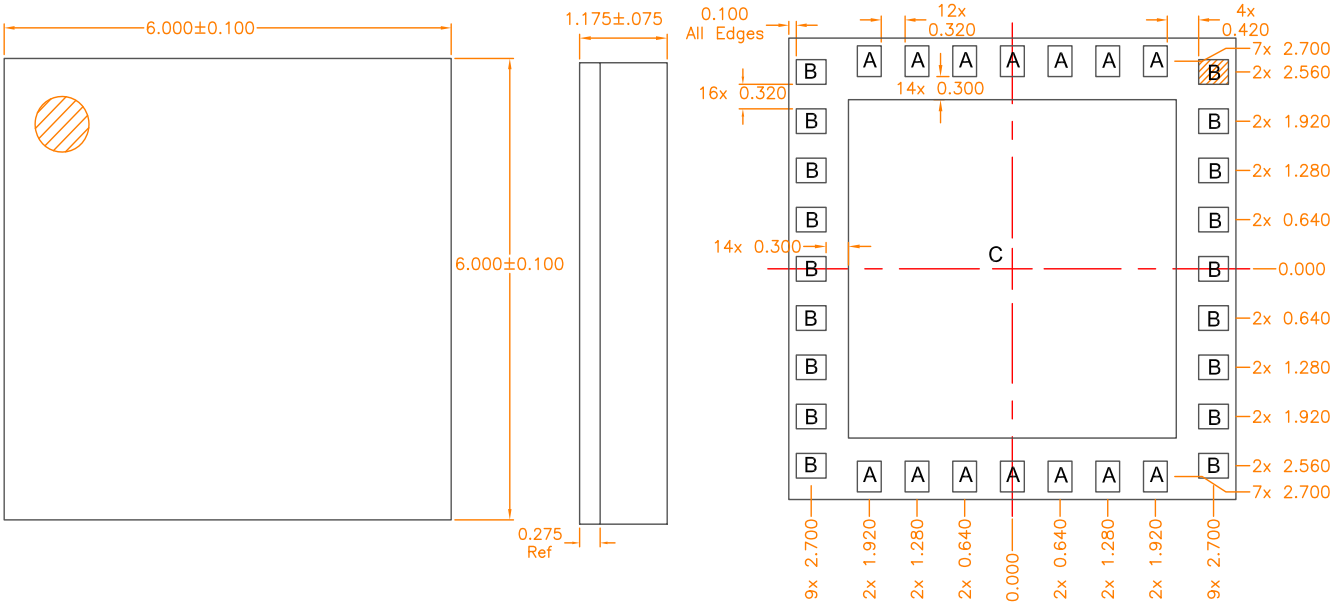
Pin Out


NC
GND
PA1_IN
GND
PA1_OUT
GND
PA2_IN
32
31
30
29
28
27
26
GND 1
RX 2
GND 3
NC 4
GND 5
CTL1 6
CTL2 7
CTL3 8
CTL4 9
25 GND
24 PA_VCC1
23 PA_VCC 2
22 GND
21 ANT 1
20 GND
19 ANT 2
18 GND
17 GND
10
11
12
13
14
15
16
CTL5
VDIG
LNA_VCC
LNA_Bias
LNA_IN
GND
ASW_RX

Package Drawing



Notes:
1. Shaded area represents Pin 1 location.

A = 0.320 x 0.400 mm
B = 0.400 x 0.320 mm
C = 4.400 x 4.400 mm

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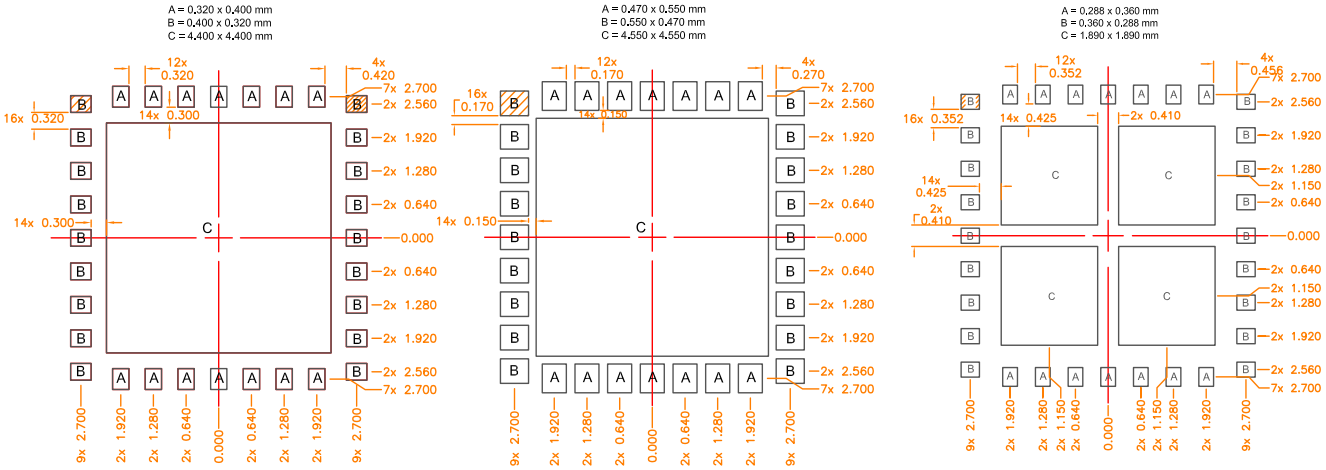
Recommended PCB Patterns



PCB Metal Land Pattern

PCB Solder Mask Pattern

PCB Stencil Pattern

Notes:
1. Shaded area represents Pin 1 location.

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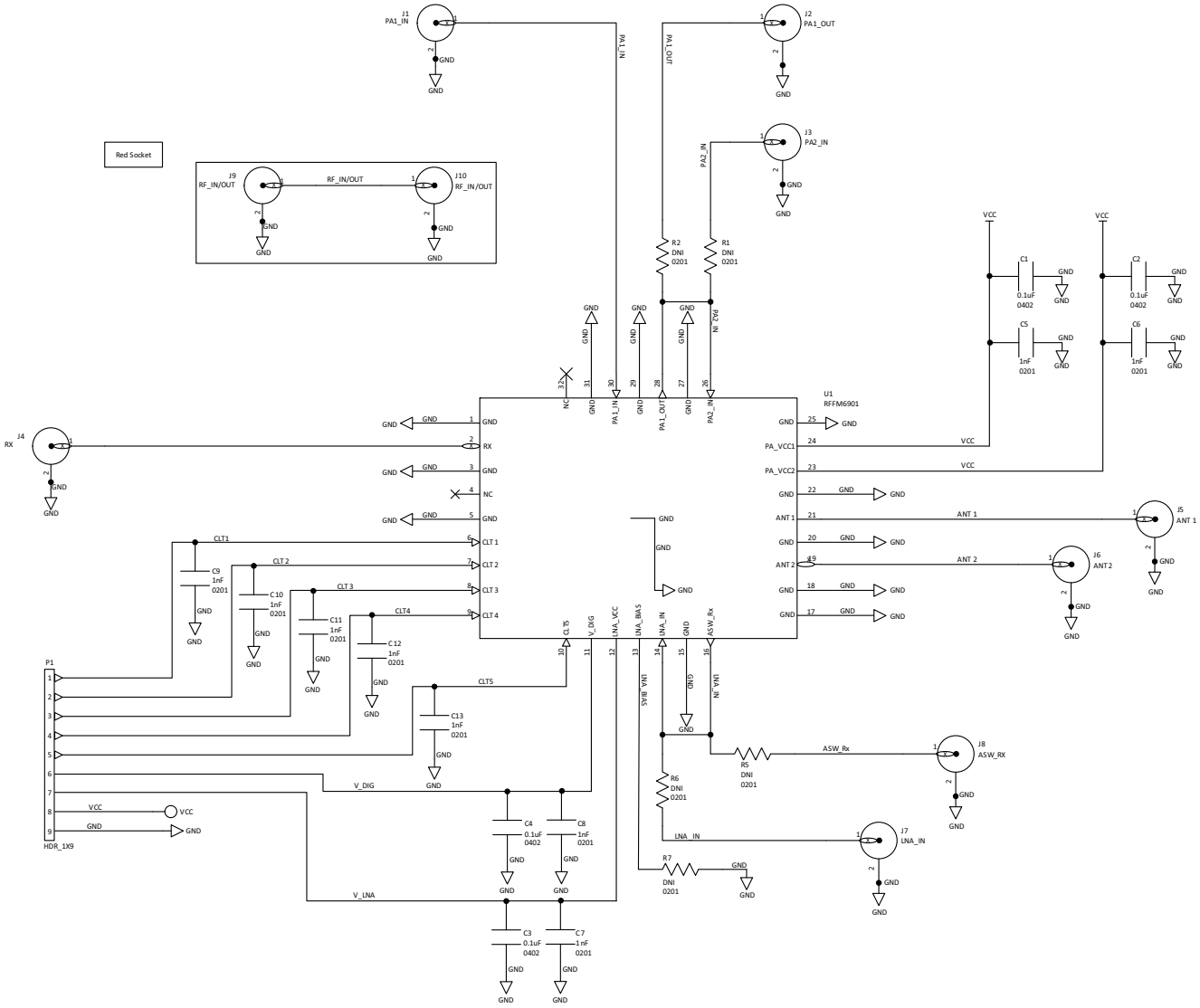
Evaluation Board Schematic



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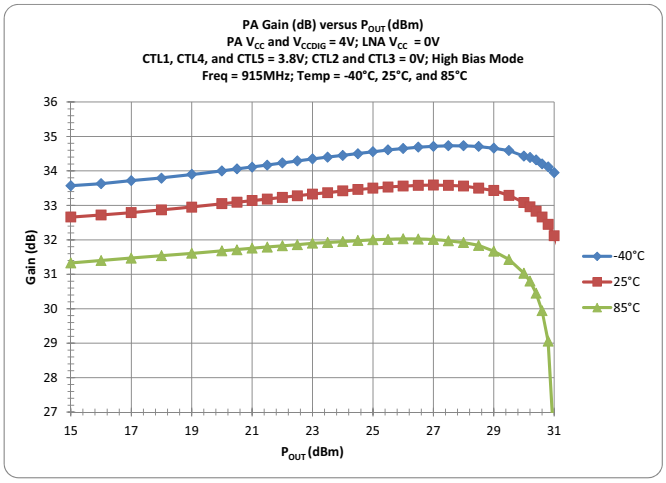
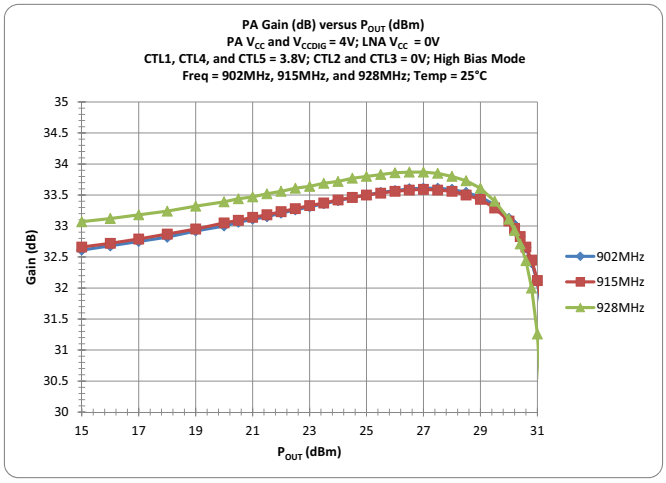
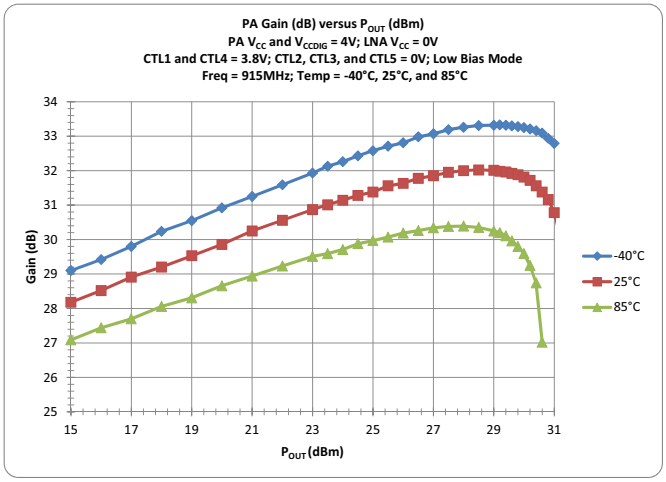
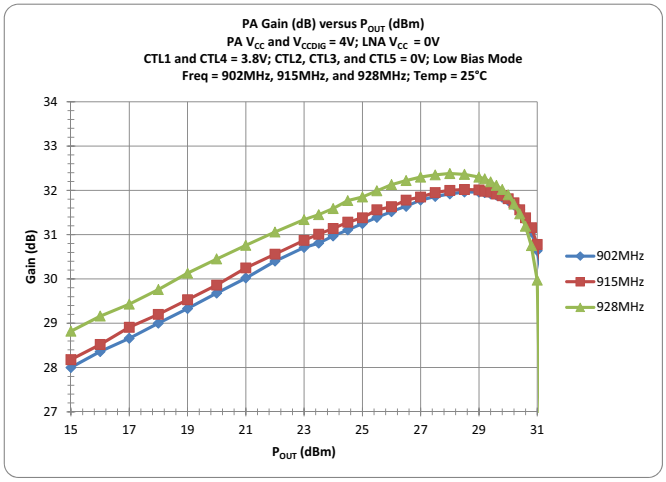
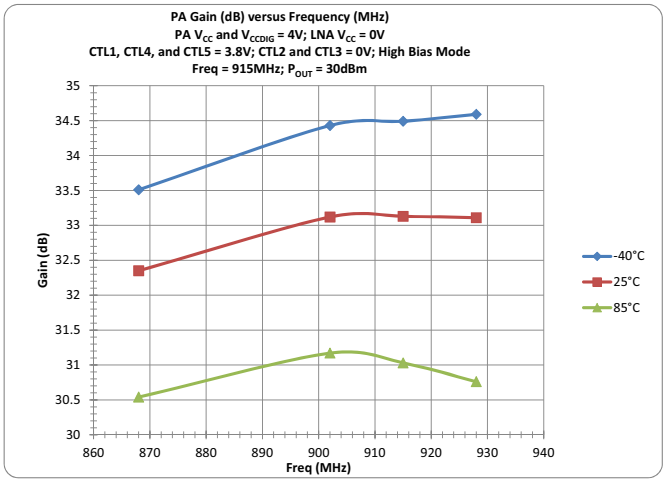
Performance Plots

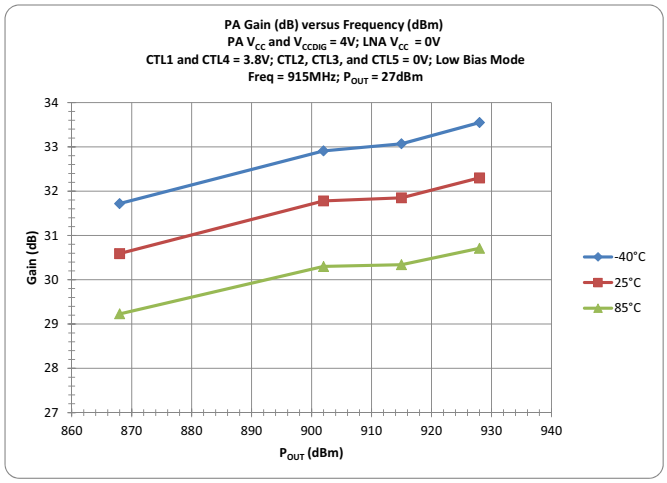




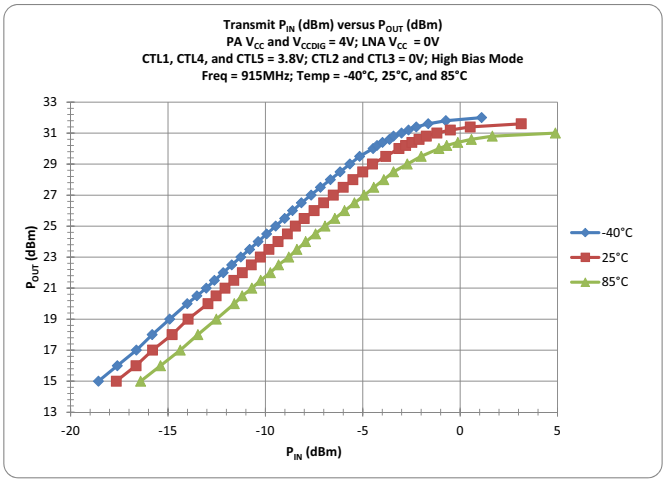


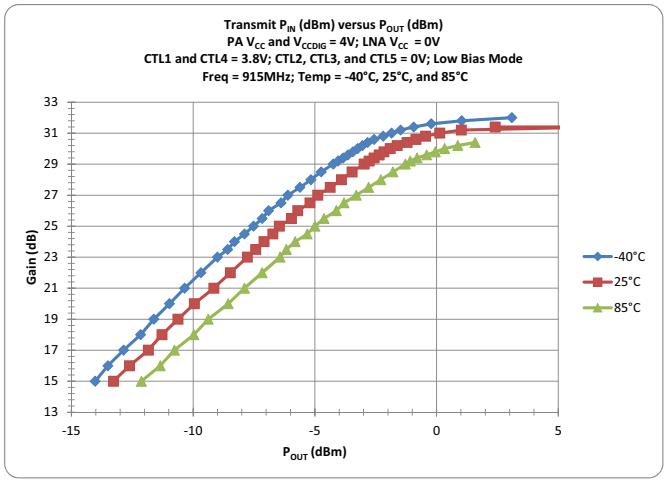


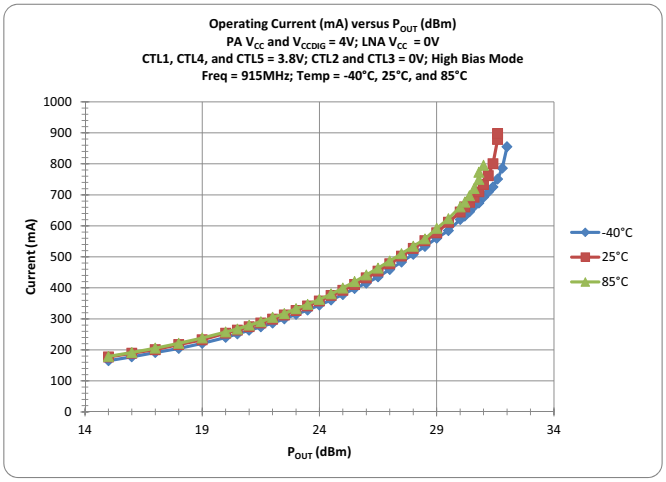


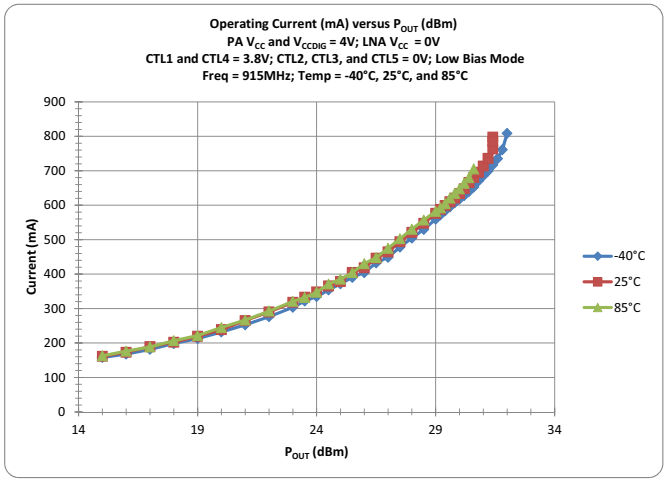


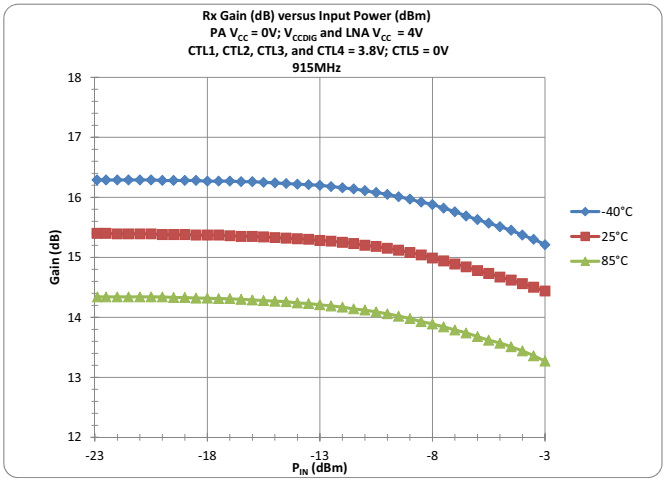
Performance Plots (continued)

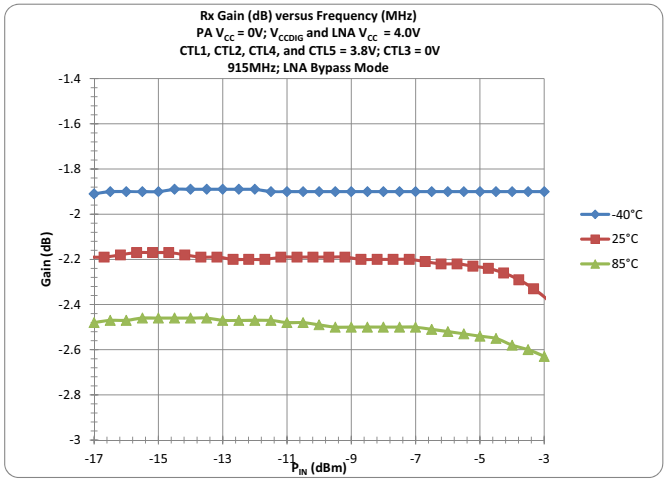












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Performance Plots (continued)