

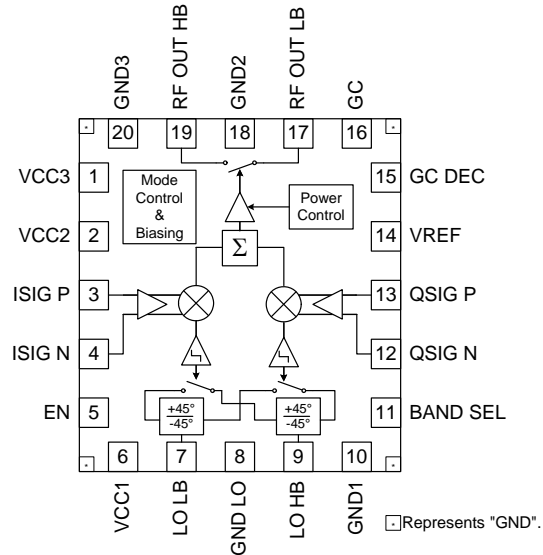


### Features

- Dual-Band Operation 700 MHz to 2700 MHz
- -156dBm/Hz noise at 20MHz offset
- +19dBm OIP3
- +6dBm OP1dB
- 35dB Gain Control Range
- Single 2.7V to 3.3V Supply

### Applications

- TDMA/GSM/EDGE Handsets
- GSM/EDGE Handsets
- W-CDMA Handsets
- TDMA-Based Wireless Applications
- Wireless Local Loop
- Base Stations



Functional Block Diagram

### Product Description

The RF2483 is a dual-band direct I/Q to RF modulator designed for handset applications where multiple modes of operation are required. The device provides common differential I/Q inputs and a common AGC amplifier. Independent single-ended LO inputs and single-ended high and low band RF outputs are provided. The device achieves a very low out-of-band noise density of -156dBm/Hz minimizing RF filtering. Operating from a single 2.7V supply, the device is assembled in a 4 mm x 4 mm, 20-pin, QFN package.

### Ordering Information

RF2483SQ	Sample Bag with 25 Pieces
RF2483SR	7" Sample Reel with 100 Pieces
RF2483TR7	7" Reel with 750 Pieces
RF2483TR13	13" Reel with 2500 Pieces
RF2483PCK-410	2400MHz PCBA with 5-piece Sample Bag

### Optimum Technology Matching® Applied

- |                                      |   |                                     |                                   |
|--------------------------------------|---|-------------------------------------|-----------------------------------|
| <input type="checkbox"/> GaAs HBT    | <input checked="" type="checkbox"/> SiGe BiCMOS | <input type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET | <input type="checkbox"/> Si BiCMOS              | <input type="checkbox"/> Si CMOS    |                                   |
| <input type="checkbox"/> InGaP HBT   | <input type="checkbox"/> SiGe HBT               | <input type="checkbox"/> Si BJT     |                                   |

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## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 3.6	V
Storage Temperature	-40 to +150	°C
Operating Ambient Temperature	-40 to +85	°C
Input Voltage, any pin	-0.5 to 3.6	V
Input Power, any pin	+10	dBm



**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

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RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Operating Range</b>					
Supply Voltage*	2.7		3.3	V	
Temperature Range*	-40		+85	°C	
High Band Frequency Range*	1700		2700	MHz	Bandssel = 2.7V
Low Band Frequency Range*	700		1000	MHz	Bandssel = 0V
<b>DC Parameters</b>					
High Band Supply Current	65	85	110	mA	GC = 2.0V, V <sub>CC</sub> = 2.7V, EN = 2.7V, Bandssel = 2.7V, IQ = 1.2V <sub>DC</sub> , T <sub>A</sub> = 25°C
Low Band Supply Current	65	85	110	mA	GC = 2.0V, V <sub>CC</sub> = 2.7V, EN = 2.7V, Bandssel = 0V, IQ = 1.2V <sub>DC</sub> , T <sub>A</sub> = 25°C
Sleep Current		<1.0	10	µA	EN = 0V
<b>Logic Levels</b>					
Input Logic Low	0		0.5	V	
Input Logic High	1.4		V <sub>CC</sub>	V	
Logic Pins Input Current*		<1.0		µA	
<b>LO Input Port</b>					
High Band Frequency Range*	1700		2700	MHz	Bandssel = 2.7V
Low Band Frequency Range*	700		1000	MHz	Bandssel = 0V
High Band LO Input Power*	-3	0	6	dBm	Bandssel = 2.7V
LO Band LO Input Power*	-3	0	6	dBm	Bandssel = 0V
Input Impedance*		50		Ω	

\* = Not tested in production

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>I/Q Modulator High Band (1700MHz to 2200MHz)</b>					$V_{CC}=2.7V$ , $EN=2.7V$ , $BandSel=2.7V$ , $FLO=1900MHz$ , $PLO=0dBm$ , LO HB and RF OUT HB ports are matched to $50\Omega$ . $IQ=800mV_{P-P}$ at $100kHz$ $1.2V_{DC}$ . Input IQ signals driven differentially and in quadrature from a $50\Omega$ source impedance. $T_A=25^\circ C$
Baseband Input Voltage*	1.15	1.2	1.25	V	Common mode voltage
Baseband Input Level		0.8		$V_{PP}$	Measured differentially
Baseband Input Impedance*		5.5		$k\Omega$	Measured at $100kHz$
Input Bandwidth*	50	150		MHz	I/Q source impedance $50\Omega$
Sideband Suppression	30	43		dBc	GC=2.0V, no I/Q adjustment
	30	43		dBc	GC=1.5V, no I/Q adjustment
	30	42		dBc	GC=1.0V, no I/Q adjustment
	30	40		dBc	GC=0.5V, no I/Q adjustment
Carrier Suppression	30	37		dBc	GC=2.0V, no I/Q adjustment
	30	35		dBc	GC=1.5V, no I/Q adjustment
	20	23		dBc	GC=1.0V, no I/Q adjustment
	20	22		dBc	GC=0.5V, no I/Q adjustment
3rd Harmonic of Modulation					
Suppression at FLO-3x100kHz	40	47		dBc	GC=2.0V
	40	47		dBc	GC=1.5V
	40	54		dBc	GC=1.0V
	40	46		dBc	GC=0.5V
Baseband Inputs DC Current Drain*			100	$\mu A$	
Baseband Inputs AC Current Drain*			100	$\mu A_{PP}$	
<b>I/Q Modulator Low Band (700MHz to 1000MHz)</b>					$V_{CC}=2.7V$ , $EN=2.7V$ , $BandSel=0V$ , $FLO=900MHz$ , $PLO=0dBm$ , LO LB and RF OUT LB ports are matched to $50\Omega$ . $IQ=800mV_{P-P}$ at $100kHz$ $1.2V_{DC}$ . Input IQ signals driven differentially and in quadrature from a $50\Omega$ source impedance. $T_A=25^\circ C$
Baseband Input Voltage*	1.15	1.2	1.25	V	Common mode voltage
Baseband Input Level		0.8		$V_{PP}$	Measured differentially
Baseband Input Impedance*		5.5		$k\Omega$	Measured at $100kHz$
Input Bandwidth*	50	150		MHz	I/Q source impedance $50\Omega$
Sideband Suppression	30	41		dBc	GC=2.0V, no I/Q adjustment
	30	43		dBc	GC=1.5V, no I/Q adjustment
	30	42		dBc	GC=1.0V, no I/Q adjustment
	30	40		dBc	GC=0.5V, no I/Q adjustment
Carrier Suppression	35	48		dBc	GC=2.0V, no I/Q adjustment
	35	45		dBc	GC=1.5V, no I/Q adjustment
	30	40		dBc	GC=1.0V, no I/Q adjustment
	25	33		dBc	GC=0.5V, no I/Q adjustment
3rd Harmonic of Modulation					

\* = Not tested in production

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>I/Q Modulator Low Band, cont.</b>					
Suppression at FLO-3x100kHz	40	57		dBc	GC=2.0V
	40	57		dBc	GC=1.5V
	40	60		dBc	GC=1.0V
	40	52		dBc	GC=0.5V
Baseband Inputs DC Current Drain*			100	μA	
Baseband Inputs AC Current Drain*			100	μA <sub>pp</sub>	
<b>Variable Gain Amplifiers High Band (1700MHz to 2200MHz)</b>					
					V <sub>CC</sub> =2.7V, EN=2.7V, BandSel=2.7V, FLO=1900MHz, PLO=0dBm, LO HB and RF OUT HB ports are matched to 50Ω. Input IQ signals driven differentially and in quadrature from a 50Ω source impedance. T <sub>A</sub> =25°C
Gain Control Voltage Range	0		2.0	V	
Gain Control Range	32	35		dB	Difference between output power at GC=2.0V and GC=0.5V
Gain Control Slope	26	29	33	dB/V	Calculated GC=1.0V and 1.5V
Gain Control Input Impedance*		10		kΩ	
Output Power	-3	0.4	3	dBm	GC=2.0V, IQ=800mV <sub>p,p</sub> at 100kHz
	-8	-5	-2	dBm	GC=1.5V, IQ=800mV <sub>p,p</sub> at 100kHz
	-24	-20	-16	dBm	GC=1.0V, IQ=800mV <sub>p,p</sub> at 100kHz
	-38	-35	-30	dBm	GC=0.5V, IQ=800mV <sub>p,p</sub> at 100kHz
Output Noise at FLO+20MHz*		-155		dBm/Hz	GC=2.0V, IQ=800mV <sub>p,p</sub> at 100kHz
		-156.7		dBm/Hz	GC=2.0V, IQ=0mV <sub>p,p</sub>
Output P1dB*		+6		dBm	IQ at 100kHz
Output IP3*		+20		dBm	GC=2.0V. Extrapolated from IM3 with two baseband tones at 90kHz applied differentially, in quadrature, at both I and Q inputs, each tone 400mV <sub>p,p</sub>
Intermodulation IM3 tone at FLO+70kHz and FLO+130kHz relative to tone at FLO+90kHz					Two baseband tones at 90kHz and 110kHz applied differentially, in quadrature, at both I and Q inputs, each tone 400mV <sub>p,p</sub>
	40	50		dBc	GC=2.0V
	40	50		dBc	GC=1.5V
	40	50		dBc	GC=1.0V
	40	47		dBc	GC=0.5V

\* = Not tested in production

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Variable Gain Amplifiers Low Band (700MHz to 1000MHz)</b>					$V_{CC}=2.7V$ , $EN=2.7V$ , $BandSel=0V$ , $FLO=900MHz$ , $PLO=0dBm$ , LO LB and RF OUT LB ports are matched to $50\Omega$ . Input IQ 1.2Vdc, signals driven differentially and in quadrature from a $50\Omega$ source impedance. $T_A=25^\circ C$
Gain Control Voltage Range	0		2.0	V	
Gain Control Range	32	36		dB	Difference between output power at GC=2.0V and 0.5V
Gain Control Slope	26	29.5	33	dB/V	Calculated using output power at GC=1.0V and 1.5V
Gain Control Input Impedance*		10		k $\Omega$	
Output Power	-3	0.8	3	dB	GC=2.0V, IQ=800mV <sub>p,p</sub> at 100kHz
	-7.5	-4.5	-1.5	dB	GC=1.5V, IQ=800mV <sub>p,p</sub> at 100kHz
	-24	-21	-16	dB	GC=1.0V, IQ=800mV <sub>p,p</sub> at 100kHz
	-41	-35	-33	dB	GC=0.5V, IQ=800mV <sub>p,p</sub> at 100kHz
Output Noise at FLO+20MHz*		-156.4		dBm/Hz	GC=2.0V, IQ=800mV <sub>p,p</sub> at 100kHz
		-157.2		dBm/Hz	GC=2.0V, IQ=0mV <sub>p,p</sub>
Output P1dB*		+6		dBm	IQ at 100kHz
Output IP3*		+19		dBm	GC=2.0V. Extrapolated from IM3 with two baseband tones at 90kHz and 110kHz applied differentially, in quadrature, at both I and Q inputs, each tone 400mV <sub>p,p</sub>
Intermodulation IM3 tone at FLO+70kHz and FLO+130kHz relative to tone at FLO+90kHz					Two baseband tones at 90kHz and 110kHz applied at both I and Q inputs, each tone 400mV <sub>p,p</sub>
	40	50		dBc	GC=2.0V
	40	50		dBc	GC=1.5V
	40	50		dBc	GC=1.0V
	40	50		dBc	GC=0.5V

\* = Not tested in production

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>I/Q Modulator High Band (2400MHz)</b>					$V_{CC}=2.7V$ , $EN=2.7V$ , $Bandset=2.7V$ , $FLO=2400MHz$ , $PL0=0dBm$ , LO HB and RF OUT HB ports are matched to $50\Omega$ . $IQ=800mV_{p,p}$ at $100kHz$ $1.2V_{DC}$ . Input IQ signals driven differentially and in quadrature from a $50\Omega$ source impedance. $T_A=25^\circ C$
Baseband Input Voltage*	1.15	1.2	1.25	V	Common mode voltage
Baseband Input Level		0.8		$V_{pp}$	Measured differentially
Baseband Input Impedance*		5.5		$k\Omega$	Measured at 100kHz
Input Bandwidth*	50	150		MHz	I/Q source impedance $50\Omega$
Sideband Suppression	30	34		dBc	GC=2.0V, no I/Q adjustment
	30	37		dBc	GC=1.5V, no I/Q adjustment
	38	43		dBc	GC=1.0V, no I/Q adjustment
	40	47		dBc	GC=0.5V, no I/Q adjustment
Carrier Suppression	30	38		dBc	GC=2.0V, no I/Q adjustment
	30	38		dBc	GC=1.5V, no I/Q adjustment
	22	32		dBc	GC=1.0V, no I/Q adjustment
	16	22		dBc	GC=0.5V, no I/Q adjustment
3rd Harmonic of Modulation					
Suppression at FLO-3x100kHz	50	58		dBc	GC=2.0V
	50	58		dBc	GC=1.5V
	50	59		dBc	GC=1.0V
	50	62		dBc	GC=0.5V
Baseband Inputs DC Current Drain*			100	$\mu A$	
Baseband Inputs AC Current Drain*			100	$\mu A_{pp}$	
<b>Variable Gain Amplifiers High Band (2400MHz)</b>					$V_{CC}=2.7V$ , $EN=2.7V$ , $Bandset=2.7V$ , $FLO=2400MHz$ , $PL0=0dBm$ , LO HB and RF OUT HB ports are matched to $50\Omega$ . Input IQ signals driven differentially and in quadrature from a $50\Omega$ source impedance. $T_A=25^\circ C$
Gain Control Voltage Range	0		2.0	V	
Gain Control Range	32	35		dB	Difference between output power at GC=2.0V and GC=0.5V
Gain Control Slope	26	29	33	dB/V	Calculated GC=1.0V and 1.5V
Gain Control Input Impedance*		10		$k\Omega$	
Output Power	-3	0.4	3	dB	GC=2.0V, $IQ=800mV_{p,p}$ at 100kHz
	-10	-7	-3	dB	GC=1.5V, $IQ=800mV_{p,p}$ at 100kHz
	-22	-18	-14	dB	GC=1.0V, $IQ=800mV_{p,p}$ at 100kHz
	-39	-35	-30	dB	GC=0.5V, $IQ=800mV_{p,p}$ at 100kHz
Output Noise at FLO+20MHz*		-155		dBm/Hz	GC=2.0V, $IQ=800mV_{p,p}$ at 100kHz
		-156.7		dBm/Hz	GC=2.0V, $IQ=0mV_{p,p}$
Output P1dB*		+6		dBm	$IQ$ at 100kHz
Output IP3*		+20		dBm	GC=2.0V. Extrapolated from IM3 with two baseband tones at 90kHz applied differentially, in quadrature, at both I and Q inputs, each tone $400mV_{p,p}$ .

\* =Not tested in production

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>I/Q Modulator High Band (2700MHz)</b>					$V_{CC}=2.7V$ , $EN=2.7V$ , Bandsel=2.7V, FLO=2700MHz, PLO=0dBm, LO HB and RF <sub>OUT</sub> HB ports are matched to 50Ω IQ=800mV <sub>P,P</sub> at 100kHz 1.2V <sub>DC</sub> . Input IQ signals driven differentially and in quadrature from a 50Ω source impedance. T <sub>A</sub> =25 ° C
Baseband Input Voltage*		1.2		V	Common mode voltage
Baseband Input Level*		0.8		V <sub>PP</sub>	Measured differentially
Baseband Input Impedance*		5.5		kΩ	Measured at 100kHz
Input Bandwidth*		150		MHz	I/Q source impedance 50Ω
Sideband Suppression*		34		dBc	GC=2.0V, no I/Q adjustment
		37		dBc	GC=1.5V, no I/Q adjustment
		43		dBc	GC=1.0V, no I/Q adjustment
		47		dBc	GC=0.5V, no I/Q adjustment
Carrier Suppression*		38		dBc	GC=2.0V, no I/Q adjustment
		38		dBc	GC=1.5V, no I/Q adjustment
		32		dBc	GC=1.0V, no I/Q adjustment
		22		dBc	GC=0.5V, no I/Q adjustment
3rd Harmonic of Modulation					
Suppression at FLO-3x100kHz*		58		dBc	GC=2.0V
		58		dBc	GC=1.5V
		59		dBc	GC=1.0V
		62		dBc	GC=0.5V
Baseband Input DC Current Drain*			100	μA	
Baseband Input AC Current Drain*			100	μA <sub>PP</sub>	
<b>Variable Gain Amplifiers High Band (2700MHz)</b>					$V_{CC}=2.7V$ , $EN=2.7V$ , Bandsel=2.7V, FLO=2700MHz, PLO=0dBm, LO HB and RF <sub>OUT</sub> HB ports are matched to 50Ω IQ=800mV <sub>P,P</sub> at 100kHz 1.2V <sub>DC</sub> . Input IQ signals driven differentially and in quadrature from a 50Ω source impedance. T <sub>A</sub> =25 ° C
Gain Control Voltage Range*	0		2.0	V	
Gain Control Range*		35		dB	Difference between output power at GC=2.0V and GC=0.5V
Gain Control Slope*		29		dB/V	Calculated GC=1.0V and 1.5V
Gain Control Input Impedance*		10		kΩ	
Output Power*		0.4		dB	GC=2.0V, IQ=800mV <sub>P,P</sub> at 100kHz
		-7		dB	GC=1.5V, IQ=800mV <sub>P,P</sub> at 100kHz
		-18		dB	GC=1.0V, IQ=800mV <sub>P,P</sub> at 100kHz
		-35		dB	GC=0.5V, IQ=800mV <sub>P,P</sub> at 100kHz
Output Noise at FLO + 20MHz*		-155		dBm/Hz	GC=2.0V, IQ=800mV <sub>P,P</sub> at 100kHz
		-156.7		dBm/Hz	GC=2.0V, IQ=0mV <sub>P,P</sub>
Output P1dB*		+6		dBm	IQ at 100kHz
Output IP3*		+20		dBm	GC=2.0V. Extrapolated from IM3 with two baseband tones at 90kHz applied differentially, in quadrature, at both I and Q inputs, each tone 400mV <sub>P,P</sub>

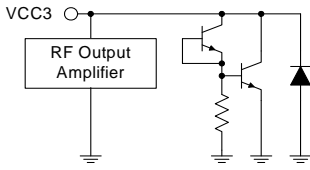
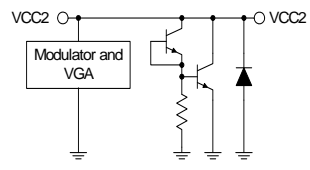
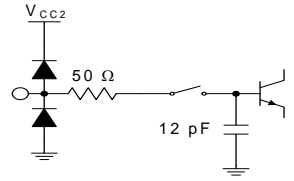
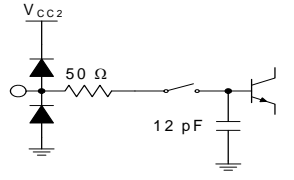
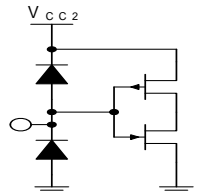
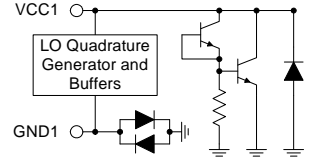
\* = Not tested in production

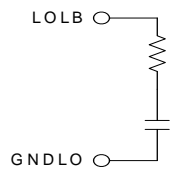
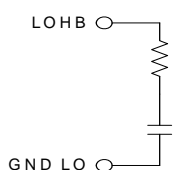
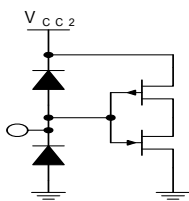
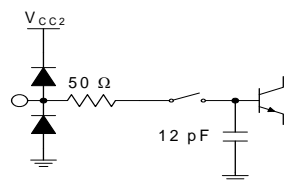
### Mode Truth Table

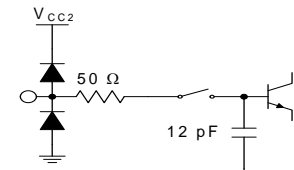
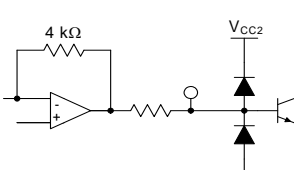
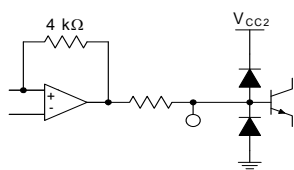
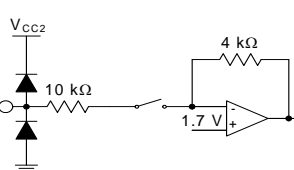
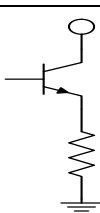
Mode	ENABLE	BAND SEL	Condition
Sleep	0	X	I/Q and GC inputs go open circuit through the use of a FET switch in sleep mode
High Band Mode	1	1	LO input LO HB RF output = RF OUT HB
Low Band Mode	1	0	LO input LO LB RF output = RF OUT LB

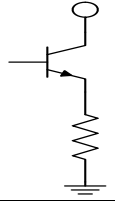



**Pin Names and Descriptions**

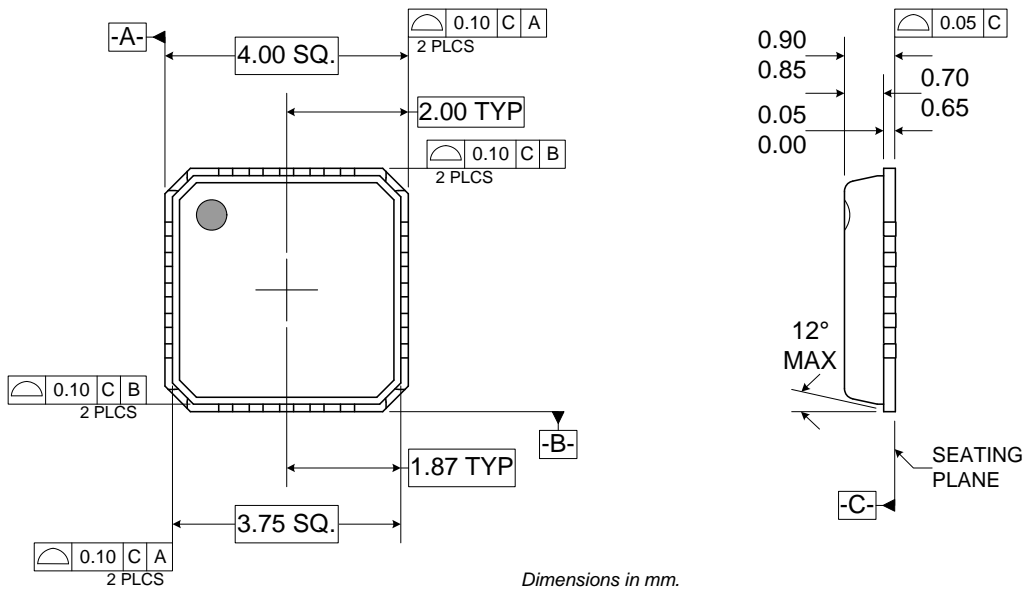
Pin	Function	Description	Interface Schematic
1	VCC3	Supply for RF output circuits.	
2	VCC2	Supply for modulator and biasing circuits.	
3	ISIG P	In phase I channel positive baseband input port. Best performance is achieved when the ISIGP and ISIGN are driven differentially. The recommended CW differential drive level ( $V_{ISIGP}-V_{ISIGN}$ ) is 800mV <sub>P-P</sub> . This input should be DC-biased at 1.2V±0.05V. The common-mode DC coltage on the ISIGP and ISIGN input signals is used to bias the modulator. In sleep mode an internal FET switch is opened, the input goes high impedance and the modulator is de-biased. The input impedance is typically 5.5kΩ at low frequencies and at higher frequencies can be modeled as 50Ω in series with 12pF to ground.	
4	ISIG N	In phase I channel negative baseband input port. See ISIGP.	
5	ENABLE	Enables power to the device. CMOS input. Logic 1 (1.4V to VCC)=Enabled. Logic 0 (0V to 0.5V)=Powered Down.	
6	VCC1	Supply for the LO buffers and quadrature network. The sideband suppression is a function of the VCC1 voltage. The inclusion of R3 (39Ω) lowers the voltage on VCC1 by around 400mV and results an improvement in sideband suppression but around a 0.2dB increase in noise at 20MHz offset.	

Pin	Function	Description	Interface Schematic
7	LOLB	Local oscillator input low band. This input is biased internally at around 1.6V when the chip is in low band mode and 0V when the chip is in high band mode or powered down. The LO signal typically needs to be AC coupled. The noise performance, carrier suppression at low output powers and side-band suppression are all a function of LO power. The optimum LO power is between 0dBm and 3dBm. The device will work with LO powers as low as -20dBm however this is at the expense of higher noise performance at high output powers and poorer sideband suppression.	
8	GND LO	Ground return for the local oscillator input signals. The GND LO pin is effectively the complementary LO input for both the high band and low band LO signals. It has significant amounts of LO signal flowing through it. This pin is brought out as an independent ground to enable the PCB board designer to isolate the LO return from the RF outputs ground and the general chip ground. It is recommended that this ground is kept isolated from the die flag ground. Any connections between the GND LO and any other ground should be made through a ground plane.	See pins 7 and 9.
9	LOHB	Local oscillator input high band. This input is biased internally at around 1.6V when the chip is in high band mode and 0V when the chip is in low band mode or powered down. The LO HB signal typically needs to be AC coupled. The noise performance, carrier suppression at low output powers and side-band suppression are all a function of LO power. The optimum LO power is between 0dBm and 3dBm. The device will work with LO powers as low as -20dBm however this is at the expense of higher noise performance at high output powers and poorer sideband suppression.	
10	GND1	Ground for LO buffers.	See pin 6.
11	BAND SEL	Band select input to define active mode. CMOS input. Logic 1 (1.4V to VCC)=High band mode. Logic 2 (0V to 0.5V)=Low band mode.	
12	QSIG N	Quadrature channel negative baseband input port. See QSIGP.	

Pin	Function	Description	Interface Schematic
13	QSIG P	<p>Quadrature Q channel positive baseband input port. Best performance is achieved when the ISIGP and ISIGN are driven differentially. The recommended CW differential drive level (<math>V_{QSIGP} - V_{QSIGN}</math>) is 800mV<sub>P-P</sub>.</p> <p>This input should be DC-biased at 1.2V±0.05V. The common-mode DC voltage on the QSIGP and QSIGN input signals is used to bias the modulator. In sleep mode an internal FET switch is opened, the input goes high impedance and the modulator is de-biased. The input impedance is typically 5.5kΩ at low frequencies and at higher frequencies can be modeled as 50Ω in series with 12pF to ground.</p> <p>Phase or amplitude errors between the QSIGP and QSIGN signals which may result in an increase in the even order distortion of the modulation in the output spectrum.</p> <p>DC offsets between the QSIGP and QSIGN signals will result in an increased carrier leakage. Small DC offsets may be deliberately applied between the ISIGP/ISIGN and QSIGP/QSIGN inputs to cancel out the LO leakage. The optimum corrective DC offsets will change with mode, frequency and gain control.</p> <p>Common-mode noise on the QSIGP and QSIGN should be kept low as it may degrade the noise performance of the modulator.</p> <p>Phase offsets may be applied between the I and Q channels to improve the sideband suppression performance.</p>	
14	VREF	<p>Voltage reference decouple with an external 10nF capacitor to ground. The voltage on this pin is typically 1.67V when the chip is enabled. The voltage is 0V when the chip is powered down.</p> <p>The purpose of this decoupling capacitor is to filter out low frequency noise (20MHz) on the gain control lines.</p> <p>Poor positioning of the VREF decoupling capacitor can cause a degradation in LO leakage.</p> <p>A voltage of around 2.5V on this pin indicates that the die flag under the chip is not grounded and the chip is not biased correctly.</p>	
15	GC DEC	<p>Voltage reference decouple with an external 1nF decoupling capacitor to ground.</p> <p>The voltage on this pin is a function of gain control (GC) voltage when the chip is enabled. The voltage is 0V when the chip is powered down.</p> <p>The purpose of this decoupling capacitor is to filter out low frequency noise (20MHz) on the gain control lines. The size of the capacitor on the GC DEC line will effect the settling time response to a change in gain control voltage. A 1nF capacitor equates to around 200ns settling time and a 0.5nF capacitor equates to a 100ns settling time. There is a trade-off between settling time and noise contributions by the gain control circuitry as gain control is applied.</p> <p>Poor positioning of the VREF decoupling capacitor can cause a degradation in LO leakage.</p>	
16	GC	<p>Gain control voltage. Maximum output power at 2.0V. Minimum output power at 0V. When the chip is enabled the input impedance is 10kΩ referred to 1.7V<sub>DC</sub>. When the chip is powered down a FET switch is opened and the input goes high impedance.</p>	
17	RF OUT LB	<p>RF low band output. Open collector output. The output should be biased at VCC through an inductor that can be used to form part of an output matching circuit.</p> <p>In our proposed applications circuit some power is dissipated in R6 (130Ω) which appears as a de-Qing resistor in parallel with the output inductor L4. If R6 is eliminated and the RFOUT LB pin is re-matched to 50Ω it is possible to get approximately 5dB extra power out of the device in low band mode.</p>	
18	GND2	Ground for RF output sections.	

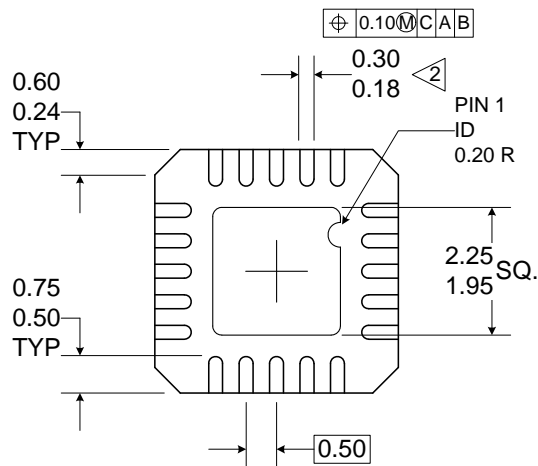
Pin	Function	Description	Interface Schematic
19	RF OUT HB	RF high band output. Open collector output. The output should be biased at VCC through an inductor that can be used to form part of an output matching circuit. In our proposed applications circuit some power is dissipated in R4 (180Ω) which appears as a de-Qing resistor in parallel with the output inductor L3. If R4 is eliminated and the RFOUT HB pin is re-matched to 50Ω it is possible to get approximately 3dB extra power out of the device in high band mode.	
20	GND3	Ground for RF output sections.	
Die Flag	GND4	Ground for modulator, variable gain amplifier and substrate.	

## Package Drawing



### NOTES:

- Shaded lead is Pin 1.
- Dimension applies to plated terminal: to be measured between 0.20 mm and 0.25 mm from terminal end.



## Application Notes

The baseband inputs must be driven with balanced differential signals. We suggest amplitude and phase matching  $<0.5\text{dB}$  and  $<0.5^\circ$ . Phase or gain imbalances between the complementary input signals will cause additional distortion including some second order baseband distortion.

The common-mode voltage on the baseband inputs should be well controlled at 1.2V. We suggest that the common-mode DC voltage be  $1.2\text{V} \pm 0.05\text{V}$ . The common-mode DC voltage is used to bias the modulator; hence, deviations from 1.2V will result in changes in the current consumption, noise and intermodulation performance.

The chip is designed to be driven with a single-ended LO signal.

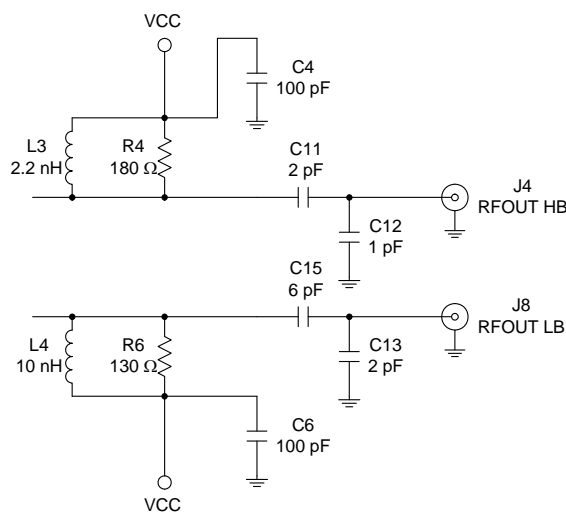
The GC DEC and VREF output pins should be decoupled to ground. We recommend a 10nF capacitor on VREF, and a 1nF capacitor on GC DEC. The purpose of this capacitor is to filter out low frequency noise (20MHz) in the gain control lines, which may cause noise on the RF signal. The capacitor on the GC DEC line will effect the settling time response to a change in power control voltage. A 1nF capacitor equates to around a 200ns settling time, and a 0.5nF capacitor equates to a 100ns settling time. There is a trade-off between settling time and phase noise as you start to apply gain control.

The ground lines for the LO sections, GNDLO and GND1, are brought out of the chip independently from the ground to the RF and modulator sections. This isolates the LO signals from the RF output sections.

The GND LO pin is effectively the complementary LO input for both the high band and low band LO signals. It has significant amounts of LO signal flowing through it. This is brought out as an independent ground to try to enable the PCB board designer to isolate the LO return from the RF output sections and general chip ground.

The RF output ports of the RF2483 consist of open collector architecture and require pull up inductors to the supply voltage. This, in conjunction with a DC blocking capacitor provides a simple, broadband L-match network as shown in the schematic diagram. A shunt resistor is included to control the Q of the matching network and set the modulator output power. In this case, both outputs were designed to provide 0dBm.

An alternate output match containing a third harmonic trap was evaluated. This circuit uses a tapped-C matching network, whereby the shunt C provides a low impedance path near the third harmonic frequency. Although an additional component is required, the benefit of suppressing the third harmonic distortion may improve overall system intermodulation. This network has been shown to provide better than 20dB of improved suppression in high-band mode.



**Figure 1. Alternate RF output match with third-harmonic suppression.**

## High Band LOHB (S11) and RFHB (S22) Parameters

( $V_{CC}=2.7V$ ,  $V_{GC}=2.0V$ , Band Sel=2.7V, EN=2.7V,  $T=+25^{\circ}C$ )

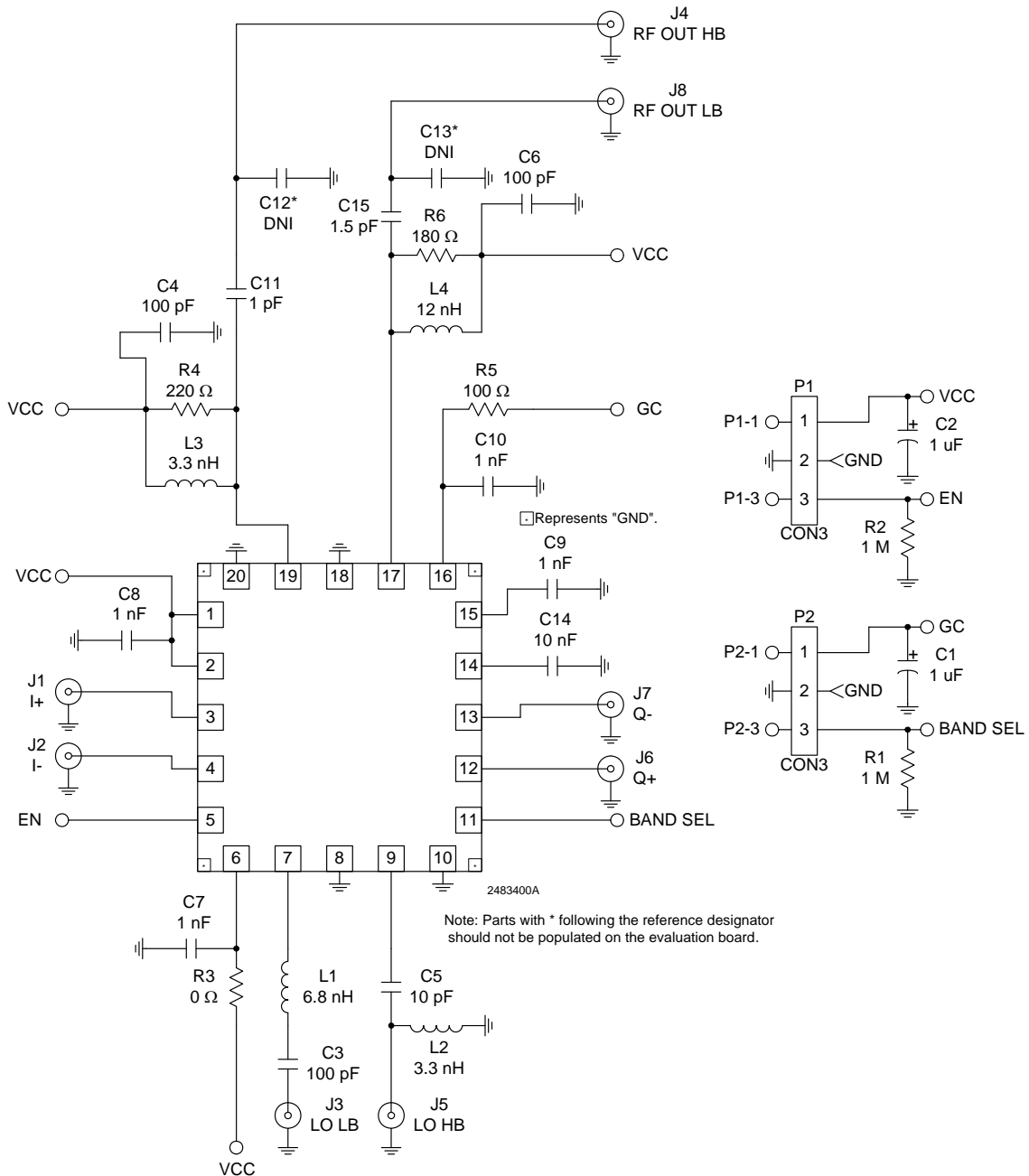
Freq. (MHz)	S11 MAG	S11 ANG	S22 MAG	S22 ANG
1700	0.478	-110.8	0.903	-55.0
1750	0.469	-112.4	0.901	-56.2
1800	0.465	-115.1	0.902	-57.2
1850	0.472	-117.2	0.902	-58.0
1900	0.476	-117.6	0.904	-59.0
1950	0.465	-118.4	0.905	-59.6
2000	0.457	-120.8	0.906	-60.3
2050	0.452	-122.6	0.909	-60.9
2100	0.464	-123.0	0.916	-61.9
2150	0.453	-123.4	0.914	-64.0
2200	0.442	-125.4	0.879	-64.5

## Low Band LOLB (S11) and RFLB (S22) Parameters

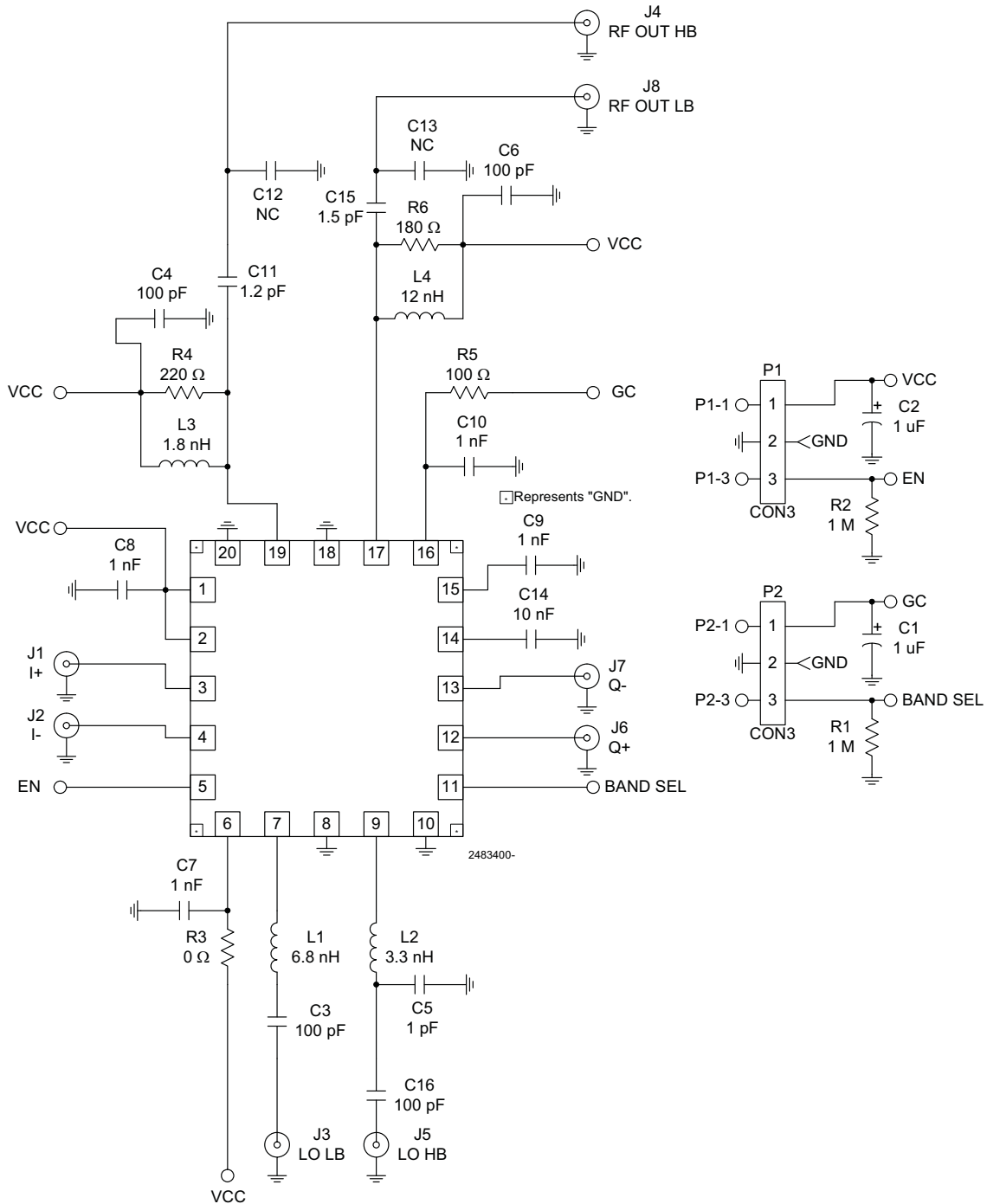
( $V_{CC}=2.7V$ ,  $V_{GC}=2.0V$ , Band Sel=0V, EN=2.7V,  $T=+25^{\circ}C$ )

Freq. (MHz)	S11 MAG	S11 ANG	S22 MAG	S22 ANG
700	0.468	-63.2	0.92	-9.9
750	0.452	-67.6	0.915	-11.3
800	0.437	-72.1	0.913	-12.6
850	0.425	-76.6	0.908	-14.0
900	0.414	-81.2	0.905	-15.6
950	0.407	-85.6	0.901	-17.1
1000	0.402	-89.8	0.898	-18.8

**Evaluation Board Schematic**  
(700MHz to 1000MHz Low Band)  
(1700MHz to 2200MHz High Band)

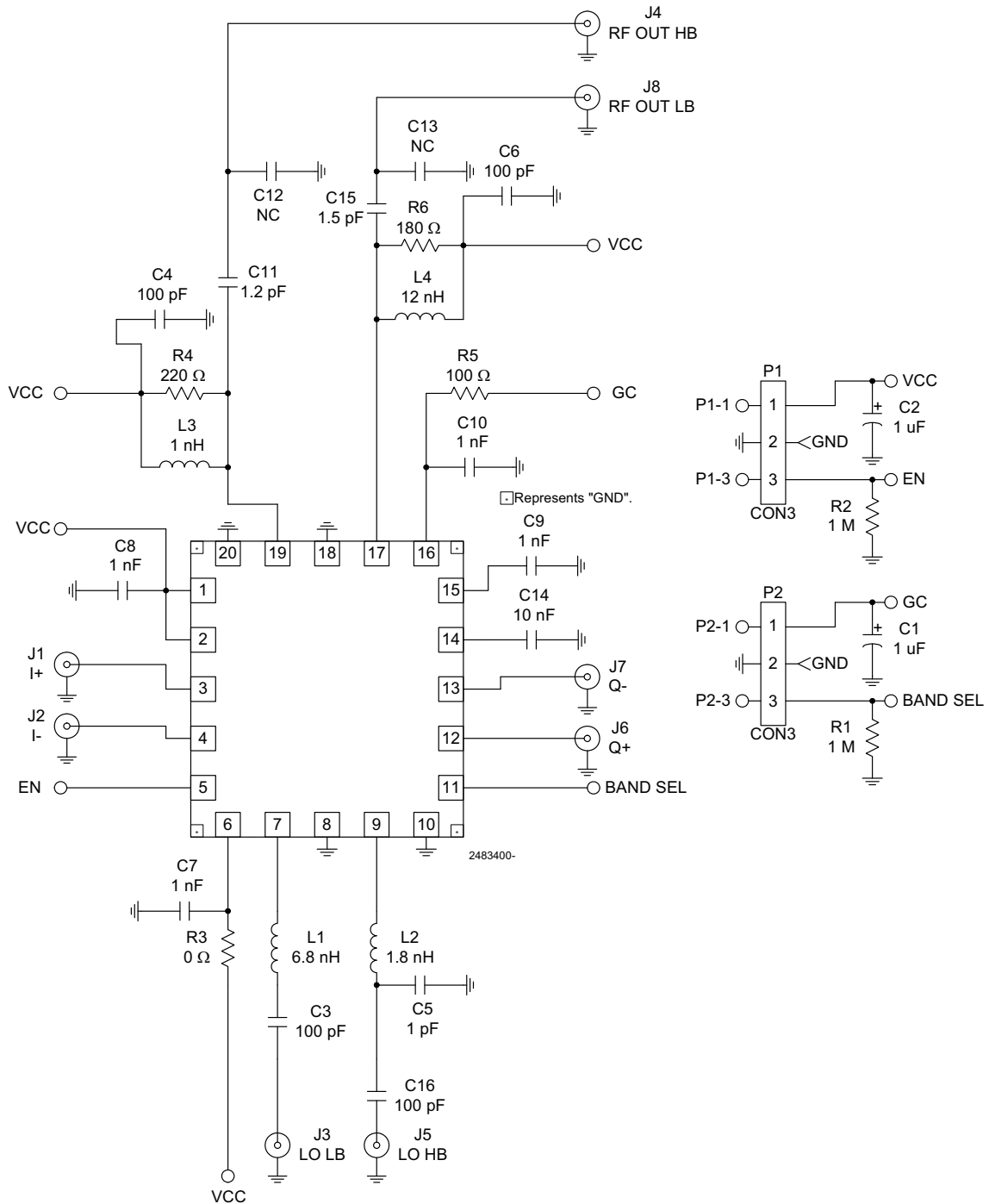


## Evaluation Board Schematic (2400MHz - High Band Tune Only)





**Evaluation Board Schematic**  
(2700MHz - High Band Tune Only)



**Evaluation Board Build of Materials (BOM)**(700MHz to 1000MHz Low Band)  
(1700MHz to 2200MHz High Band)

Description	Reference Designator	Manufacturer	Manufacturer's P/N
PCB, 2483		DYNAMIC DETAILS CANADA, INC.	RF2483410(B)
	U1	RFMD	RF2483SB
RES, 1M, 5%, 1/16W, 0402	R1, R2	PANASONIC INDUSTRIAL CO	ERJ-2GEJ105
RES, 0 $\Omega$ , 0402	R3	PANASONIC INDUSTRIAL CO	ERJ-2GEOR00
RES, 100 $\Omega$ , 5%, 1/16W, 0402	R5	PANASONIC INDUSTRIAL CO	ERJ-2GEJ101
RES, 180 $\Omega$ , 5%, 1/16W, 0402	R6	PANASONIC INDUSTRIAL CO	ERJ-2GEJ181
RES, 220 $\Omega$ , 5%, 1/16W, 0402	R4	PANASONIC INDUSTRIAL CO	ERJ-2GEJ221
CAP, 1000pF, 10%, 25V, X7R, 0402	C7, C8, C9, C10	PANASONIC INDUSTRIAL CO	ECJ-0EB1E102K
CAP, 1pF, +/-0.25pF, 50V, COG, 0402	C11	PANASONIC INDUSTRIAL CO	ECJ-0EC1H010C
CAP, 1.5pF, +/-0.25pF, 50V, COG, 0402	C15	PANASONIC INDUSTRIAL CO	ECJ-0EC1H1R5C
CAP, 10000pF, 10%, 16V, X7R, 0402	C14	PANASONIC INDUSTRIAL CO	ECJ-0EB1C103K
CAP, 10pF, +/-0.5pF, 50V, COG, 0402	C5	PANASONIC INDUSTRIAL CO	ECJ-0EC1H100D
CAP, 100pF, 5%, 50V, COG, 0402	C3, C4, C6	PANASONIC INDUSTRIAL CO	ECJ-0EC1H101J
CAP, 1uF, 20%, 25V, TANT-A	C1, C2	AVX Corporation	TAJA105M025R
IND, 3.3nH, +/-0.3nH, M/L, 0402	L2, L3	Taiyo Yuden (USA), Inc.	LG HK10053N3S-T
IND, 6.8nH, 5%, M/L, 0402	L1	Taiyo Yuden (USA), Inc.	LG HK10056N8J-T
IND, 12nH, 5%, M/L, 0402	L4	Taiyo Yuden (USA), Inc.	LG HK100512NJ-T
NOT POPULATED ITEM-1 FOR PCBA BOM	C12*, C13*		DUMMY PART
CONN, HDR, ST, PLRZD, 3-PIN, 0.100"	P1, P2	ITW Pancon	MPSS100-3-C
CONN, SMA END LNCH, MINI, RND, 0.062"	J1, J2, J3, J4, J5, J6, J7, J8	JOHNSON COMPONENTS, INC.	142-0711-821

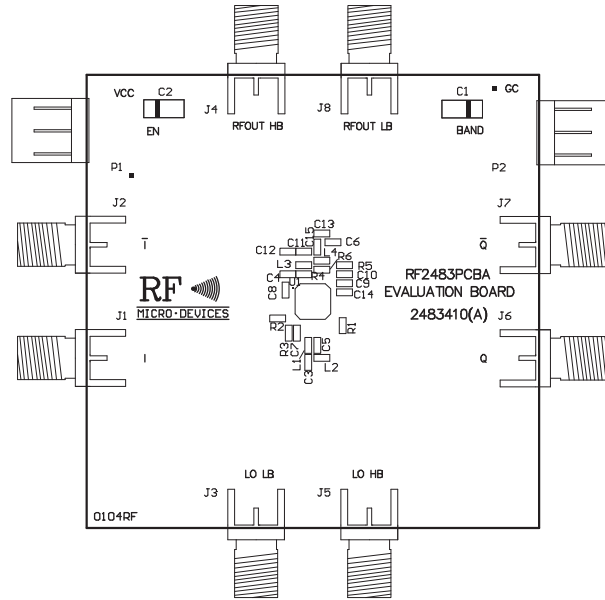
## Notes:

1. Parts with \* following the Reference Designator should not be populated on PCBA.
2. RFMD devices (DUT) may require baking per IPC/JEDEC J-STD-020 for a minimum of 24 hours at 125 +/-0 deg C. Assembly must take place within 12 hours of bake completion.
3. Manufacturers' P/Ns are subject to change by the manufacturers following the issue of this document and are thereby included for reference only. Contact RFMD Corporate Engineering Materials with questions regarding specific Manufacturers' P/Ns.

**Evaluation Board Assembly Layout**

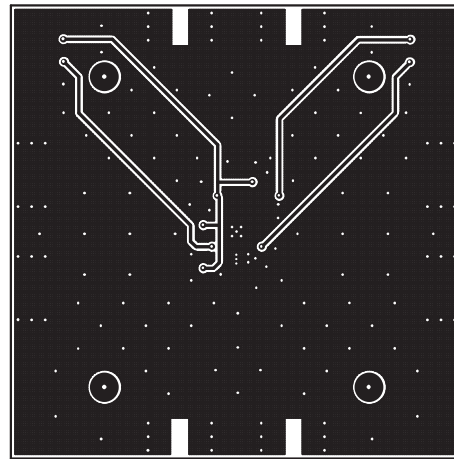
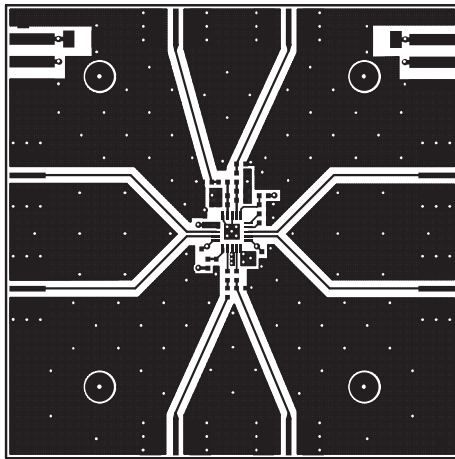
(Board Size 2.0" x 2.0")

Board Thickness 0.062", Board Material FR-4, Multi-Layer



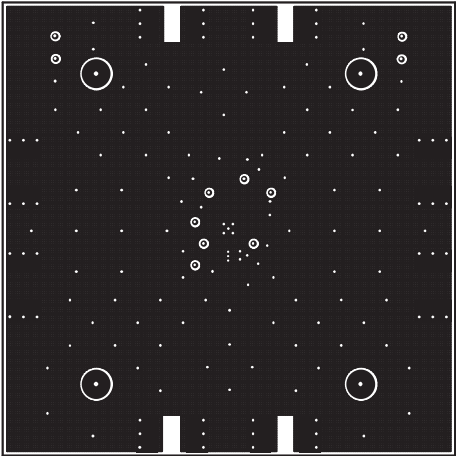
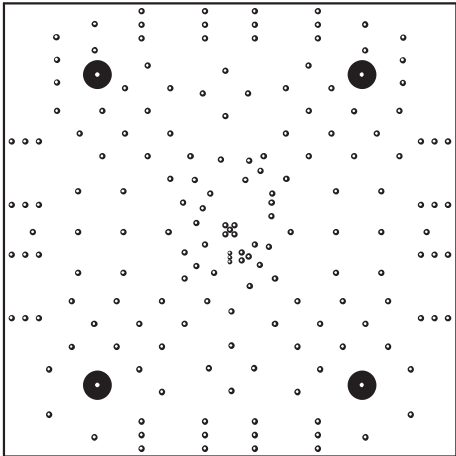
Top

Inner 1

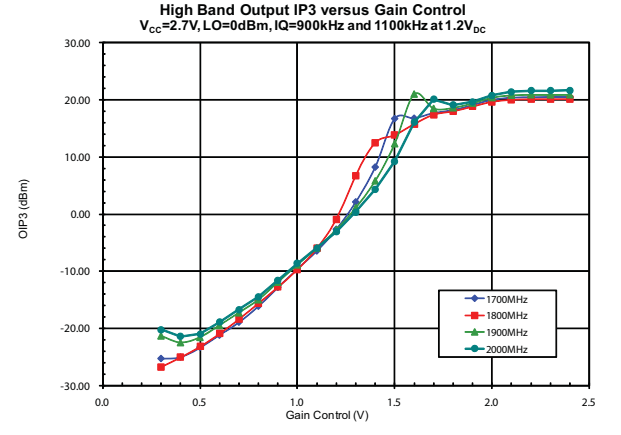
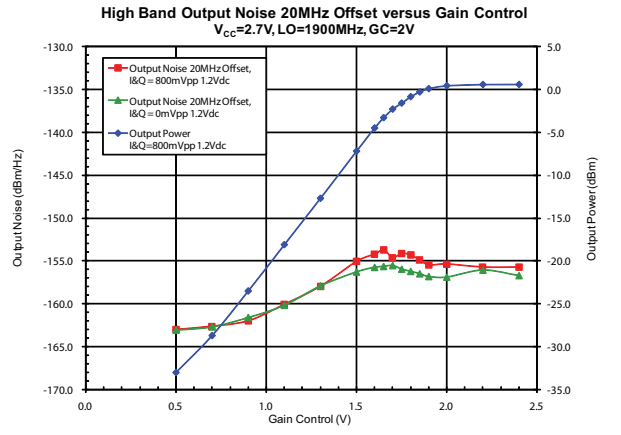
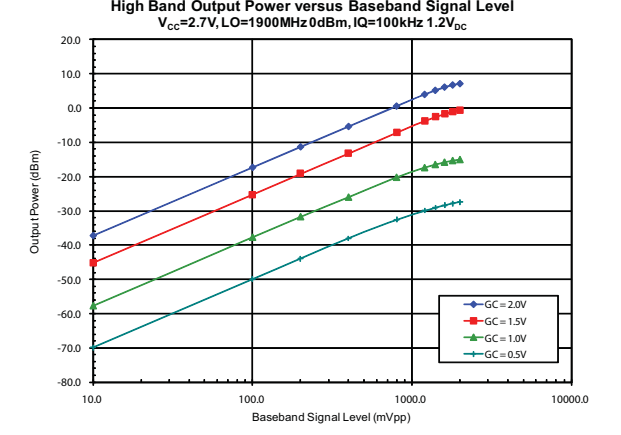
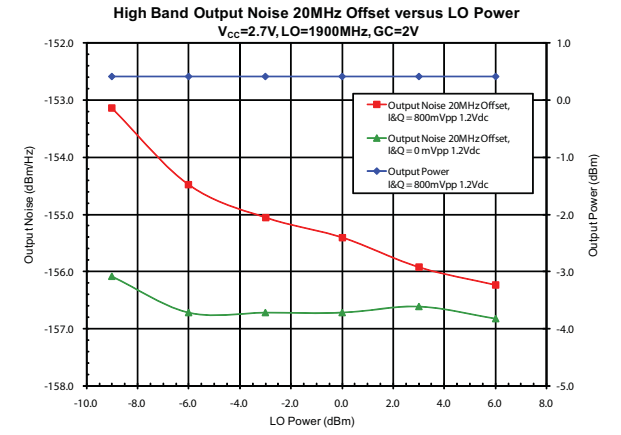
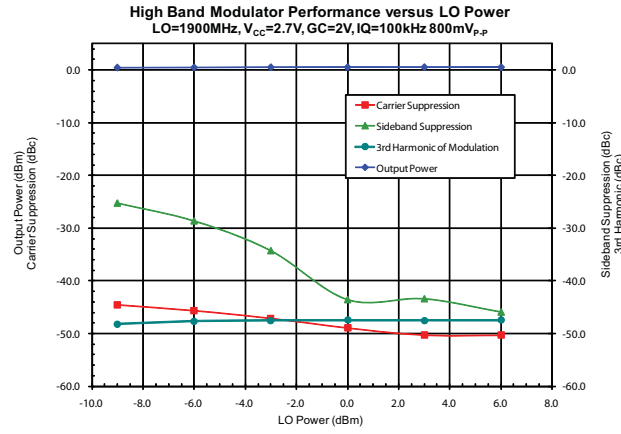
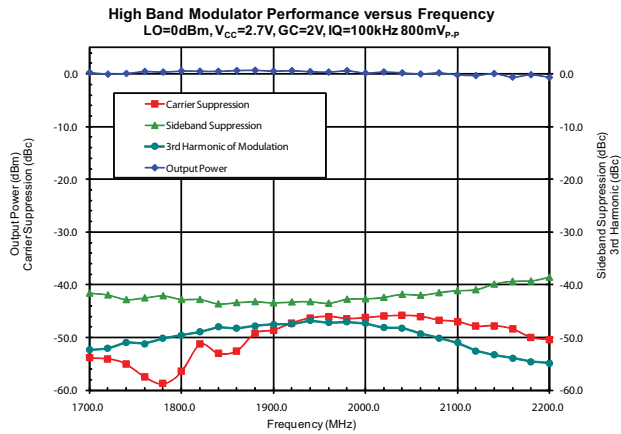


Inner 2

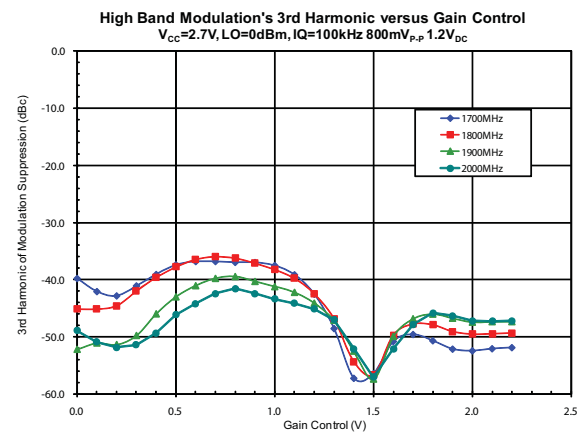
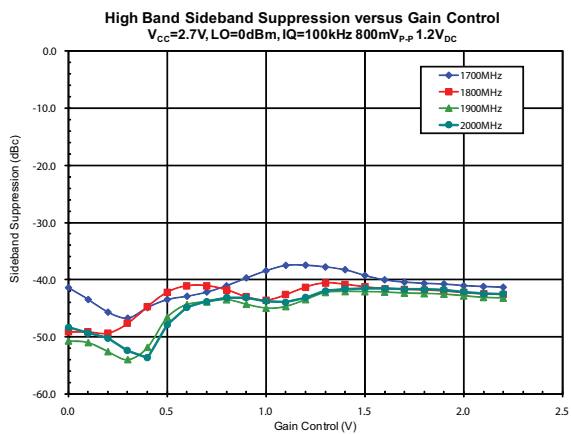
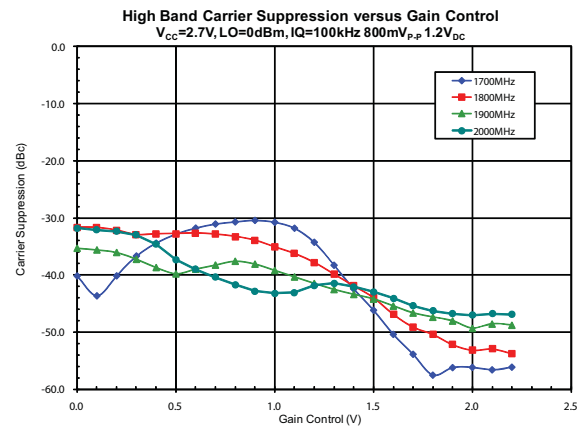
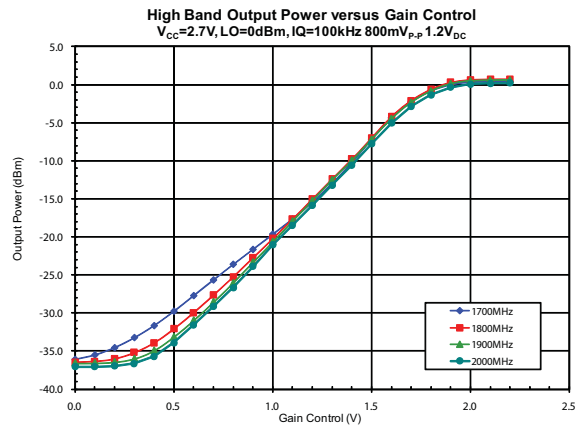
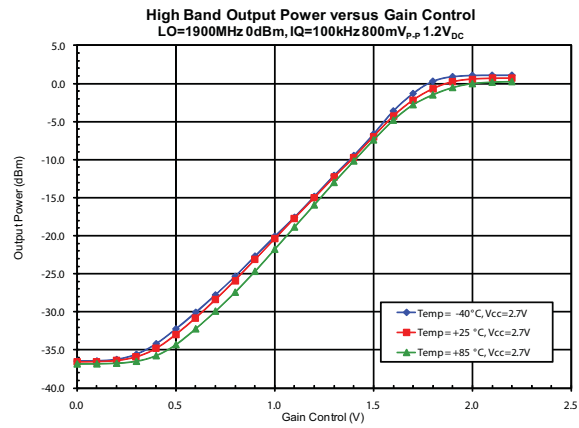
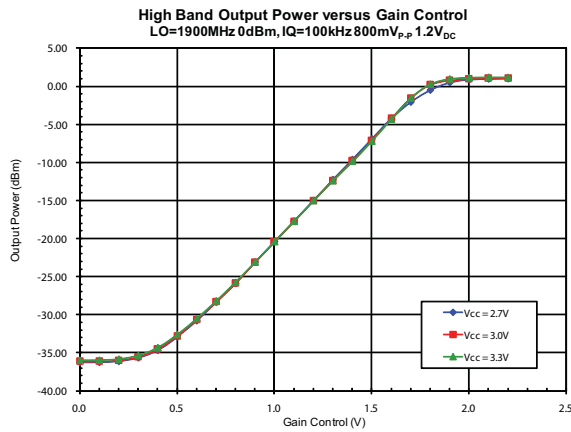
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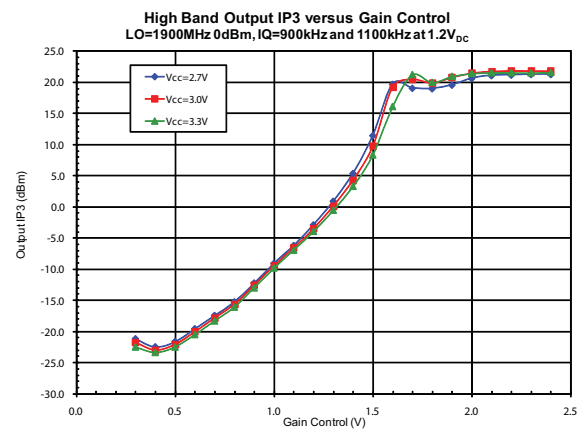
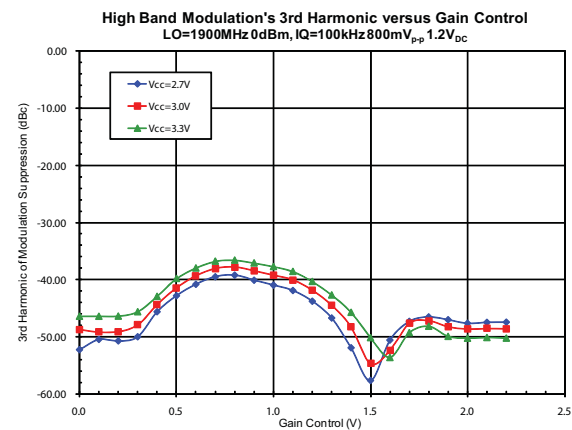
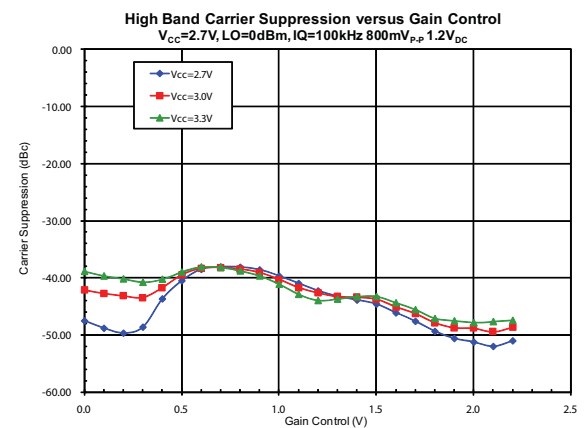
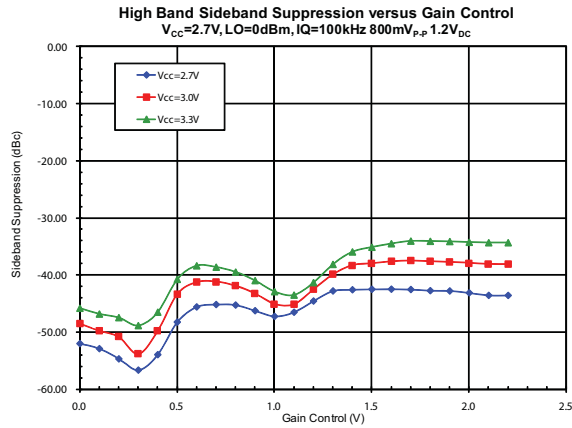
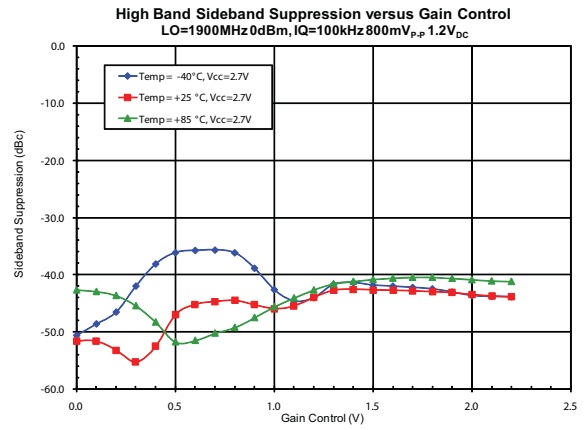
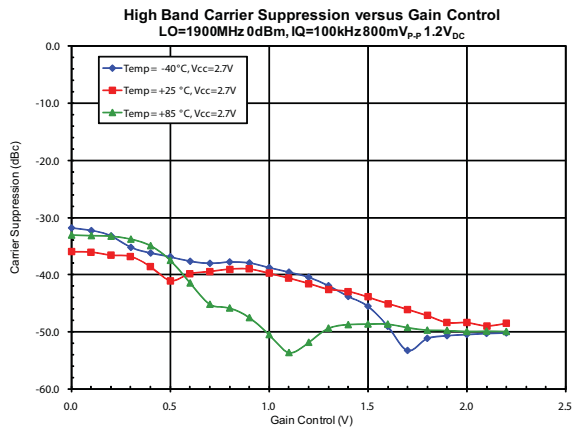
### Typical Performance: 1700MHz to 2200MHz Application Circuit



## Typical Performance: 1700MHz to 2200MHz Application Circuit

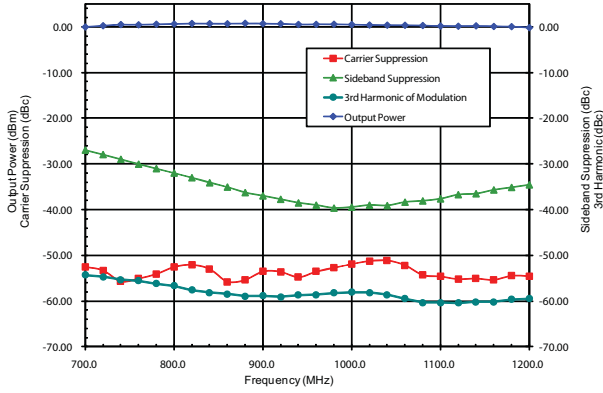


## Typical Performance: 1700MHz to 2400MHz Application Circuit

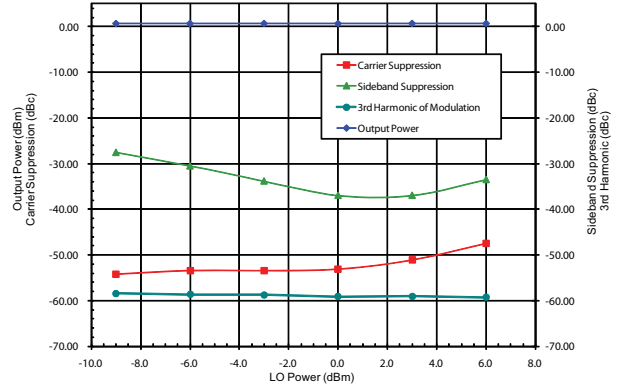


## Typical Performance: 700MHz to 1000MHz Application Circuit

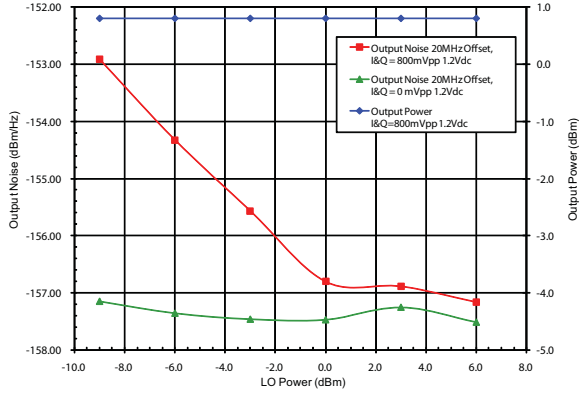
**Low Band Modulator Performance versus Frequency**  
 LO=0dBm, V<sub>CC</sub>=2.7V, GC=2V, IQ=100kHz 800mV<sub>p-p</sub>



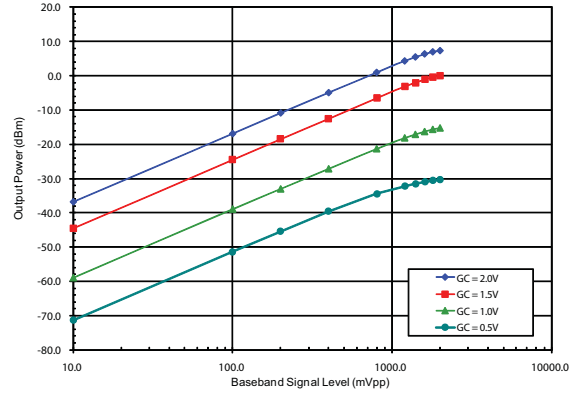
**Low Band Modulator Performance versus LO Power**  
 LO=900MHz, V<sub>CC</sub>=2.7V, GC=2V, IQ=100kHz 800mV<sub>p-p</sub>



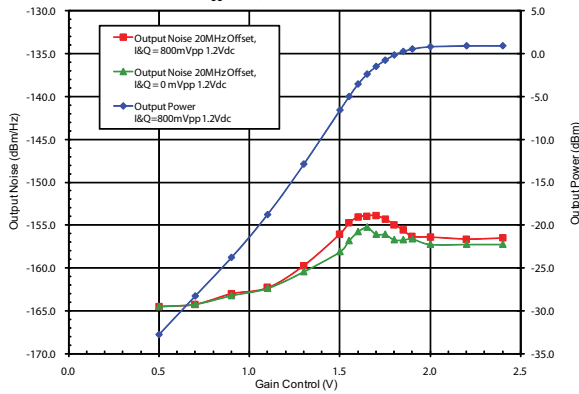
**Low Band Output Noise 20MHz Offset versus LO Power**  
 V<sub>CC</sub>=2.7V, LO=900MHz, GC=2V



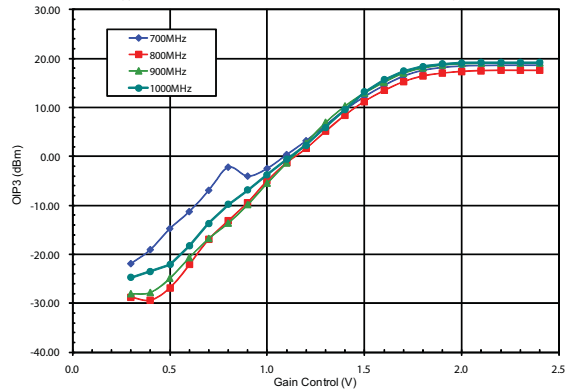
**Low Band Output Power versus Baseband Signal Level**  
 V<sub>CC</sub>=2.7V, LO=900MHz, IQ=100kHz 1.2V<sub>DC</sub>



**Low Band Output Noise at 20MHz Offset versus GC**  
 V<sub>CC</sub>=2.7V, LO=900MHz 0dBm

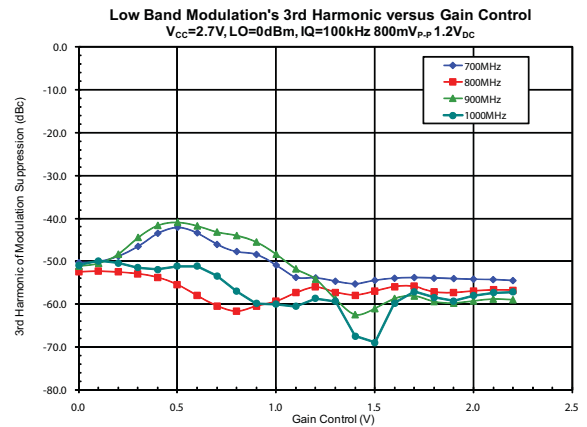
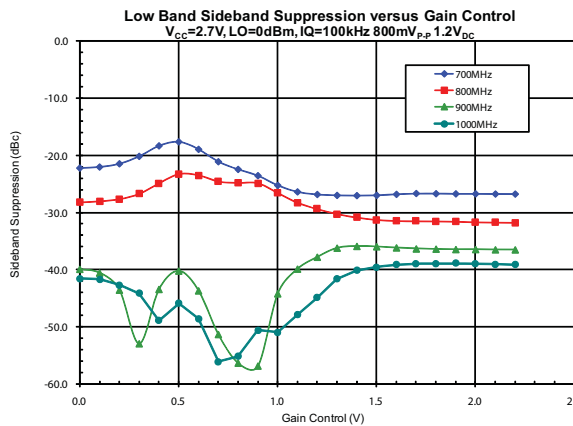
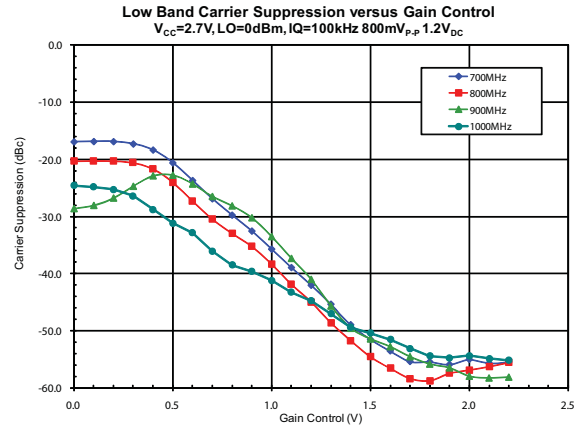
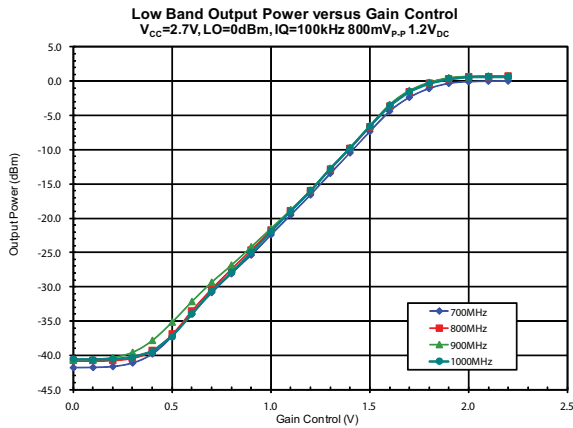
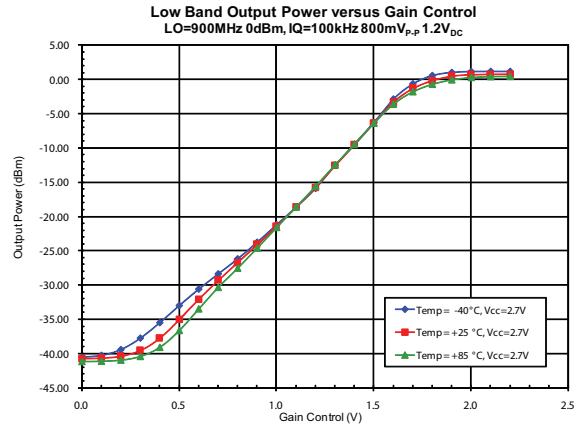
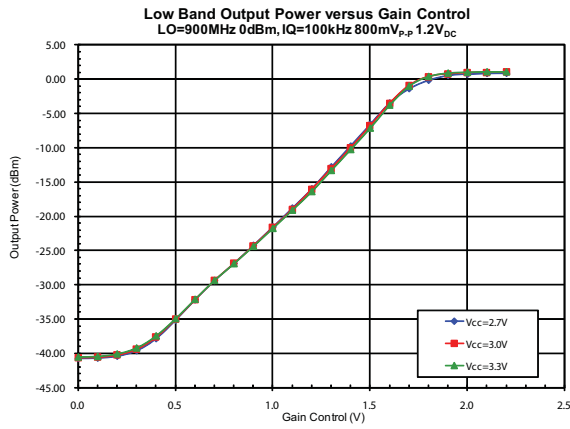


**Low Band Output IP3 versus Gain Control**  
 V<sub>CC</sub>=2.7V, LO=0dBm, IQ=900kHz and 1100kHz at 1.2V<sub>DC</sub>

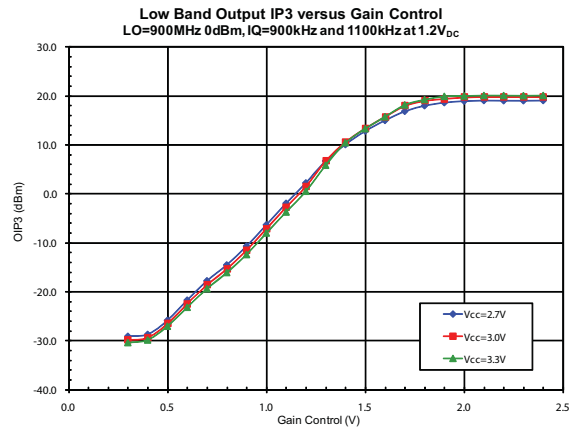
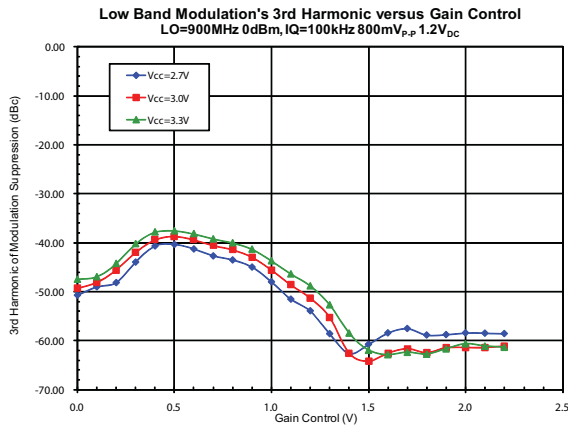
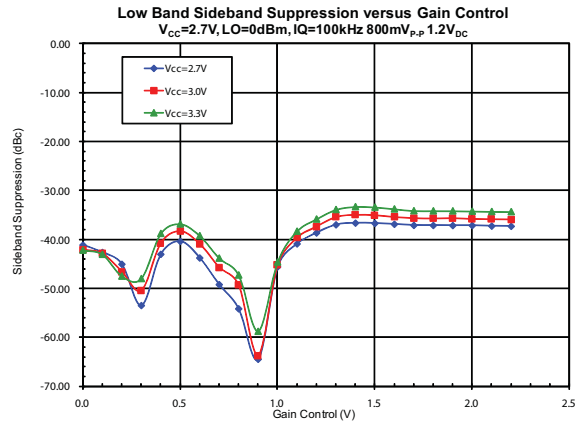
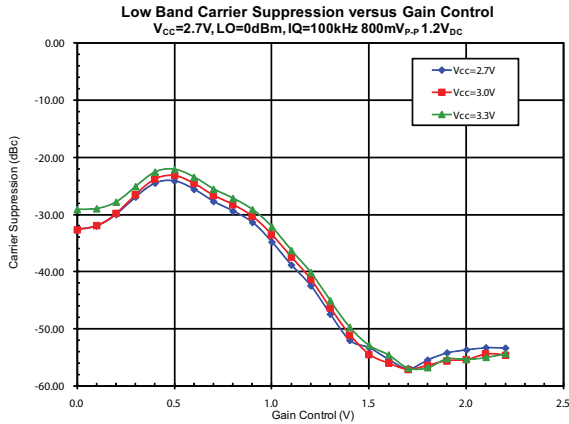
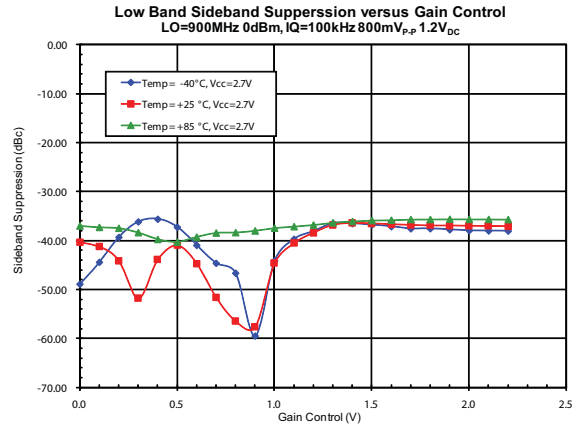
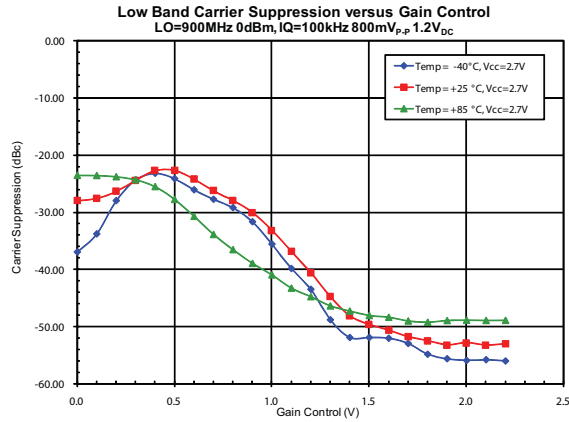




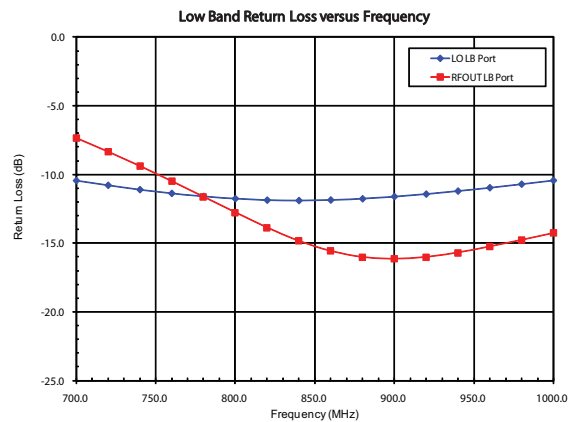
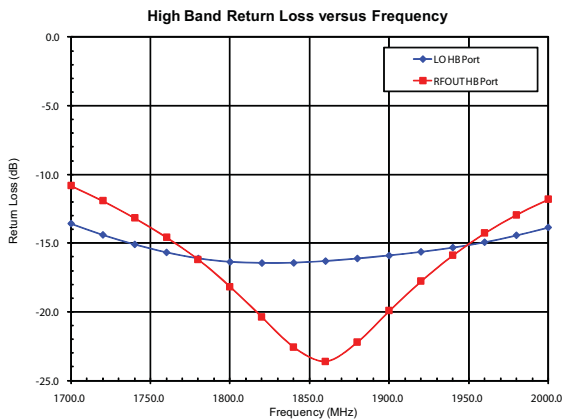
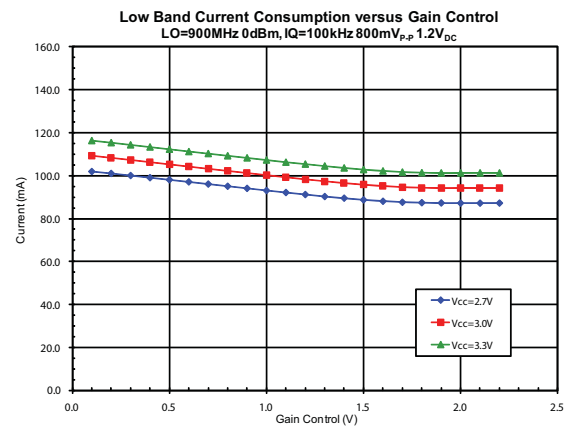
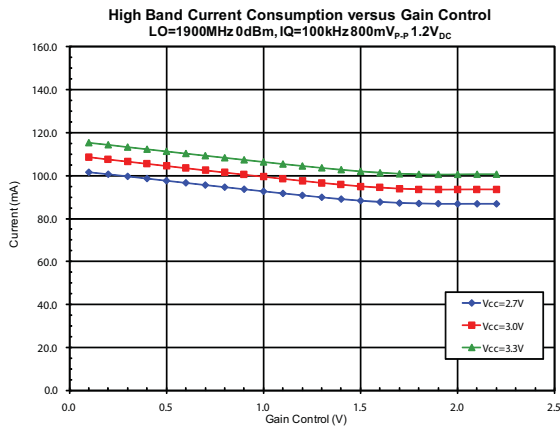
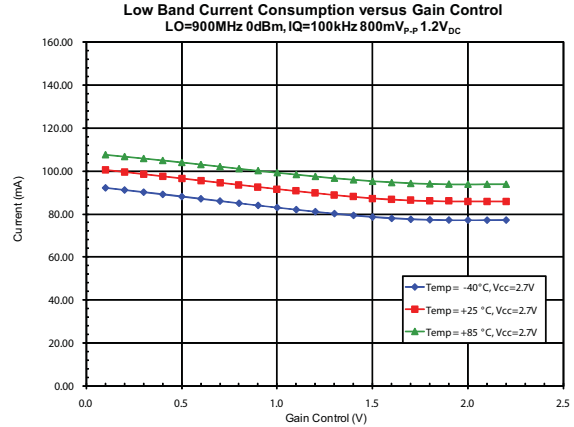
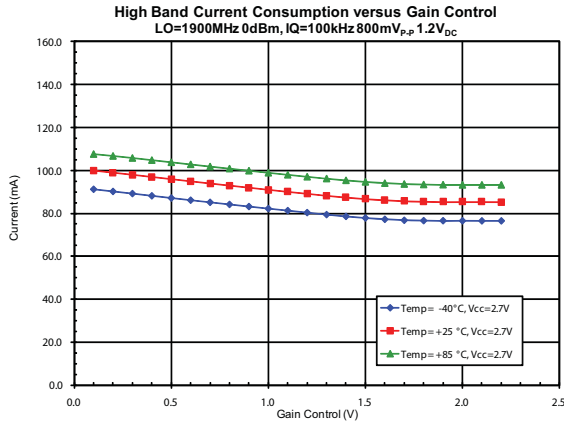
## Typical Performance: 700MHz to 1000MHz Application Circuit



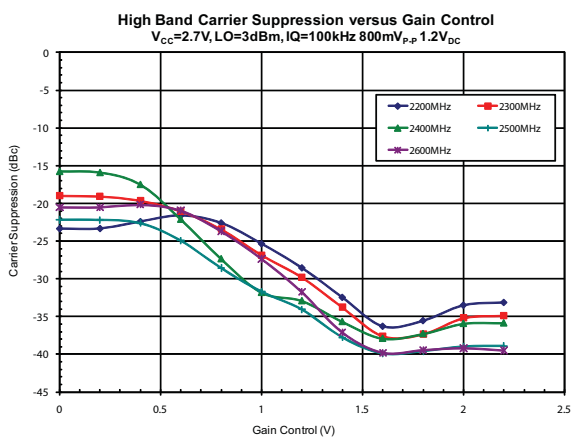
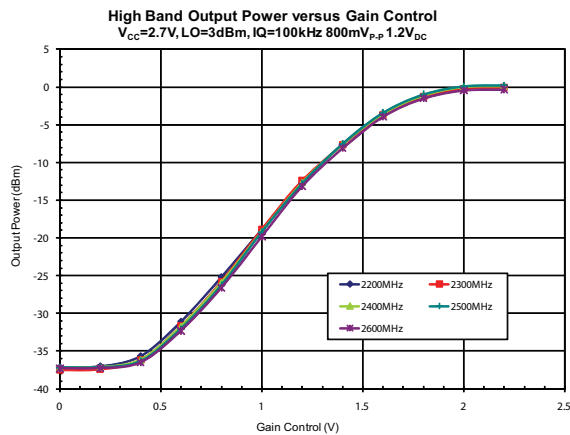
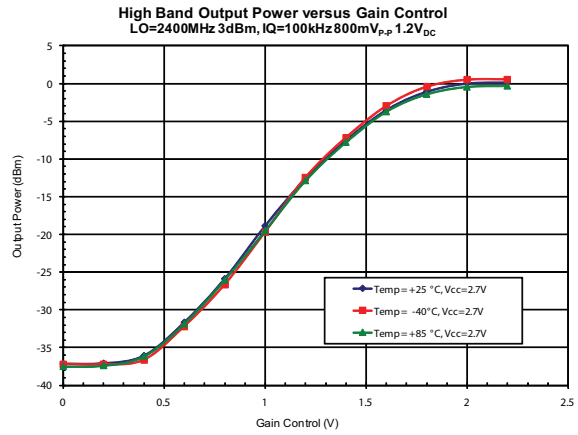
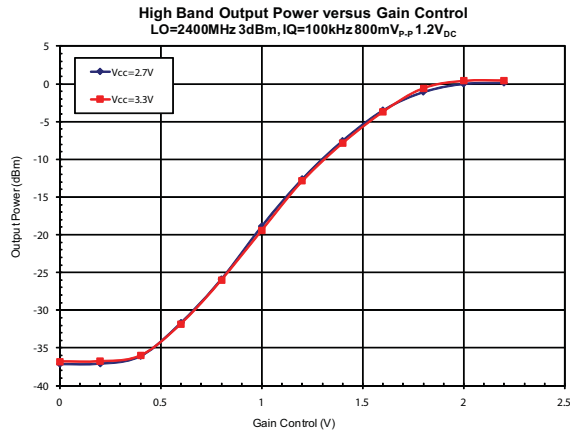
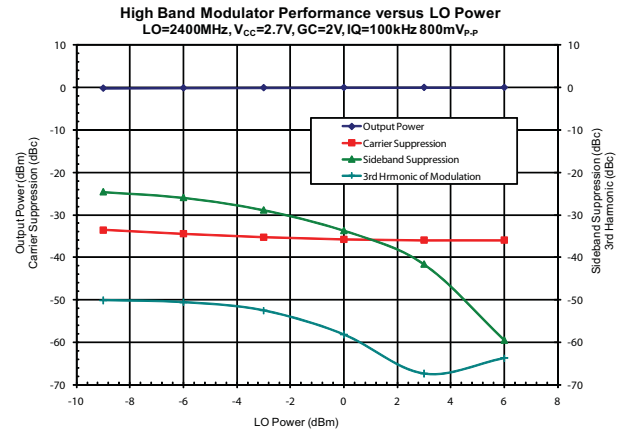
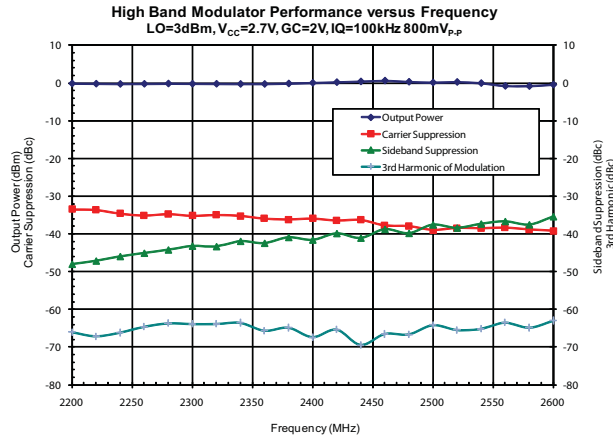
## Typical Performance: 700MHz to 1000MHz Application Circuit



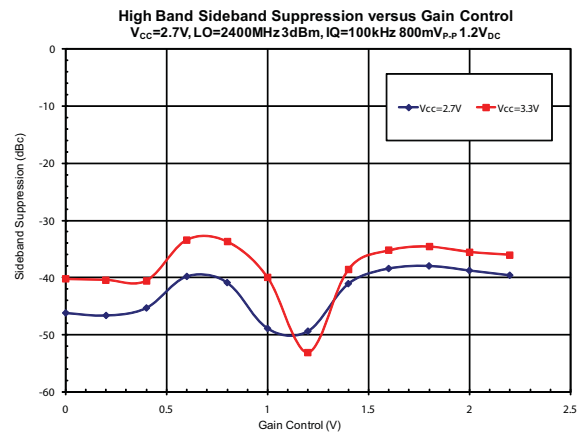
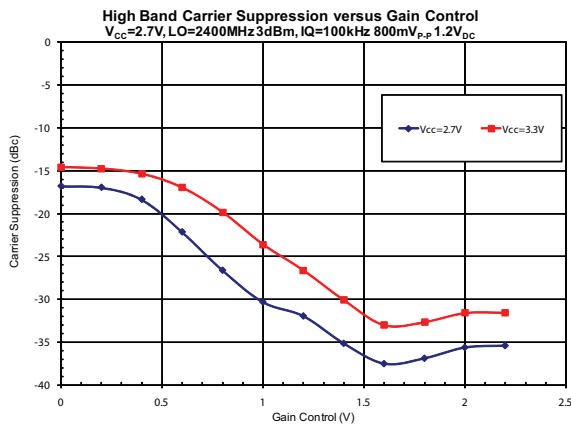
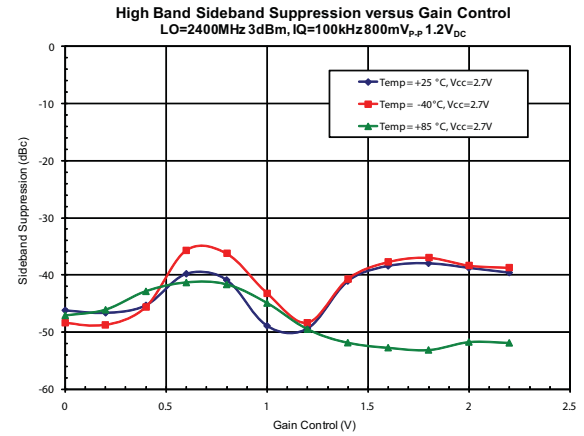
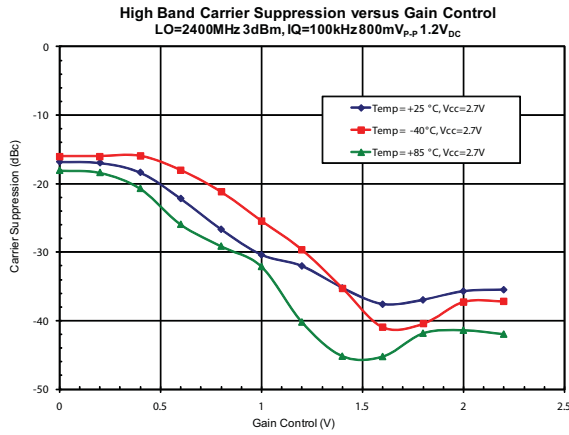
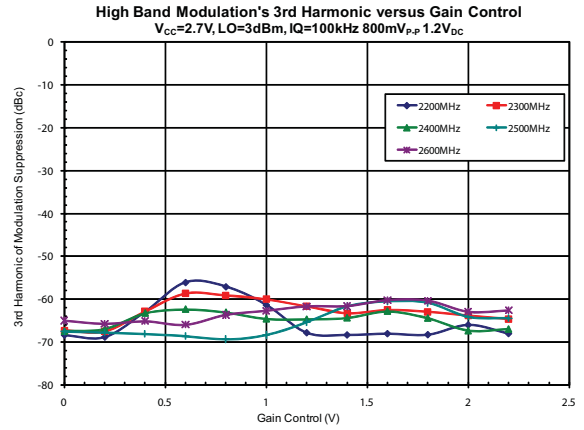
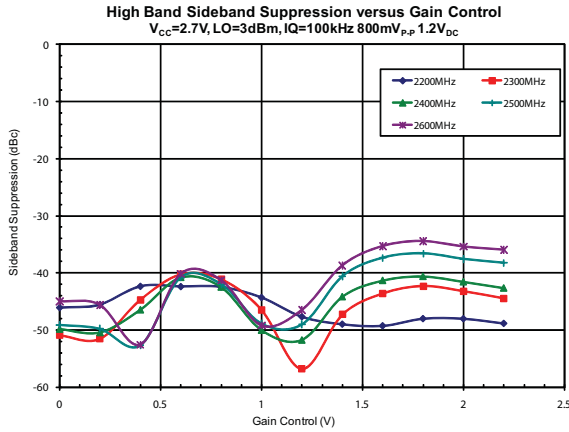
**Typical Performance: 700MHz to 1000MHz Application Circuit for Low Band;  
1700MHz to 2200MHz Application Circuit for High Band**



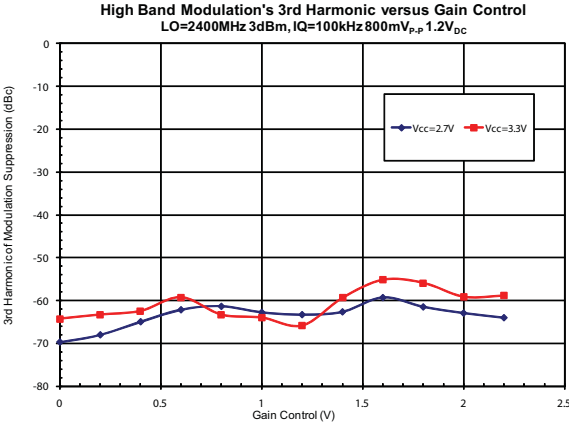
## Typical Performance: 2400MHz Application Circuit



## Typical Performance: 2400MHz Application Circuit

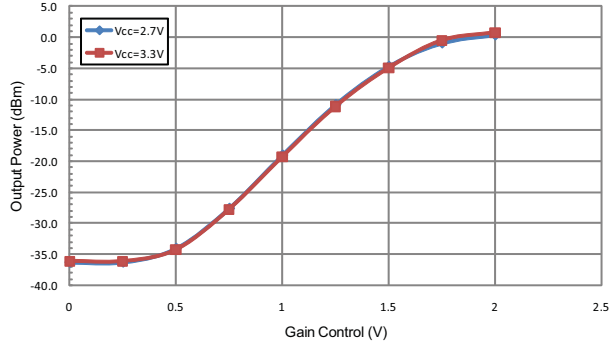


Typical Performance: 2400MHz Application Circuit

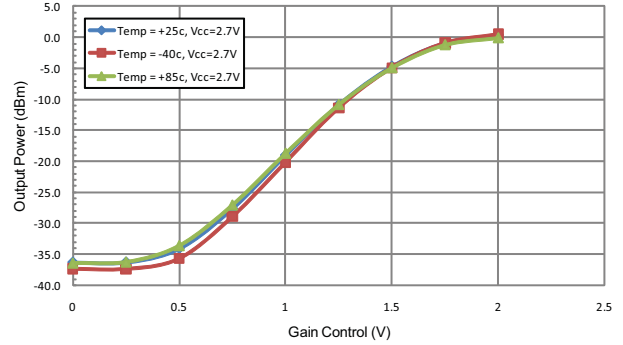


**Typical Performance: 2700MHz Application Circuit**

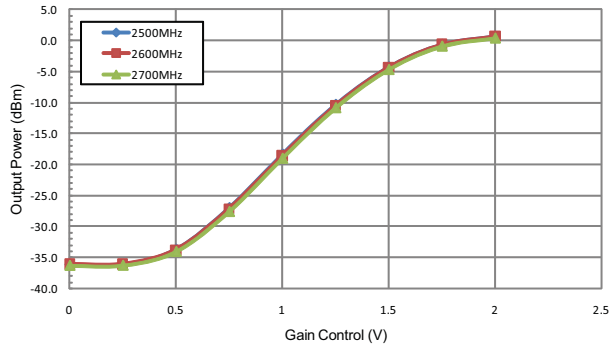
**High Band Output Power versus Gain Control**  
LO=2700MHz 0dBm, IQ=100kHz 800mV<sub>p-p</sub> 1.2V<sub>DC</sub>



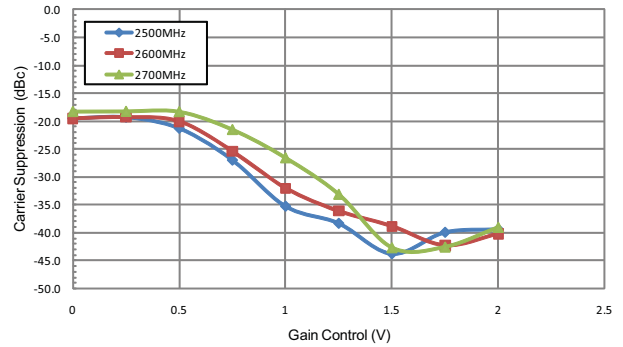
**High Band Output Power versus Gain Control**  
LO=2700MHz 0dBm, IQ=100kHz 800mV<sub>p-p</sub> 1.2V<sub>DC</sub>



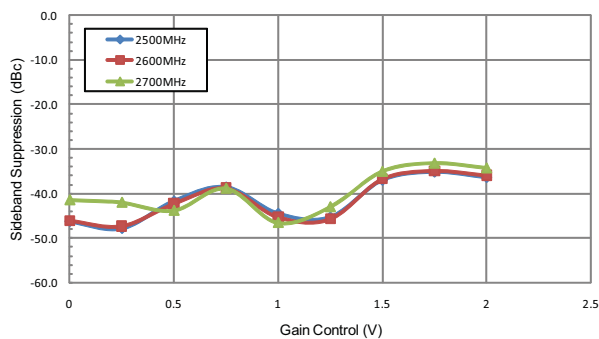
**High Band Output Power versus Gain Control**  
Vcc=2.7V, LO=0dBm, IQ=100kHz 800mV<sub>p-p</sub> 1.2V<sub>DC</sub>



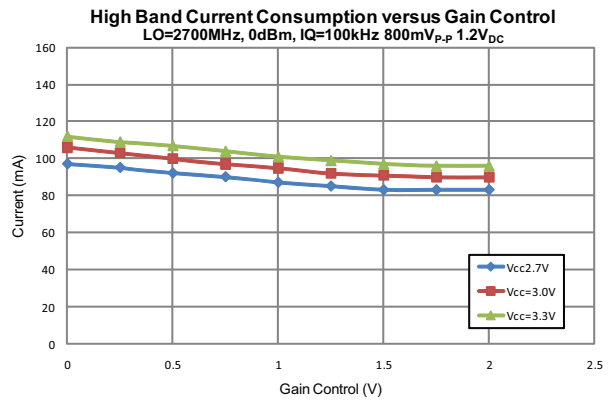
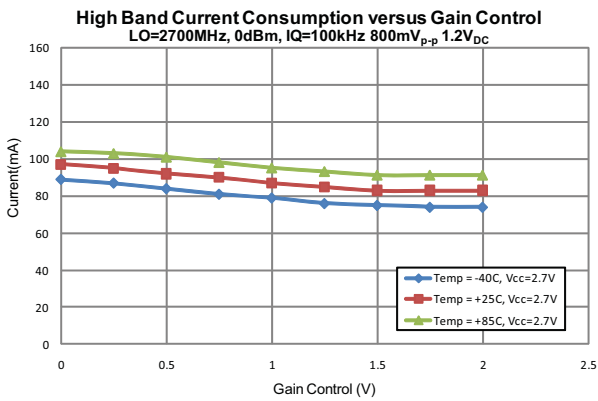
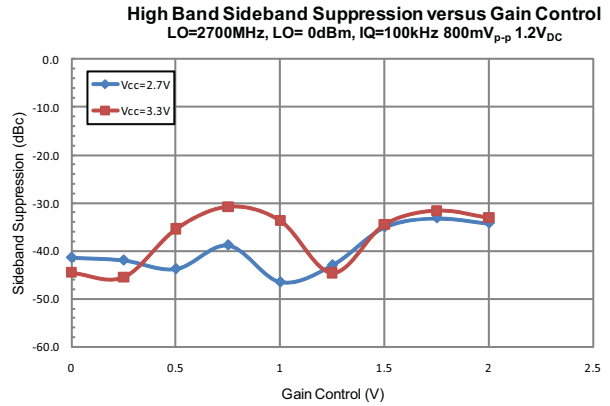
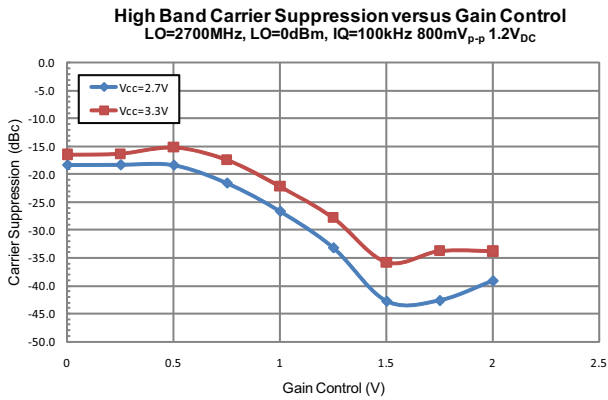
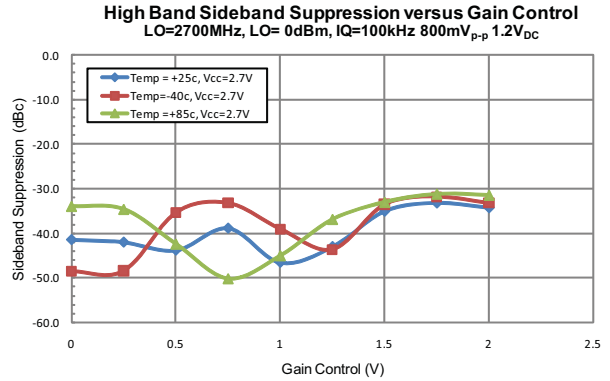
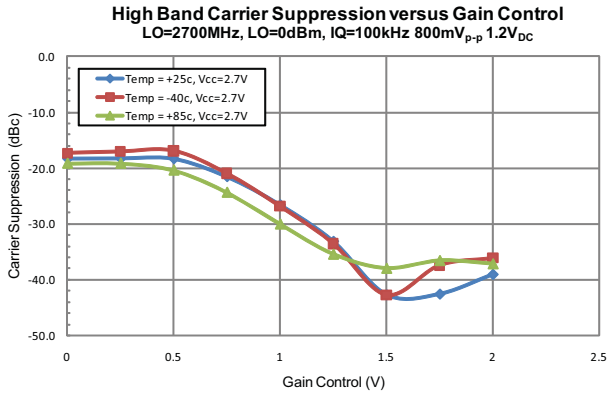
**High Band Carrier Suppression versus Gain Control**  
Vcc=2.7V, LO=0dBm, IQ=100kHz 800mV<sub>p-p</sub> 1.2V<sub>DC</sub>



**High Band Sideband Suppression versus Gain Control**  
Vcc=2.7V, LO= 0dBm, IQ=100kHz 800mV<sub>p-p</sub> 1.2V<sub>DC</sub>

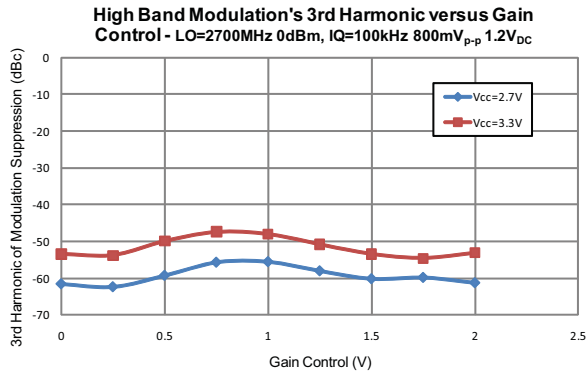
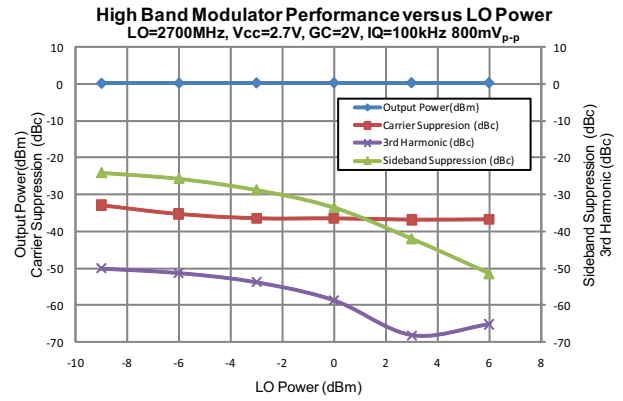
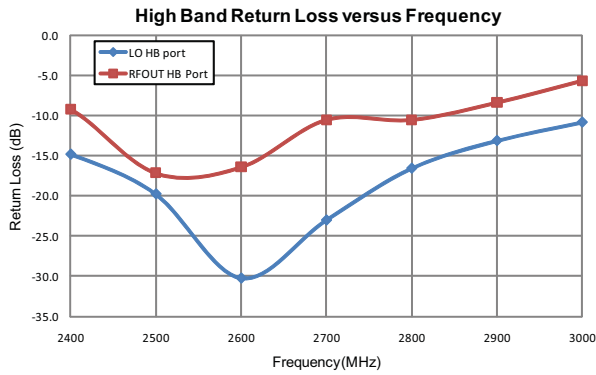


## Typical Performance: 2700MHz Application Circuit





### Typical Performance: 2700MHz Application Circuit



## RoHS\* Banned Material Content

RoHS Compliant: Yes  
Package total weight in grams (g): 0.042  
Compliance Date Code: 0522  
Bill of Materials Revision: -  
Pb Free Category: e3

Bill of Materials	Parts Per Million (PPM)					
	Pb	Cd	Hg	Cr VI	PBB	PBDE
Die	0	0	0	0	0	0
Molding Compound	0	0	0	0	0	0
Lead Frame	0	0	0	0	0	0
Die Attach Epoxy	0	0	0	0	0	0
Wire	0	0	0	0	0	0
Solder Plating	0	0	0	0	0	0

**This RoHS banned material content declaration was prepared solely on information, including analytical data, provided to RFMD by its suppliers, and applies to the Bill of Materials (BOM) revision noted above.**

\* DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment