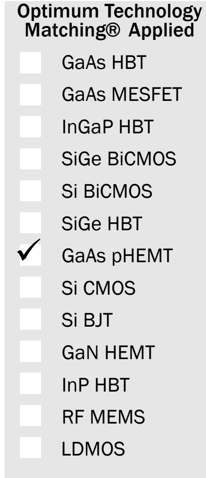
SDA-4000

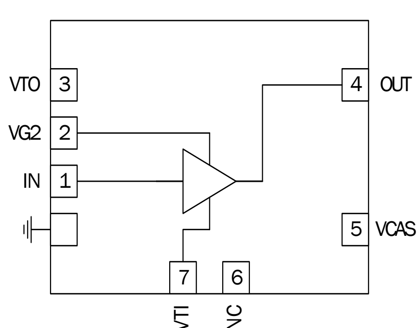
GaAs DISTRIBUTED AMPLIFIER

Die: 3.1mm x 1.45mm x 0.102mm

Product Description

RFMD's SDA-4000 is a directly coupled (DC) GaAs microwave monolithic integrated circuit (MMIC) driver amplifier die. It is designed for use as an electro-absorptive modulated laser (EML) driver employing single-ended (SE) architectures with V_π (V-pi) ranging from 2V to 5V, and as a clock driver for return-to-zero (RZ) and carrier select (CS) carver modulators. It can also be used for broadband automated test equipment (ATE), instrumentation, military, and aerospace applications.





Features

- DC to 32GHz Operation
- 22dBm P_{3dB}
- Gain=15dB Typical
- Noise Figure≤3.0dB
- Output Voltage to $5V_{PP}$
- Single Supply Voltage
- 160mA Total Current

Applications

- Driver for Single-ended (SE) EML
- Clock Driver for RZ and CS Pulse Carver
- Broadband ATE
- Instrumentation
- Military
- Aerospace

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Electrical Specifications					TA=+25°C, V_{DD}=+5V_{DC}, VG2@=+2V_{DC}, I_{DD}=160mA*
Operating Frequency	0		32	GHz	3dB BW
Gain	13.5	14.5		dB	16GHz
Output Voltage		5		±V_{P-P}	
IP3 @ Mid-Band		27		dBm	P_{OUT} ≈+0dBm/tone, 16GHz
P1dB @ Mid- Band		18		dBm	16GHz
P_{3dB} @ Mid-Band		22		dBm	16GHz
Noise Figure at Mid-Band		3.2		dB	16GHz
Input Return Loss		15		dB	DC to 25GHz
Output Return Loss		20		dB	DC to 25GHz
Supply Current		160		mA	
Supply Voltage		5		V_{DC}	

*Adjust VTI between -1.5V_{DC} to +0.2V_{DC} to achieve I_{DD}=160mA typical., V_{G2}=2V_{DC}

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Absolute Maximum Ratings

Parameter	Rating	Unit
Voltage (V_{DD})	+6.0	V_{DC}
Gate Bias Voltage (V_{TI})	-1.5 to +0.2	V_{DC}
Gate Bias Voltage (V_{G2})	(V_{DD}-5.0) V_{DC} to V_{DD}	V
RF Input Power (V_{DD}=+5.0V_{DC})	+15	dBm
Operating Junction Temperature (T_J)	+125	°C
Continuous Power Dissipation (T=+85°C)	1	W
Thermal Resistance (Pad to Die Bottom)	84	°C/W
Storage Temperature	-40 to +150	°C
Operating Temperature	0 to +85	°C
ESD JESD22-A114 Human Body Model (HBM)	Class 0 (All Pads)	

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

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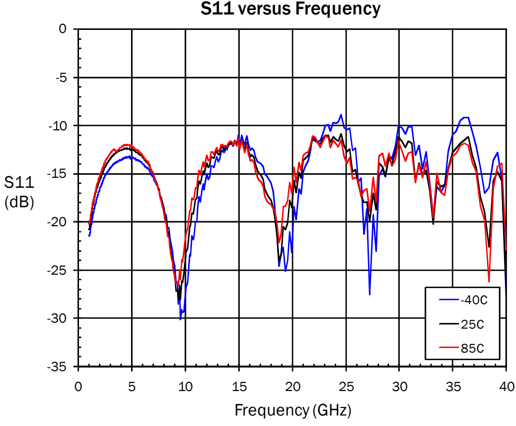
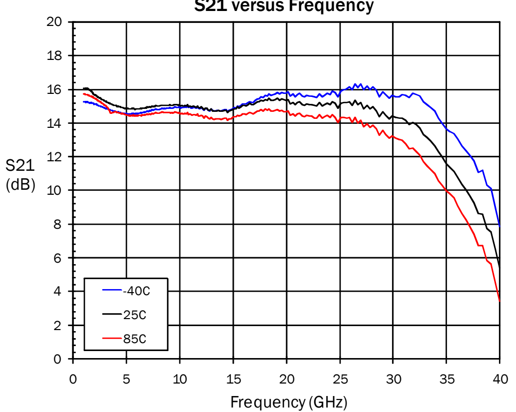
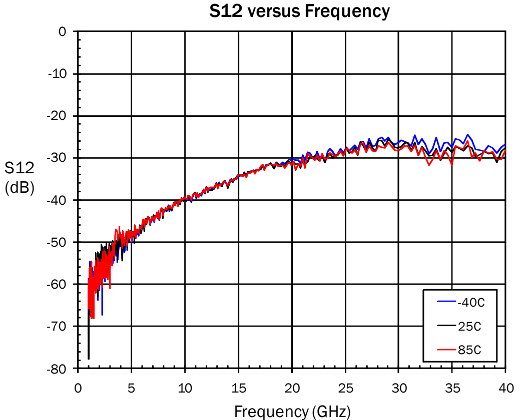
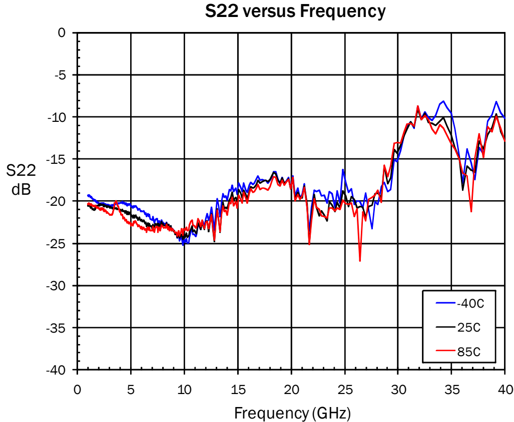
Typical Electrical Performance









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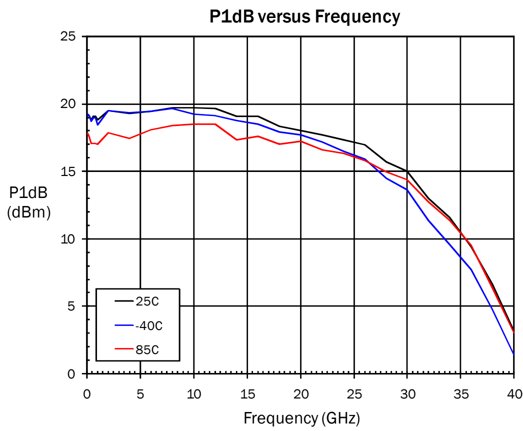
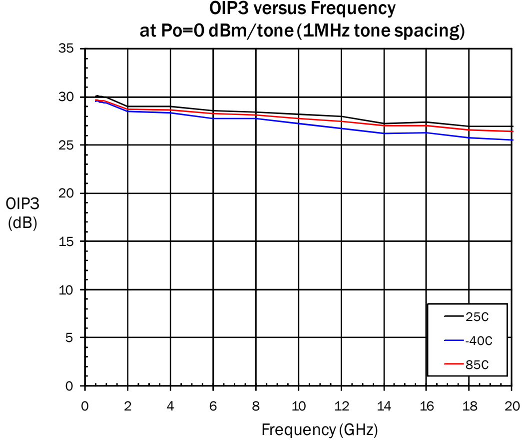
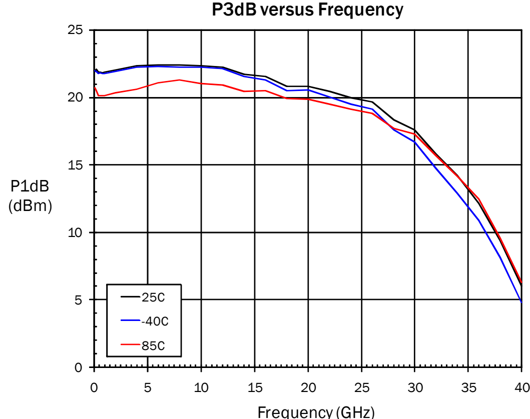
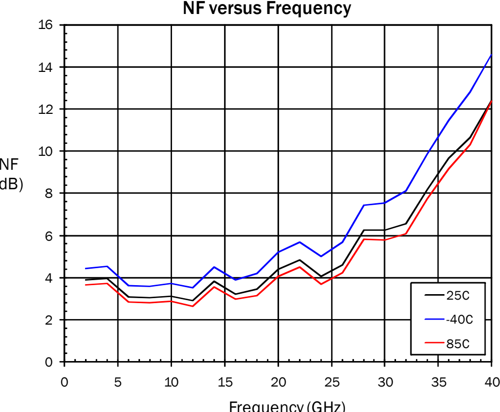
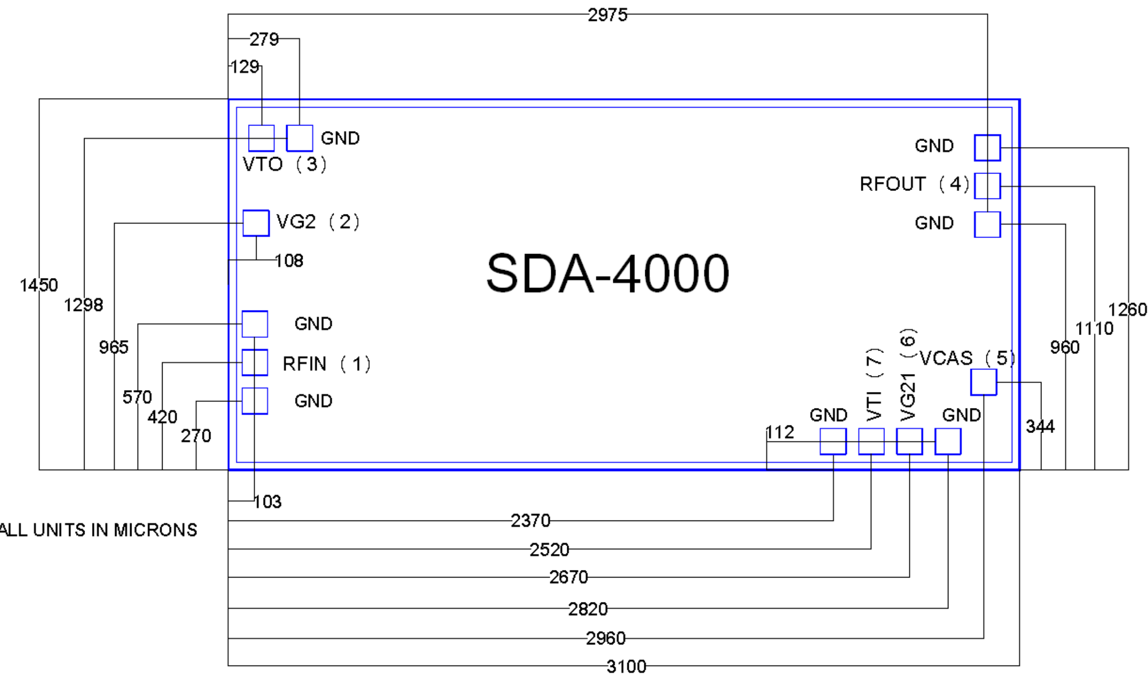








Outline Drawing



Notes:

1. All dimensions in microns

2. No connection required for unlabeled bond pads

3. Die thickness is 0.102 mm (4 mil)

4. Typical bond pad is 0.100 mm square

5. Backside metalization: Gold

6: Backside metal is ground

7: Bond pad metalization: Gold

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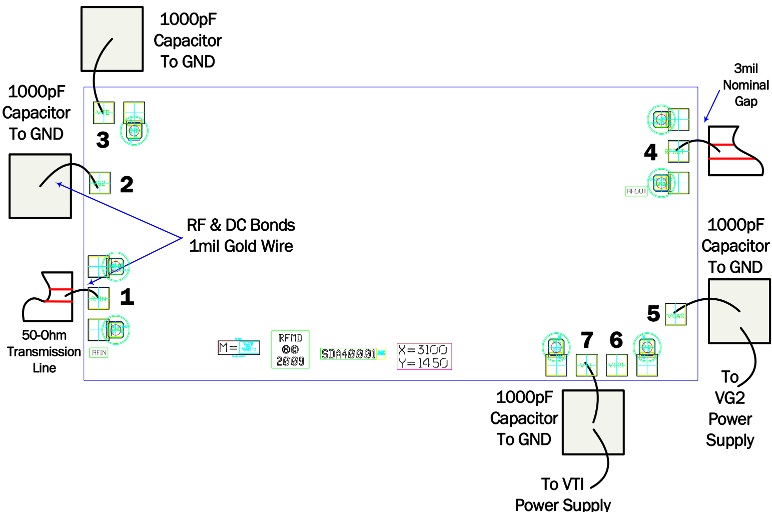
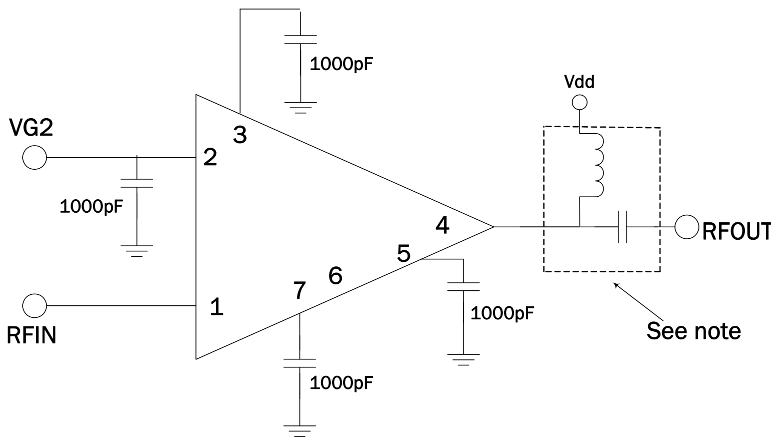
Pin	Function	Description	Interface Schematic
1	RFIN	RF Input. This pad is DC coupled and matched to 50Ω from DC to 32GHz. 50Ω microstrip transmission line on 0.127mm (5mil) thick alumina thin film substrate is recommended for RF input and output.	RFIN
2	VG2	VG2 is an optional pad. It may be used to bias the cascode gate of the amplifier. If this port is used, a 1000pF bypass capacitor with the shortest wirebond length possible is recommended to prevent low frequency gain ripple.	1000 pF
3	VTO	The output drain termination pad. This pad requires a suggested 1000pF bypass capacitor with the shortest wirebond length to prevent low frequency gain ripple. The value of the external capacitance limits the low frequency response of the amplifier.	Term Resistor 10pF
4	RFOUT and VDD	RF Output. 50Ω microstrip transmission line on 0.127mm (5mil) thick alumina thin film substrate is recommended for RF input and output. Connect the DC bias (V_{DD}) network to provide drain current (I_{DD}).	1000 pF RFOUT VDD RFOUT Note: Drain Bias (VDD) must be applied through a broadband bias tee or external bias network
5	VCAS	Provides VG2 gate voltage to the cascode amplifier. The value is ~ (V_{CC}/2 - absolute value of VTI).	1000 pF
6	VG21	Not connected.	
7	VTI	Input gate voltage, used to bias the amplifier. The value is between -1.5V_{DC} (device is pinched OFF) to +0.2V_{DC} (fully ON). This pad requires a bypass capacitor to ground with the shortest possible wirebond length to prevent low frequency gain ripple. The value of the external capacitance limits the low frequency response of the amplifier.	1000 pF
Die	GND	Ground connection. Connect die bottom directly to ground plane for best performance. Note: The die should be connected directly to the ground plane with conductive epoxy.	

Assembly Diagram



Application Circuit Schematic



Note: Drain Bias (Vdd) must be applied through a broadband bias tee or external bias network.

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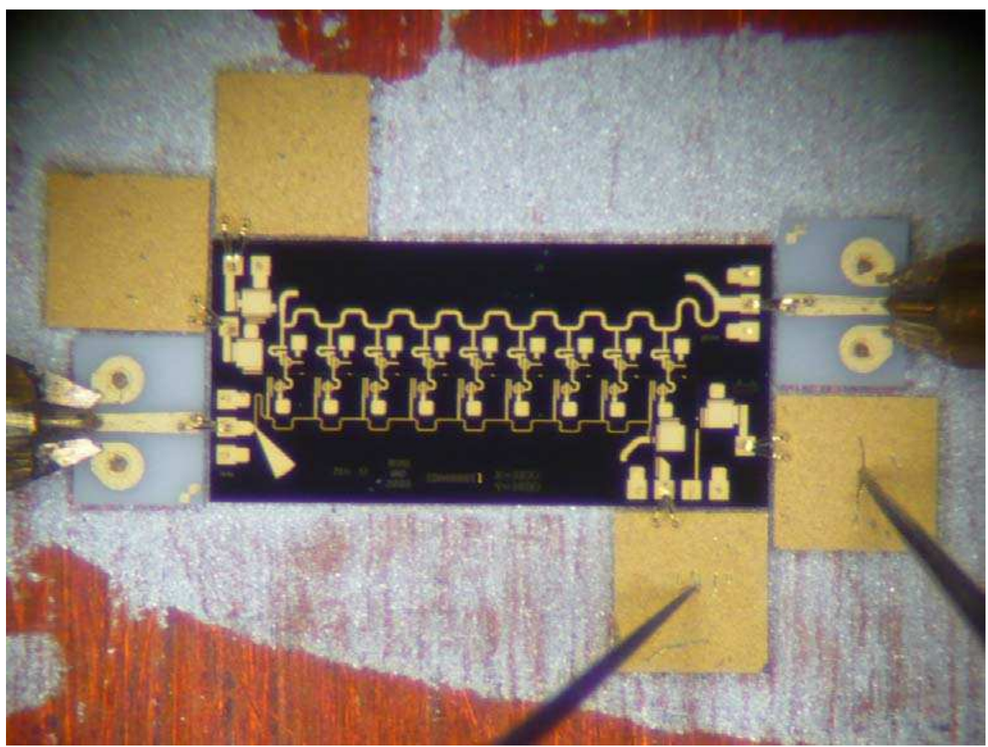
Measurement Technique

All specifications and typical performances reported in this document were measured in the following manner. Data was taken using a temperature controlled probe station utilizing 150µm pitch GSG probes. The interface between the probes and integrated circuit was made with a coplanar to microstrip ceramic test interface. The test interface was then wire bonded to the die as shown in the figure below using 1mil diameter bondwires. The spacing between the test interface and the die was 200µm, and the bond wire loop height was 100µm. The thickness of the test interface is 125µm. (5mil). The calibration of the test fixture included the probes and test interfaces, so that the measurement reference plane was at the point of bond wire attachment. Therefore, all data represents the integrated circuit and accompanying bond wires.



Ordering Information

Part Number	Description	Delivery Method	Die/GelPak
SDA4000	GaAs distributed amplifier, 32GHz, 3.10mmx1.45mm die	GelPak	10 pcs or more
SDA4000SB	GaAs distributed amplifier, 32GHz, 3.10mmx1.45mm die	GelPak	2 pcs

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