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FPD1500SOT89CE

LOW-NOISE HIGH-LINEARITY PACKAGED pHEMT

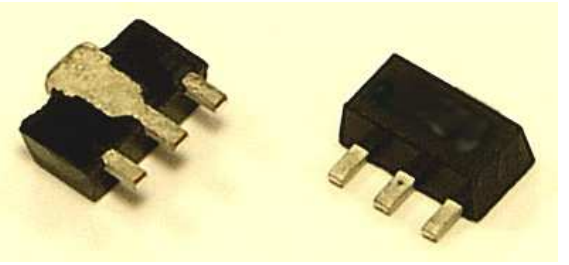
Package: SOT89

Product Description

The FPD1500SOT89CE is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It features a 0.25µmx1500µm Schottky barrier gate, defined by high-resolution stepper-based photolithography. The double recessed gate structure minimizes parasitics to optimize performance. The epitaxial structure is designed for improved linearity over a range of bias conditions and input power levels.

Optimum Technology Matching® Applied

- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ InGaP HBT
- ☐ SiGe BiCMOS
- ☐ Si BiCMOS
- ☐ SiGe HBT
- ☑ GaAs pHEMT
- ☐ Si CMOS
- ☐ Si BJT
- ☐ GaN HEMT
- ☐ InP HBT
- ☐ RF MEMS
- ☐ LDMOS



Features

- 27.5dBm Output Power (P1dB)
- 17dB Small-Signal Gain (SSG)
- 0.9dB Noise Figure
- 42dBm O_{IP3}
- 50% Power-Added Efficiency
- FPD1500SOT89CE: RoHS Compliant

Applications

- Drivers or Output Stages in PCS/Cellular Base Station Transmitter Amplifiers
- High Intercept-point LNAs
- WLL, WLAN, and Other Types of Wireless Infrastructure Systems.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
P_{1dB} Gain Compression	26.0	27.5		dBm	V_{DS}=5V, I_{DS}=50% I_{DSS}
Small-Signal Gain (SSG)	15.5	17		dB	V_{DS}=5V, I_{DS}=50% I_{DSS}
PAE		50		%	V_{DS}=5V, I_{DS}=50% I_{DSS}, P_{OUT}=P_{1dB}
Noise Figure (NF)		0.9		dB	V_{DS}=5V, I_{DS}=50% I_{DSS}; V_{DS}=5V, I_{DS}=25% I_{DSS}
OIP_3	38	40		dBm	V_{DS}=5V, I_{DS}=50% I_{DSS}. Matched for optimal power.
		42		dBm	Matched for best IP_3
Saturated Drain-Source Current (I_{DSS})	375	465	550	mA	V_{DS}=1.3V, V_{GS}=0V
Maximum Drain-Source Current (I_{MAX})		750		mA	V_{DS}=1.3V, V_{GS}≈+1V
Transconductance (GM)		400		ms	V_{DS}=1.3V, V_{GS}=0V
Gate-Source Leakage Current (IGSO)		1	15	µA	V_{GS}=-5V
Pinch-Off Voltage (V_P)	|0.7|	|1.0|	|1.3|	V	V_{DS}=1.3V, I_{DS}=1.5mA
Gate-Source Breakdown Voltage (V_{BDGS})	|12|	|16|		V	I_{GS}=1.5mA
Gate-Drain Breakdown Voltage (V_{BDGD})	|12|	|16|		V	I_{GD}=1.5mA
Thermal Resistivity (θJC) *		60		°C/W	

*Note: $T_{AMBIENT}$=22°C, RF specifications measured at f=1850GHz using CW signal (except as noted).

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Absolute Maximum Ratings[1]

Parameter	Rating	Unit
Drain-Source Voltage (V_{DS}) (-3V<V_{GS}<-0.5V)	8	V
Gate-Source Voltage (V_{GS}) (0V<V_{DS}<+8V)	-3	V
Drain-Source Current (I_{DS}) (For V_{DS}>2V)	I_{DSS}	
Gate Current (I_G) (Forward or reverse)	15	mA
RF Input Power (P_{IN})[2] (Under any acceptable bias state)	350	mW
Channel Operating Temperature (T_{CH}) (Under any acceptable bias state)	175	°C
Storage Temperature (T_{STG}) (Non-Operating Storage)	-55 to 150	°C
Total Power Dissipation (P_{TOT})[3, 4]	2.3	W
Gain Compression (Under bias conditions)	5	dB
Simultaneous Combination of Limits[6] (2 or more max. limits)		

Notes:
[1] $T_{AMBIENT}$=22 °C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device.
[2] Max. RF input limit must be further limited if input VSWR>2.5:1.
[3] Users should avoid exceeding 80% of 2 or more Limits simultaneously.
[4] Total Power Dissipation (P_{TOT}) defined as (P_{DC}+P_{IN})−P_{OUT}, where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power.
Total Power Dissipation to be de-rated as follows above 22 °C:
P_{TOT}=2.3-(0.016W/°C)xT_{PACK}, where T_{PACK}=source tab lead temperature above 22 °C. (Coefficient of de-rating formula is Thermal Conductivity.)
Exampe: For a 65 °C carrier temperature: P_{TOT}=2.3W-(0.016x(65-22))=1.61W

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Biasing Guidelines

Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that gate bias is applied before drain bias.

Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices.

For standard Class A operation, an operating point of 50% of I_{DSS} is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. A class A/B Bias of 25% to 33% of I_{DSS} to achieve better OIP_3 and Noise Figure performance is suggested.

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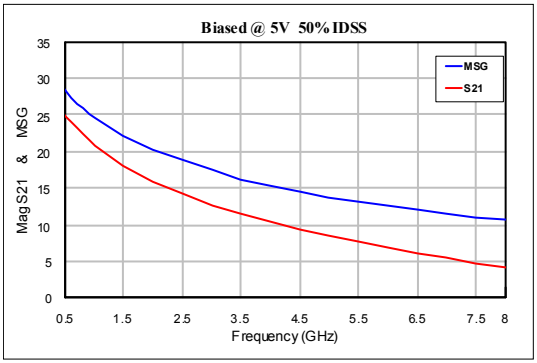
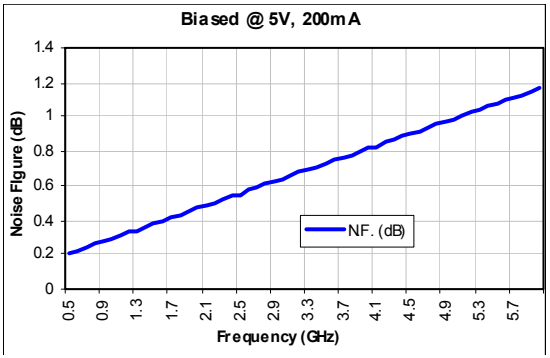
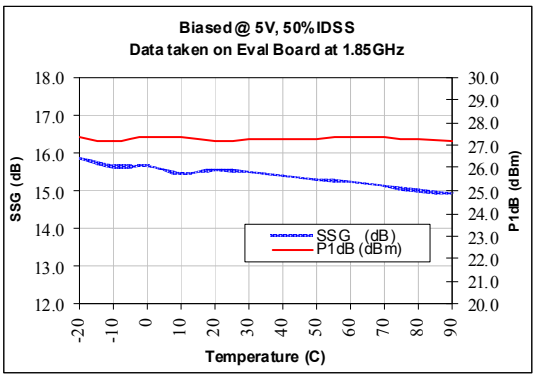
Frequency Response

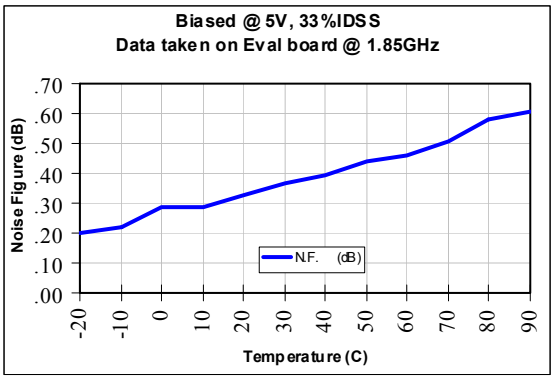




Device tuned for minimum noise figure.

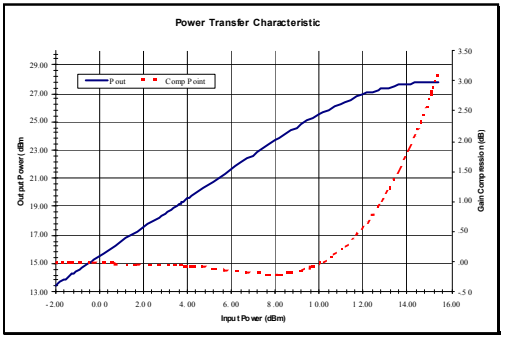
Temperature Response

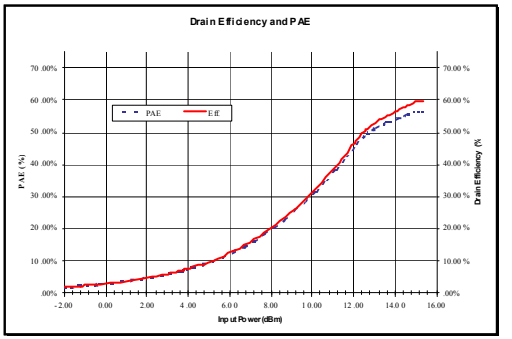




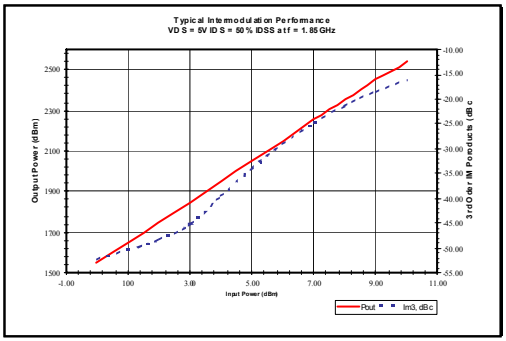
Evaluation board tuned for maximum power.

Typical Tuned RF Performance



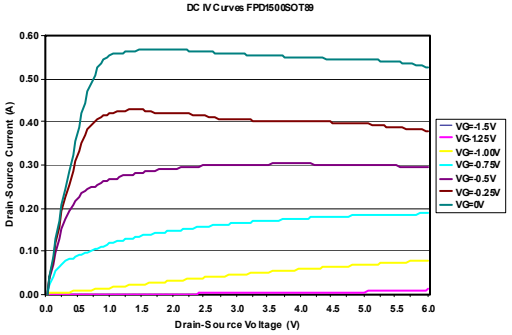


Note: Typical power and efficiency are shown above. The devices were biased nominally at V_{DS}=5V, I_{DS}=50% of I_{DSS}, at a test frequency of 1.85GHz. The test devices were tuned (input and output) for maximum output power at 1dB gain compression.



Note: pHEMT devices have enhanced intermodulation performance. This yields OIP3 values of about P1dB+14dBm. This IMD enhancement is affected by the quiescent bias and the matching applied to the device.

Typical I-V Characteristics



Note: The recommended method for measuring I_{DSS}, or any particular I_{DS}, is to set the Drain-Source voltage (V_{DS}) at 1.3V. This measurement point avoids the onset of spurious self-oscillation which would normally distort the current measurement (this effect has been filtered from the I-V curves presented above). Setting the V_{DS}>1.3V will generally cause errors in the current measurements, even in stabilized circuits.

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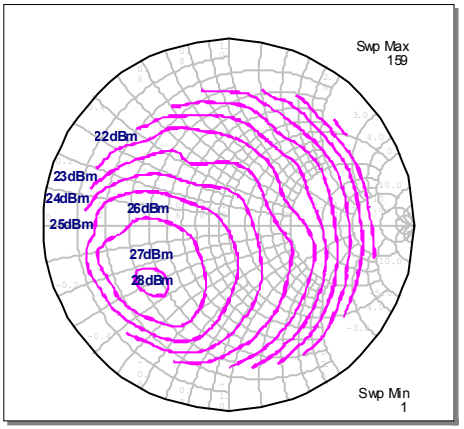
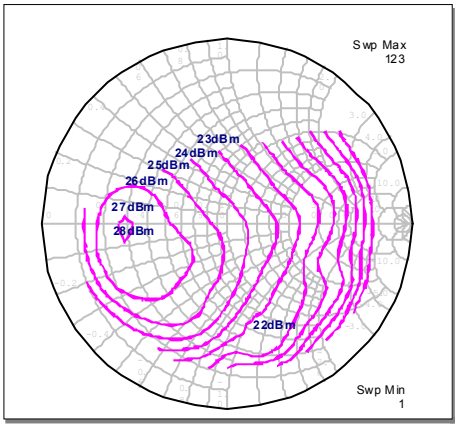
Typical Output Plane Power Contours

(V_{DS}=5V, I_{DS}=50% I_{DSS})



1850 MHz



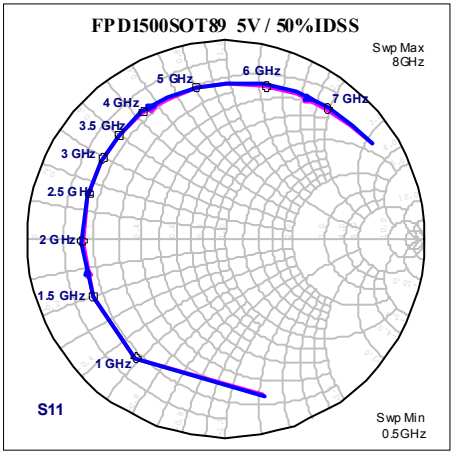
900 MHz

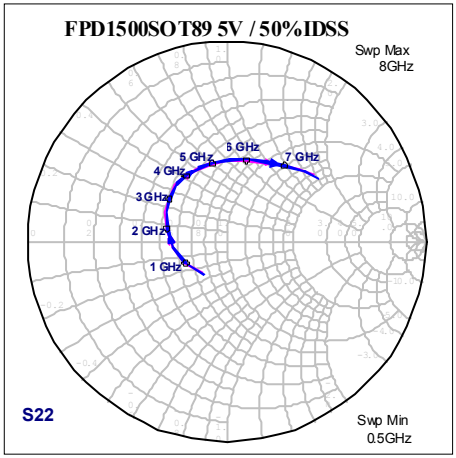
Contours swept with a constant input power, set so that optimum P1dB is achieved at the point of output match.
Input (Source plane) Γs:
0.74∠168.2°
0.15+j0.1 (normalized)
7.5+j5.0Ω
Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.

Contours swept with a constant input power, set so that optimum P1dB is achieved at the point of output match.
Input (Source plane) Γs:
0.67∠103.6°
0.30+j0.74 (normalized)
15+j37.0Ω
Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.

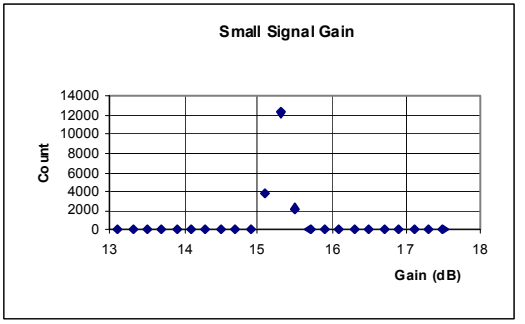
Typical Scattering Parameters

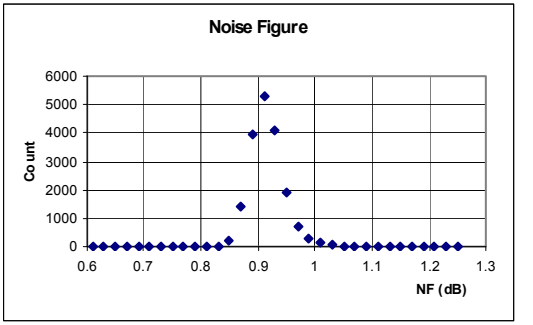
(50Ω System)

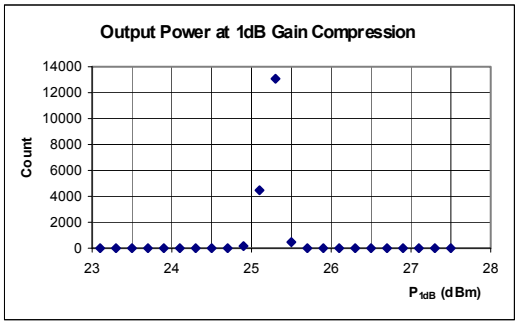


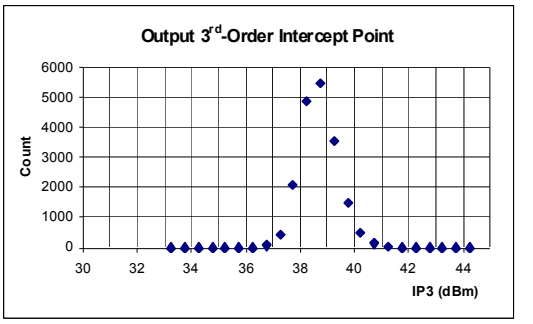


Typical Sample of RF Performance









Note: The devices were tested by a high-speed automatic test system in a matched circuit based on a 2GHz evaluation board. This circuit is a dual-bias single-pole lowpass topology, and the devices were biased at V_{DS}=4.5V, I_{DS}=120mA, test frequency=2.0GHz. The performance data is summarized below:

Parameter	Median	Standard Deviation	Test Limit	CPK
Small-Signal Gain	15.5	0.20	14.5	1.7
Noise Figure	0.91	0.03	1.20	3.2
Output Power (P1dB)	25.2	0.25	24.5	0.93
3rd-Order Intercept	38.7	1.1	36.5	0.67

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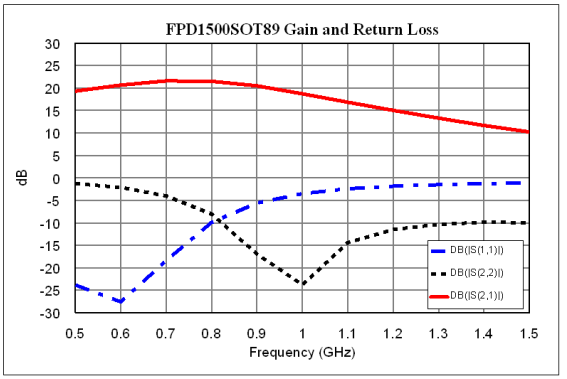
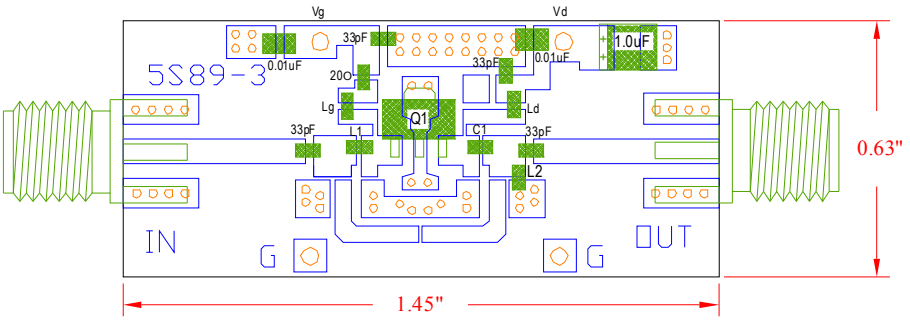
Reference Design (0.9 GHz)

Parameter	Typical	Unit
Gain	20	dB
P1dB	27	dBm
OIP_3	39	dBm
NF	0.7	dB
S11	-5	dB
S22	-15	dB
V_D	5	V
V_G	-0.4 to -0.6	V
I_D	200	mA

Note: OIP_3 measured at 15 dBm per tone.



Evaluation Board Layout

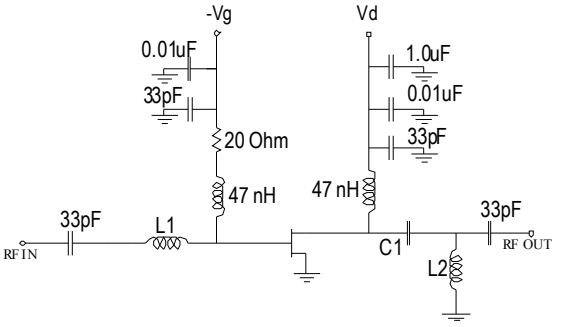


Component Values

Component	Value	Description
Lg	47 nH	LL 1608 Toko chip inductor
Ld	47 nH	LL 1608 Toko chip inductor
L1	12 nH	LL 1005 Toko chip inductor
L2	4.7 nH	LL 1005 Toko chip inductor
C1	5.6 pF	ATC 600S chip capacitor

Evaluation board material: 31 mil thick FR4 with 1/2 oz. Cu on both sides.

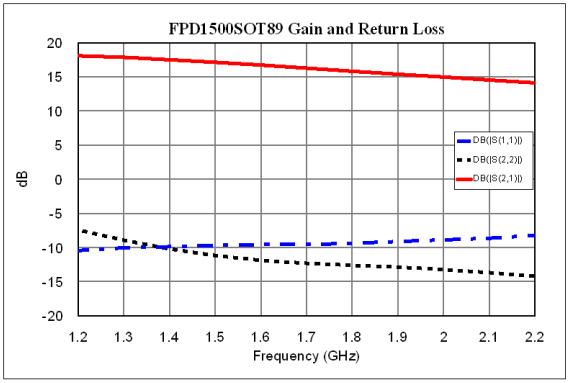
DC-blocking capacitors are ATC series 600S. A tantalum 1.0 µF is used at the drain terminal. All other capacitors are 0603 and 0805 standard chip capacitors. A 0603 size 20 Ω chip resistor from Vishay is used on the gate DC bias line for stability.



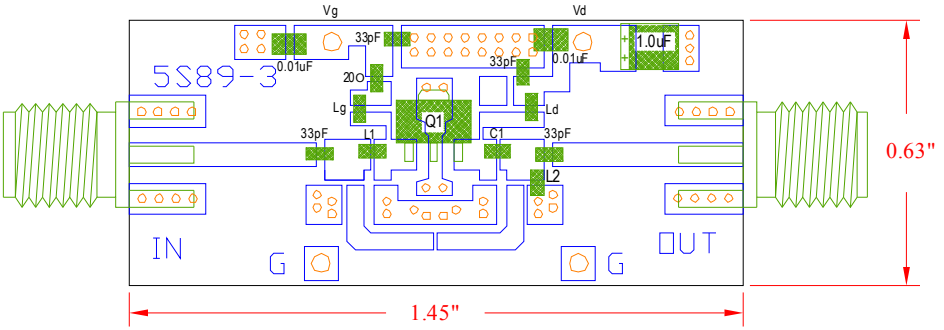
Reference Design (1.85GHz)

Parameter	Typical	Unit
Gain	16	dB
P1dB	27	dBm
OIP_3	41	dBm
NF	0.9	dB
S11	-9	dB
S22	-14	dB
V_D	5	V
V_G	-0.4 to -0.6	V
I_D	200	mA

Note: OIP_3 measured at 15dBm per tone.



Evaluation Board Layout

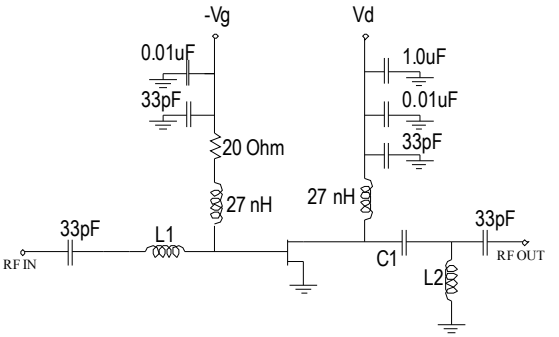


Component Values

Component	Value	Description
Lg	27nH	LL 1608 Toko chip inductor
Ld	27nH	LL 1608 Toko chip inductor
L1	1.5nH	LL 1005 Toko chip inductor
L2	4.7nH	LL 1005 Toko chip inductor
C1	2.2pF	ATC 600S chip capacitor

Evaluation board material: 31mil thick FR4 with 1/2oz. Cu on both sides.

DC-blocking capacitors are ATC series 600S. A tantalum 1.0µF is used at the drain terminal. All other capacitors are 0603 and 0805 standard chip capacitors. A 0603 size 20Ω chip resistor from Vishay is used on the gate DC bias line for stability.



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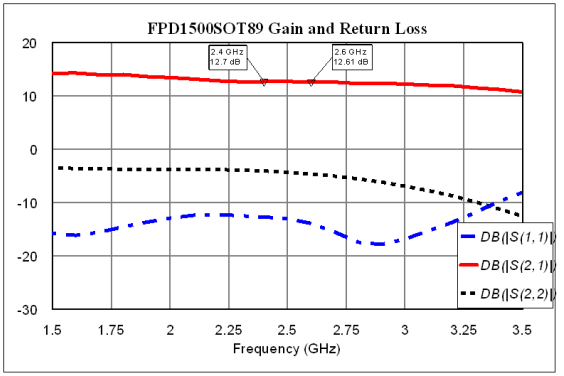
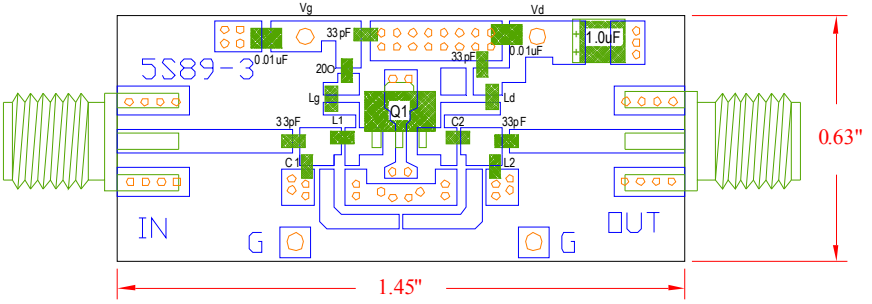
Reference Design (2.4GHz to 2.6GHz)

Parameter	@ 2.4GHz	@ 2.6GHz	Unit
Gain	12.5	12.4	dB
P1dB	28	28	dBm
OIP_3	39	40	dBm
NF	1.0	0.9	dB
S11	-14	-16	dB
S22	-5	-6	dB
V_D	5	5	V
V_G	-0.4 to -0.6	-0.4 to -0.6	V
I_D	200	200	mA

Note: OIP_3 measured at 15dBm per tone.



Evaluation Board Layout

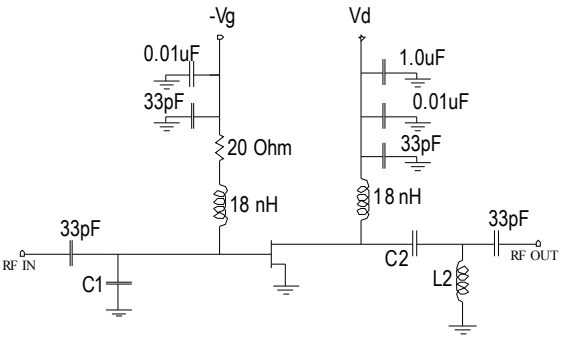


Component Values

Component	Value	Description
Lg	18nH	LL 1608 Toko chip inductor
Ld	18nH	LL 1608 Toko chip inductor
L1	0.0nH	no component (Cu tab)
L2	3.9nH	LL 1005 Toko chip inductor
C1 and C2	1.0pF	ATC 600S chip capacitor

Evaluation board material: 31mil thick FR4 with 1/2oz. Cu on both sides.

DC-blocking capacitors are ATC series 600S. A tantalum 1.0µF is used at the drain terminal. All other capacitors are 0603 and 0805 standard chip capacitors. A 0603 size 20Ω chip resistor from Vishay is used on the gate DC bias line for stability.



S-Parameters

(Biased @ 5V, 50% I_{DSS})

FREQ[GHz]	S11m	S11a	S21m	S21a	S12m	S12a	S22m	S22a
0.500	0.865	-91.9	18.828	121.6	0.027	52.3	0.293	-130.2
0.750	0.763	-118.7	14.373	107.4	0.033	46.3	0.287	-141.8
1.000	0.728	-136.4	11.562	95.9	0.038	42.6	0.293	-154.9
1.250	0.714	-149.6	9.707	87.0	0.043	39.6	0.285	-162.6
1.500	0.701	-162.1	8.254	79.1	0.047	37.4	0.284	-172.6
1.750	0.694	-171.3	7.225	71.2	0.052	34.6	0.288	-178.7
2.000	0.692	179.8	6.460	64.2	0.057	32.1	0.279	175.2
2.250	0.684	171.3	5.820	57.4	0.061	29.4	0.279	168.4
2.500	0.685	163.7	5.320	50.7	0.067	26.1	0.271	161.9
2.750	0.683	155.8	4.884	44.6	0.071	23.5	0.273	153.9
3.000	0.681	148.1	4.506	37.8	0.076	19.7	0.273	147.1
3.250	0.692	141.4	4.199	31.4	0.080	16.0	0.276	138.5
3.500	0.690	134.1	3.913	25.1	0.085	12.4	0.290	131.2
3.750	0.698	127.7	3.651	18.8	0.089	8.5	0.302	124.2
4.000	0.706	120.8	3.418	12.7	0.093	4.6	0.318	118.0
4.250	0.711	114.3	3.207	6.5	0.096	0.5	0.335	112.5
4.500	0.730	108.9	3.018	0.8	0.100	-3.5	0.349	107.0
4.750	0.742	103.2	2.834	-5.0	0.102	-7.4	0.367	101.4
5.000	0.757	98.2	2.672	-10.6	0.105	-11.1	0.381	96.3
5.250	0.765	92.4	2.531	-16.1	0.108	-14.6	0.396	91.7
5.500	0.769	87.7	2.408	-21.7	0.111	-18.6	0.406	87.3
5.750	0.790	83.4	2.300	-26.9	0.114	-22.2	0.417	83.2
6.000	0.847	77.1	2.263	-33.3	0.121	-27.1	0.457	79.0
6.250	0.830	73.0	2.139	-38.4	0.122	-30.6	0.457	75.1
6.500	0.850	67.3	2.046	-45.2	0.124	-36.0	0.476	68.2
6.750	0.826	63.8	1.926	-49.9	0.125	-39.1	0.471	62.2
7.000	0.829	60.2	1.839	-54.7	0.127	-42.7	0.471	55.5
7.250	0.828	56.4	1.763	-59.5	0.128	-46.1	0.470	50.2
7.500	0.823	52.8	1.698	-64.6	0.130	-49.9	0.477	44.5
7.750	0.836	48.9	1.641	-69.8	0.133	-54.2	0.491	39.2
8.000	0.855	44.5	1.580	-75.7	0.135	-58.9	0.507	33.8
8.250	0.858	38.3	1.512	-81.5	0.135	-63.5	0.531	29.3
8.500	0.855	32.9	1.442	-86.8	0.136	-68.0	0.552	24.7
8.750	0.863	27.9	1.374	-92.3	0.136	-72.8	0.575	21.2
9.000	0.874	22.0	1.311	-97.5	0.136	-77.2	0.596	17.7
9.250	0.875	16.9	1.247	-102.5	0.135	-81.6	0.618	15.4
9.500	0.885	11.9	1.182	-107.8	0.134	-86.4	0.637	13.0
9.750	0.890	7.4	1.124	-112.5	0.133	-91.4	0.652	11.0
10.000	0.895	3.8	1.069	-117.4	0.131	-96.4	0.663	8.0
10.250	0.897	0.5	1.012	-121.7	0.128	-101.8	0.673	5.1
10.500	0.899	-2.9	0.975	-126.0	0.125	-106.8	0.680	2.5
10.750	0.902	-5.6	0.928	-130.2	0.120	-111.1	0.693	0.0
11.000	0.902	-8.1	0.894	-134.3	0.117	-114.6	0.698	-2.9
11.250	0.907	-10.5	0.865	-138.4	0.115	-118.0	0.701	-6.0
11.500	0.913	-13.5	0.845	-142.1	0.114	-120.9	0.695	-9.7
11.750	0.912	-16.4	0.822	-146.4	0.114	-124.3	0.691	-13.3
12.000	0.908	-19.4	0.806	-150.7	0.117	-128.3	0.684	-18.1

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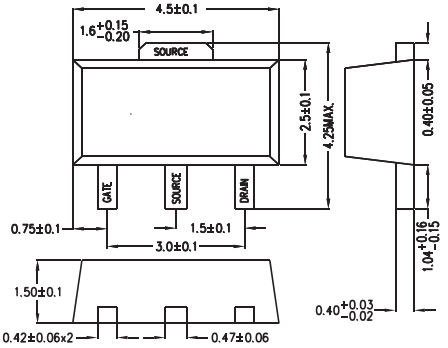
Part Identification

Package Outline

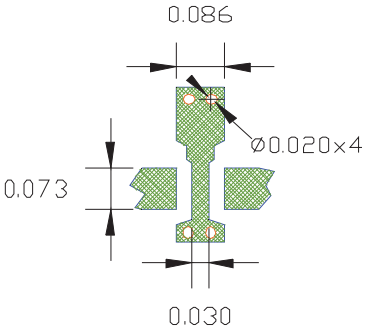
Dimensions in millimeters (mm)



Tape and Reel Dimensions and Part Orientation

Tape and Reel information on this material is in accordance with EIA-481-1 except where exceptions are identified

Device Footprint



Units in inches

Preferred Assembly Instructions

This package is compatible with both lead-free and leaded solder reflow processes as defined within IPC/JEDEC J-STD-020C. The maximum package temperature should not exceed 260 °C.

Handling Precautions

To avoid damage to the devices, care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing.

ESD Rating

These devices should be treated as Class 0 (0V to 250V) using the human body model as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

MSL Rating

The device has an MSL rating of Level 2. To determine this rating, preconditioning was performed to the device per the Pb-free solder profile defined within IPC/JEDEC J-STD-020C, moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices.

Application Notes and Design Data

Application Notes and design data including S-parameters, noise paramters, and device model are available on request and from www.rfmd.com.

Disclaimers

An MTTF of 7.4 million hours at a channel temperature of 150 °C is achieved for the process used to manufacture this device.

Disclaimers

This product is not designed for use in any space-based or life-sustaining/supporting equipment.

Ordering Information

Ordering Code	Description
FPD1500SOT89CESQ	Sample bag with 25 pieces
FPD1500SOT89CESR	7" Reel with 100 pieces
FPD1500SOT89CE	7" Reel with 1000 pieces
FPD1500SOT89PCK	1.85GHz PCBA with 5-piece sample bag

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