

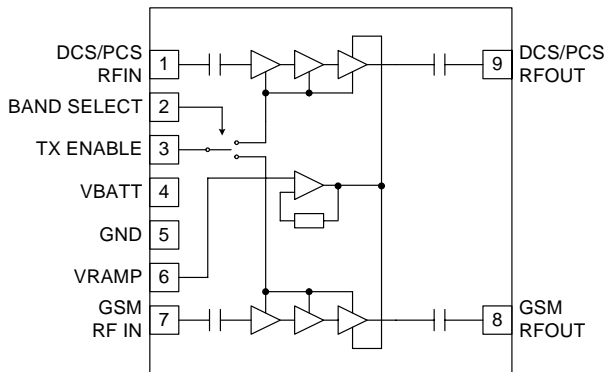


Features

- Ultra-Small, Ultra-Thin
6mmx6mmx1mm Package Size
- Integrated V_{REG}
- Complete Power Control Solution
- Large Signal Polar Modulation EDGE Compatible
- No External Components or Routing
- Improved Power Flatness through Integrated Current Limiter, 2.5A Maximum Current Draw over VSWR, all Phase Angles

Applications

- 3V Quad-Band GSM and EDGE Handsets
- EDGE Capable Large Signal Polar Modulation Handsets
- Portable Battery-Powered Equipment
- GSM850/EGSM900/DCS/PCS Products
- GPRS Class 12
- Power Star™ Module



Functional Block Diagram

Product Description

The RF3161 is a high-power, high-efficiency power amplifier module with integrated power control that provides over 50dB of control range. The device is a self-contained 6mmx6mmx1mm module with 50Ω input and output terminals. The device is designed for use as the final RF amplifier in GSM850, EGSM900, DCS and PCS handheld digital cellular equipment and other applications in the 824MHz to 849MHz, 880MHz to 915MHz, 1710MHz to 1785MHz and 1850MHz to 1910MHz bands. The RF3161 can be used for GSM and Polar Mod EDGE applications. The RF3161 requires no external routing or external components, simplifying layout and reducing board space.

Ordering Information

RF3161	Quad-Band GSM850/GSM900/DCS/PCS GMSK/EDGE Power amp Module
RF3161 SB	Power Amp Module 5-Piece Sample Pack
RF3161PCBA-410	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

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|--|--------------------------------------|---|------------------------------------|
| <input checked="" type="checkbox"/> GaAs HBT | <input type="checkbox"/> SiGe BiCMOS | <input type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET | <input type="checkbox"/> Si BiCMOS | <input checked="" type="checkbox"/> Si CMOS | <input type="checkbox"/> BiFET HBT |
| <input type="checkbox"/> InGaP HBT | <input type="checkbox"/> SiGe HBT | <input type="checkbox"/> Si BJT | <input type="checkbox"/> LDMOS |

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage Overshoot1 t < 1.0 μs	7.0	V _{DC}
Supply Voltage Overshoot2 t < 150ms	6.0	V _{DC}
Supply Voltage	-0.5 to +6.0	V _{DC}
Power Control Voltage (V _{RAMP})	-0.5 to +1.8	V
Input RF Power	+12	dBm
Max Duty Cycle	50	%
Output Load VSWR	10:1	
Operating Case Temperature	-20 to +85	°C
Storage Temperature	-55 to +150	°C



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall Power Control					
V _{RAMP}					
Power Control "ON"			1.6	V	Max. P _{OUT} , Voltage supplied to the input
Power Control "OFF"		0.26		V	Min. P _{OUT} , Voltage supplied to the input
V _{RAMP} 3dB Bandwidth	2.5	10		MHz	V _{BATT} =3.0V to 4.6V, T _{CASE} =-20 °C to +85 °C, P _{IN} =0dBm to 6dBm
V _{RAMP} Input Capacitance		2	20	pF	DC to 2MHz
TX Enable "ON"	1.3			V	
TX Enable "OFF"			0.5	V	
GSM Band Enable			0.5	V	
DCS/PCS Band Enable	1.3			V	
Overall Power Supply					
Power Supply Voltage		3.6		V	Specifications
	3.0		4.6	V	Nominal operating limits
Maximum Power Supply Current			2.5	A	VSWR=4:1 all phase angles, V _{RAMP} =V _{RAMP_RP} *, V _{BATT} =3.0V to 4.6V, T _{CASE} =-20 °C to +85 °C
Power Supply Current		1		μA	P _{IN} <-30dBm, TX Enable=Low, Temp=-20 °C to +85 °C
Overall Control Signals					
Band Select "Low"	0	0	0.5	V	
Band Select "High"	1.3	2.0	3.0	V	
Band Select "High" Current		20	50	μA	
TX Enable "Low"	0	0	0.5	V	
TX Enable "High"	1.3	2.0	3.0	V	
TX Enable "High" Current		1	2	μA	

*V_{RAMP_RP} is defined as the V_{RAMP} voltage required to achieve rated power at V_{BATT}=3.6V, T=25 °C, P_{IN}=3dBm.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (GSM850 Mode)					Temp=+25 °C, V _{BATT} =3.6V, V _{RAMP} =V _{RAMP_RP} , P _{IN} =3dBm, Freq=824MHz to 849MHz, 25% Duty Cycle, Pulse Width=1154µs
Operating Frequency Range	824		849	MHz	
Maximum Output Power 1	34.5			dBm	Temp=+25 °C, V _{BATT} =3.6V, V _{RAMP} ≤1.6V
Maximum Output Power 2	32.5			dBm	Temp=+85 °C, V _{BATT} =3.0V, V _{RAMP} ≤1.6V
Total Efficiency	45	51		%	At P _{OUT MAX} , V _{BATT} =3.6V, V _{RAMP} =1.6V
I _{BATT}		2.2	2.5	A	At P _{OUT MAX} , V _{BATT} =3.6V, V _{RAMP} =1.6V
Input Power Range	0	+3	+6	dBm	Maximum output power guaranteed at minimum drive level
Output Noise Power		-85	-82	dBm	RBW=100kHz, 869MHz to 894MHz, P _{OUT} ≤ +34.5dBm
Forward Isolation 1		-38	-30	dBm	TXEnable=Low, P _{IN} =+6dBm
Forward Isolation 2			-10	dBm	TXEnable=High, P _{IN} =+6dBm, V _{RAMP} =0.26V
Cross Band Isolation at 2f ₀			-18	dBm	V _{RAMP} =0.26V to V _{RAMP_RP}
Second Harmonic		-15	-6	dBm	V _{RAMP} =0.26V to V _{RAMP_RP}
Third Harmonic		-30	-11	dBm	V _{RAMP} =0.26V to V _{RAMP_RP}
All Other Non-Harmonic Spurious			-36	dBm	V _{RAMP} =0.26V to V _{RAMP_RP}
Input Impedance		50		Ω	
Input VSWR		2:1	2.5:1		P _{IN} =0dBm to +6dBm, V _{RAMP} set to P _{OUT} =6dBm to V _{RAMP} =V _{RAMP_RP} T=-20 °C to +85 °C
Output Load VSWR Stability	8:1				Spurious<-36dBm, RBW=3MHz Set V _{RAMP} where P _{OUT} ≤34.5dBm into 50Ω load
Output Load VSWR Ruggedness	10:1				Set V _{RAMP} where P _{OUT} ≤34.5dBm into 50Ω load. No damage or permanent degradation to part.
Output Load Impedance		50		Ω	Load impedance presented at RF OUT pad
Power Control V_{RAMP}					
Power Control Range	50	55		dB	V _{RAMP} =0.26V to V _{RAMP_RP}
Transient Spectrum		-35		dBm	V _{RAMP} =V _{RAMP_RP}
Transient Spectrum Under Extreme Conditions			-22	dBm	Temp=-20 °C to +85 °C, V _{BATT} ≥3.0V. Ramping shape same as for Condition: Temp=25 °C, V _{BATT} =3.6V, V _{RAMP} =V _{RAMP_RP}
Power Degradation from Nominal Conditions					V _{BATT} =3.0V to 4.6V, Temp=-20 °C to +85 °C, P _{IN} =0dBm to 5dBm,
5dBm to 15dBm	-5		+5	dB	Relative to output power for condition: V _{BATT} =3.6V, P _{IN} =+3dBm, Temp=25 °C,
15dBm to 31dBm	-3		+3	dB	Freq=836.5MHz.
34.5dBm	-2		+2	dB	Output power variation measured at set V _{RAMP}

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
GSM850 8-PSK Parameters				MHz	Temp = +25 °C, V _{CC} = 3.6V, P _{IN} = 3 dBm, 25% Duty Cycle, Pulse Width = 1154 μs, V _{RAMP} MAX = V _{RAMP} RP
Peak Output Power	32.5			dBm	
Efficiency		21.5		%	Output Power = 29 dBm
V _{RAMP} Loop Bandwidth	2.5	10		MHz	
V _{RAMP} Group Delay		35		nS	
V _{RAMP} Group Delay Variation	-12		12	nS	

Notes:

V_{RAMP}RP = V_{RAMP} set for 34.5 dBm at nominal conditions.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (GSM900 Mode)					Temp=+25 °C, V _{BATT} =3.6V, V _{RAMP} =V _{RAMP_RP} , P _{IN} =3dBm, Freq=880MHz to 915 MHz, 25% Duty Cycle, Pulse Width=1154 μs
Operating Frequency Range	880		915	MHz	
Maximum Output Power 1	34.5			dBm	Temp=+25 °C, V _{BATT} =3.6V, V _{RAMP} ≤1.6V
Maximum Output Power 2	32.5			dBm	Temp=+85 °C, V _{BATT} =3.0V, V _{RAMP} ≤1.6V
Total Efficiency	48	52		%	At P _{OUT MAX} , V _{BATT} =3.6V, V _{RAMP} =1.6V
I _{BATT}		1.9	2.5	A	At P _{OUT MAX} , V _{BATT} =3.6V, V _{RAMP} =1.6V
Input Power Range	0	+3	+6	dBm	Maximum output power guaranteed at minimum drive level
Output Noise Power		-83	-80	dBm	RBW=100kHz, 925MHz to 935MHz, P _{OUT} ≤ +34.5dBm
		-85	-83	dBm	RBW=100kHz, 935MHz to 960MHz, P _{OUT} ≤ +34.5dBm
Forward Isolation 1		-38	-30	dBm	TXEnable=Low, P _{IN} =+6dBm
Forward Isolation 2			-10	dBm	TXEnable=High, P _{IN} =+6dBm, V _{RAMP} =0.26V
Cross Band Isolation 2f ₀			-20	dBm	V _{RAMP} =0.26V to V _{RAMP_RP}
Second Harmonic		-15	-6	dBm	V _{RAMP} =0.26V to V _{RAMP_RP}
Third Harmonic		-30	-11	dBm	V _{RAMP} =0.26V to V _{RAMP_RP}
All Other Non-Harmonic Spurious			-36	dBm	V _{RAMP} =0.26V to V _{RAMP_RP}
Input Impedance		50		Ω	
Input VSWR		2:1	2.5:1		P _{IN} =0dBm to +6dBm, V _{RAMP} set to P _{OUT} =6dBm to V _{RAMP} =V _{RAMP_RP} T=-20 °C to +85 °C
Output Load VSWR Stability	8:1				Spurious<-36dBm, RBW=3MHz Set V _{RAMP} where P _{OUT} ≤34.5dBm into 50Ω load
Output Load VSWR Ruggedness	10:1				Set V _{RAMP} where P _{OUT} ≤34.5dBm into 50Ω load. No damage or permanent degradation to part.
Output Load Impedance		50		Ω	Load impedance presented at RF OUT pad
Power Control V_{RAMP}					
Power Control Range	50	55		dB	V _{RAMP} =0.26V to V _{RAMP_RP}
Transient Spectrum		-35		dBm	V _{RAMP} =V _{RAMP_RP}
Transient Spectrum Under Extreme Conditions			-22	dBm	Temp=-20 °C to +85 °C, V _{BATT} ≥3.0V. Ramping shape same as for Condition: Temp=25 °C, V _{BATT} =3.6V, V _{RAMP} =V _{RAMP_RP}
Power Degradation from Nominal Conditions					V _{BATT} =3.0V to 4.6V, Temp=-20 °C to +85 °C, P _{IN} =0dBm to 5dBm,
5dBm to 15dBm	-5		+5	dB	Relative to output power for condition: V _{BATT} =3.6V, P _{IN} =+3dBm, Temp=25 °C, Freq=836.5MHz.
15dBm to 31dBm	-3		+3	dB	Output power variation measured at set V _{RAMP}
34.5dBm	-2		+2	dB	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
GSM900 8-PSK Parameters				MHz	Temp = +25 °C, V _{CC} = 3.6V, P _{IN} = 3 dBm, 25% Duty Cycle, Pulse Width = 1154 μs, V _{RAMP} MAX = V _{RAMP} RP
Peak Output Power	32.5			dBm	
Efficiency		23		%	Output Power = 29 dBm
V _{RAMP} Loop Bandwidth	2.5	10		MHz	
V _{RAMP} Group Delay		35		nS	
V _{RAMP} Group Delay Variation	-12		12	nS	

Notes:

V_{RAMP}RP = V_{RAMP} set for 34.5 dBm at nominal conditions.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (DCS Mode)					Temp=25 °C, V _{BATT} =3.6V, V _{RAMP} =V _{RAMP_RP} , P _{IN} =3dBm, Freq=1710MHz to 1785MHz, 25% Duty Cycle, pulse width=1154μs
Operating Frequency Range	1710		1785	MHz	
Maximum Output Power 1	32.0			dBm	Temp=+25 °C, V _{BATT} =3.6V, V _{RAMP} ≤1.6V
Maximum Output Power 2	30.0			dBm	Temp=+85 °C, V _{BATT} =3.0V, V _{RAMP} ≤1.6V
Total Efficiency	46	51		%	At P _{OUT MAX} , V _{BATT} =3.6V, V _{RAMP} =1.6V
I _{BATT}		1.2	1.6	A	At P _{OUT MAX} , V _{BATT} =3.6V, V _{RAMP} =1.6V
Input Power Range	0	+3	+6	dBm	Maximum output power guaranteed at minimum drive level
Output Noise Power			-80	dBm	RBW=100kHz, 1805MHz to 1880MHz, P _{OUT} ≤ 32dBm
Forward Isolation 1			-30	dBm	TXEnable=Low, P _{IN} =+6dBm
Forward Isolation 2			-10	dBm	TXEnable=High, V _{RAMP} =0.26V, P _{IN} =+6dBm
Second Harmonic		-15	-7	dBm	V _{RAMP} =0.26V to V _{RAMP_RP}
Third Harmonic		-30	-11	dBm	V _{RAMP} =0.26V to V _{RAMP_RP}
All Other Non-Harmonic Spurious			-36	dBm	V _{RAMP} =0.26V to V _{RAMP_RP}
Input Impedance		50		Ω	
Input VSWR		2:1	2.5:1		P _{IN} =0dBm to +6dBm, V _{RAMP} set to P _{OUT} =6dBm to V _{RAMP} =V _{RAMP_RP} T=-20 °C to +85 °C
Output Load VSWR Stability	8:1				Spurious<-36dBm, RBW=3MHz Set V _{RAMP} where P _{OUT} ≤32dBm into 50Ω load
Output Load VSWR Ruggedness	10:1				Set V _{RAMP} where P _{OUT} ≤32dBm into 50Ω load. No damage or permanent degradation to part.
Output Load Impedance		50		Ω	Load impedance presented at RF OUT pad
Power Control V_{RAMP}					
Power Control Range	50			dB	V _{RAMP} =0.26V to V _{RAMP_RP}
Transient Spectrum		-35		dBm	V _{RAMP} =V _{RAMP_RP}
Transient Spectrum Under Extreme Conditions			-22	dBm	Temp=-20 °C to +85 °C, V _{BATT} ≥3.0V. Ramping shape same as for Condition: Temp=25 °C, V _{BATT} =3.6V, V _{RAMP} =V _{RAMP_RP}
Power Degradation from Nominal Conditions					V _{BATT} =3.0V to 4.6V, Temp=-20 °C to +85 °C, P _{IN} =0dBm to 5dBm,
0dBm to 15dBm	-5		+5	dB	Relative to output power for condition: V _{BATT} =3.6V, P _{IN} =+3dBm, Temp=25 °C,
15dBm < 32dBm	-3		+3	dB	Freq=1747.5MHz.
32dBm	-2		+2	dB	Output power variation measured at set V _{RAMP}

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DCS 8-PSK Parameters				MHz	Temp = +25 °C, V _{CC} = 3.6V, P _{IN} = 3 dBm, 25% Duty Cycle, Pulse Width = 1154 μs, V _{RAMP} MAX = V _{RAMP} RP
Peak Output Power	31.7			dBm	
Efficiency		25.5		%	Output Power = 28.2 dBm
V _{RAMP} Loop Bandwidth	2.5	10		MHz	
V _{RAMP} Group Delay		35		nS	
V _{RAMP} Group Delay Variation	-12		12	nS	

Notes:

V_{RAMP}RP = V_{RAMP} set for 32 dBm at nominal conditions.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (PCS Mode)					Temp=25 °C, V _{BATT} =3.6V, V _{RAMP} =V _{RAMP_RP} , P _{IN} =3dBm, Freq=1850 MHz to 1910MHz, 25% Duty Cycle, pulse width =1154μs
Operating Frequency Range	1850		1910	MHz	
Maximum Output Power 1	32.0			dBm	Temp=+25 °C, V _{BATT} =3.6V, V _{RAMP} ≤1.6V
Maximum Output Power 2	30.0			dBm	Temp=+85 °C, V _{BATT} =3.0V, V _{RAMP} ≤1.6V
Total Efficiency	46	53		%	At P _{OUT MAX} , V _{BATT} =3.6V, V _{RAMP} =1.6V
I _{BATT}		1.0	1.6	A	At P _{OUT MAX} , V _{BATT} =3.6V, V _{RAMP} =1.6V
Input Power Range	0	+3	+6	dBm	Maximum output power guaranteed at minimum drive level
Output Noise Power			-80	dBm	RBW=100 kHz, 1930MHz to 1990MHz, P _{OUT} ≤ 32 dBm
Forward Isolation 1			-30	dBm	TXEnable=Low, P _{IN} =+6dBm
Forward Isolation 2			-10	dBm	TXEnable=High, V _{RAMP} =0.26V, P _{IN} =+6dBm
Second Harmonic		-15	-7	dBm	V _{RAMP} =0.26V to V _{RAMP_RP}
Third Harmonic		-30	-11	dBm	V _{RAMP} =0.26V to V _{RAMP_RP}
All Other Non-Harmonic Spurious			-36	dBm	V _{RAMP} =0.26V to V _{RAMP_RP}
Input Impedance		50		Ω	
Input VSWR		2:1	2.5:1		P _{IN} =0dBm to +6dBm, V _{RAMP} set to P _{OUT} =6dBm to V _{RAMP} =1.6V, T=-20 °C to +85 °C
Output Load VSWR Stability	8:1				Spurious<-36dBm, RBW=3MHz Set V _{RAMP} where P _{OUT} ≤32dBm into 50Ω load
Output Load VSWR Ruggedness	10:1				Set V _{RAMP} where P _{OUT} ≤32dBm into 50Ω load. No damage or permanent degradation to part.
Output Load Impedance		50		Ω	Load impedance presented at RF OUT pad
Power Control V_{RAMP}					
Power Control Range	50			dB	V _{RAMP} =0.26V to V _{RAMP_RP}
Transient Spectrum		-35		dBm	V _{RAMP} =V _{RAMP_RP}
Transient Spectrum Under Extreme Conditions			-22	dBm	Temp=-20 °C to +85 °C, V _{BATT} ≥3.0V. Ramping shape same as for Condition: Temp=25 °C, V _{BATT} =3.6V, V _{RAMP} =V _{RAMP_RP}
Power Degradation from Nominal Conditions					V _{BATT} =3.0V to 4.6V, Temp=-20 °C to +85 °C, P _{IN} =0dBm to 5dBm,
0dBm to 15dBm	-5		+5	dB	Relative to output power for condition: V _{BATT} =3.6V, P _{IN} =+3dBm, Temp=25 °C,
15dBm < 32dBm	-3		+3	dB	Freq=1747.5MHz.
32dBm	-2		+2	dB	Output power variation measured at set V _{RAMP}

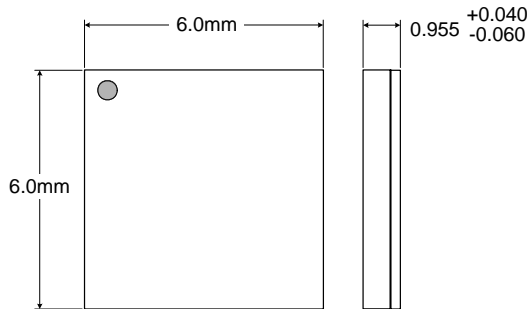
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
PCS 8-PSK Parameters				MHz	Temp = +25 °C, V _{CC} = 3.6V, P _{IN} = 3 dBm, 25% Duty Cycle, Pulse Width = 1154 μs, V _{RAMP} MAX = V _{RAMP} RP
Peak Output Power	31.7			dBm	
Efficiency		27		%	Output Power = 28.2 dBm
V _{RAMP} Loop Bandwidth	2.5	10		MHz	
V _{RAMP} Group Delay		35		nS	
V _{RAMP} Group Delay Variation	-12		12	nS	

Notes:

V_{RAMP}RP = V_{RAMP} set for 32 dBm at nominal conditions.

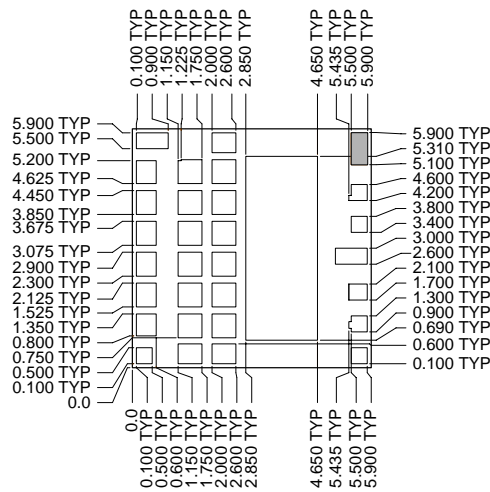
Pin	Function	Description
1	DCS/PCS IN	RF input to the DCS band. This is a 50Ω input.
2	BAND SELECT	Allows external control to select the GSM or DCS band with a logic high or low. A logic low enables the GSM band whereas a logic high enables the DCS band.
3	TX ENABLE	This signal enables the PA module for operation with a logic high.
4	VBATT	Power supply for the module. This should be connected to the battery.
5	GND	
6	VRAMP	Ramping signal from DAC. No external filtering is required.
7	GSM IN	RF input to the GSM band. This is a 50Ω input.
8	GSM OUT	RF output for the GSM band. This is a 50Ω output. The output load line matching is contained internal to the package.
9	DCS/PCS OUT	RF output for the DCS band. This is a 50Ω output. The output load line matching is contained internal to the package.
Pkg Base	GND	

Package Drawing

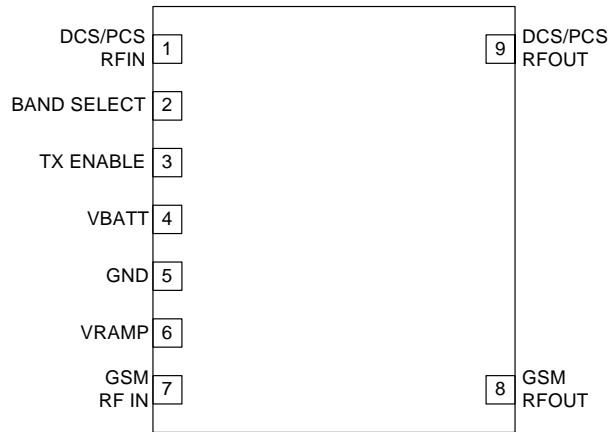


Shaded areas represent pin 1.

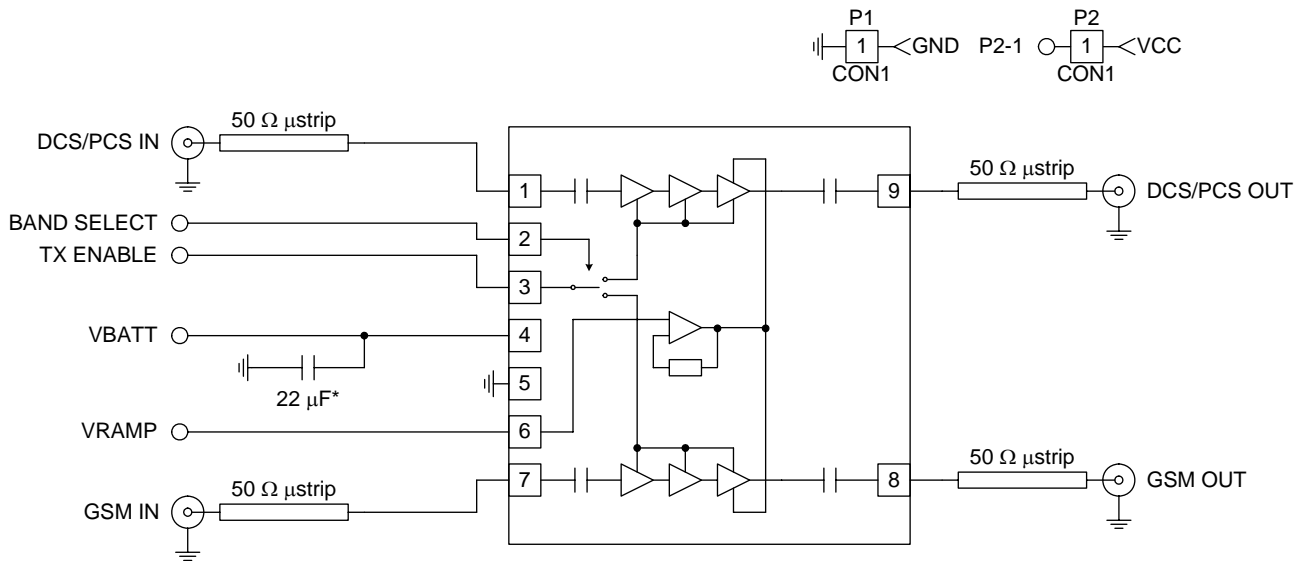
Dimensions in mm.



Pin Out Top Down View



Evaluation Board Schematic



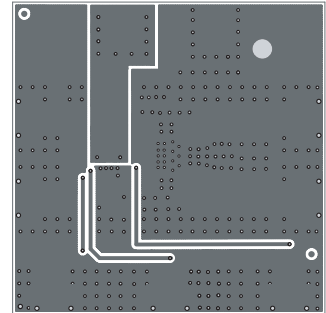
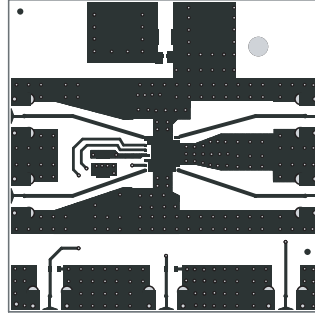
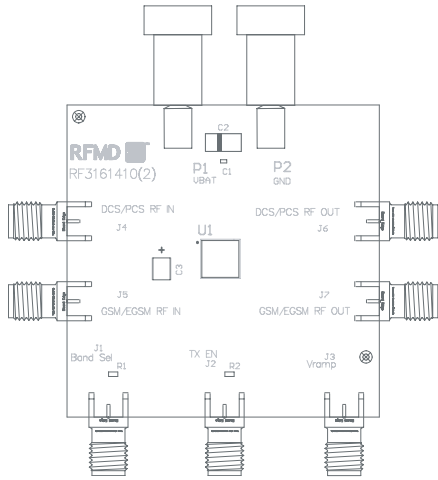
Notes:

- * The value of the VBATT decoupling capacitor depends on the noise level of the phone board. Capacitor type may be either tantalum or ceramic. Some applications may not require this capacitor.
- 1. All the PA output measurements are referenced to the PA output pad (pins 8 and 9).
- 2. The 50 Ω μ strip between the PA output pad and the SMA connector has an approximate insertion loss of 0.1 dB for GSM850/EGSM900 and 0.2 dB for DCS1800/PCS1900 bands.

Evaluation Board Layout

Board Size 2.0" x 2.0"

Board Thickness 0.032", Board Material FR-4, Multi-Layer



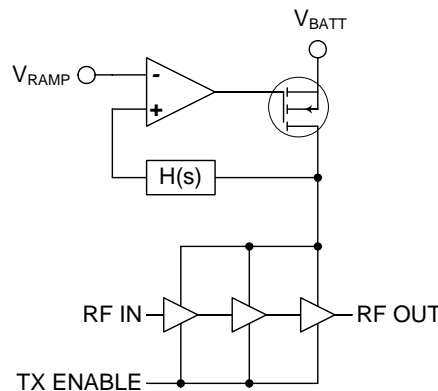
Theory of Operation

Overview

The RF3161 is a quad-band GSM850, EGSM900, DCS1800, and PCS1900 power amplifier module that incorporates an indirect closed loop method of power control. This simplifies the phone design by eliminating the need for the complicated control loop design. The indirect closed loop appears as an open loop to the user and can be driven directly from the DAC output in the baseband circuit.

Theory of Operation

The indirect closed loop is essentially a closed loop method of power control that is invisible to the user. Most power control systems in GSM sense either forward power or collector/drain current. The RF3161 does not use a power detector. A high-speed control loop is incorporated to regulate the collector voltage of the amplifier while the stage are held at a constant bias. The basic circuit is shown in the following diagram.



By regulating the power, the stages are held in saturation across all power levels. As the required output power is decreased from full power down to 0dBm, the collector voltage is also decreased. This regulation of output power is demonstrated in Equation 1 where the relationship between collector voltage and output power is shown. Although load impedance affects output power, supply fluctuations are the dominate mode of power variations. With the RF3161 regulating collector voltage, the dominant mode of power fluctuations is eliminated.

$$P_{dBm} = 10 \cdot \log \left[\frac{(2 \cdot V_{CC} - V_{SAT})^2}{8 \cdot R_{LOAD} \cdot 10^{-3}} \right] \quad (\text{Eq. 1})$$

There are several key factors to consider in the implementation of a transmitter solution for a mobile phone. Some of them are:

- Current draw and system efficiency
- Power variation due to Supply Voltage
- Power variation due to frequency
- Power variation due to temperature
- Input impedance variation
- Noise power
- Loop stability
- Loop bandwidth variations across power levels
- Burst timing and transient spectrum trade offs
- Harmonics

Output power does not vary due to supply voltage under normal operating conditions if V_{RAMP} is sufficiently lower than V_{BATT} . By regulating the collector voltage to the PA the voltage sensitivity is essentially eliminated. This covers most cases where the PA will be operated. However, as the battery discharges and approaches its lower power range the maximum output power from the PA will also drop slightly. In this case it is important to also decrease V_{RAMP} to prevent the power control from inducing switching transients. These transients occur as a result of the control loop slowing down and not regulating power in accordance with V_{RAMP} .

The components following the power amplifier often have insertion loss variation with respect to frequency. Usually, there is some length of microstrip that follows the power amplifier. There is also a frequency response found in directional couplers due to variation in the coupling factor over frequency, as well as the sensitivity of the detector diode. Since the RF3161 does not use a directional coupler with a diode detector, these variations do not occur.

Input impedance variation is found in most GSM power amplifiers. This is due to a device phenomena where C_{BE} and C_{CB} (C_{GS} and C_{SG} for a FET) vary over the bias voltage. The same principle used to make varactors is present in the power amplifiers. The junction capacitance is a function of the bias across the junction. This produces input impedance variations as the V_{apc} voltage is swept. Although this could present a problem with frequency pulling the transmit VCO off frequency, most synthesizer designers use very wide loop bandwidths to quickly compensate for frequency variations due to the load variations presented to the VCO.

The RF3161 presents a very constant load to the VCO. This is because all stages of the RF3161 are run at constant bias. As a result, there is constant reactance at the base emitter and base collector junction of the input stage to the power amplifier.

Noise power in PA's where output power is controlled by changing the bias voltage is often a problem when backing off of output power. The reason is that the gain is changed in all stages and according to the noise formula (Equation 2),

$$F_{TOT} = F1 + \frac{F2 - 1}{G1} + \frac{F3 - 1}{G1 \cdot G2} \tag{Eq. 2}$$

the noise figure depends on noise factor and gain in all stages. Because the bias point of the RF3161 is kept constant the gain in the first stage is always high and the overall noise power is not increased when decreasing output power.

Power control loop stability often presents many challenges to transmitter design. Designing a proper power control loop involves trade-offs affecting stability, transient spectrum and burst timing.

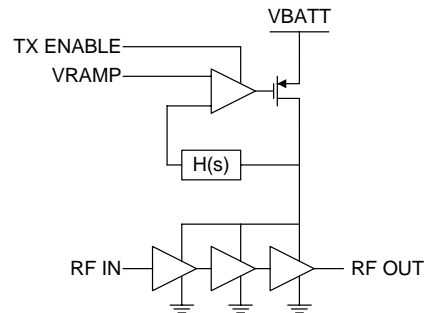
In conventional architectures the PA gain (dB/ V) varies across different power levels, and as a result the loop bandwidth also varies. With some power amplifiers it is possible for the PA gain (control slope) to change from 100dB/V to as high as 1000dB/V. The challenge in this scenario is keeping the loop bandwidth wide enough to meet the burst mask at low slope regions which often causes instability at high slope regions.

The RF3161 loop bandwidth is determined by internal bandwidth and the RF output load and does not change with respect to power levels. This makes it easier to maintain loop stability with a high bandwidth loop since the bias voltage and collector voltage do not vary.

An often overlooked problem in PA control loops is that a delay not only decreases loop stability it also affects the burst timing when, for instance the input power from the VCO decreases (or increases) with respect to temperature or supply voltage. The burst timing then appears to shift to the right especially at low power levels. The RF3161 is insensitive to a change in input power and the burst timing is constant and requires no software compensation.

Switching transients occur when the up and down ramp of the burst is not smooth enough or suddenly changes shape. If the control slope of a PA has an inflection point within the output power range or if the slope is simply too steep it is difficult to prevent switching transients. Controlling the output power by changing the collector voltage is as earlier described based on the physical relationship between voltage swing and output power. Furthermore all stages are kept constantly biased so inflection points are nonexistent.

Harmonics are natural products of high efficiency power amplifier design. An ideal class “E” saturated power amplifier will produce a perfect square wave. Looking at the Fourier transform of a square wave reveals high harmonic content. Although this is common to all power amplifiers, there are other factors that contribute to conducted harmonic content as well. With most power control methods a peak power diode detector is used to rectify and sense forward power. Through the rectification process there is additional squaring of the waveform resulting in higher harmonics. The RF3161 address this by eliminating the need for the detector diode. Therefore the harmonics coming out of the PA should represent the maximum power of the harmonics throughout the transmit chain. This is based upon proper harmonic termination of the transmit port. The receive port termination on the T/R switch as well as the harmonic impedance from the switch itself will have an impact on harmonics. Should a problem arise, these terminations should be explored.



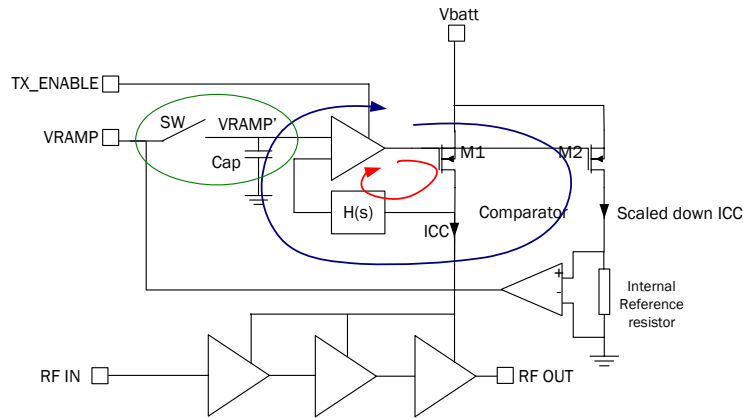
Performance under VSWR

Often overlooked when designing transmitters is the fact that they normally operate under mismatch conditions while they are designed to operate only under perfect 50 ohm loads. This means that in the real application, performance is degraded. This performance degradation may include reduction in output power, increased harmonic levels, increased transient spectrum and catastrophic failures, breakdown. Traditionally designers have verified that the PA does not break during mismatch and this is all verification that has been carried out during mismatch. Modern antennas in handsets often present a load that significantly deviates from nominal impedance. A VSWR of 4:1 is not uncommon. In order not to disturb other phones in the same and close by cells, it is important that the ETSI specifications for transient spectrum, burst timing and spurious emission are fulfilled even during mismatch conditions. The RF3161 is designed to maintain its performance even under high antenna mismatch conditions.

Unlike a current controlled power control loop, the voltage controlled loop is almost impossible to force out of lock. For the current controlled loop this easily happens as the current to the power amplifier that the controller tries to keep constant can not be maintained during some phase angles. If the output stage of the power amplifier faces a high impedance due to mismatch at the antenna, then the last stage simply cannot sink the current it does in a 50Ω load condition. As the loop detects the lower current, the control voltage to the power amplifier increases in an attempt to keep the current constant. As it is impossible to reach the desired current, the control voltage for the power amplifier rails and the error is accumulated in the integrator in the control loop. When the reference value is lowered when the down ramp starts, the integrator still contains the accumulated error and the control voltage to the power amplifier does not track the reference signal. This means that the burst will be too long and that when the error finally reaches zero in the integrator, the control voltage to the power amplifier suddenly decreases and this will contribute to increased levels of transient spectrum at the down ramp.

The Power Star methodology is superior the traditional current control method; it allows the transient spectrum in normal operation to be in the order of -35dBm to -40dBm but also both transient spectrum and the power versus time performance is unaffected even with severe mismatch. In addition to this, the harmonics of the RF3161 is designed to be within ETSI limits for usage with realistic antennas.

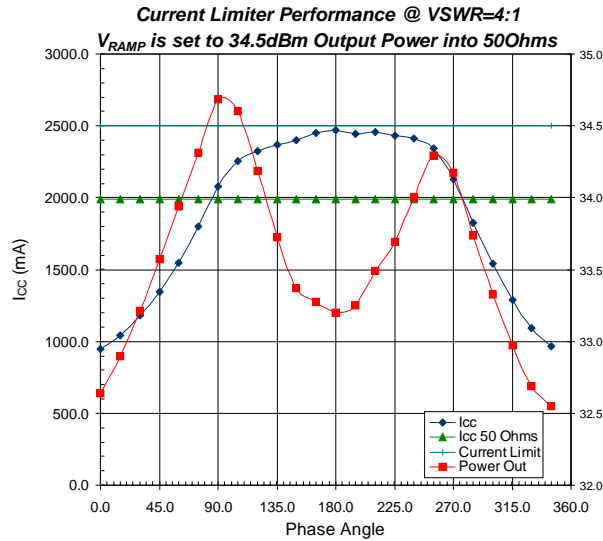
In order to minimize power variation in mismatch conditions, a current limiting circuit is incorporated that limits the PA to 2.5A maximum current drain under all conditions of output power and VSWR.



Integrated Current Limiter Block Diagram

The inner (red) loop is the standard PowerStar control loop described above. The current limiter loop (blue) operates in addition to the PowerStar® control loop.

- FET M2 acts as a current mirror & generates a current through the Internal Reference Resistor proportional to the current in the PA.
- When the voltage across the Internal Reference Resistor exceeds a threshold the comparator is triggered.
- This activates the sample and hold circuit (green oval) at the input to the PowerStar® control loop.
- Thus preventing the collector voltage to the PA from increasing.
- This limits the PA current to a value set by the Internal Reference Resistor.
- The RF3161 is limited to 2.5A maximum current in the PA.
- If the current limiter circuit is triggered, the sample and hold circuit is reset when the V_{RAMP} signal goes low at the end of the burst.
- In normal operation the current limiter is not engaged, and has no affect on the quality of the GMSK or 8-PSK signal through the PA.

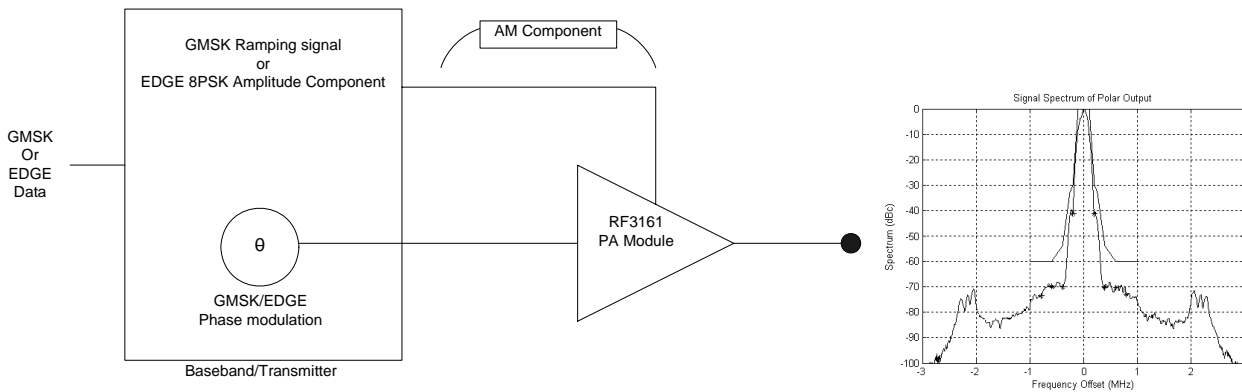


Typical Current and Output Power of the RF3161 into 4:1 VSWR

In poor output VSWR conditions, the current limiter acts to limit peak output power, and peak current draw as shown in the figure.

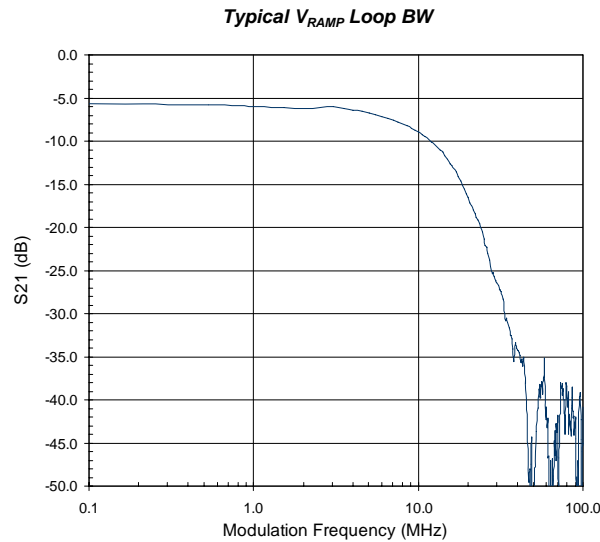
Polar Modulation EDGE

The RF3161 is a non-linear PA module designed for use in open loop Polar Modulation systems. This allows designers to have the efficiency of a PowerStar® PA module as well as the enhanced data rates of EDGE 8PSK modulation. Due to the repeatability and reproducibility of the PowerStar® process, the RF3161 can be operated in an open loop fashion. After initial calibration, the RF3161 will maintain EDGE performance over RF input drive variation, battery voltage variation and case temperature variation. The RF3161 has an internal temperature compensation stage that minimizes RF performance variation over temperature.



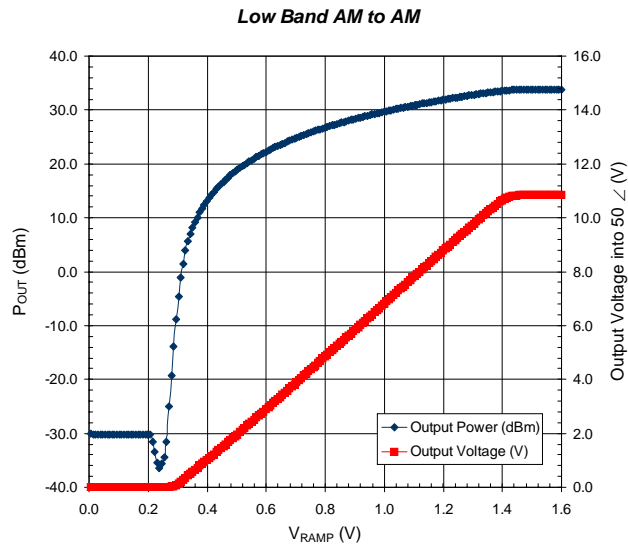
Polar Modulation Power Amplifier

In an EDGE Polar Modulation system, the V_{RAMP} control loop must be capable of tracking the envelope of the EDGE modulation. In order to achieve required EVM and ORFS at the output of the PA module, that envelope signal may contain frequencies up to 5 times the EDGE data rate. Therefore the loop filter in the RF3161 has been broadened to a 3dB Bandwidth of over 2MHz.

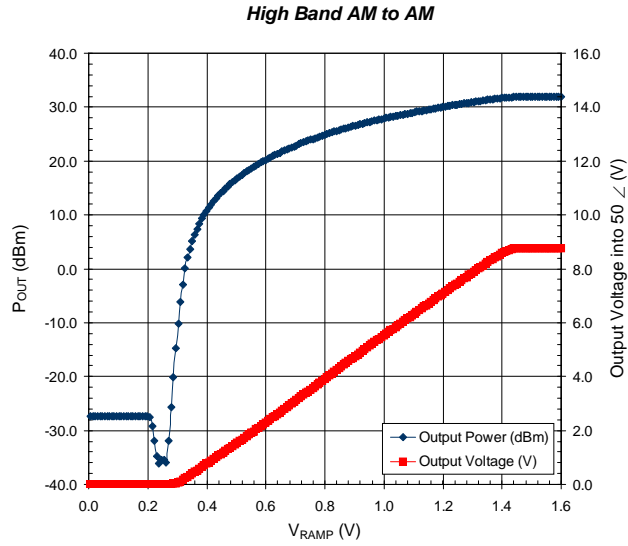


Typical V_{RAMP} Modulation Frequency Response

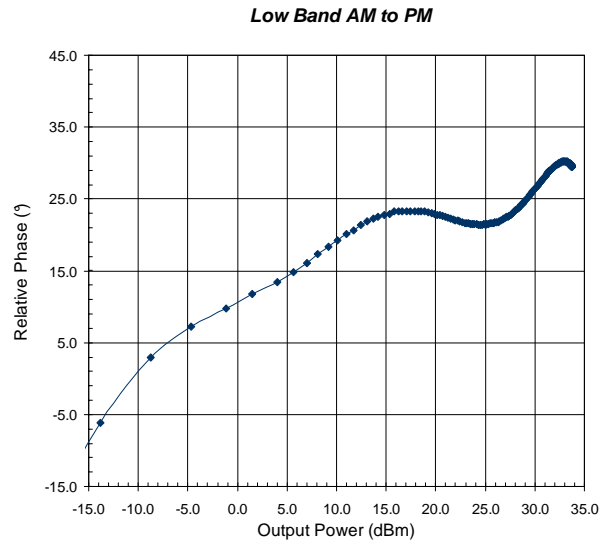
The V_{RAMP} to RF output relationship is also important to system performance. This has both an amplitude and a phase component. The amplitude or AM to AM component is a linear relation between V_{RAMP} level and Output power as described in equation 1 above.



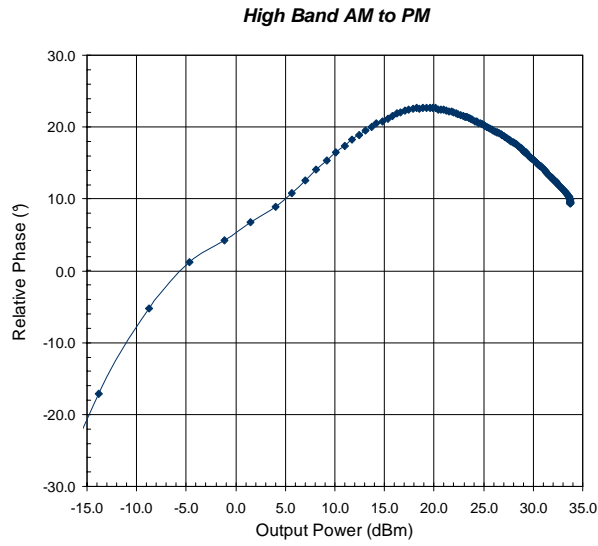
Typical Low Band AM to AM Response



Typical High Band AM to AM Response



Typical Low Band AM to PM Response



Typical High Band AM to PM Response

PCB Design Requirements

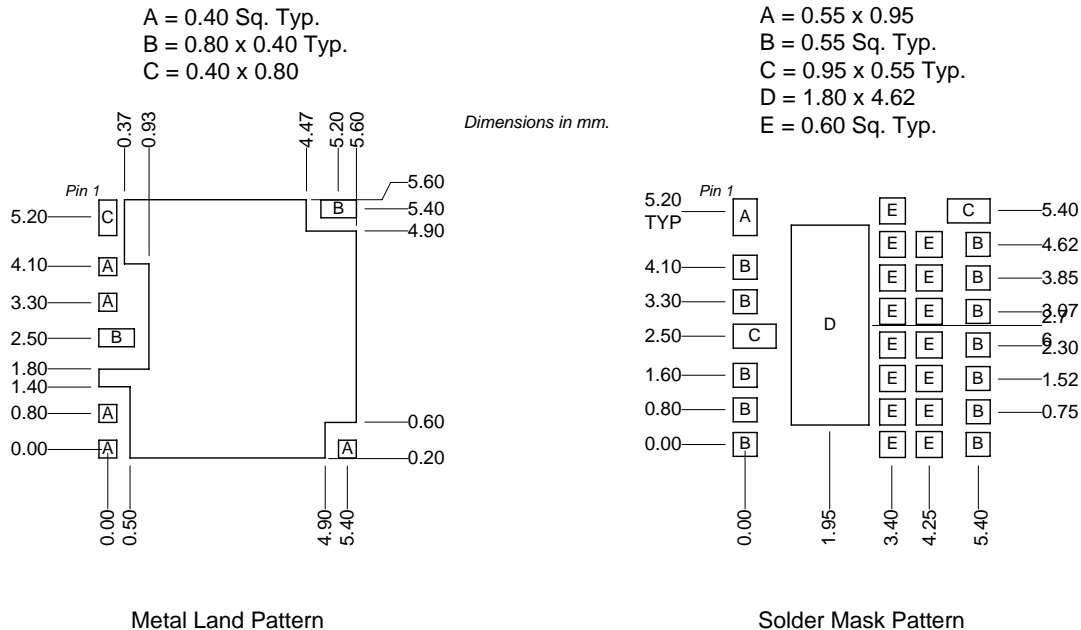
PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern



PCB Metal Land and Solder Mask Patterns (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

Thermal Pad and Via Design

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.