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RF5122

3V TO 3.6V, 2.4GHz TO 2.5GHz LINEAR POWER AMPLIFIER

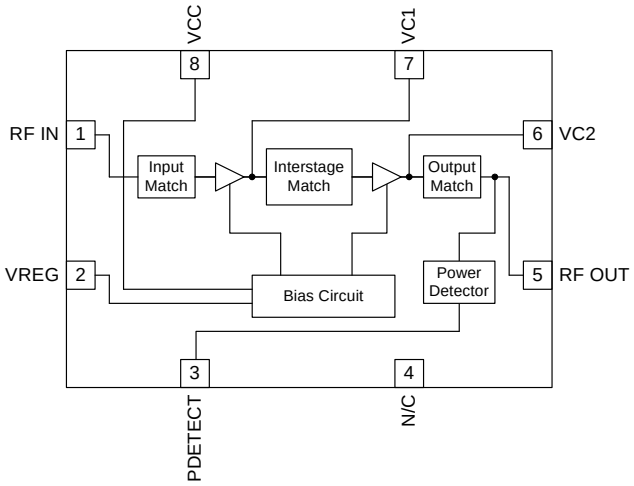
Package Style: QFN, 8-Pin, 2.2mmx2.2mmx0.6mm

Features

- Single Power Supply 3.0V to 3.6V
- 24.5dB Minimum Gain
- Input and Output Matched to 50Ω
- 2400MHz to 2500MHz Frequency Range
- +18dBm @ <2.5% typ EVM, 120mA @ 3.3V_{CC}

Applications

- IEEE802.11b/g/n WiFi Applications
- 2.5GHz ISM Band Applications
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment
- Spread-Spectrum and MMDS Systems



Functional Block Diagram

Product Description

The RF5122 is a linear, medium-power, high-efficiency, two-stage amplifier IC designed specifically for battery-powered WiFi applications such as PC cards, mini PCI, and compact flash applications. The device is manufactured on an advanced InGaP Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 2.5GHz OFDM and other spread-spectrum transmitters. The device is provided in a 2.2mmx2.2mm, 8-pin, QFN with a backside ground. The RF5122 is designed to maintain linearity over a wide range of supply voltages and power outputs. The RF5122 also has built-in power detector and incorporates the input, interstage, and output matching components internally which reduces the component count used externally and makes it easier to incorporate on any design.

Ordering Information

RF5122	Standard 25 piece bag
RF5122SR	Standard 100 piece reel
RF5122TR7	Standard 2500 piece reel
RF5122PCK-410	Fully assembled evaluation board tuned for 2.4GHz to 2.5GHz and 5 loose sample pieces

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ RF MEMS
☑ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V_{DC}
Power Control Voltage (V_{REG})	-0.5 to 3.5	V
DC Supply Current	400	mA
Input RF Power	+5	dBm
Operating Ambient Temperature	-30 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture sensitivity	JEDEC Level 2	
ESD HBM	450	V
MM	50	V

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					Temperature=+25°C, V_{CC}=3.3V, V_{REG}=2.8V pulsed at 1% to 100% duty cycle, Frequency=2450MHz, circuit per evaluation board schematic, unless otherwise specified
Frequency	2.40		2.50	GHz	IEEE802.11g IEEE802.11n
Output Power	18			dBm	At max data rate, OFDM modulation
EVM*		2.5	4	%	RMS, mean
Gain	24.5	25.5		dB	At +18dBm RF P_{OUT} and 54Mbps
Gain Variance			1.25	±dB	-30°C to +85°C
Power Detector					
P_{OUT}=8dBm		0.4	0.7	V	
P_{OUT}=18dBm	1.25	1.35	1.50	V	
Current					
Operating		120	145	mA	At +18dBm RF P_{OUT} and 54Mbps
Quiescent		85		mA	Data rate @≤3.5% EVM RMS, mean, T=-30°C to +50°C
I_{REG} Current		2		mA	V_{CC}=+3.3V_{DC}
Shutdown			10	µA	
Power Supply	3.0	3.3	3.6	V_{DC}	Operating Range
V_{REG1}, V_{REG2} Input Voltage	2.75	2.8	2.9	V_{DC}	Operating Range
Output VSWR			10:1		
Input Return Loss		-15	-10	dB	
Turn-on Time**		0.5	1.0	µS	Output stable to within 90% of final gain
Second Harmonic			-27	dBm	Fundamental frequency is between 2400MHz and 2500MHz; RF P_{OUT}=+18dBm. See note 2.

Notes:
*The EVM specification is obtained with a signal generator that has an EVM floor of less than 0.7%.
**The PA must operate with gated bias voltage input at 1% to 99% duty cycles without any EVM or other parameter degradation.
Note 2: For best harmonic rejection please refer to the harmonic rejection application schematic.

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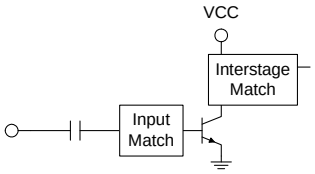
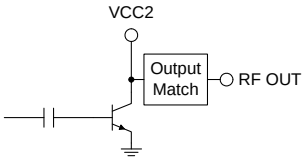
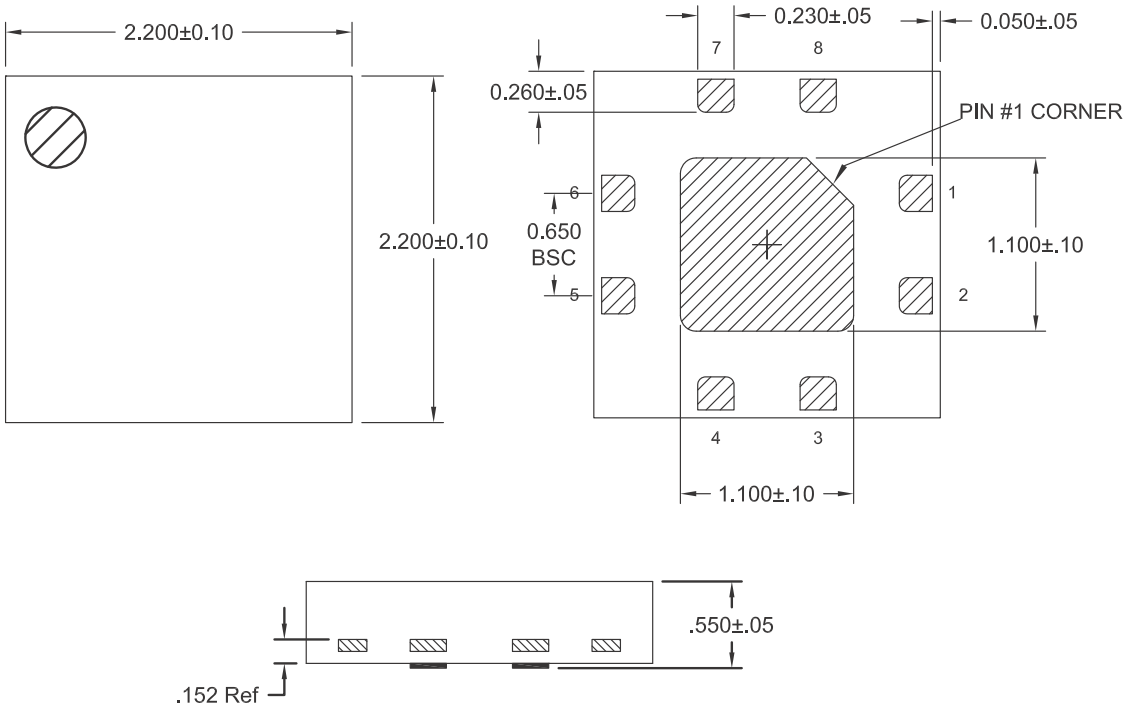
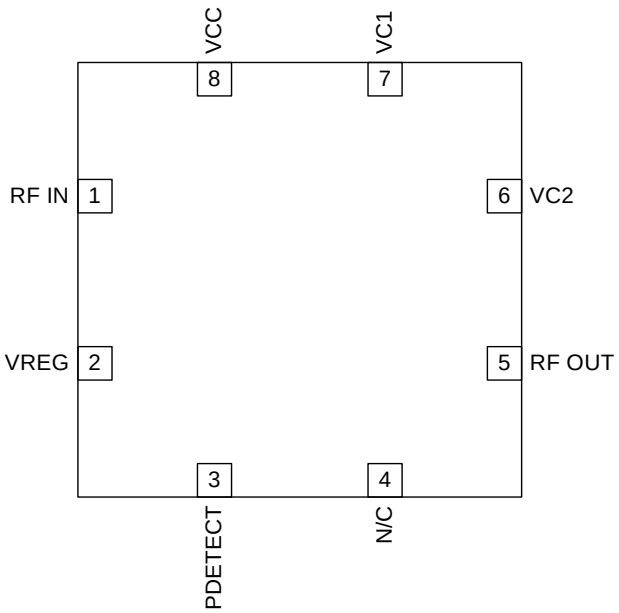
Pin	Function	Description	Interface Schematic
1	RF IN	RF input. Input is matched to 50Ω and DC block is provided internally.	
2	VREG	Bias current control voltage for the first and second amplifier stage.	
3	PDETECT	Power detector which provides an output voltage proportional to the RF output power level. May need external decoupling capacitor for stability. May need external circuitry to bring output voltage to desired level.	
4	N/C	Must be left as no connect, not grounded.	
5	RF OUT	RF output. Output is matched to 50Ω and DC block is provided internally.	
6	VC2	Voltage supply for the second amplifier stage.	
7	VC1	Voltage supply for the first amplifier stage.	
8	VCC	Supply voltage for the bias reference and control circuit. May be connected with V_{C1} and V_{C2} (with a single supply voltage) as long as V_{CC} does not exceed +4.5V_{DC} in this configuration.	
Pkg Base	GND	The center metal base of the QFN package provides DC and RF ground as well as heat sink for the amplifier.	

Package Drawing



Pin Out



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Theory of Operation and Application Information

The RF5122 is a two-stage power amplifier (PA) with a minimum gain of 24.5dB minimum gain in the 2.4GHz to 2.5GHz ISM band. The RF5122 has integrated input, interstage and output matching components thus allowing minimal bill of material (BOM) parts count in end applications. The RF5122 is designed primarily for IEEE802.11b/g/n WiFi applications where the available supply voltage and current are limited. This amplifier will operate to (and below) the lowest expected voltage made available by a typical PCMCIA slot in a laptop PC, and will maintain required linearity at decreased supply voltages.

The RF5122 requires only a single positive supply of 3.3V nominal (or greater) to operate to full specifications. Power control is provided through one bias control input pin (V_{REG}). DC blocking caps are provided internally and the evaluation board circuit (available from RF Micro Devices, Inc. (RFMD)) is optimized for $3.3V_{DC}$ applications.

For best results, the PA circuit layout from the evaluation board should be copied as closely as possible, particularly the ground layout and ground vias. Pin 4 *must* be left as a no-connect on the PCB in order for the PA to work properly. Other configurations may also work, but the design process is much easier and quicker if the layout is copied from the RF5122 evaluation board. Gerber files of RFMD PCBA designs can be provided on request. The RF5122 is a very easy part to implement, but care in circuit layout and component selection is always advisable when designing circuits to operate at 2.5GHz. The RF5122 evaluation board layout and schematic are available using 0201 (US) size components which will help shrink the overall size of the total area of the PA and components of the intended design. Please contact RFMD Sales or Application Engineering for additional data and guidance.

For best performance, it is important to duplicate (as closely as possible) the layout of the evaluation board. The RF5122 has primarily been characterized with a voltage on V_{REG} of $2.8V_{DC}$. If you prefer to use a control voltage that is significantly different than $2.8V_{DC}$, or a different frequency than the recommended frequency range, contact RFMD Sales or Applications Engineering for additional data and guidance.

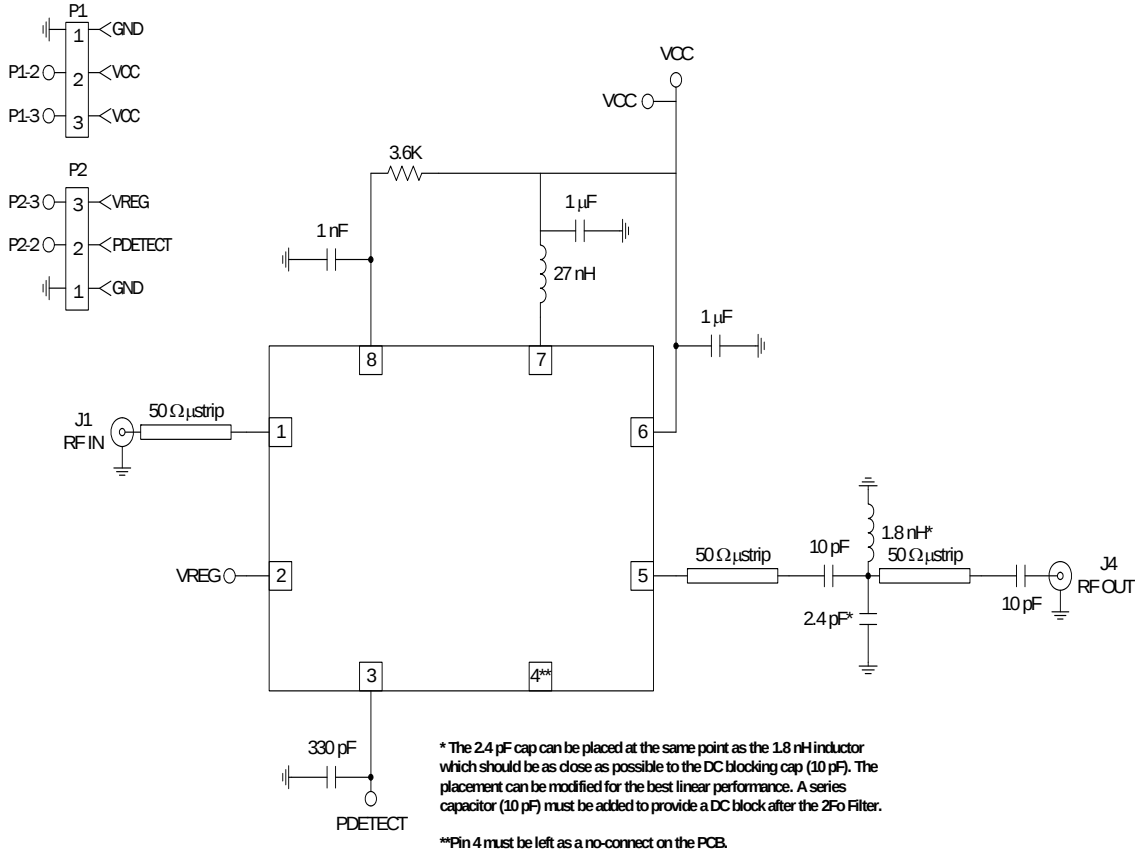
QFN8 Package Area versus Other Small Form Factor Package Areas

Package Type	Length (mm)	Width (mm)	Area (mm^2)	Delta (Δ) (mm^2) to QFN8
SOT 23-6	3.1	3.0	9.30	4.46
QFN12	3.0	3.0	9.00	4.16
SOT 23-5	2.9	2.8	8.12	3.28
QFN8	2.2	2.2	4.84	0.00

An application schematic for 2.5GHz operation is included that has two additional components, one shunt inductor, and one shunt capacitor, on the output for improved second harmonic rejection. This layout provides ~20dB rejecetion at 5GHz with a minimal BOM count.

Application Schematic

for Improved Second Harmonic Performance



*** The 2.4 pF cap can be placed at the same point as the 1.8 nH inductor which should be as close as possible to the DC blocking cap (10 pF). The placement can be modified for the best linear performance. A series capacitor (10 pF) must be added to provide a DC block after the 2Fo Filter.**

****Pin 4 must be left as a no-connect on the PCB.**

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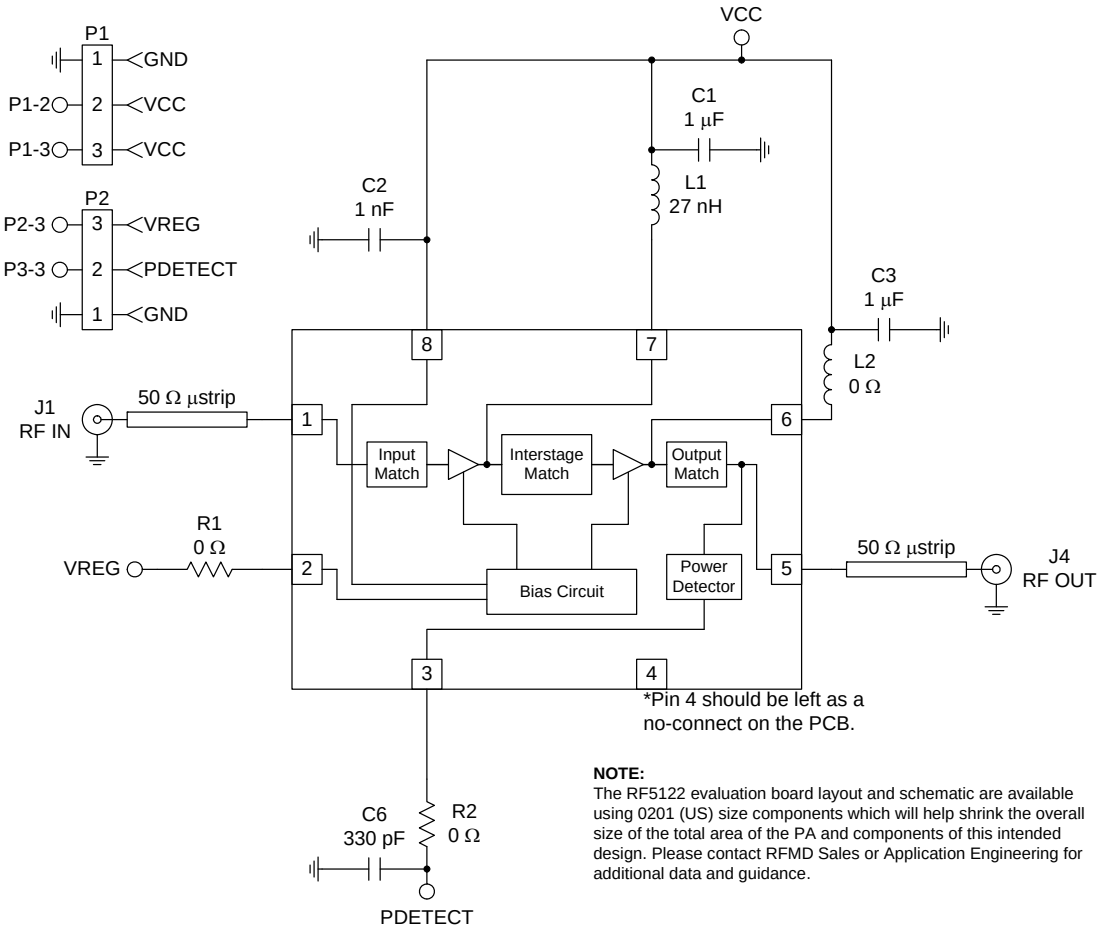
Evaluation Board Schematic



NOTE:
The RF5122 evaluation board layout and schematic are available using 0201 (US) size components which will help shrink the overall size of the total area of the PA and components of this intended design. Please contact RFMD Sales or Application Engineering for additional data and guidance.

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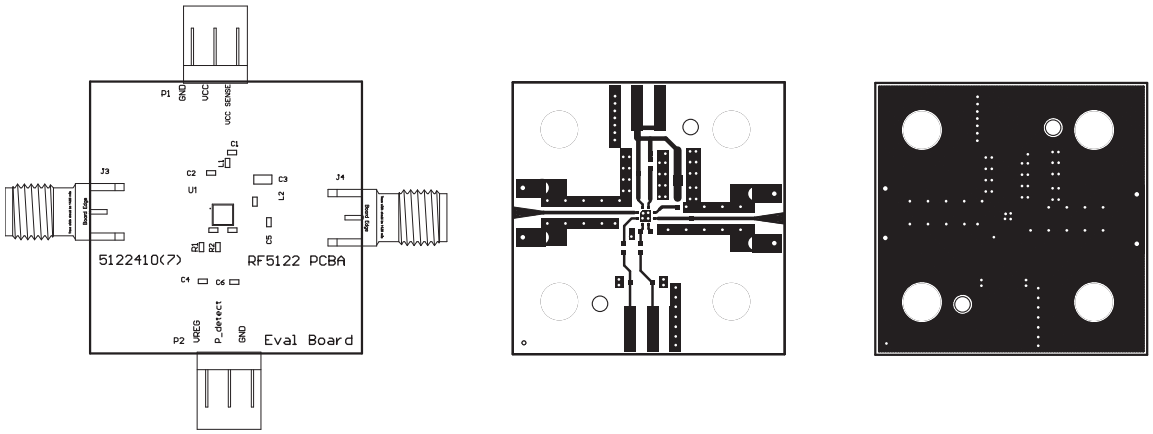
Evaluation Board Layout
Board Size 1.0” x 1.0”
Board Thickness 0.031”; Board Material FR-4; Multi-Layer



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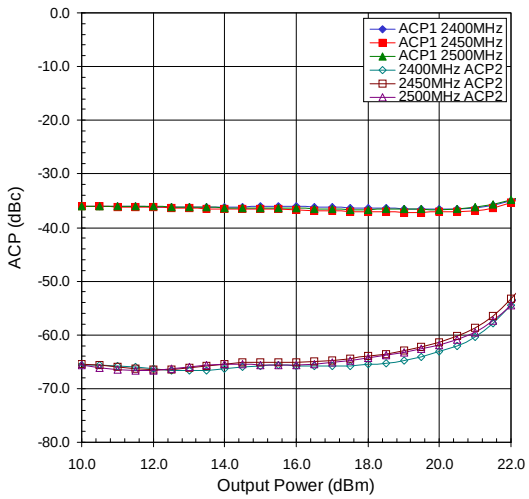
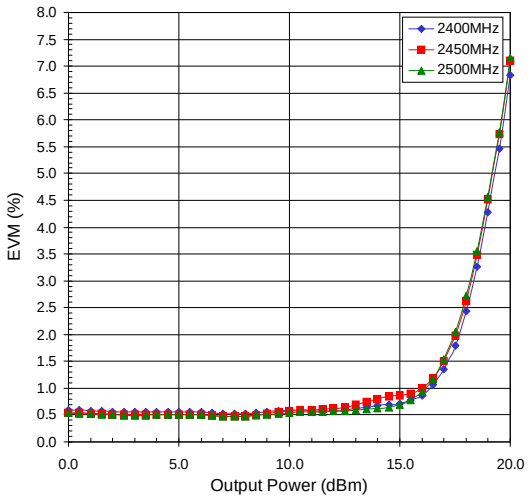
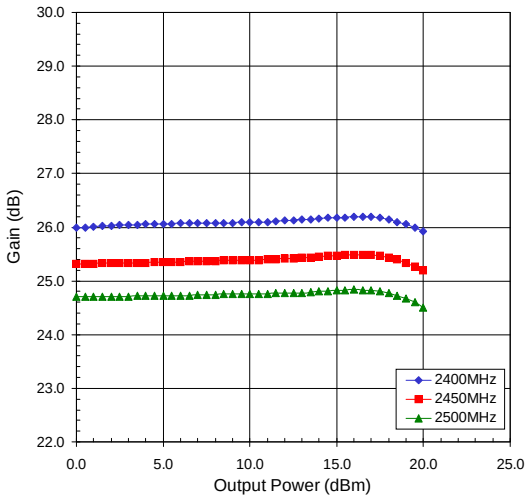
ACP versus P_{OUT}



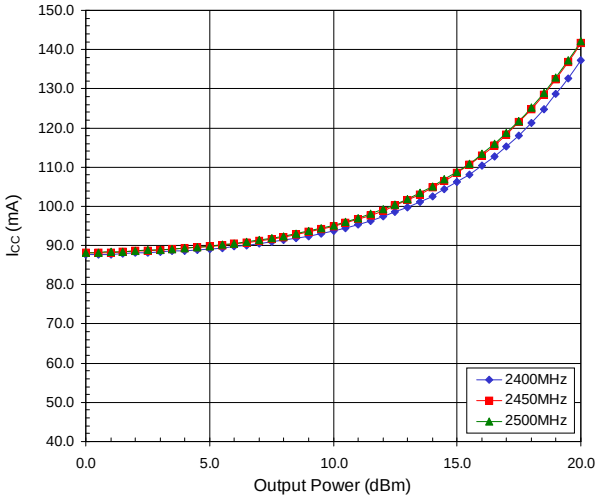
EVM versus P_{OUT}



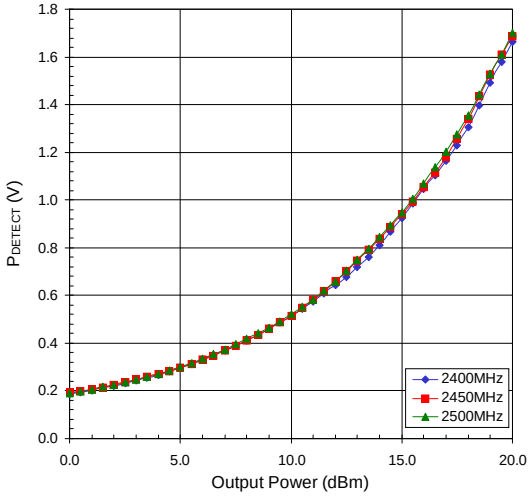
Gain verus P_{OUT}



Operating Current versus P_{OUT}



P_{DETECT} versus P_{OUT}



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PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

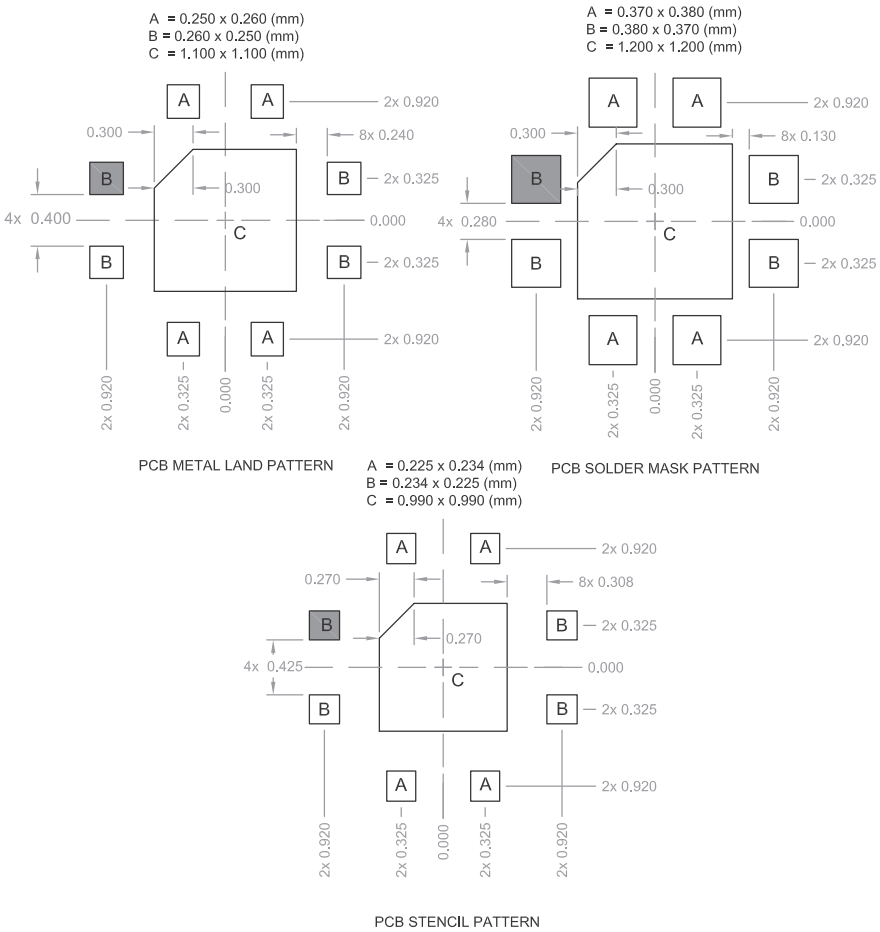
PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

PCB Metal Land and Solder Pattern



Note:
Shaded area represents Pin 1.

Thermal vias for center slug “C” should be incorporated into the PCB design. The number and size of thermal vias will depend on the application, the power dissipation, and this electrical requirements. Example of the number and size of vias can be found on the RFMD evaluation board layout.

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RoHS* Banned Material Content

RoHS Compliant:	Yes
Package total weight in grams (g):	0.008
Compliance Date Code:	N/A
Bill of Materials Revision:	-
Pb Free Category:	e3

Bill of Materials	Parts Per Million (PPM)					
	Pb	Cd	Hg	Cr VI	PBB	PB
Die	0	0	0	0	0	
Molding Compound	0	0	0	0	0	
Lead Frame	0	0	0	0	0	
Die Attach Epoxy	0	0	0	0	0	
Wire	0	0	0	0	0	
Solder Plating	0	0	0	0	0	

This RoHS banned material content declaration was prepared solely on information, including ana
data, provided to RFMD by its suppliers, and applies to the Bill of Materials (BOM) revision no

* DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction o
use of certain hazardous substances in electrical and electronic equipment

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