

Package: Laminate Package, 10-pin, 4 mm x 4 mm x 0.975mm

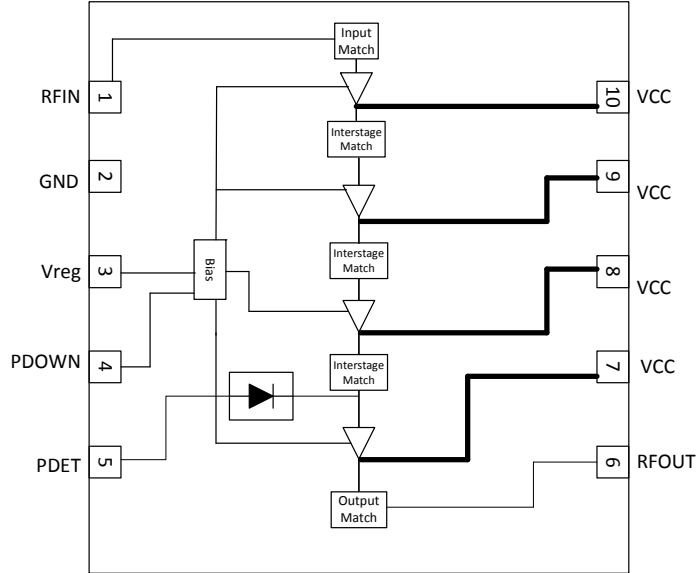


**Features**

- Single Voltage: 5.0V
- 24.5dBm Linear Output Power
- 50Ω Input and Output
- High Gain - 32dB typical

**Applications**

- WLAN 11a/n
- Commercial and Consumer Systems



Functional Block Diagram

**Product Description**

The RF5626 is a fully integrated MMIC which is in a 4 mm x 4 mm laminate package. This fully integrated MMIC is intently specified to address the general market for high power, high band (4.9GHz to 5.85 GHz) 802.11a/n WLAN systems. The RF5626 is a WLAN MMIC PA with integrated detector and integrated input/output match to 50Ω.

**Ordering Information**

RF5626	Power Amplifier
RF5626PCKA-410	Fully Assembled Evaluation Board

**Optimum Technology Matching® Applied**

- |   |                                      |                                     |                                   |
|---|--------------------------------------|-------------------------------------|-----------------------------------|
| <input type="checkbox"/> GaAs HBT             | <input type="checkbox"/> SiGe BiCMOS | <input type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET          | <input type="checkbox"/> Si BiCMOS   | <input type="checkbox"/> Si CMOS    | <input type="checkbox"/> RF MEMS  |
| <input checked="" type="checkbox"/> InGaP HBT | <input type="checkbox"/> SiGe HBT    | <input type="checkbox"/> Si BJT     | <input type="checkbox"/> LD MOS   |

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## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF Applied)	-0.5 to +5.25	V
Supply Voltage (No RF Applied)	-0.5 to +6.0	V
DC Supply Current	TBD	mA
Input RF Power with 50Ω Output Load	TBD	dBm
Input RF Power with Non-50Ω Output Load	TBD	dBm
Operating Ambient Temperature	-30 to +85	°C
Storage Temperature	-40 to +150	°C



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

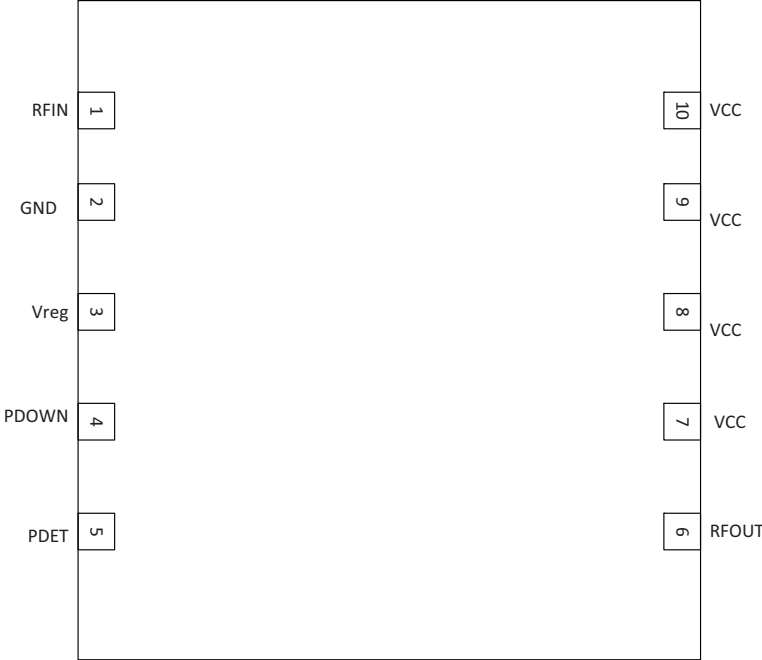
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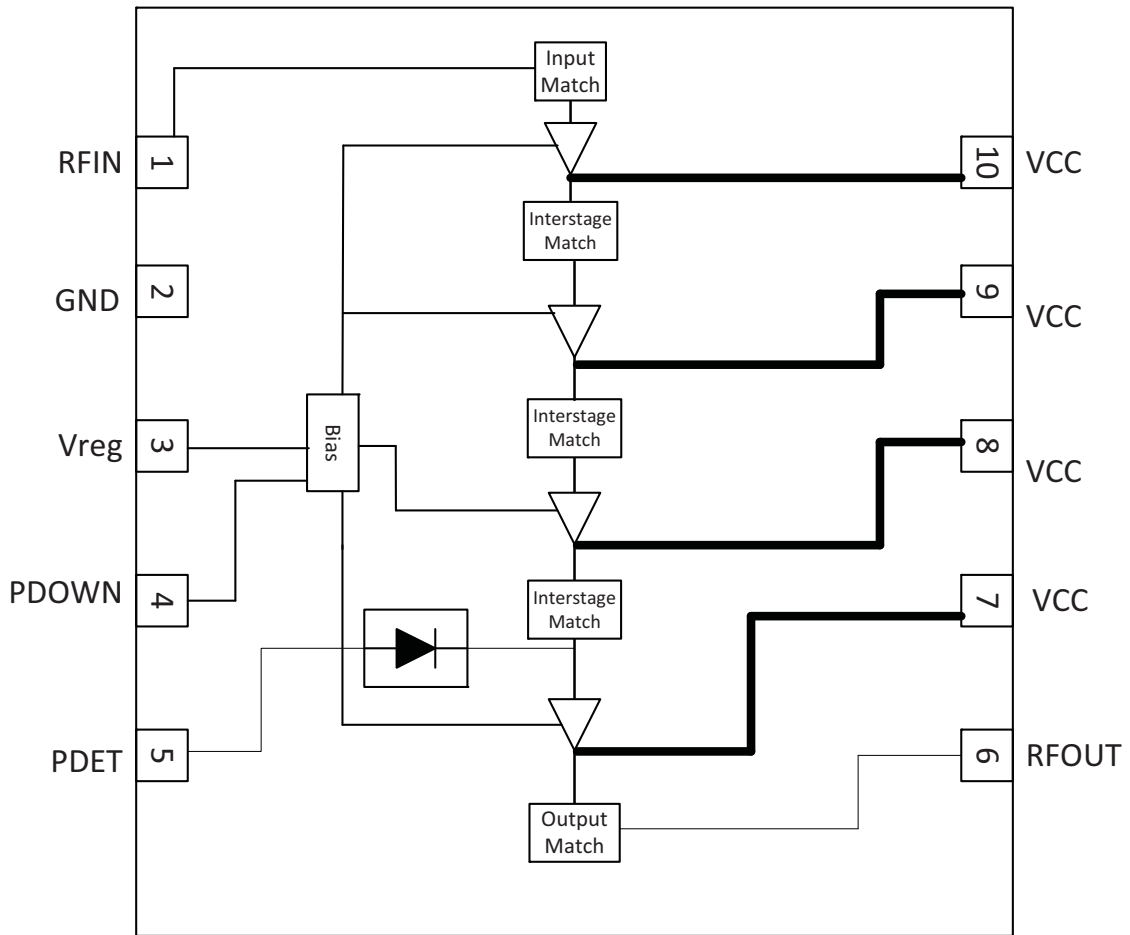
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Typical Conditions</b>					T = 25 °C, V <sub>CC</sub> = 5.0V, V <sub>REG</sub> = 3.0V, P <sub>DOWN</sub> = 3.0V, using a standard IEEE802.11a waveform at 54 Mbps, 64 QAM, unless otherwise noted.
Frequency	4900		5150	MHz	De-rated performance
	5150		5850	MHz	
Output Power		24.5		dBm	V <sub>CC</sub> = 5.0V, V <sub>REG</sub> = 0N
EVM		3		%	At rated P <sub>OUT</sub> , V <sub>CC</sub> = 5V
Gain		32		dB	At rated P <sub>OUT</sub> , 11a modulation
Gain Variation			2.5	dB	
Power Supply					
V <sub>CC</sub>		5		V	
Quiescent Current		500		mA	At V <sub>CC</sub> = 5V
Operation Current		600		mA	At V <sub>CC</sub> = 5V, 11a modulation
Leakage		100		μA	At V <sub>CC</sub> = 5V, V <sub>REG</sub> = 0.2V
V <sub>REG</sub>		3.0		V	
Input Return Loss		15		dB	
Second Harmonic (F <sub>C</sub> = 5.3GHz to 5.85GHz)			-43	dBm	At rated P <sub>OUT</sub> , measured in 1MHz RSB

Pin	Function	Description
<b>1</b>	<b>RFIN</b>	RF input port - DC blocked and 50Ω internally matched.
<b>2</b>	<b>GND</b>	Ground connection.
<b>3</b>	<b>VREG</b>	Bias control pin - requires a regulated supply to maintain nominal bias current.
<b>4</b>	<b>PDOWN</b>	Power down pin - apply <0.6VDC to power down the power amplifier stages; apply 1.75VDC to 5.0VDC to power up. If function is not desired, pin may be connected to VREG
<b>5</b>	<b>PDET</b>	Power detector pin - provides an output voltage proportional to the RF output power level.
<b>6</b>	<b>RFOUT</b>	RF output port - 50Ω internally matched.
<b>7</b>	<b>VCC</b>	Amplifier supply voltage.
<b>8</b>	<b>VCC</b>	Amplifier supply voltage.
<b>9</b>	<b>VCC</b>	Amplifier supply voltage.
<b>10</b>	<b>VCC</b>	Amplifier supply voltage.
<b>Pkg Base</b>	<b>GND</b>	Ground connection - the backside of the package should be connected to the ground plane through as short a connection as possible (e.g.: PCB vias under the device.)

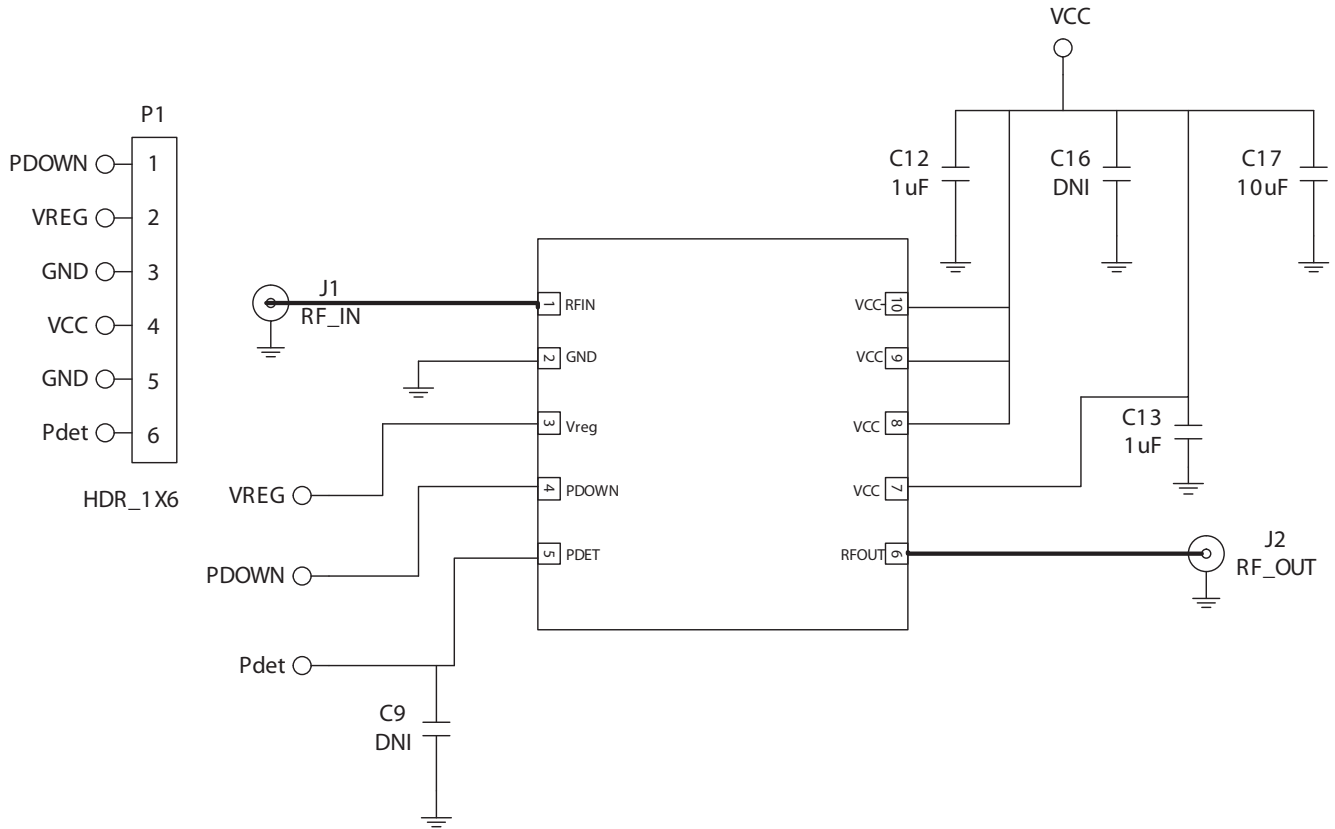
### Pin Out



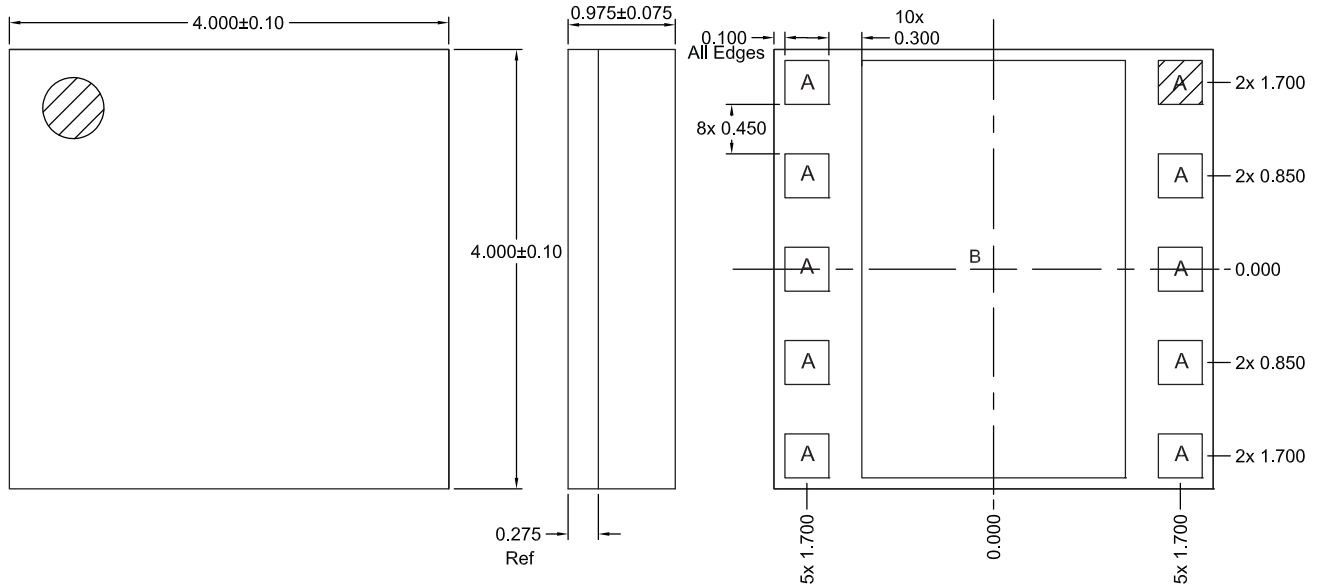
**Detailed Functional Block Diagram**



## Evaluation Board Layout



**Package Drawing**



Notes:

1. Shaded area represents Pin 1 location

A =  $0.400 \times 0.400$  mm  
 B =  $2.400 \times 3.800$  mm

## PCB Design Requirements

### PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

### PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

### PCB Metal Land and Solder Mask Pattern

