Freescale Semiconductor
Data Sheet: Advance Information

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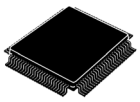
MPC5604E



100 LQFP
14 mm x 14 mm

64 LQFP
10 mm x 10 mm

MPC5604E Microcontroller Data Sheet

- Single issue, 32-bit CPU core complex (e200z0h)
  - Compliant with Power Architecture® embedded category
  - Variable Length Encoding (VLE) only
- Memory
  - 512 KB on-chip Code Flash with ECC and erase/program controller
  - additional 64 (4 × 16) KB on-chip Data Flash with ECC for EEPROM emulation
  - 96 KB on-chip SRAM with ECC
- Fail-safe protection
  - Programmable watchdog timer
  - Non-maskable interrupt
  - Fault collection unit
- Nexus 2+ interface
- Interrupts and events
  - 16-channel eDMA controller
  - 16 priority level controller
  - Up to 32 external interrupts
  - PIT implements four 32-bit timers
  - 120 interrupts are routed via INTC
- General purpose I/Os
  - Individually programmable as input, output or special function
  - 39 on LQFP64
  - 71 on LQFP100[1]
- 1 general purpose eTimer unit
  - 6 timers each with up/down capabilities
  - 16-bit resolution, cascadeable counters
  - Quadrature decode with rotation direction flag
  - Double buffer input capture and output compare
- Communications interfaces
  - 2 LINFlex channels (1 × Master/Slave, 1 × Master Only)
  - 3 DSPI controllers with automatic chip select generation (up to 2/2/4 chip selects)
  - 1 FlexCAN interface (2.0B Active) with 32 message buffers
- One 10-bit analog-to-digital converter (ADC)
  - 8 input channels
    - 4 channels routed to the pins
    - 4 internal connections: 1x temperature sensor, 1x core voltage, 1x IO voltage, 1x VGate Current
  - Conversion time < 1 µs including sampling time at full precision
  - 4 analog watchdogs with interrupt capability
- On-chip CAN/UART bootstrap loader with Boot Assist Module (BAM)
- On-chip TSENS
- 100 MBit Fast Ethernet Controller (FEC)
  - Supports precision timestamps
  - MII on 100-pin LQFP package
  - MII-lite on 64-pin LQFP package
- JPEG/MJPEG 8/12bit Encoder
- 6 x stereo channels audio interface
- 2x I^2C controller module
- CRC module

1.The 100-pin package is not a production package. It is used for software development only.

Table of Contents

1 Overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5604E series of microcontroller units (MCUs).

MPC5604E microcontrollers are members of a new family of next generation microcontrollers built on the Power Architecture. This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the devices.

The MPC5604E microcontroller is a gateway system designed to move data from different sources via Ethernet to a receiving system and vice versa. The supported data sources and sinks are:

- Video data (with 8/10/12 bits per data word)
- Audio data (6× stereo channels)
- RADAR data (2 × 12 bit with <1µs per sample, digitized externally and read in via SPI)
- Other serial communication interfaces including CAN, LIN, and SPI

The Ethernet module has a bandwidth of 10/100 Mbits/sec and supports precision time stamps (IEEE1588). Unshielded twisted pair cables are used to transfer data (via Ethernet) in the car, resulting in a significant reduction of wiring costs by providing inexpensive high bandwidth data links.

1.1 Device summary

Table 1 summarizes the MPC5604E device.

NOTE

The 100-pin package is not a production package. It is used for software development only.

Table 1. Device summary

Feature	MPC5604E	
	100-pin LQFP[1]	64-pin LQFP
CPU	e200z0h, 64 MHz, VLE only, no SPE	
Flash with ECC	CFlash: 512 KB (LC) DFlash: 64 KB (LC, area optimized)	
RAM with ECC	96 KB	
DMA	16 channels	
PIT	yes	
SWT	yes	
FCU	yes	
Ethernet	100 Mbits MII	100 Mbits MII-Lite
Video Encoder	8bpp/12bpp	
Audio Interface	6x Stereo (4x synchronous + 2x synchronous/asynchronous)	
ADC (10-bit)	1× 4 channels + V_{DD_IO} + V_{DDCore} + TSens + VGate Current[2]	
Timer I/O (eTimer)	1×6 channels	
SCI (LINFlex)	2×	
SPI (DSPI)	DSPI_0: 2 chip selects DSPI_1: 2 chip selects DSPI_2: 4 chip selects	

Table 1. Device summary (continued)

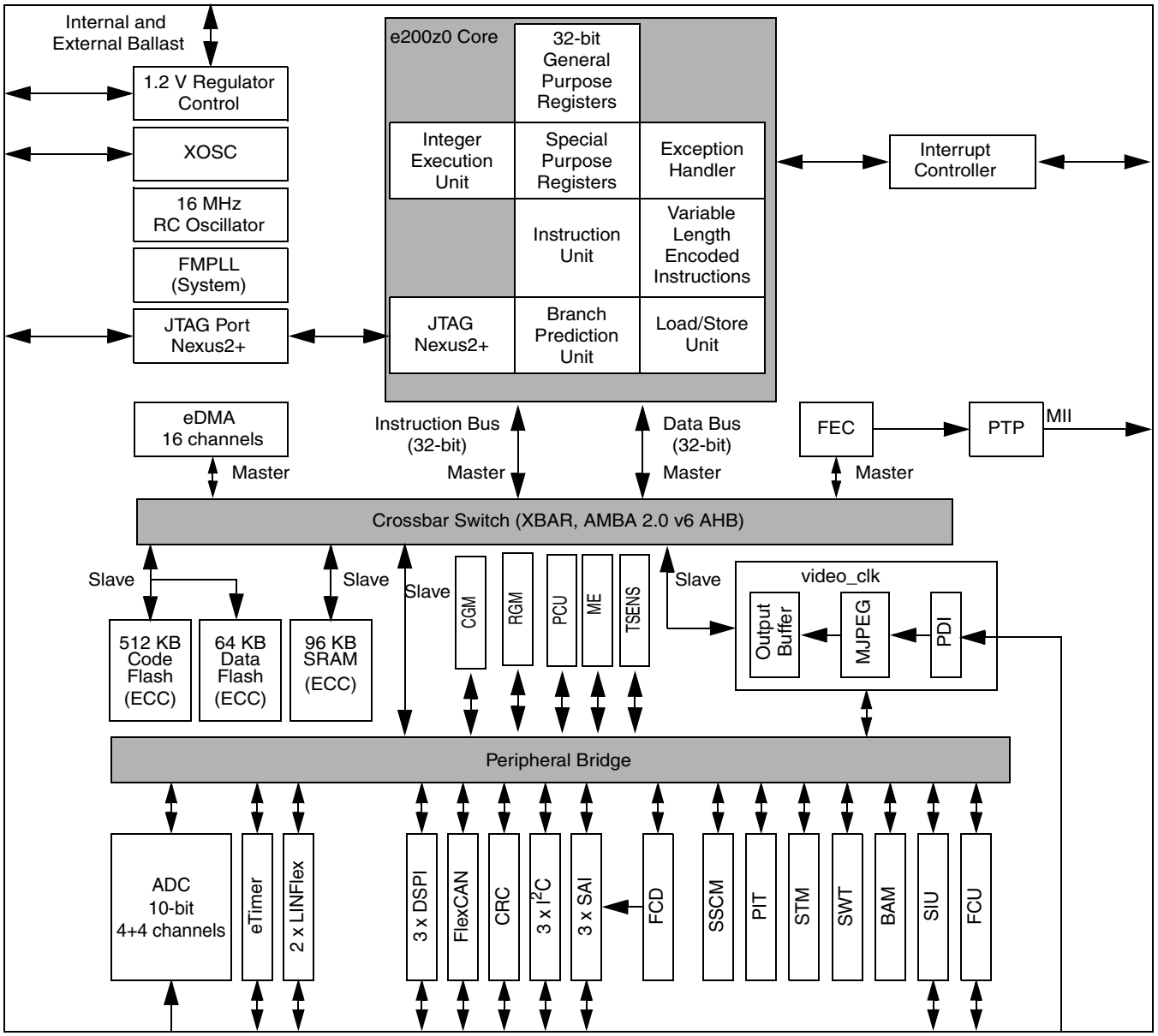
Feature	MPC5604E	
	100-pin LQFP[1]	64-pin LQFP
CAN (FlexCAN)	1×	
IIC	2×	
Supply	3.3 V IO 1.2V Core with dedicated ballast source pin in two modes: • internal ballast or • external supply (using power on reset pin)	
Phase Lock Loop (PLL)	1× FMPLL	
Internal RC Oscillator	16 MHz	
External crystal Oscillator	4 MHz - 40 MHz	
CRC	yes	
Debug	JTAG, Nexus2+	JTAG
Ambient Temperature	–40 to 125 °C	

1 The 100-pin package is not a production package. It is used for software development only.

2 This feature is supported by design, but subject to confirmation after device characterization.

1.2 Block diagram

Figure 1 shows a top-level block diagram of the MPC5604E MCU.



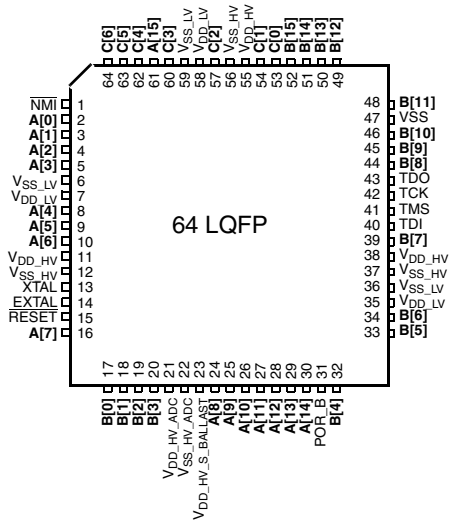
ADC	Analog-to-Digital Converter
BAM	Boot Assist Module
CRC	Cylic Redundancy Check
DSPI	Deserial Serial Peripheral Interface
eDMA	Enhanced Direct Memory Access
eTimer	Enhanced Timer
FCD	Fractional Clock Divider
FCU	Fault Collection Unit
FEC	Fast Ethernet Controller
FlexCAN	Flexible Controller Area Network
FMPLL	Frequency-Modulated Phase-Locked Loop
I2C	Inter-Integrated Circuit serial interface
SAI	Serial Audio Interface 6xStereo
LINFlex	Serial Communication Interface (LIN support)
ME	Mode Entry Module
CGM	Clock Generation Module
PCU	Power Control Unit
RGM	Reset Generation Module
TSENS	Temperature sensor
MJPEG	12-bit Motion JPEG Encoder
PDI	Parallel Data Interface (image sensor)
PIT	Periodic Interrupt Timer
PTP	IEEE 1588 Precision Time Stamps
SIU	System Integration Unit
SRAM	Static Random-Access Memory
SSCM	System Status and Configuration Module
STM	System Timer Module
SWT	Software Watchdog Timer

Figure 1. MPC5604E block diagram

2 Package pinouts and signal descriptions

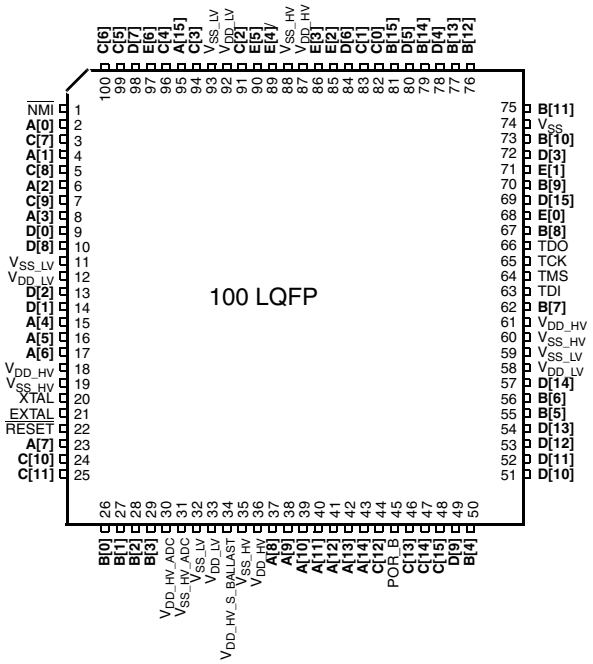
2.1 Package pinouts

The LQFP pinouts are shown in the following figures.



Note:
1. All VDD_HV and VSS_HV pins must be shorted on the board. The ADC supply (VDD_HV_ADC) and ground (VSS_HV_ADC) should be managed independently from other high-voltage supplies, (it may still be supplied from the same high-voltage source, but caution must be taken while routing it on the board.)
2. All VDD_LV and VSS_LV pins must be shorted on the board.

Figure 2. 64-pin LQFP pinout(top view)



1. All VDD_HV and VSS_HV pins must be shorted on the board. The ADC supply (VDD_HV_ADC) and ground (VSS_HV_ADC) should be managed independently from other high-voltage supplies, (it may still be supplied from the same high-voltage source, but caution must be taken while routing it on the board.)
2. All VDD_LV and VSS_LV pins must be shorted on the board.

Figure 3. 100-pin LQFP pinout (top view)[1]

1.The 100-pin package is not a production package. It is used for software development only.

2.2 Signal descriptions

The following sections provide signal descriptions and related information about the functionality and configuration of the MPC5604E devices.

2.2.1 Power supply and reference voltage pins

Table 2 lists the power supply and reference voltage for the MPC5604E devices.

Table 2. Supply pins

Supply			Pin	
Port Pin	**Multi-bonded Power Supplies/Ground**	**Description**	**64-pin**	**100-pin[1]**
VREG control and power supply pins. Pins available on 64-pin and 100-pin package.				
$V_{DD\_HV\_S\_BALLAST}$	$V_{DD\_HV\_S\_BALLAST0}$	Ballast Source/Supply Voltage	23	34
	$V_{DD\_HV\_S\_BALLAST1}$	Ballast Source/Supply Voltage	23	34
ADC0 reference and supply voltage. Pins available on 64-pin and 100-pin package.				
$V_{DD\_HV\_ADC}$	$V_{DD\_HV\_ADC0}$	ADC0 supply voltage with respect to ground ($V_{SS\_HV\_ADC}$)	21	30
	$V_{DD\_HV\_ADR0}$	ADC0 high reference voltage with respect to ground ($V_{SS\_HV\_ADC}$)	21	30
$V_{SS\_HV\_ADC}$	$V_{SS\_HV\_ADC0}$	ADC0 ground voltage with respect to ground	22	31
	$V_{SS\_HV\_ADR0}$	ADC0 low reference voltage with respect to ground	22	31
Power supply pins (3.3 V). Pins available on 64-pin and 100-pin package.				
V_{DD_HV}	$V_{DD\_HV\_IO0\_0}$	Input/output ground voltage	11	18
	$V_{DD\_HV\_OSC0}$	Crystal oscillator amplifier supply voltage	11	18
V_{SS_HV}	$V_{SS\_HV\_IO0\_0}$	Input/output ground voltage	12	19
	$V_{SS\_HV\_OSC0}$	Crystal oscillator amplifier ground	12	19
V_{DD_HV}	$V_{DD\_HV\_IO0\_2}$	3.3 V Input/Output Supply Voltage (supply).	38	61
	$V_{DD\_HV\_FLA1}$	Code and data flash supply voltage	38	61
V_{SS_HV}	$V_{SS\_HV\_IO0\_2}$	Input/output ground voltage	37	60
	$V_{ss\_HV\_FLA1}$	Code and data flash supply ground	37	60
V_{DD_HV}	$V_{DD\_HV\_IO0\_3}$	3.3 V Input/Output Supply Voltage (supply).	55	87
	$V_{DD\_HV\_FLA0}$	Code and data flash supply voltage	55	88
V_{DD_HV}	$V_{DD\_HV\_IO0\_4}$	3.3 V Input/Output Supply Voltage (supply).	—	36
V_{SS_HV}	$V_{SS\_HV\_IO0\_4}$	3.3 V Input/Output Supply Voltage (supply).	—	35

Table 2. Supply pins (continued)

Supply			Pin	
Port Pin	**Multi-bonded Power Supplies/Ground**	**Description**	**64-pin**	**100-pin[1]**
Power supply pins (1.2 V). Pins available on 64-pin and 100-pin package.				
V_{DD_LV}	$V_{DD\_LV\_COR0\_3}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR0\_3}$ pin.	7	12
	$V_{DD\_LV\_PLL0}$	1.2 V PLL supply voltage	7	12
V_{DD_LV}	$V_{DD\_LV\_COR0\_2}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR0\_2}$ pin.	58	92
	$V_{DD\_LV\_FLA0}$	Code and data flash supply voltage	58	92
	$V_{DD\_LV\_COR0\_1}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR0\_1}$ pin.	35	58
	$V_{DD\_LV\_FLA1}$	Code and data flash supply voltage	35	58
V_{SS_LV}	$V_{SS\_LV\_COR0\_3}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected betwee.n these pins and the nearest $V_{DD\_LV\_COR0\_3}$ pin.	6	11
	$V_{SS\_LV\_PLL0}$	PLL supply ground	6	11
	$V_{SS\_LV\_COR0\_2}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected betwee.n these pins and the nearest $V_{DD\_LV\_COR0\_2}$ pin.	59	93
	$V_{SS\_LV\_FLA0}$	Code and data flash supply ground	59	93
	$V_{SS\_LV\_COR0\_1}$	1.2 V supply pins for core logic and data Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR0\_2}$ pin.	36	59
	$V_{SS\_LV\_FLA1}$	Code and data flash supply ground	36	59

[1] The 100-pin package is not a production package. It is used for software development only.

2.2.2 System pins

Table 3 and Table 4 contain information on pin functions for the MPC5604E devices. The pins listed in Table 3 are single-function pins. The pins shown in Table 4 are multi-function pins, programmable via their respective Pad Configuration Register (PCR) values.

Table 3. System pins

Symbol	Description	Direction	Pad speed[1]		Pin	
			SRC = 0	SRC = 1	64-pin	100-pin[2]
Dedicated pins						
$\overline{NMI}$	Non-maskable Interrupt	Input only	Slow	—	1	1
XTAL	Oscillator amplifier output	Output only	—	—	13	20
EXTAL	Input for oscillator amplifier circuit and internal clock generator	Input only	—	—	14	21
TDI[3]	JTAG test data input	Input only	Slow	Medium	40	63
TMS[3]	JTAG state machine control	Input only	Slow	Medium	41	64
TCK[3]	JTAG clock	Input only	Slow	—	42	65
TDO[3]	JTAG test data output	Output only	Slow	Medium	43	66
Reset pin						
$\overline{RESET}$	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	15	22
POR_B	Power-on reset	Input only	—	—	31	45

1 SRC values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

2 The 100-pin package is not a production package. It is used for software development only.

3 Additional board pull resistors are recommended when JTAG pins are not being used on the board or application.

2.2.3 Pin muxing

Table 4 defines the pin list and muxing for the MPC5604E devices.

Each row of Table 4 shows all the possible ways of configuring each pin, via “alternate functions”. The default function assigned to each pin after reset is the ALT0 function.Pins marked as external interrupt capable can also be used to resume from STOP and HALT mode.

MPC5604E devices provide four main I/O pad types depending of the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved Nexus debugging capability.

Medium and Fast pads can be used in slow configuration to reduce the electromagnetic emissions, at the cost of reducing AC performance.

Table 4. Pin muxing

Port pin	PCR register	Alternate function[1,2,8]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin[6]	
						SRC = 0	SRC = 1	64-pin	100-pin[7]
Port A (16-bit)									
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[0] D[0] — — D[11] SIN EIRQ[0]	SIUL SAI0 — — VID DSPI 1 SIUL	I/O I/O — — I I I	Slow	Medium	2	2
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[1] D[1] SOUT — D[10] EIRQ[1]	SIUL SAI0 DSPI1 — VID SIUL	I/O I/O O — I I	Slow	Medium	3	4
A[2]	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] D[2] SCK D[0] D[9] ETC[5] EIRQ[2]	SIUL SAI0 DSPI1 SAI1 VID ETIMER0 SIUL	I/O I/O I/O I/O I I I	Slow	Medium	4	6
A[3]	PCR[3]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[3] D[3] — D[0] D[8] SIN EIRQ[3]	SIUL SAI0 — SAI2 VID DSPI2 SIUL	I/O I/O — I/O I I I	Slow	Medium	5	8
A[4]	PCR[4]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[4] SYNC SOUT — D[7] ETC[3] EIRQ[4]	SIUL SAI0 DSPI2 — VID ETIMER0 SIUL	I/O I/O O — I I I	Slow	Medium	8	15
A[5]	PCR[5]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[5] SYNC SCK D[0] CLK ETC[4] EIRQ[5]	SIUL SAI1 DSPI2 SAI1 VID ETIMER0 SIUL	I/O I/O I/O I/O I I I	Medium	Fast	9	16

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2,8]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin[6]	
						SRC = 0	SRC = 1	64-pin	100-pin[7]
A[6]	PCR[6]	ALT0 ALT1 ALT2 ALT3 — — — —	GPIO[6] SYNC CS0 — VSYNC D[0] ETC[1] EIRQ[6]	SIUL SAI2 DSPI2 — VID VID ETIMER0 SIUL	I/O I/O I/O — I I I I	Slow	Medium	10	17
A[7]	PCR[7]	ALT0 ALT1 ALT2 ALT3 — — — —	GPIO[7] BCLK CS1 — HREF D[1] ETC[2] EIRQ[7]	SIUL SAI0 DSPI2 — VID VID ETIMER0 SIUL	I/O I/O I/O — I I I I	Slow	Medium	16	23
A[8]	PCR[8]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[8] BCLK CS0 D[0] D[6] RX EIRQ[8]	SIUL SAI1 DSPI1 SAI2 VID LIN1 SIUL	I/O I/O I/O I/O I I I	Slow	Medium	24	37
A[9]	PCR[9]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[9] BCLK CS1 TX D[5] EIRQ[9]	SIUL SAI2 DSPI1 LIN1 VID SIUL	I/O I/O I/O O I I	Slow	Medium	25	38
A[10]	PCR[10]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[10] MCLK ETC[5] — D[4] SIN EIRQ[10]	SIUL SAI2 ETIMER0 — VID DSPI0 SIUL	I/O I/O I/O — I I I	Slow	Medium	26	39
A[11]	PCR[11]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[11] TX CS1 CS0 D[3] RX RX	SIUL CAN0 DSPI0 DSPI1 VID LIN0 LIN1	I/O O O I/O I I I	Slow	Medium	27	40

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2,8]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin[6]	
						SRC = 0	SRC = 1	64-pin	100-pin[7]
A[12]	PCR[12]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[12] TX CS0 TX D[2] RX EIRQ[11]	SIUL LIN0 DSPI0 LIN1 VID CAN0 SIUL	I/O O I/O O I I I	Slow	Medium	28	41
A[13]	PCR[13]	ALT0 ALT1 ALT2 ALT3 —	GPIO[13] CLK F[0] CS0 EIRQ[12]	SIUL IIC1 FCU0 DSPI0 SIUL	I/O I/O O I/O I	Slow	Medium	29	42
A[14]	PCR[14]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[14] DATA F[1] CS1 SIN EIRQ[13]	SIUL IIC1 FCU0 DSPI0 DSPI0 SIUL	I/O I/O O O I I	Slow	Medium	30	43
A[15]	PCR[15]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[15] SCK PPS3 MCLK SCK ETC[0] EIRQ[18]	SIUL DSPI0 CE_RTC SAI1 DSPI1 ETIMER0 SIUL	I/O I/O O I/O I I I	Slow	Medium	61	95
Port B (16-bit)									
B[0]	PCR[16]	ALT0 ALT1 ALT2 ALT3 —	GPIO[16] TX ALARM2 BCLK AN[0]	SIUL CAN0 CE_RTC SAI1 ADC0[8]	I/O O O I/O I	Slow	Medium	17	26
B[1]	PCR[17]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[17] — — D[0] AN[1] RX TRIGGER2	SIUL — — SAI1 ADC0[8] CAN0 CE_RTC	I/O — — I/O I I I	Slow	Medium	18	27
B[2]	PCR[18]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[18] TX PPS2 ALARM1 AN[2] TRIGGER1	SIUL LIN0 CE_RTC CE_RTC ADC0[8] CE_RTC	I/O O O O I I	Slow	Medium	19	28

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2,8]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin[6]	
						SRC = 0	SRC = 1	64-pin	100-pin[7]
B[3]	PCR[19]	ALT0 ALT1 ALT2 ALT3 — — — —	GPIO[19] ETC[2] SOUT PPS1 AN[3] RX EIRQ[14] —	SIUL ETIMER0 DSPI0 CE_RTC ADC0[8] LIN0 SIUL —	I/O I/O I/O O I I I —	Slow	Medium	20	29
B[4]	PCR[20]	ALT0 ALT1 ALT2 ALT3 —	GPIO[20] — — — RX_DV	SIUL — — — FEC	I/O — — — I	Slow	Medium	32	50
B[5]	PCR[21]	ALT0 ALT1 ALT2 ALT3	GPIO[21] TX_D0 DEBUG[0] —	SIUL FEC SSCM —	I/O O I/O —	Slow	Medium	33	55
B[6]	PCR[22]	ALT0 ALT1 ALT2 ALT3	GPIO[22] TX_D1 DEBUG[1] —	SIUL FEC SSCM —	I/O O I/O —	Slow	Medium	34	56
B[7]	PCR[23]	ALT0 ALT1 ALT2 ALT3	GPIO[23] TX_D2 DEBUG[2] —	SIUL FEC SSCM —	I/O O I/O —	Slow	Medium	39	62
B[8]	PCR[24]	ALT0 ALT1 ALT2 ALT3	GPIO[24] TX_D3 DEBUG[3] —	SIUL FEC SSCM —	I/O O I/O —	Slow	Medium	44	67
B[9]	PCR[25]	ALT0 ALT1 ALT2 ALT3	GPIO[25] TX_EN DEBUG[4] —	SIUL FEC SSCM —	I/O O I/O —	Slow	Medium	45	70
B[10]	PCR[26]	ALT0 ALT1 ALT2 ALT3	GPIO[26] MDC DEBUG[5] —	SIUL FEC SSCM —	I/O O I/O —	Slow	Medium	46	73
B[11]	PCR[27]	ALT0 ALT1 ALT2 ALT3	GPIO[27] MDIO DEBUG[6] —	SIUL FEC SSCM —	I/O I/O I/O —	Slow	Medium	48	75
B[12]	PCR[28]	ALT0 ALT1 ALT2 ALT3 —	GPIO[28] — DEBUG[7] — TX_CLK	SIUL — SSCM — FEC	I/O — I/O — I	Slow	Medium	49	76

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2,8]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin[6]	
						SRC = 0	SRC = 1	64-pin	100-pin[7]
B[13]	PCR[29]	ALT0 ALT1 ALT2 ALT3 —	GPIO[29] — — — RX_D0	SIUL — — — FEC	I/O — — — I	Slow	Medium	50	77
B[14]	PCR[30]	ALT0 ALT1 ALT2 ALT3 —	GPIO[30] — — — RX_D1	SIUL — — — FEC	I/O — — — I	Slow	Medium	51	79
B[15]	PCR[31]	ALT0 ALT1 ALT2 ALT3 —	GPIO[31] — — — RX_D2	SIUL — — — FEC	I/O — — — I	Slow	Medium	52	81
Port C (64-pin: 7-bit; 100-pin: 16-bit)									
C[0]	PCR[32]	ALT0 ALT1 ALT2 ALT3 —	GPIO[32] — — — RX_D3	SIUL — — — FEC	I/O — — — I	Slow	Medium	53	82
C[1]	PCR[33]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[33] — — — RX_CLK EIRQ[15]	SIUL — — — FEC SIUL	I/O — — — I I	Slow	Medium	54	83
C[2]	PCR[34]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[34] ETC[0] TX PPS1 D[0] RX EIRQ[16]	SIUL ETIMER0 CAN0 CE_RTC VID LIN0 SIUL	I/O I/O O O I I I	Slow	Medium	57	91
C[3]	PCR[35]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[35] ETC[1] TX SYNC D[1] RX EIRQ[17]	SIUL ETIMER0 LIN0 SAI1 VID CAN0 SIUL	I/O I/O O I/O I I I	Slow	Medium	60	94

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2,8]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin[6]	
						SRC = 0	SRC = 1	64-pin	100-pin[7]
C[4]	PCR[36]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[36] CLK_OUT ETC[4] MCLK TRIGGER1 ABS[0] EIRQ[19]	SIUL MC_CGL ETIMER0 SAI0 CE_RTC MC_RGM SIUL	I/O O I/O I/O I I I	Medium	Fast	62	96
C[5]	PCR[37]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[37] CLK ETC[3] CS2 ABS[2] EIRQ[20]	SIUL IIC0 ETIMER0 DSPI2 MC_RGM SIUL	I/O — I/O O I I	Slow	Medium	63	99
C[6]	PCR[38]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[38] DATA CS0 CS3 FAB EIRQ[21]	SIUL IIC0 DSPI1 DSPI2 MC_RGM SIUL	I/O — I/O O I I	Slow	Medium	64	100
C[7]	PCR[39]	ALT0 ALT1 ALT2 ALT3 —	GPIO[39] TXD — — RXD	SIUL LIN0 — — LIN1	I/O O — — I	Slow	Medium	—	3
C[8]	PCR[40]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[40] TXD — — RXD EIRQ[22]	SIUL LIN1 — — LIN0 SIUL	I/O O — — I I	Slow	Medium	—	5
C[9]	PCR[41]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[41] — — — SIN EIRQ[23]	SIUL — — — DSPI0 SIUL	I/O — — — I I	Slow	Medium	—	7
C[10]	PCR[42]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[42] ETC[5] ETC[4] — SIN EIRQ[24]	SIUL ETIMER0 ETIMER0 — DSPI1 SIUL	I/O I/O I/O — I I	Slow	Medium	—	24
C[11]	PCR[43]	ALT0 ALT1 ALT2 ALT3	GPIO[43] ETC[2] ETC[1] ETC[3]	SIUL ETIMER0 ETIMER0 ETIMER0	I/O I/O I/O I/O	Slow	Medium	—	25

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2,8]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin[6]	
						SRC = 0	SRC = 1	64-pin	100-pin[7]
C[12]	PCR[44]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[44] PPS1 PPS2 ALARM1 TRIGGER1 TRIGGER2 EIRQ[25]	SIUL CE_RTC CE_RTC CE_RTC CE_RTC CE_RTC SIUL	I/O O O O I I I	Slow	Medium	—	44
C[13]	PCR[45]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[45] — — — D[1] EIRQ[26]	SIUL — — — VID SIUL	I/O — — — I I	Slow	Medium	—	46
C[14]	PCR[46]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[46] — — — D[0] EIRQ[27]	SIUL — — — VID SIUL	I/O — — — I I	Slow	Medium	—	47
C[15]	PCR[47]	ALT0 ALT1 ALT2 ALT3 —	GPIO[47] — — — COL	SIUL — — — FEC	I/O — — — I	Slow	Medium	—	48
Port D (100-pin package: 16-bit)									
D[0]	PCR[48]	ALT0 ALT1 ALT2 ALT3	GPIO[48] MDO0 — —	SIUL NEXUS — —	I/O O — —	Slow	Medium	—	9
D[1]	PCR[49]	ALT0 ALT1 ALT2 ALT3	GPIO[49] MCK0 — —	SIUL NEXUS — —	I/O O — —	Slow	Medium	—	14
D[2]	PCR[50]	ALT0 ALT1 ALT2 ALT3	GPIO[50] EVTO — —	SIUL NEXUS — —	I/O O — —	Slow	Medium	—	13
D[3]	PCR[51]	ALT0 ALT1 ALT2 ALT3	GPIO[51] MSEO1 — —	SIUL NEXUS — —	I/O O — —	Slow	Medium	—	72
D[4]	PCR[52]	ALT0 ALT1 ALT2 ALT3	GPIO[52] MSEO0 — —	SIUL NEXUS — —	I/O O — —	Slow	Medium	—	78

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2,8]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin[6]	
						SRC = 0	SRC = 1	64-pin	100-pin[7]
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] MDO3 — —	SIUL NEXUS — —	I/O O — —	Slow	Medium	—	80
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3	GPIO[54] MDO2 — —	SIUL NEXUS — —	I/O O — —	Slow	Medium	—	84
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3	GPIO[55] MDO1 — —	SIUL NEXUS — —	I/O — — —	Slow	Medium	—	98
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3 —	GPIO[56] — — — EVTI	SIUL — — — NEXUS	I/O — — — I	Slow	Medium	—	10
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[57] ETC[3] ETC[2] — RXD EIRQ[28]	SIUL ETIMER0 ETIMER0 — CAN0 SIUL	I/O I/O I/O — I I	Slow	Medium	—	49
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] TXD — —	SIUL CAN0 — —	I/O O — —	Slow	Medium	—	51
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] ETC[0] ETC[5] ETC[4]	SIUL ETIMER0 ETIMER0 ETIMER0	I/O I/O I/O I/O	Slow	Medium	—	52
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] ETC[1] ETC[0] — SIN	SIUL ETIMER0 ETIMER0 — DSPI0	I/O I/O I/O — I	Slow	Medium	—	53
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[61] — — — CRS EIRQ[29]	SIUL — — — FEC SIUL	I/O — — — I I	Slow	Medium	—	54

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2,8]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin[6]	
						SRC = 0	SRC = 1	64-pin	100-pin[7]
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[62] — — — RX_ER EIRQ[30]	SIUL — — — FEC SIUL	I/O — — — I I	Slow	Medium	—	57
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3	GPIO[63] F[0] — —	SIUL FCU0 — —	I/O O — —	Slow	Medium	—	69
Port E (100-pin package: 7-bit)									
E[0]	PCR[64]	ALT0 ALT1 ALT2 ALT3	GPIO[64] F[1] — —	SIUL FCU0 — —	I/O O — —	Slow	Medium	—	68
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3	GPIO[65] TX_ER — —	SIUL FEC — —	I/O O — —	Slow	Medium	—	71
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[66] — — — RXD EIRQ[31]	SIUL — — — LIN1 SIUL	I/O — — — I I	Slow	Medium	—	85
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3	GPIO[67] TXD — —	SIUL LIN1 — —	I/O O — —	Slow	Medium	—	86
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3	GPIO[68] CS0 CS0 CS0	SIUL DSPI0 DSPI1 DSPI2	I/O I/O I/O I/O	Slow	Medium	—	89
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3	GPIO[69] SCK SCK SCK	SIUL DSPI0 DSPI1 DSPI2	I/O I/O I/O I/O	Slow	Medium	—	90
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[70] SOUT SOUT SOUT SIN SIN SIN	SIUL DSPI0 DSPI1 DSPI2 DSPI0 DSPI2 DSPI2	I/O O O O I I I	Slow	Medium	—	97

1 ALT0 is the primary (default) function for each port after reset.

[2] Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIU module. PCR.PA = 00 → ALT0; PCR.PA = 01 → ALT1; PCR.PA = 10 → ALT2; PCR.PA = 11 → ALT3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

[3] Module included on the MCU.

[4] Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.

[5] Programmable via the SRC (Slew Rate Control) bits in the respective Pad Configuration Register.

[6] Additional board pull resistors are recommended when JTAG pins are not being used on the board or application.

[7] The 100-pin package is not a production package. It is used for software development only.

[8] Do not use ALT multiplexing when ADC channels are used.

3 Electrical characteristics

3.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

CAUTION

All of the following figures are indicative and must be confirmed during either silicon validation, silicon characterization or silicon reliability trial.

3.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 5 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 5. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute maximum ratings

Table 6. Absolute Maximum Ratings[1]

Symbol		Parameter	Conditions	Min	Max[2]	Unit
V_{SS}	SR	Device ground	—	V_{SS}	V_{SS}	V
$V_{DD\_HV\_IO}$	SR	3.3 V Input/Output Supply Voltage (supply). Code Flash supply with $V_{DD\_HV\_IO3}$ and Data Flash with $V_{DD\_HV\_IO2}$	—	V_{SS} _ 0.3	V_{SS} + 6.0	V
$V_{SS\_HV\_IO}$	SR	3.3 VInput/Output Supply Voltage (ground). Code Flash ground with $V_{SS\_HV\_IO3}$ and Data Flash with $V_{SS\_HV\_IO2}$	—	V_{SS} _ 0.1	V_{SS} + 0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V Crystal Oscillator Amplifier Supply voltage (supply)	The oscillator and flash supply segments are double-bounded with the $V_{DD\_HV\_IO}$ segments. See $V_{DD\_HV\_IO}$ and $V_{SS\_HV\_IO}$ specifications.			—
$V_{SS\_HV\_OSC}$	SR	3.3 V Crystal Oscillator Amplifier Supply voltage (ground)				
$V_{DD\_HV\_ADC0}$[3]	SR	3.3 V ADC_0 Supply and High Reference voltage	—	V_{SS} _ 0.3	V_{SS} + 6.0	V
$V_{SS\_HV\_ADC0}$	SR	3.3 V ADC_0 Ground and Low Reference voltage	—	V_{SS} _ 0.1	V_{SS} + 0.1	V
$V_{DD\_HV\_REG}$	SR	3.3 V Voltage Regulator Supply voltage	—	V_{SS} _ 0.3	V_{SS} + 6.0	V
TV_{DD}	SR	Slope characteristics on all VDD during power up[4]	—	—	0.1	V/us
$V_{DD\_LV\_COR}$	SR	1.2 V supply pins for core logic (supply)	—	V_{SS} _ 0.3	V_{SS} + 1.4	V
$V_{SS\_LV\_COR}$	SR	1.2 V supply pins for core logic (ground)	—	V_{SS} _ 0.1	V_{SS} + 0.1	V
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IO}$)	—	$V_{SS\_HV\_IO}$ _ 0.3	$V_{DD\_HV\_IO}$ +0.5	V
I_{INJPAD}	SR	Input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all input currents during overload condition	—	–50	50	mA
$T_{STORAGE}$	SR	Storage temperature	—	–55	150	°C
T_J	SR	Junction temperature under bias	—	–40	150	°C
T_A	SR	Ambient temperature under bias	f_{CPU}<64 MHz	–40	125	°C
			f_{CPU}<64 MHz Video use case with internal supply	–40	105	°C

1 Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.

3 MPC5604E's I/O, flash, and oscillator circuit supplies are interconnected. The ADC supply managed independently from other supplies.

4 Guaranteed by device validation.

3.4 Recommended operating conditions

Table 7. Recommended operating conditions

Symbol		Parameter	Conditions	Min	Max[1]	Unit
V_{SS}	SR	Device ground	—	V_{SS}	V_{SS}	V
$V_{DD\_HV\_IO}$	SR	3.3 V input/output supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_IO}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	3.3 V Crystal Oscillator Amplifier Supply voltage (supply)	The oscillator and flash supply segments are double-bounded with the $V_{DD\_HV\_IOx}$ segments. See $V_{DD\_HV\_IOx}$ and $V_{SS\_HV\_IOx}$ specifications.			—
$V_{SS\_HV\_OSC}$	SR	3.3 V Crystal Oscillator Amplifier Supply voltage (ground)				
$V_{DD\_HV\_ADC0}$[2]	SR	3.3 V ADC_0 Supply and High Reference voltage	—	3.0	3.6	V
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.6	V
$V_{DD\_LV\_EXTCOR}$	SR	Externally supplied core voltage	—	1.15	1.32	V
$V_{DD\_LV\_REGCOR}$	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_COR}$	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_COR}$	SR	Internal reference voltage	—	0	0	V
$V_{SS\_HV\_ADC0}$	SR	Ground and Low Reference voltage	—	0	0	V
T_J	SR	Junction temperature under bias		–40	150	°C
T_A	SR	Ambient temperature under bias	f_{CPU}<64 MHz	–40	125	°C
			f_{CPU}<64 MHz Video use case with internal supply	–40	105	°C

1 Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.

2 MPC5604E's I/O, flash, and oscillator circuit supplies are interconnected. The ADC supply managed independently from other supplies.

3.5 Thermal characteristics

Table 8. Thermal characteristics for 100-pin LQFP[1]

Symbol	Parameter	Conditions	Typical value	Unit
$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection[2]	Single layer board—1s	51	°C/W
		Four layer board—2s2p	38	°C/W
$R_{\theta JMA}$	Thermal resistance junction-to-ambient[2]	@ 200 ft./min.[3], single layer board—1s	41	°C/W
		@ 200 ft./min.[3], four layer board—2s2p	32	°C/W
$R_{\theta JB}$	Thermal resistance junction to board[4]	—	23	°C/W
$R_{\theta JCtop}$	Thermal resistance junction to case (top)[5]	—	11	°C/W
Ψ_{JT}	Junction to package top natural convection[6]	—	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Flow rate of forced air flow.

4 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

5 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

6 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 9. Thermal characteristics for 64-pin LQFP[1]

Symbol	Parameter	Conditions	Typical value	Unit
$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection[2]	Single layer board—1s	64	°C/W
		Four layer board—2s2p	45	°C/W
$R_{\theta JMA}$	Thermal resistance junction-to-ambient[2]	@ 200 ft./min.[3], single layer board—1s	52	°C/W
		@ 200 ft./min.[3], four layer board—2s2p	39	°C/W
$R_{\theta JB}$	Thermal resistance junction to board[4]	—	28	°C/W
$R_{\theta JCtop}$	Thermal resistance junction to case (top)[5]	—	14	°C/W
Ψ_{JT}	Junction to package top natural convection[6]	—	3	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

[3] Flow rate of forced air flow.

[4] Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

[5] Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

[6] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.5.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from Equation 1:

$$T_J = T_A + (R_{\theta JA} * P_D) \qquad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in Equation 2 as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using Equation 3:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134 U.S.A.
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, *An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module*, Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
2. G. Kromann, S. Shidore, and S. Addison, *Thermal Modeling of a PBGA for Air-Cooled Applications*, Electronic Packaging and Production, pp. 53-58, March 1998.
3. B. Joiner and V. Adams, *Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*, Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

3.6 Electromagnetic Interference (EMI) characteristics

Table 10. EMI Testing Specifications[1]

Symbol	Parameter	Conditions	Clocks	Frequency Range	Level (Typ)	Unit
Radiated emissions	V_{EME}	V_{DD} = 3.3 V T_A = +25 °C Device Configuration, test conditions and EM testing per standard IEC61967-2.	Oscillator Frequency = 8 MHz; System Bus Frequency = 64 MHz; CPU Freq = 64MHZ No PLL Frequency Modulation	150 kHz–50 MHz	2	dBμV
				50–150 MHz	14	
				150–500 MHz	11	
				500–1000 MHz	7	
				IEC Level	M	
			External Oscillator Freq = 8 MHz System Bus Freq = 64 MHz CPU Freq = 64MHZ 2% PLL Freq Modulation	150 kHz–50 MHz	1	dBμV
				50–150 MHz	11	
				150–500 MHz	7	
				500–1000 MHz	1	
				IEC Level	N	

[1] EMI testing and I/O port waveforms per standard IEC61967-2.

3.7 Electrostatic Discharge (ESD) characteristics

Table 11. ESD ratings[1,2]

Symbol		Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	—	2000	V
$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	—	750 (corners)	V
				500 (other)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification

3.8 Power management electrical characteristics

3.8.1 Power Management Overview

The device supports the following power modes:

- Internal voltage regulation mode
- External voltage regulation mode

3.8.1.1 Internal voltage regulation mode

In this mode, the following supplies are involved:

- $V_{DD\_HV\_IO}$ (3.3V) — This is the main supply provided externally.

- $V_{DD\_LV\_COR}$ (1.2V) — This is the core logic supply. In the internal regulation mode, the core supply is derived from the main supply via an on-chip linear regulator driving an internal PMOS ballast transistor. The PMOS ballast transistors are located in the pad ring and their source connectors are directly bonded to a dedicated pin. See Figure 4.

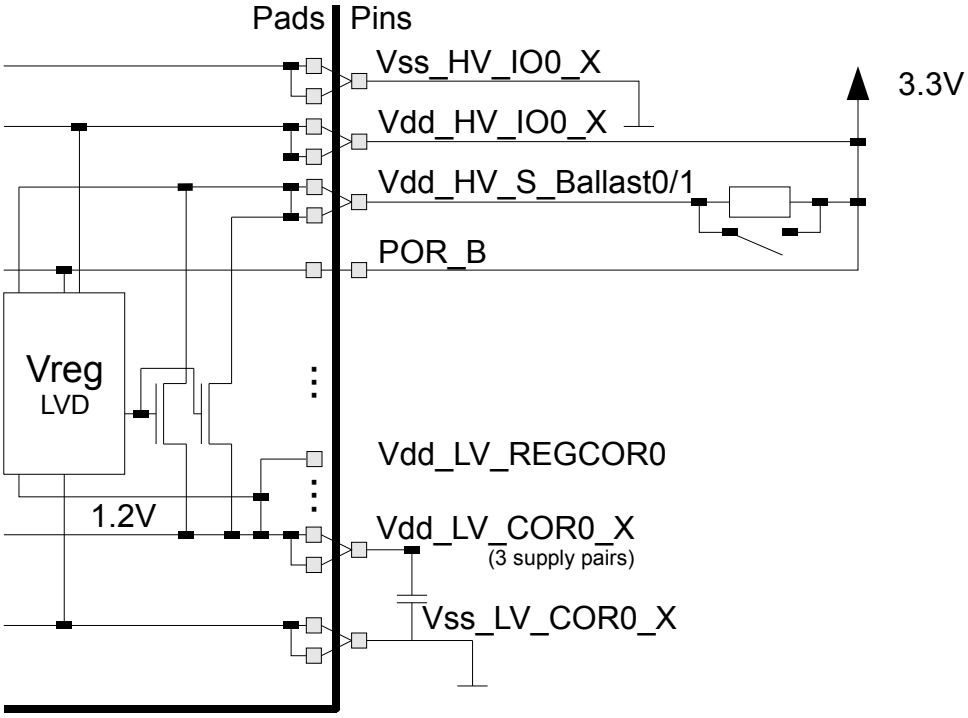


Figure 4. Internal Regulation Mode

The core supply can also be provided externally. Table 12 shows how to connect $V_{DD\_HV\_S\_BALLAST}$ pin for internal and external core supply mode.

NOTE

$V_{DD\_HV\_S\_BALLAST}$ pin is the supply pin, which carries the entire core logic current in the internal regulation mode, while in external regulation mode it is used as a signal to bypass the regulator.

Table 12. Core Supply Select

Mode	$V_{DD\_HV\_S\_Ballast}$
Internal supply mode (via internal PMOS ballast transistors)	$V_{DD\_HV\_IO}$ (3.3V)
External supply mode (e.g., via external switched regulator)	$V_{DD\_LV\_COR}$ (1.2V)

3.8.1.2 External voltage regulation mode

In the external regulation mode, the core supply is provided externally using a switched regulator. This saves on-chip power consumption by avoiding the voltage drop over the ballast transistor. The external supply mode is selected via a board level supply change at the $V_{DD\_HV\_S\_BALLAST}$ pin.

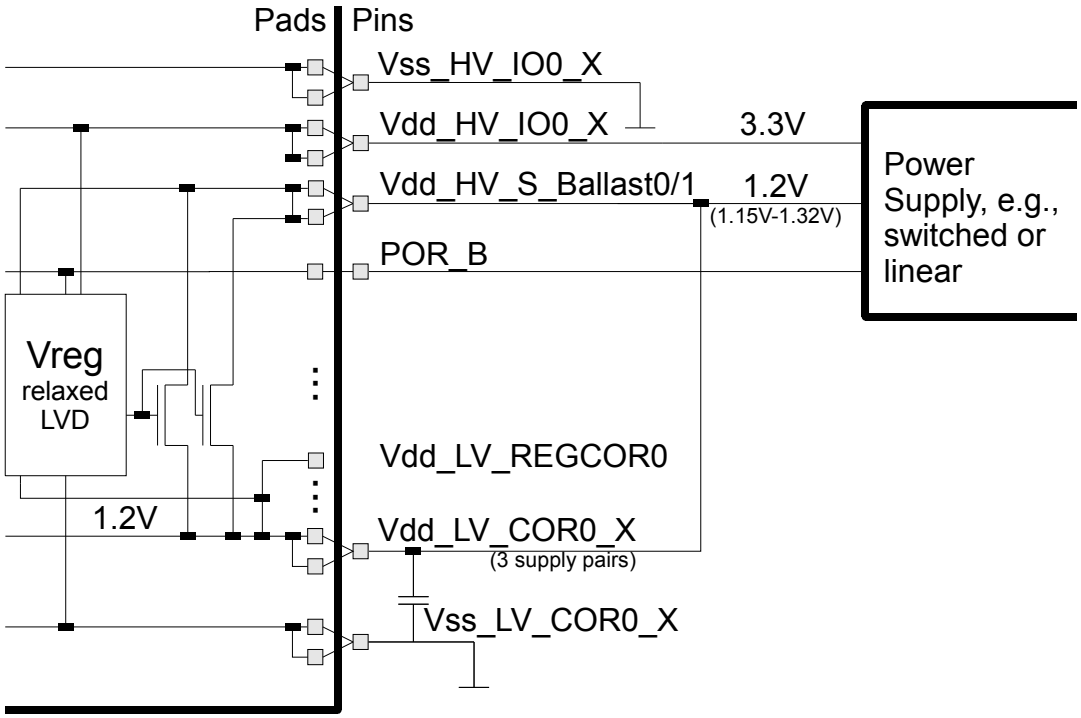


Figure 5. External Regulation Mode

3.8.1.3 Recommended power supply sequencing[1]

For MPC5604E, the external supplies need to be maintained as per the following relations:

- $V_{DD\_HV\_IO}$ should be always greater or equal to $V_{DD\_HV\_S\_Ballast}$
- $V_{DD\_HV\_IO}$ should be always greater than $V_{DD\_LV\_COR0\_X}$
- $V_{DD\_HV\_IO}$ should be always greater than $V_{DD\_HV\_ADC}$

3.8.2 Voltage regulator electrical characteristics

1.Investigations are in process to relax power supply sequencing recommendation.

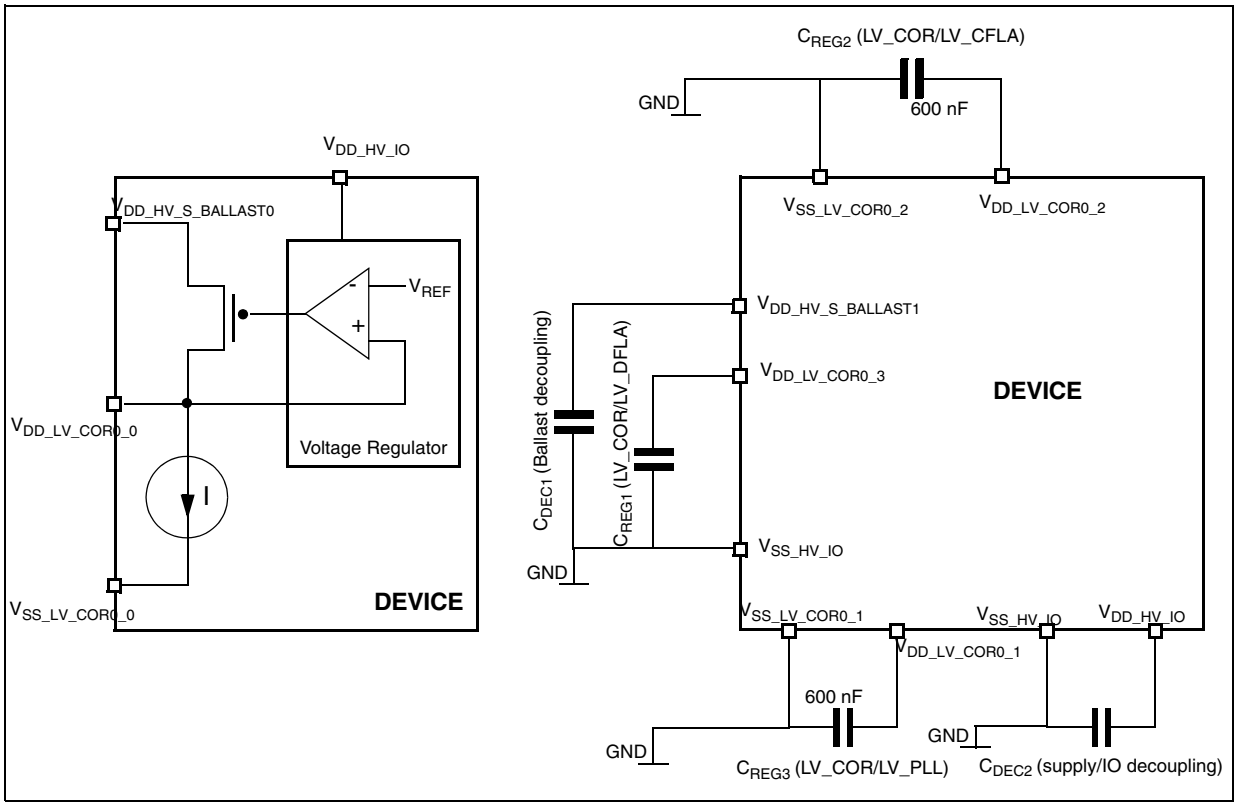


Figure 6. Voltage regulator capacitance connection

Table 13. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{REGn}[2]	SR	—	Internal voltage regulator external capacitance	—	200	—	600	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	—	0.05	—	0.2	Ω
C_{DEC1}	SR	—	Decoupling capacitance[3] ballast	—	100[4]	470[5]	—	nF
				—	400		—	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	—	100 nF	1 μF	—	—
V_{MREG}	CC	T	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
		P		After trimming	1.15	1.28	1.32	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	

Table 13. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{DD_BV}	CC	D	In-rush current on V_{DD_BV} during power-up[6]	—	—	—	40[7]	mA

1 V_{DD} = 3.3 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 It is required by the device in internal voltage regulation mode only.

3 This capacitance value is driven by the constraints of the external voltage regulator that supplies the V_{DD_BV} voltage. A typical value is in the range of 470 nF. This capacitance should be placed close to the device pin.

4 This value is acceptable to guarantee operation from 3.0 V to 3.6 V

5 External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.

6 In-rush current is seen only for short time during power-up and on standby exit (max 20 µs, depending on external LV capacitances to be load)

7 The duration of the in-rush current depends on the capacitance placed on LV pins. BV decaps must be sized accordingly. Refer to IMREG value for minimum amount of current to be provided in cc.

3.8.3 Voltage monitor electrical characteristics

The device implements a POR module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V_{DD_HV} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD_HV} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD_HV} to ensure device reset below minimum functional supply
- LVDLVCOR monitors low voltage digital power domain

Table 14. Low voltage monitor electrical characteristics

Symbol		Parameter	Conditions[1]	Value		Unit
				Min	Max	
V_{PORH}	T	Power-on reset threshold	—	1.5	2.7	V
V_{PORUP}	D	Supply for functional POR module	T_A = 25°C	1.0	—	V
$V_{DDHVLVDMOK\_H}$	P	V_{DD_HV} low voltage detector high threshold	—	—	2.95	V
$V_{DDHVLVDMOK\_L}$	P	V_{DD_HV} low voltage detector low threshold	—	2.6	—	V
$V_{MLVDDOK\_H}$	P	Digital supply low voltage detector high	—	—	1.235	V
$V_{MLVDDOK\_L}$	P	Digital supply low voltage detector low	—	1.095	—	V

1 $V_{DD–HV}$ = 3.3V ± 10% T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified

3.9 Power Up/Down reset sequencing

The MPC5604E implements a precise sequence to ensure each module is started only when all conditions for switching it ON are available. This prevents overstress event or miss-functionality within and outside the device:

- A POR module working on voltage regulator supply is controlling the correct start-up of the regulator. This is a key module ensuring safe configuration for all Voltage regulator functionality when supply is below 1.5 V. Associated POR (or POR) signal is active low.

- Several Low Voltage Detectors, working on voltage regulator supply are monitoring the voltage of the critical modules (Voltage regulator, I/Os, Flash and Low voltage domain). LVDs are gated low when POWER_ON is active.
- A POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, Flash and RC16 oscillator needed during power-up phase and reset phase. When POWER_OK is low the associated module are set into a safe state.

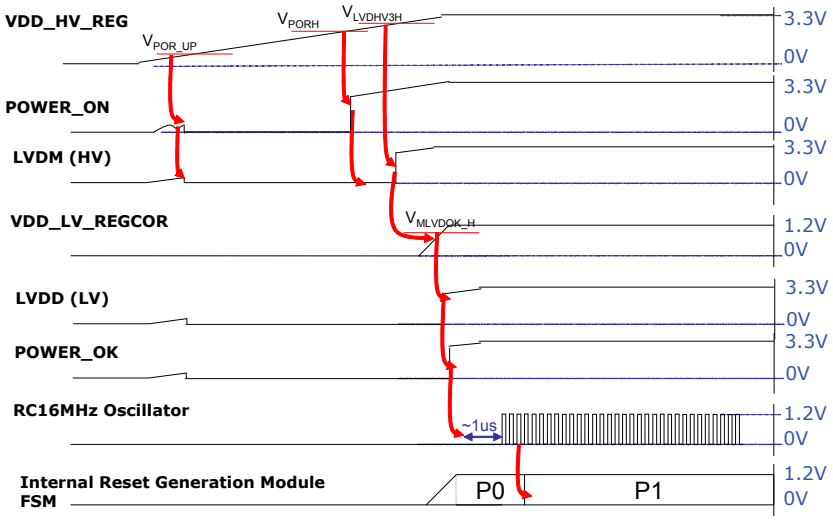


Figure 7. Power-up typical sequence

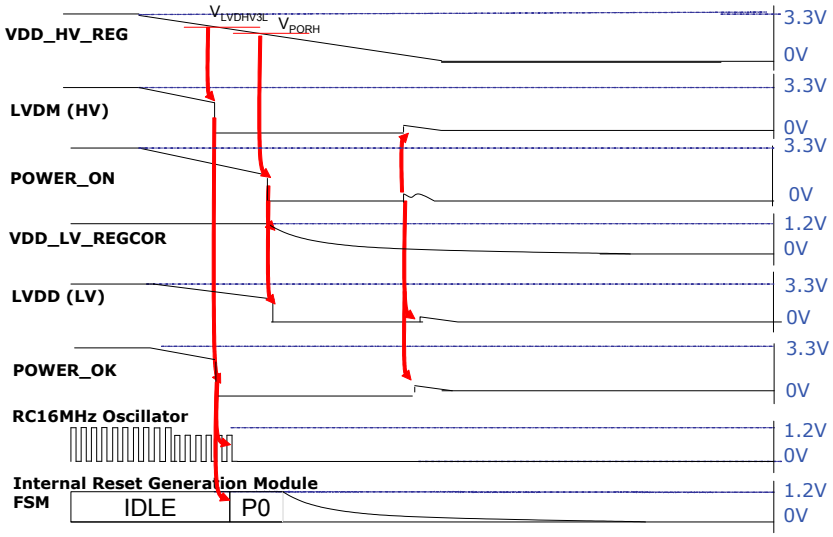


Figure 8. Power-down typical sequence

3.10 DC electrical characteristics

Table 15 gives the DC electrical characteristics at 3.3 V (3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V).

Table 15. DC electrical characteristics (3.3 V)[1]

Symbol		Parameter	Conditions	Min	Max	Unit
V_{IL}	D	Minimum low level input voltage	—	–0.4[2]	—	V
V_{IL}	P	Maximum low level input voltage	—	—	0.35 $V_{DD\_HV\_IO}$	V
V_{IH}	P	Minimum high level input voltage	—	0.65 $V_{DD\_HV\_IO}$	—	V
V_{IH}	D	Maximum high level input voltage	—	—	$V_{DD\_HV\_IO}$ + 0.4[2]	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IO}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 2 mA	—	0.1$V_{DD_HV_IO}$	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –2 mA	0.8$V_{DD_HV_IO}$	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	0.1$V_{DD_HV_IO}$	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –3 mA	0.8$V_{DD_HV_IO}$	—	V
V_{OL_F}	P	Fast, high level output voltage	I_{OL} = 11 mA	—	0.1$V_{DD_HV_IO}$	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –11 mA	0.8$V_{DD_HV_IO}$	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–95	—	µA
I_{PD}	P	Equivalent pull-down current	V_{IN} = V_{IH}	—	95	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	—	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	—	0.5	µA
V_{ILR}	D	Minimum $\overline{\text{RESET}}$, low level input voltage	—	–0.4[2]	—	V
V_{ILR}	P	Maximum $\overline{\text{RESET}}$, low level input voltage	—	—	0.35 $V_{DD\_HV\_IO}$	V
V_{IHR}	P	Minimum $\overline{\text{RESET}}$, high level input voltage	—	0.65 $V_{DD\_HV\_IO}$	—	V
V_{IHR}	D	Maximum $\overline{\text{RESET}}$, high level input voltage	—	—	$V_{DD\_HV\_IO}$ + 0.4[2]	V
V_{HYSR}	D	$\overline{\text{RESET}}$, Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IO}$	—	V
V_{OLR}	D	$\overline{\text{RESET}}$, low level output voltage	I_{OL} = 0.5 mA	—	0.1$V_{DD_HV_IO}$	V
I_{PU}	D	$\overline{\text{RESET}}$, equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	
C_{IN}	D	Input capacitance	—	—	10	pF

1 These specifications are design targets and subject to change per device characterization.

2 “SR” parameter values must not exceed the absolute maximum ratings shown in Table 6.

Table 16. Supply current

Symbol		Parameter		Conditions	Value[1]			Unit
					Min	Typ	Max	
$I_{DD\_LV\_CORE}$	C	Supply current	RUN Mode, I/O currents not included, worst case over temperature for system clock		—	75	120	mA
	P		HALT Mode[2]	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	—	4	25	
	P		STOP Mode[3]	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	—	4	25	
I_{DD_FLASH}	C		**Code Flash**					
			FLASH supply current during read	$V_{DD\_HV\_IO}$ at 3.3 V	—	4	7	
			FLASH supply current during erase operation on 1 Flash module	$V_{DD\_HV\_IO}$ at 3.3 V	—	9	14	
			Data Flash					
			FLASH supply current during read	$V_{DD\_HV\_IO}$ at 3.3 V	—	3.5	6	
			FLASH supply current during erase operation on 1 Flash module	$V_{DD\_HV\_IO}$ at 3.3 V	—	7.5	12	
I_{DD_ADC}	C		ADC supply current	$V_{DD\_HV\_ADC0}$ at 3.3 V ADC Freq = 16MHz	—	1.8	3	
I_{DD_OSC}	C		OSC supply current	$V_{DD\_HV\_OSC}$ at 3.3 V 16 MHz	—	0.74	4	

1 All values to be confirmed after characterization/data collection.

2 Halt mode configurations: Code fetched from SRAM, Code Flash and Data Flash in low power mode, OSC/PLL0 are OFF, Core clock frozen, all peripherals are disabled.

3 STOP "P" mode DUT configuration: Code fetched from SRAM, Code Flash and Data Flash off, OSC/PLL0 are OFF, Core clock frozen, all peripherals are disabled.

3.11 Main oscillator electrical characteristics

The MPC5604E provides an oscillator/resonator driver.

Table 17. Main oscillator electrical characteristics

Symbol		Parameter	Min	Max	Unit
f_{OSC}	SR	Oscillator frequency	4	40	MHz
g_m	P	Transconductance	4	15.846	mA/V
V_{OSC}	T	Oscillation amplitude on XTAL pin	1.3	2.25	V
t_{OSCSU}	T	Start-up time[1,2]	—	5	ms

[1] The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.

[2] Value captured when amplitude reaches 90% of XTAL

Table 18. Input clock characteristics

Symbol		Parameter	Min	Typ	Max	Unit
f_{OSC}	SR	Oscillator frequency	4	—	40	MHz
f_{CLK}	SR	Frequency in bypass	—	—	100	MHz
t_{rCLK}	SR	Rise/fall time in bypass	—	—	1	ns
t_{DC}	SR	Duty cycle	47.5	50	52.5	%

3.12 FMPLL electrical characteristics

Table 19. PLLMRFM electrical specifications[1]
(V_{DDPLL} = 3.0 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)

Symbol		Parameter		Conditions	Value		Unit
					Min	Max	
$f_{ref\_crystal}$ f_{ref_ext}	D	PLL reference frequency range[2]		Crystal reference	4	40	MHz
f_{pll_in}	D	Phase detector input frequency range (after pre-divider)		—	4	16	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode		—	4	120	MHz
f_{VCO}	P	VCO free running frequency		Measured using clock division—typically /16	20	150	MHz
f_{sys}	D	On-chip PLL frequency[2]		—	16	64	MHz
t_{CYC}	D	System clock period		—	—	1 / f_{sys}	ns
f_{SCM}	D	Self-clocked mode frequency[3,4]		—	20	150	MHz
C_{JITTER}	T	CLKOUT period jitter[5,6,7,8]	Peak-to-peak (clock edge to clock edge)	f_{SYS} maximum	500	500	ps
			Long-term jitter (avg. over 2 ms interval)		–6	6	ns
t_{lpll}	D	PLL lock time [9, 10]		—	—	200	µs
t_{dc}	D	Duty cycle of reference		—	40	60	%
f_{LCK}	D	Frequency LOCK range		—	–6	6	% f_{sys}

Table 19. PLLMRFM electrical specifications[1] (V_{DDPLL} = 3.0 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
f_{UL}	D	Frequency un-LOCK range	—	–18	18	% f_{sys}
f_{CS} f_{DS}	D	Modulation Depth	Center spread	±0.25	±4.0[11]	%f_{sys}
			Down Spread	–0.5	–8.0	
f_{MOD}	D	Modulation frequency[12]	—	—	100	kHz

1 All values given are initial design targets and subject to change.

2 Considering operation with PLL not bypassed.

3 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.

4 f_{VCO} self clock range is 20-150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.

5 This value is determined by the crystal manufacturer and board design.

6 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.

7 Proper PC board layout procedures must be followed to achieve specifications.

8 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).

9 This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.

10 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

11 This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).

12 Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.13 16 MHz RC oscillator electrical characteristics

Table 20. 16 MHz RC oscillator electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
f_{RC}	C	RC oscillator frequency	T_A = 25 °C	8.5	16	24	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation in temperature and supply with respect to f_{RC} at T_A = 55 °C in high-frequency configuration	—	–5	—	5	%
$\Delta_{RCMTRIM}$	T	Post Trim Accuracy: The variation of the PTF[1] from the 16 MHz oscillator	T_A = 25 °C	–2	—	2	%

1 PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature

3.14 Analog-to-Digital Converter (ADC) electrical characteristics

The device provides a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

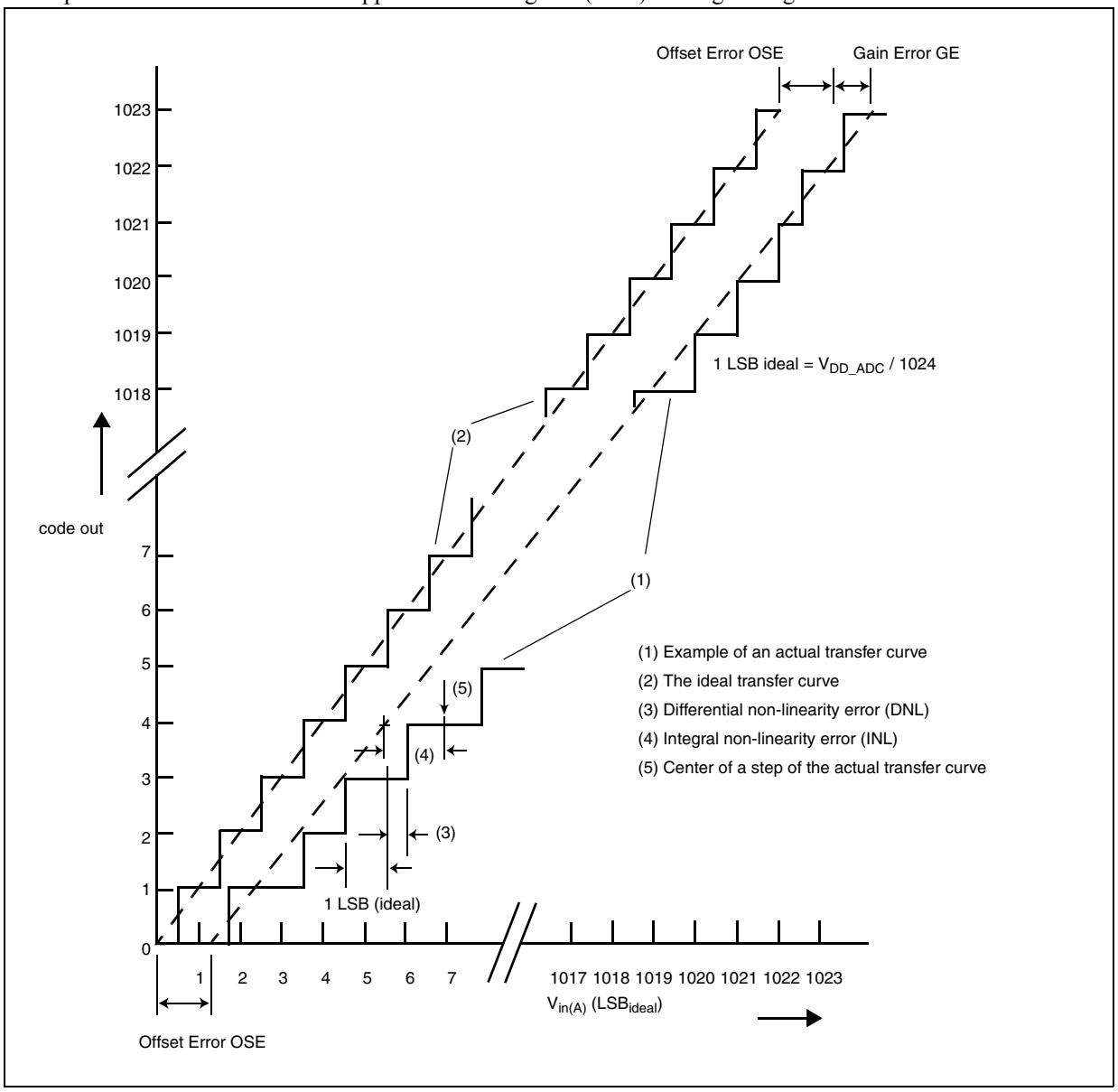


Figure 9. ADC characteristics and error definitions

3.14.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to

be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (fc \times C_S)$, where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the Equation 4:

Eqn. 4

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

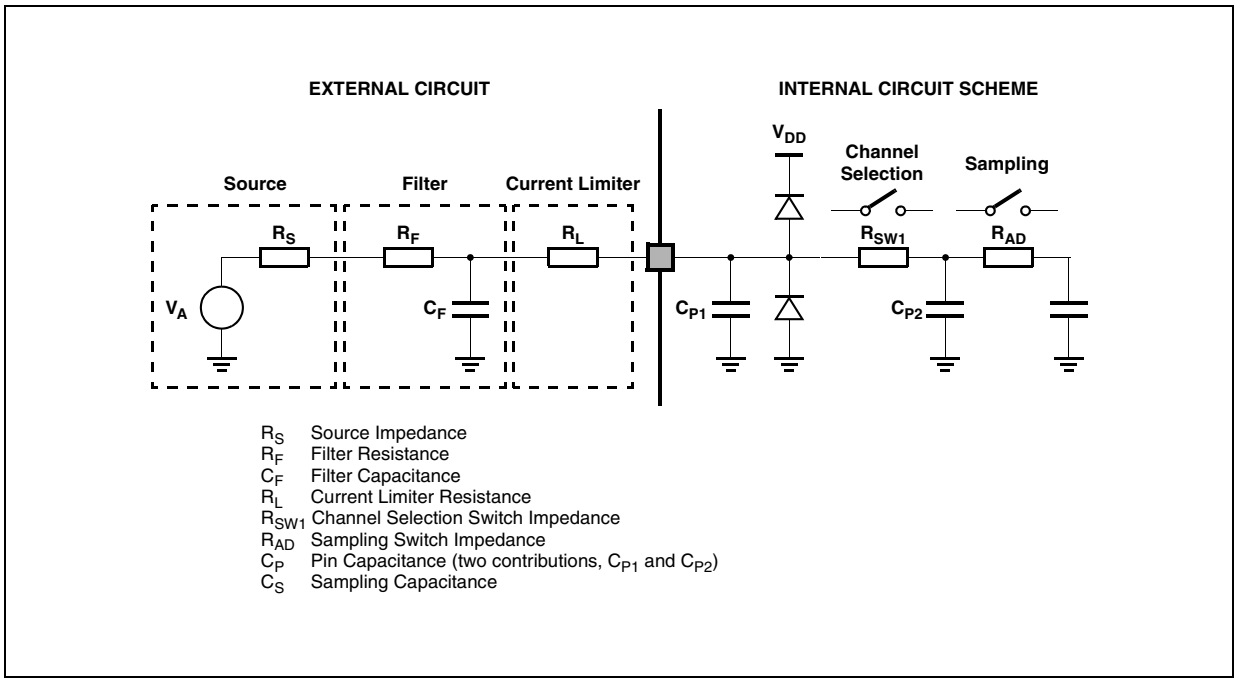


Figure 10. Input equivalent circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 10): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

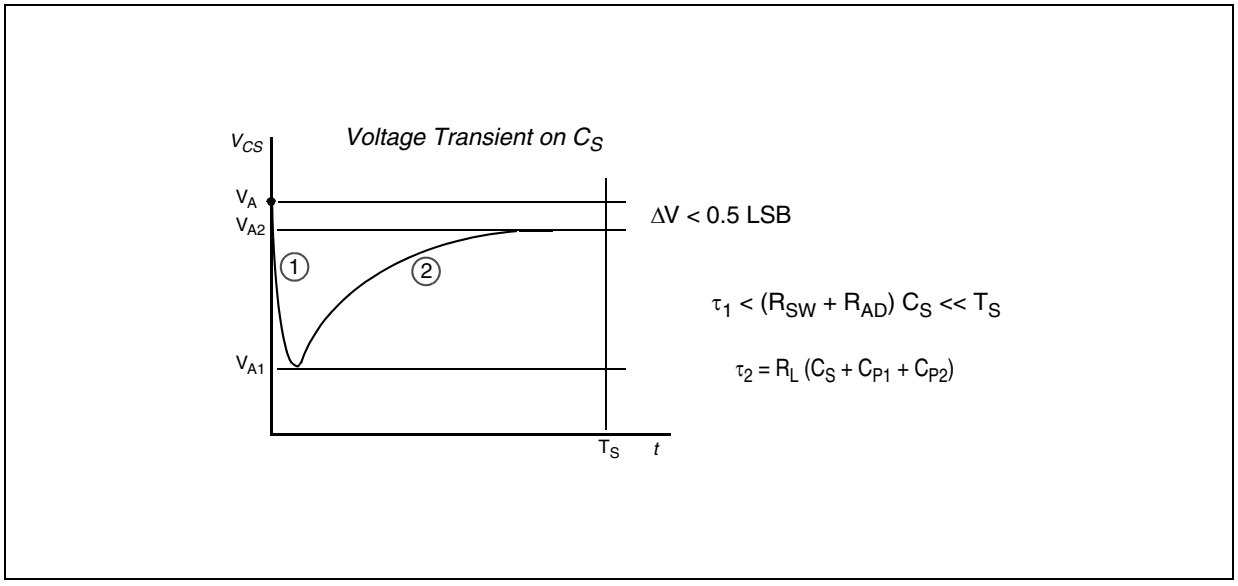


Figure 11. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

Eqn. 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Eqn. 9

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

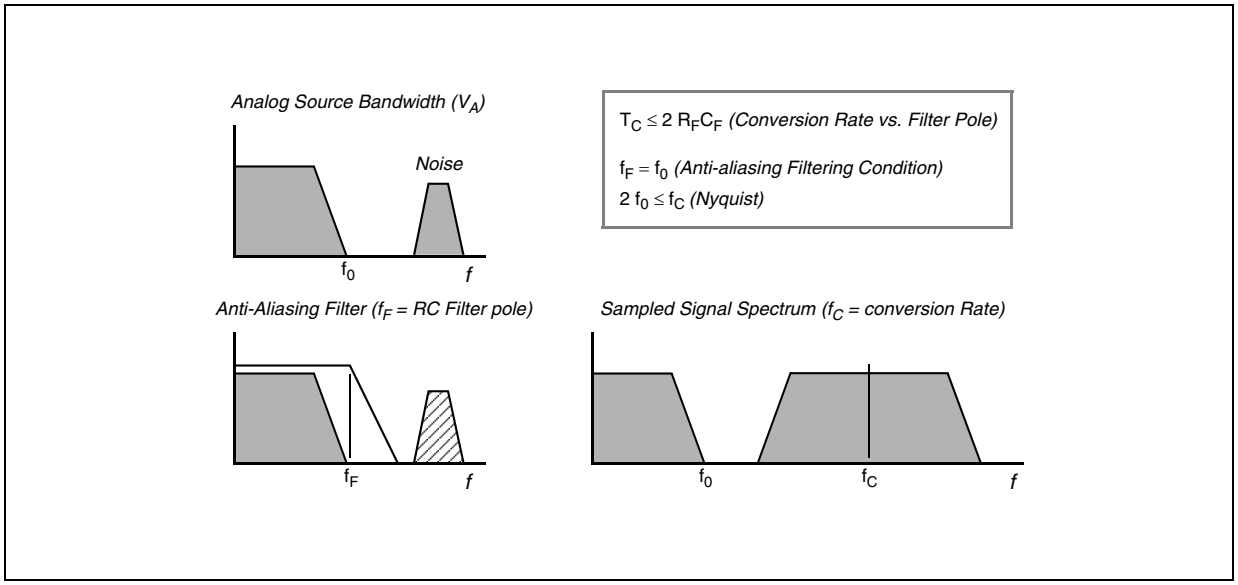


Figure 12. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on C_S:

Eqn. 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 12

$$C_F > 2048 \bullet C_S$$

3.14.2 ADC conversion characteristics

Table 21. ADC conversion characteristics

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
f_{CK}	SR	ADC clock frequency (depends on ADC configuration) (The duty cycle depends on ADCClk[2] frequency)	—	1	—	64	MHz
f_s	SR	Sampling frequency	—	—	—	1.53	MHz
t_{ADC_S}	D	Sample time[3]	f_{ADC} = 20 MHz, ADC_conf_sample_input = 17	500	—	—	ns
			f_{ADC} = 9 MHz, INPSAMP = 255	—	—	28.2	µs
t_{ADC_C}	P	Conversion time[4]	f_{ADC} = 20 MHz[5], ADC_conf_comp = 3	500	—	—	ns
C_S[6]	D	ADC input sampling capacitance	—	—	—	2.5	pF
C_{P1}[6]	D	ADC input pin capacitance 1	—	—	—	0.8[7]	pF
C_{P2}[6]	D	ADC input pin capacitance 2	—	—	—	1	pF
R_{SW1}[6]	D	Internal resistance of analog source	—	—	—	0.6	kΩ
R_{AD}[6]	D	Internal resistance of analog source	—	—	—	2	kΩ
I_{INJ}	T	Input current injection	Current injection on one ADC input, different from the converted one. Remains within TUE specification	–5	—	5	mA
INL	P	Integral Non Linearity	No overload	–1.5	—	1.5	LSB
DNL	P	Differential Non Linearity	No overload	–1.0	—	1.0	LSB
OFS	T	Offset error	—	—	±1	—	LSB
GNE	T	Gain error	—	—	±1	—	LSB
TUE	P	Total unadjusted error without current injection	—	–3	—	3	LSB
TUE	T	Total unadjusted error with current injection	—	–3	—	3	LSB
TUE	P	Total unadjusted error	—	–3	—	3	LSB
TUEP	CC	Total Unadjusted Error for precise channels, input only pins	No overload	-2	—	2	LSB
			overload conditions on adjacent channel	—	—	—	LSB
TUEX	CC	Total Unadjusted Error for extended channel,	No overload	-3	—	3	LSB
			overload conditions on adjacent channel	—	—	—	LSB

1 V_{DD} = 3.3 V to 3.6 V, T_A = –40 to +125 °C, unless otherwise specified and analog input voltage from V_{AGND} to V_{AREF}

2 ADCClk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.

3 During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.

4 This parameter does not include the sample time t_{ADC_S}, but only the time for determining the digital result and the time to load the result register with the conversion result.

5 20 MHz ADC clock. Specific prescaler is programmed on MC_PLL_CLK to provide 20 MHz clock to the ADC.

6 See Figure 10.

7 Does not include packaging and bonding capacitances

3.15 Temperature sensor electrical characteristics

Table 22. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					min	typical	max	
—	CC	C	Temperature monitoring range	—	–40	—	150	°C
—	CC	C	Sensitivity	—	—	5.14	—	mV/°C
—	CC	C	Accuracy	T_J = –40 to 25 °C	–10	—	10	°C
—	CC	C		T_J = –25 to 125 °C	–10	—	10	°C

3.16 Flash memory electrical characteristics

Table 23. Code flash program and erase specifications[1]

Symbol	Parameter	Min Value	Typical Value[2] (0 Cycles)	Initial Max[3] (100 Cycles)	Max[4] (100000 Cycles)	Unit
T_{DWPRG}	Double Word Program[5]	—	22	50	500	µs
T_{BKPRG}	Bank Program (512 KB)[5, 6]	—	1.45	1.65	33	s
T_{ER8K}	Sector Erase (8KB)	—	0.2	0.4	5.0	s
T_{ER16K}	Sector Erase (16KB)	—	0.3	0.5	5.0	s
T_{ER32K}	Sector Erase (32KB)	—	0.3	0.6	5.0	s
T_{ER64K}	Sector Erase (64KB)	—	0.6	0.9	5.0	s
T_{ER128K}	Sector Erase (128KB)	—	0.8	1.3	7.5	s
T_{ER512K}	Bank Erase (512KB)	—	4.8	7.6	55	s
T_{PABT}	Program Abort Latency	—	—	10	10	µs
T_{EABT}	Erase Abort Latency	—	—	30	30	µs

Table 23. Code flash program and erase specifications[1]

Symbol	Parameter	Min Value	Typical Value[2] (0 Cycles)	Initial Max[3] (100 Cycles)	Max[4] (100000 Cycles)	Unit
T_{EABT}	Erase Suspend Latency	—	—	30	30	µs
T_{EABT}	Erase Suspend Request Rate	10	—	—	—	ms
NER	Endurance (8KB, 16KB sectors) Endurance (32KB, 64KB sectors) Endurance (128KB sectors)	100 10 1	—	—	—	Kcycles
T_{DR}	Data Retention at 1K cycles Data Retention at 10K cycles Data Retention at 100K cycles	20 10 5	—	—	—	Years

1 TBC = To be confirmed

2 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

3 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

4 The maximum program & erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

5 Actual hardware programming times. This does not include software overhead.

6 Typical Bank programming time assumes that all cells are programmed in a single pulse. In reality some cells will require more than one pulse, adding a small overhead to total bank programming time (see Initial Max column).

Table 24. Data flash program and erase specifications[1]

Symbol	Parameter	Min Value	Typical Value[2] (0 Cycles)	Initial Max[3] (100 Cycles)	Max[4] (100000 Cycles)	Unit
T_{DWPRG}	Word Program[5]	—	30	TBC	TBC	µs
T_{BKPRG}	Bank Program (64 KB)[5, 6]	—	0.49	TBC	TBC	s
T_{ER16K}	Sector Erase (16KB)	—	0.7	TBC	TBC	s
T_{ER512K}	Bank Erase (64KB)	—	1.9	TBC	TBC	s
T_{PABT}	Program Abort Latency	—	—	12	12	µs
T_{EABT}	Erase Abort Latency	—	—	30	30	µs
T_{EABT}	Erase Suspend Latency	—	—	30	30	µs
T_{EABT}	Erase Suspend Request Rate	10	—	—	—	ms
NER	Endurance (16KB sectors)	100	—	—	—	K cycles
T_{DR}	Data Retention at 1K cycles Data Retention at 10K cycles Data Retention at 100K cycles	20 10 1	—	—	—	Years @85C

1 TBC = To be confirmed

2 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

3 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

4 The maximum program & erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

5 Actual hardware programming times. This does not include software overhead.

6 Typical Bank programming time assumes that all cells are programmed in a single pulse. In reality some cells will require more than one pulse, adding a small overhead to total bank programming time (see Initial Max column).

Table 25. Flash read access timing

Symbol	C	Parameter	Conditions[1]	Max	Unit
Fmax	C	Maximum working frequency for Code Flash at given number of WS in worst conditions	2 wait states	66	MHz
			0 wait states	18	
Fmax	C	Maximum working frequency for Data Flash at given number of WS in worst conditions	8 wait states	66	MHz

1 VDD_HV = 3.3 V ± 10%, TA = –40 to 125 °C, unless otherwise specified

3.17 AC specifications

3.17.1 Pad AC specifications

Table 26 gives the AC electrical characteristics at 3.3 V (3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V) operation.

Table 26. Pad AC specifications (3.3 V, INVUSRO[PAD3V5V] = 1)

Pad	Symbol	Parameter	Load drive (pF)	Rise/Fall[1] (ns)			Unit
				Min	Typ	Max	
Slow	Tswitchon	Propagation delay from vdd/2 of internal signal to Pchannel / Nchannel switch on condition	25	3	—	40	ns
			50	3	—	40	ns
			100	3	—	40	ns
			200	3	—	40	ns
	tr/tf	Slope at rising/falling edge	25	4	—	40	ns
			50	6	—	50	ns
			100	10	—	75	ns
			200	14	—	100	ns
	Freq	Frequency of Operation	25	—	—	4	MHz
			50	—	—	2	MHz
			100	—	—	2	MHz
			200	—	—	2	MHz
	Current Slew	Slew rate at rising edge of current	25	0.01	—	2	mA/ns
			50	0.01	—	2	mA/ns
			100	0.01	—	2	mA/ns
			200	0.01	—	2	mA/ns

Table 26. Pad AC specifications (3.3 V, INVUSRO[PAD3V5V] = 1)

Pad	Symbol	Parameter	Load drive (pF)	Rise/Fall[1] (ns)			Unit
				Min	Typ	Max	
Medium	Tswitchon	Propagation delay from vdd/2 of internal signal to Pchannel / Nchannel switch on condition	25	1	—	15	ns
			50	1	—	15	ns
			100	1	—	15	ns
			200	1	—	15	ns
	tr/tf	Slope at rising/falling edge	25	2	—	12	ns
			50	4	—	25	ns
			100	8	—	40	ns
			200	14	—	70	ns
	Freq	Frequency of Operation	25	—	—	40	MHz
			50	—	—	20	MHz
			100	—	—	13	MHz
			200	—	—	7	MHz
	Current Slew	Slew rate at rising edge of current	25	2.5	—	7	mA/ns
			50	2.5	—	7	mA/ns
			100	2.5	—	7	mA/ns
			200	2.5	—	7	mA/ns
Fast	Tswitchon	Propagation delay from vdd/2 of internal signal to Pchannel / Nchannel switch on condition	25	1	—	6	ns
			50	1	—	6	ns
			100	1	—	6	ns
			200	1	—	6	ns
	tr/tf	Slope at rising/falling edge	25	1	—	4	ns
			50	1.5	—	7	ns
			100	3	—	12	ns
			200	5	—	18	ns
	Freq	Frequency of Operation	25	—	—	72	MHz
			50	—	—	55	MHz
			100	—	—	40	MHz
			200	—	—	25	MHz
	Current Slew	Slew rate at rising edge of current	25	3	—	40	mA/ns
			50	3	—	40	mA/ns
			100	3	—	40	mA/ns
			200	3	—	40	mA/ns

Table 26. Pad AC specifications (3.3 V, INVUSRO[PAD3V5V] = 1)

Pad	Symbol	Parameter	Load drive (pF)	Rise/Fall[1] (ns)			Unit
				Min	Typ	Max	
Symmetric	Tswitchon	Propagation delay from vdd/2 of internal signal to Pchannel / Nchannel switch on condition	25	1	—	8	ns
	tr/tf	Slope at rising/falling edge	25	1	—	5	ns
	TRise/TFall	Delay at rising/falling edge	25	3	—	12	ns
	|TRise - TFall	Delay between rising and falling edge	25	0.05	—	1	ns
	Freq	Frequency of Operation	25	—	—	50	MHz
	Current Slew	Slew rate at rising edge of current	25	3	—	25	mA/ns

1 Slope at rising/falling edge

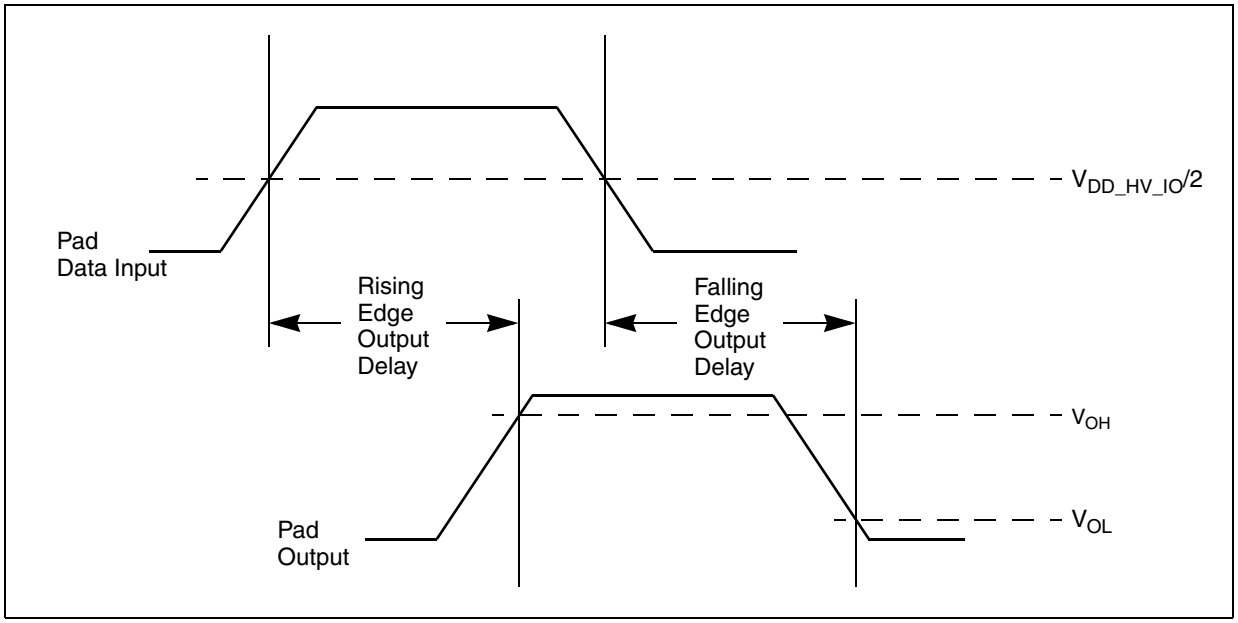


Figure 13. Pad output delay

3.18 AC timing characteristics

3.18.1 Generic timing diagrams

The generic timing diagrams in Figure 14 and Figure 15 apply to all I/O pins with pad types fast, slow and medium. See Section 2.2, “Signal descriptions for the pad type for each pin.

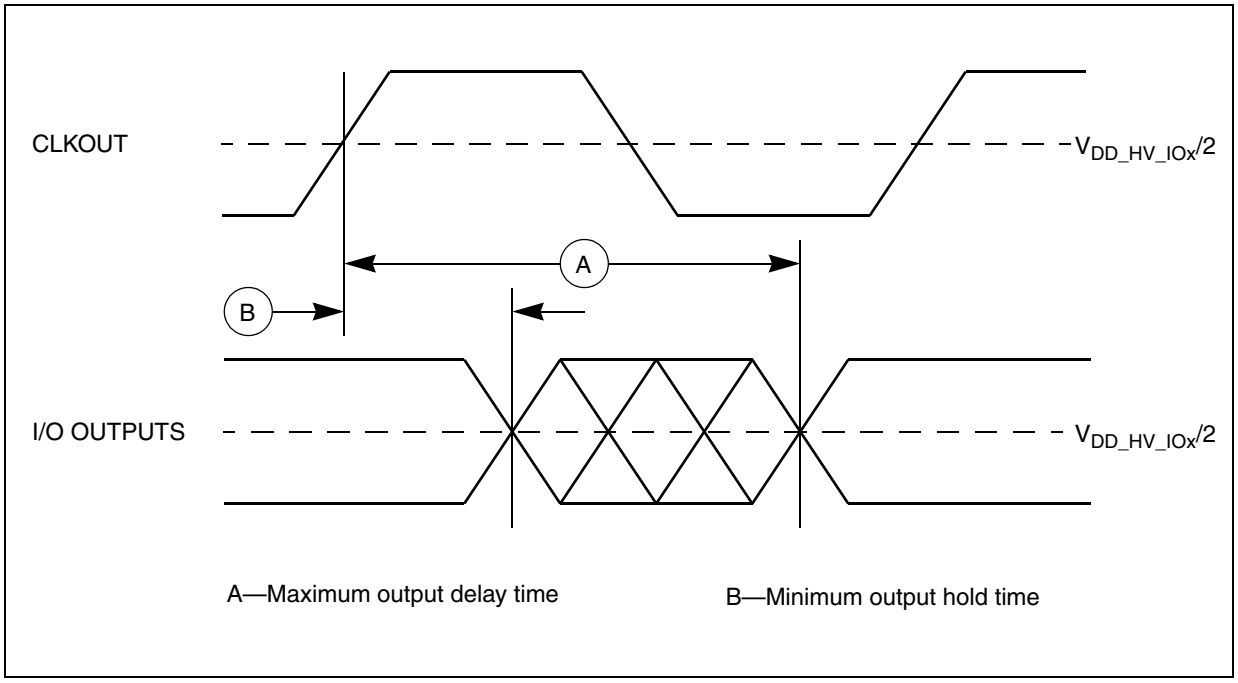


Figure 14. Generic output delay/hold timing

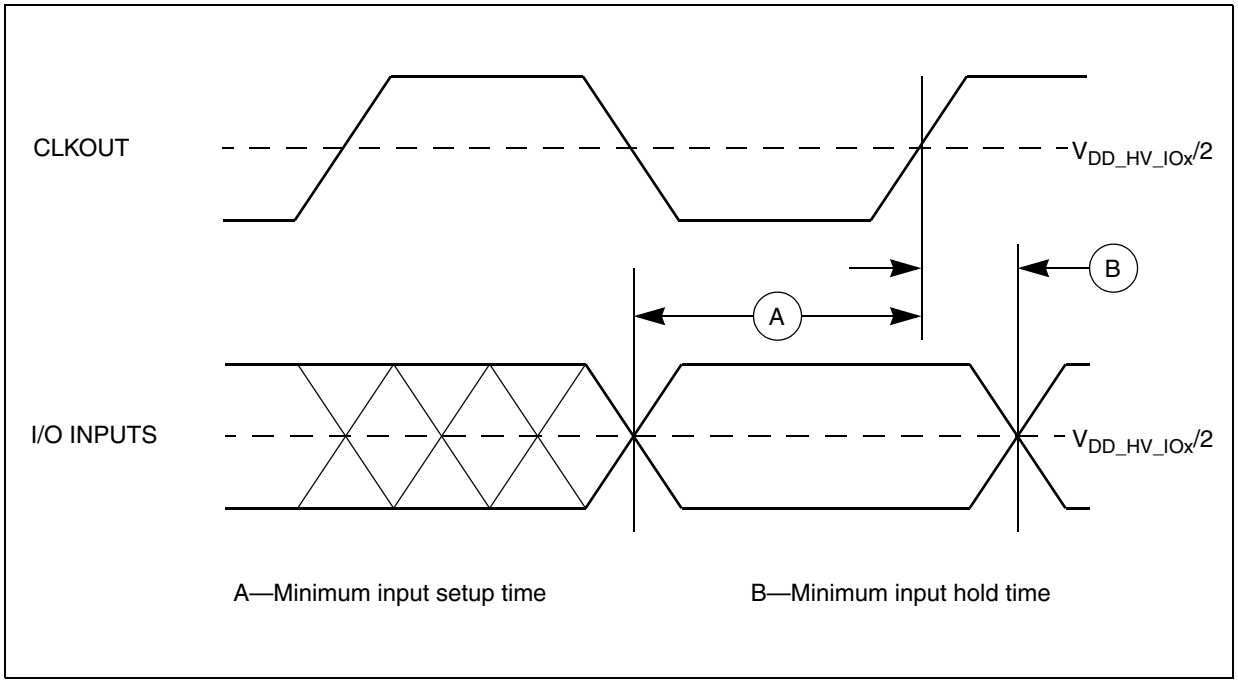


Figure 15. Generic Input setup/hold timing

3.18.2 $\overline{\text{RESET}}$ pin characteristics

The MPC5604E implements a dedicated bidirectional RESET pin.

Figure 16. Start-up reset requirements

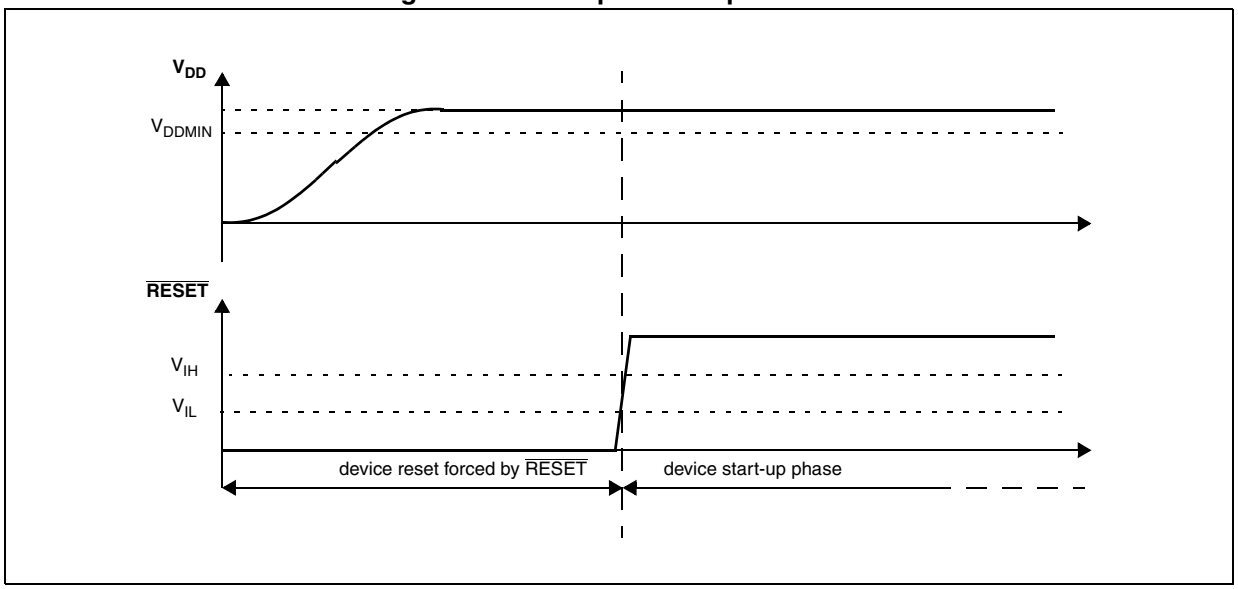


Figure 17. Noise filtering on reset signal

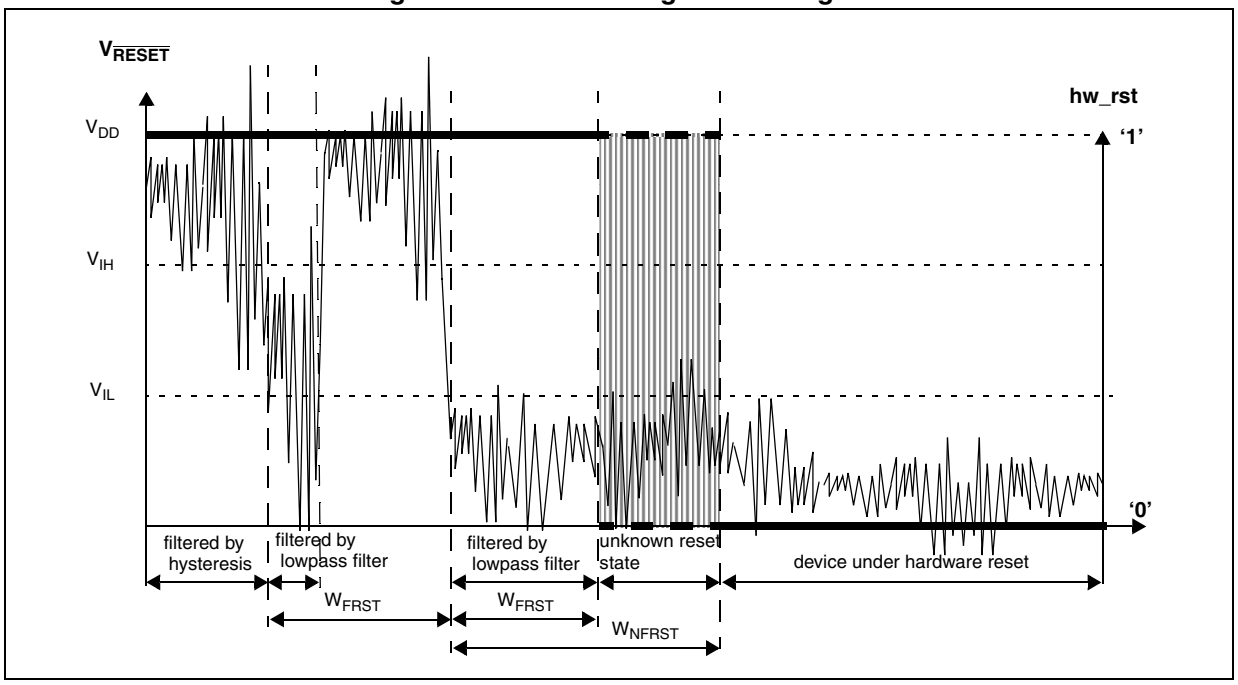


Table 27. $\overline{\text{RESET}}$ electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 3 mA,	—	—	$0.1V_{DD}$	V
T_{tr}	CC	D	Output transition time output pin[3] MEDIUM configuration	C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	12	ns
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	25	
				C_L = 100 pF, V_{DD} = 3.3 V ± 10%	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	500	—	—	ns
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%	10	—	150	µA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 C_L includes device and package capacitance (C_{PKG} < 5 pF).

3.18.3 Nexus and JTAG timing

Table 28. Nexus debug port timing[1]

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{MCYC}	CC	D	MCKO Cycle Time	2	—	8	t_{CYC}
2A	t_{MCYCP}	CC	D	MCKO cycle period	15	—	—	ns
2B	t_{MDC}	CC	D	MCKO duty cycle	48	—	52	%
3	t_{MDOV}	CC	D	MCKO low to MDO data valid[2]	–0.1	—	0.22	t_{MCYC}
4	t_{MSEOV}	CC	D	MCKO low to $\overline{\text{MSEO}}$ data valid[2]	–0.1	—	0.22	t_{MCYC}
5	t_{EVTOV}	CC	D	MCKO low to $\overline{\text{EVTO}}$ data valid[2]	–0.1	—	0.22	t_{MCYC}
6	t_{TCYC}	CC	D	TCK cycle time	50	—	—	ns
7	t_{TDC}	CC	D	TCK Duty Cycle	40	—	60	%

Table 28. Nexus debug port timing[1] (continued)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
8	t_{NTDIS}	CC	D	TDI data setup time	0.2	—	—	t_{TCYC}
	t_{NTMSS}	CC	D	TMS data setup time	0.2	—	—	t_{TCYC}
9	t_{NTDIH}	CC	D	TDI data hold time	0.1	—	—	t_{TCYC}
	t_{NTMSH}	CC	D	TMS data hold time	0.1	—	—	t_{TCYC}
10	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	25	ns
11	t_{TDOV}	CC	D	TCK low to TDO data invalid	0.1	—	—	t_{TCYC}

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.

2 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

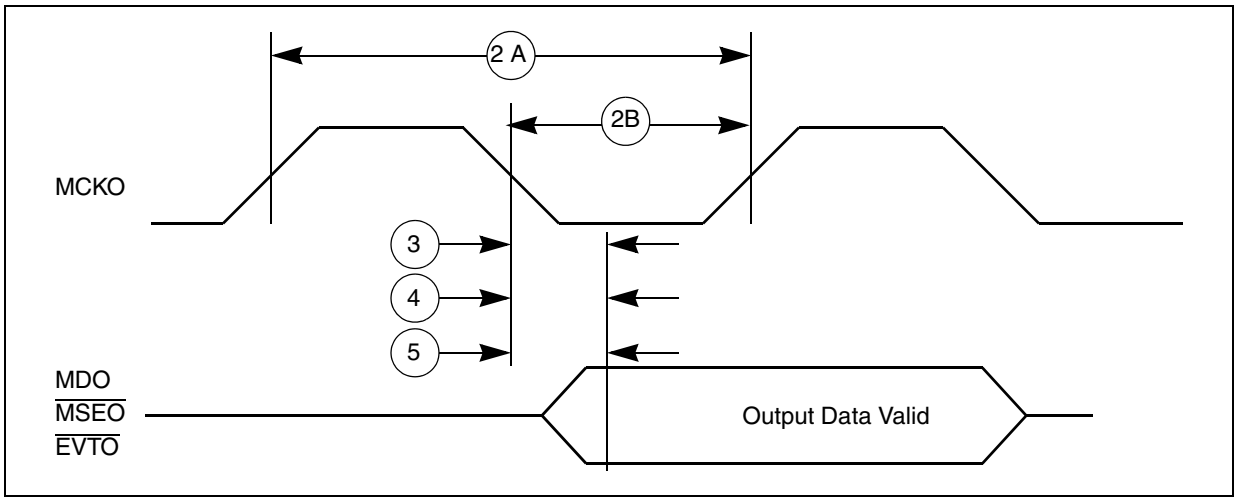


Figure 18. Nexus output timing

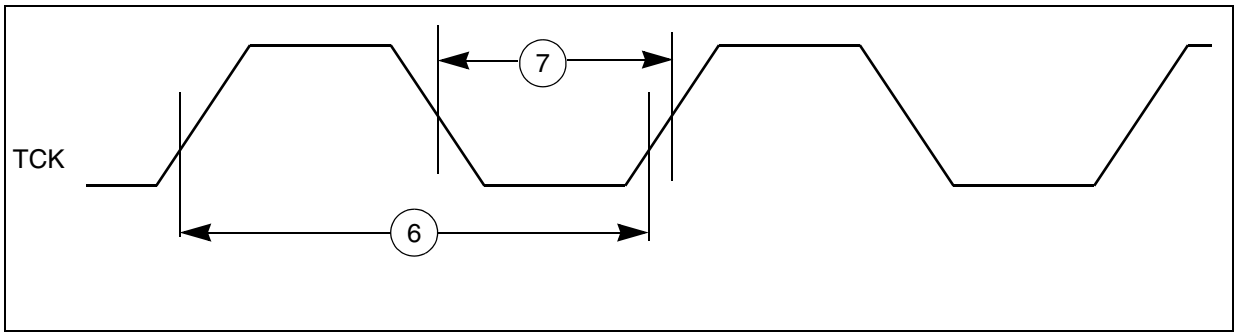


Figure 19. Nexus event trigger and test clock timings

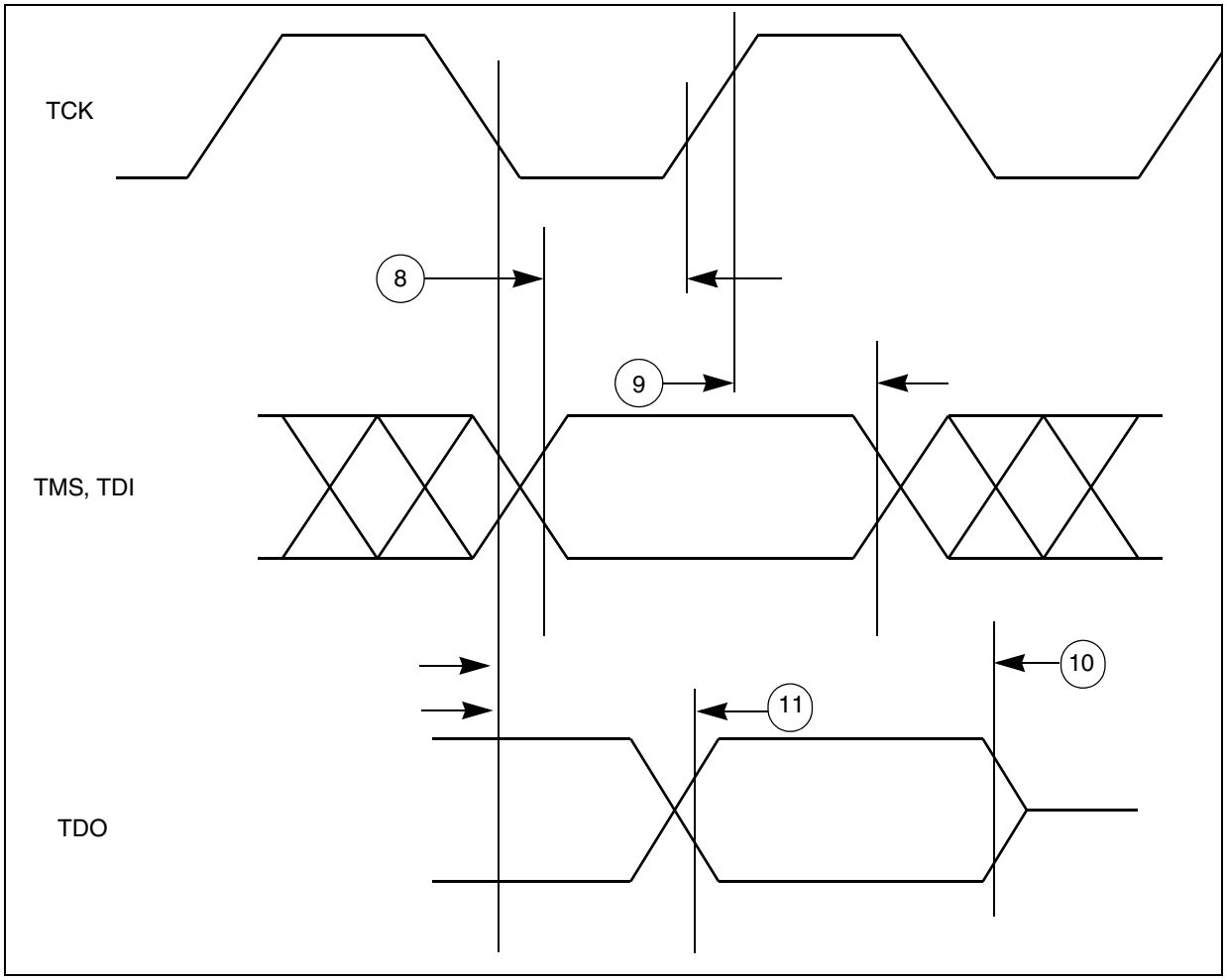


Figure 20. Nexus TDI, TMS, TDO Timing

3.18.4 GPIO timing

The GPIO specifications for setup time and output valid relative to CLKOUT are the same for all pins on the device regardless of the primary pin function.

Table 29. GPIO Timing

No.	Symbol	Characteristic	Min.	Max.	Unit
1	t_{READ}	GPIO Read Time	5	—	t_{CYC}
2	t_{WRITE}	GPIO Write Time	6	—	t_{CYC}

3.18.5 External interrupt timing (IRQ pin)

Table 30. External interrupt timing[1]

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	CC	D	IRQ pulse width low	—	4	—	t_{CYC}
2	t_{IPWH}	CC	D	IRQ pulse width high	—	4	—	t_{CYC}
3	t_{ICYC}	CC	D	IRQ edge to edge time[2]	—	4+N[3]	—	t_{CYC}

1 IRQ timing specified at f_{SYS} = 64 MHz and $V_{DD\_HV\_IOx}$ = 3.0 V, $T_A = T_L$ to T_H, and CL = 200 pF with SRC = 0b00.

2 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

3 N = ISR time to clear the flag

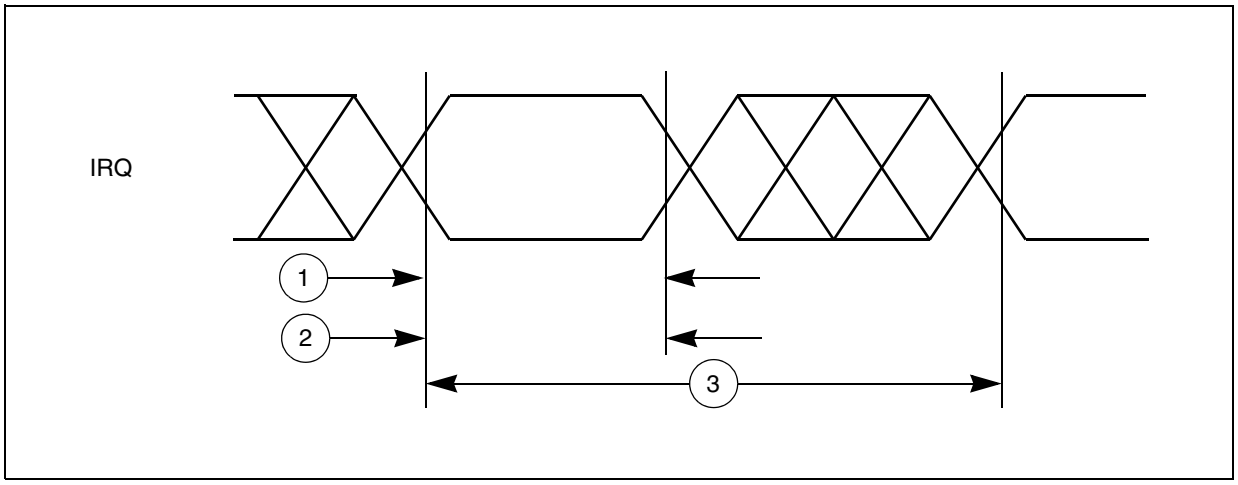


Figure 21. External interrupt timing

3.18.6 FlexCAN timing

Table 31. FlexCAN timing[1]

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	CTNX Output Valid after CLKOUT Rising Edge (Output Delay)	t_{CANOV}	—	26.0	ns
2	CNRX Input Valid to CLKOUT Rising Edge (Setup Time)	t_{CANSU}	—	9.8	ns

1 FlexCAN timing specified at f_{SYS} = 64 MHz, VDD = 1.35 V to 1.65 V, VDDEH = 3.0 V to 5.5 V, VRC33 and VDDPLL = 3.0 V to 3.6 V, T_A = TL to TH, and CL = 50 pF with SRC = 0b00.

3.18.7 LINFlex timing

Minimum design target for interface frequency is 2 MBit/s.

3.18.8 DSPI timing

Table 32. DSPI timing

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	CC	D	DSPI cycle time	Master (MTFE = 0)	62.5	—	ns
					Slave (MTFE = 0)	128	—	
					Master (MTFE = 1,CPHA=1)	31.25	—	
2	t_{CSC}	CC	D	CS to SCK delay	—	16	—	ns
3	t_{ASC}	CC	D	After SCK delay	—	16	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	—	0.4 * t_{SCK}	0.6 * t_{SCK}	ns
5	t_A	CC	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	ns
6	t_{DIS}	CC	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	10	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	CC	D	Data setup time for inputs	Master (MTFE = 0)	12	—	ns
					Slave	2	—	
					Master (MTFE = 1, CPHA = 0)	NA[1]		
					Master (MTFE = 1, CPHA = 1)	12	—	
10	t_{HI}	CC	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	NA[1]		
					Master (MTFE = 1, CPHA = 1)	–5	—	
11	t_{SUO}	CC	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	4	ns
					Slave	—	33	
					Master (MTFE = 1, CPHA = 0)	NA[1]		
					Master (MTFE = 1, CPHA = 1)	—	11	
12	t_{HO}	CC	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
					Slave	6	—	
					Master (MTFE = 1, CPHA = 0)	NA[1]		
					Master (MTFE = 1, CPHA = 1)	–2	—	

[1] This mode is not feasible at 32 MHz.

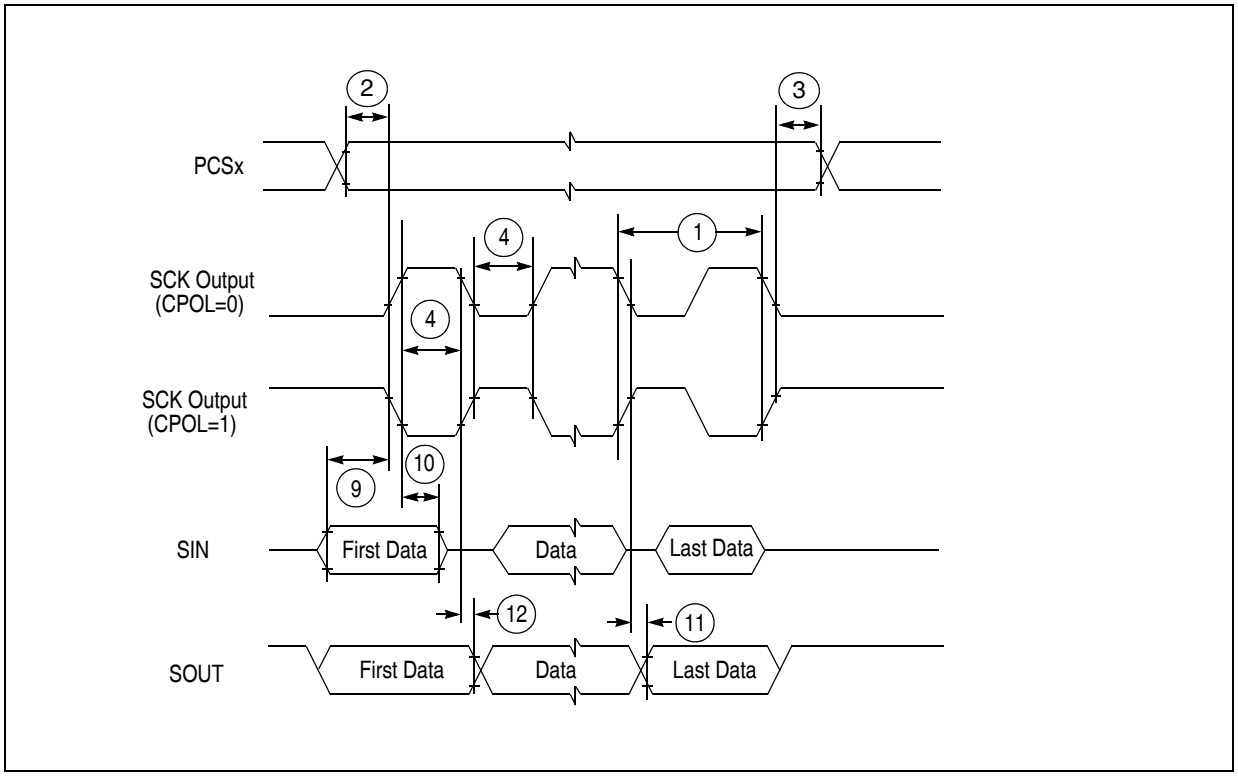


Figure 22. DSPI classic SPI timing — Master, CPHA = 0

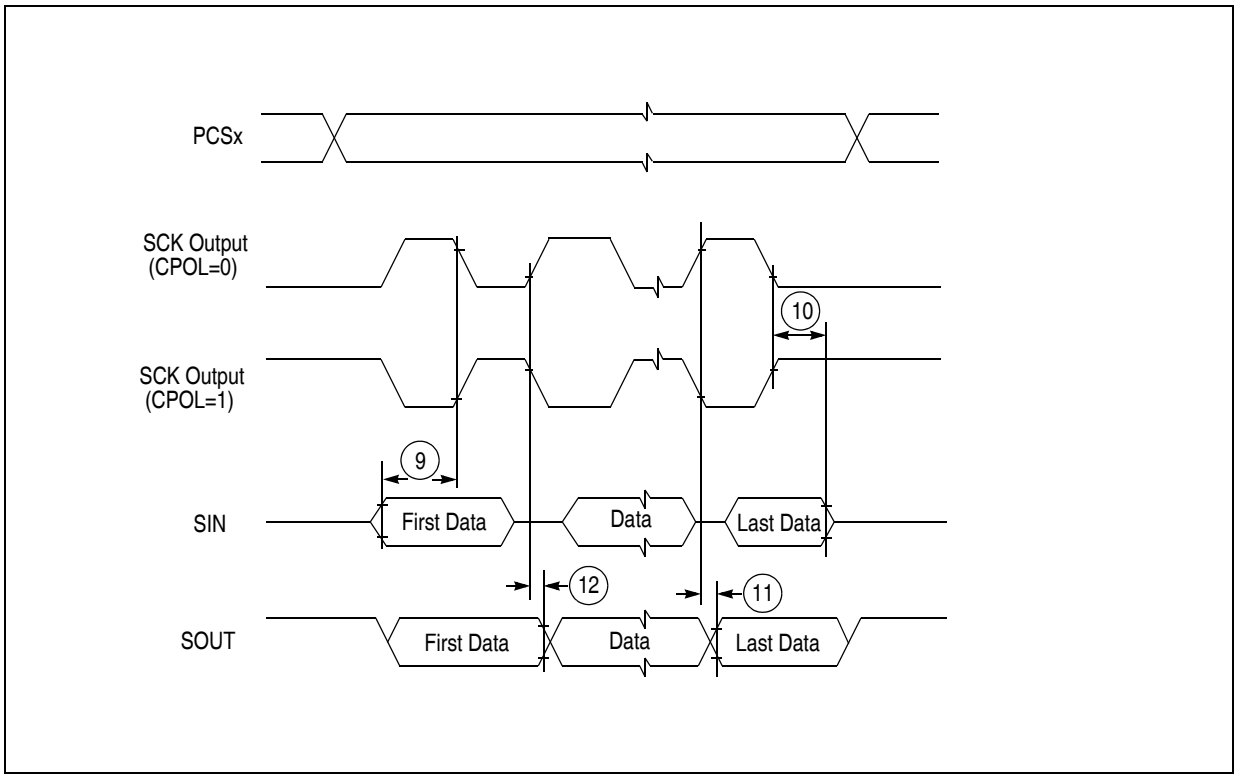


Figure 23. DSPI classic SPI timing — Master, CPHA = 1

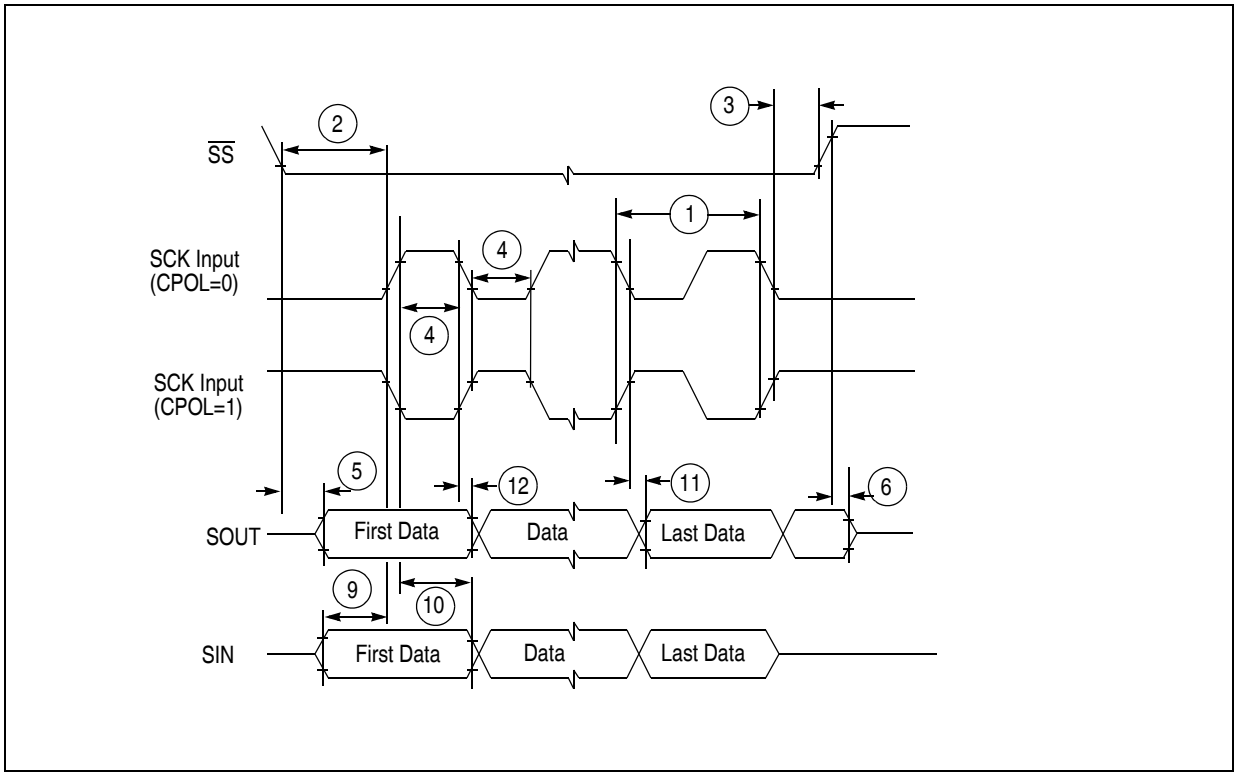


Figure 24. DSPI classic SPI timing — Slave, CPHA = 0

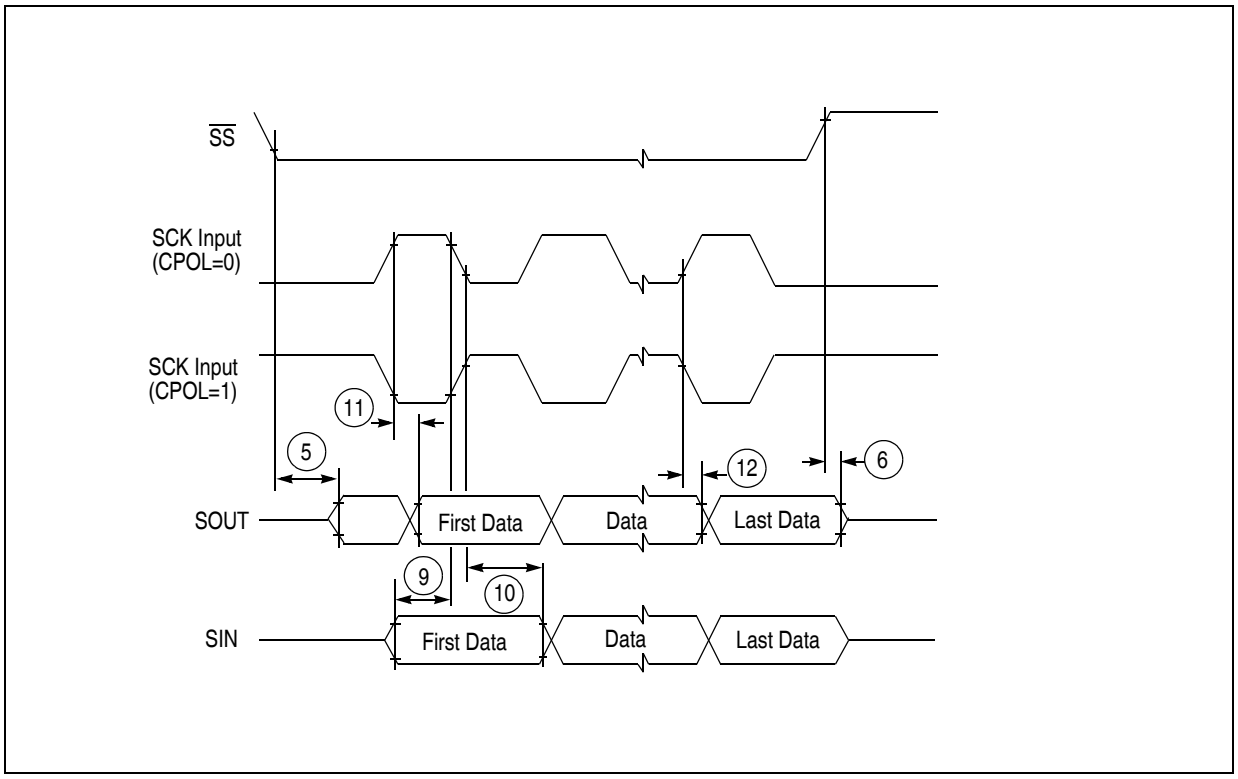


Figure 25. DSPI classic SPI timing — Slave, CPHA = 1

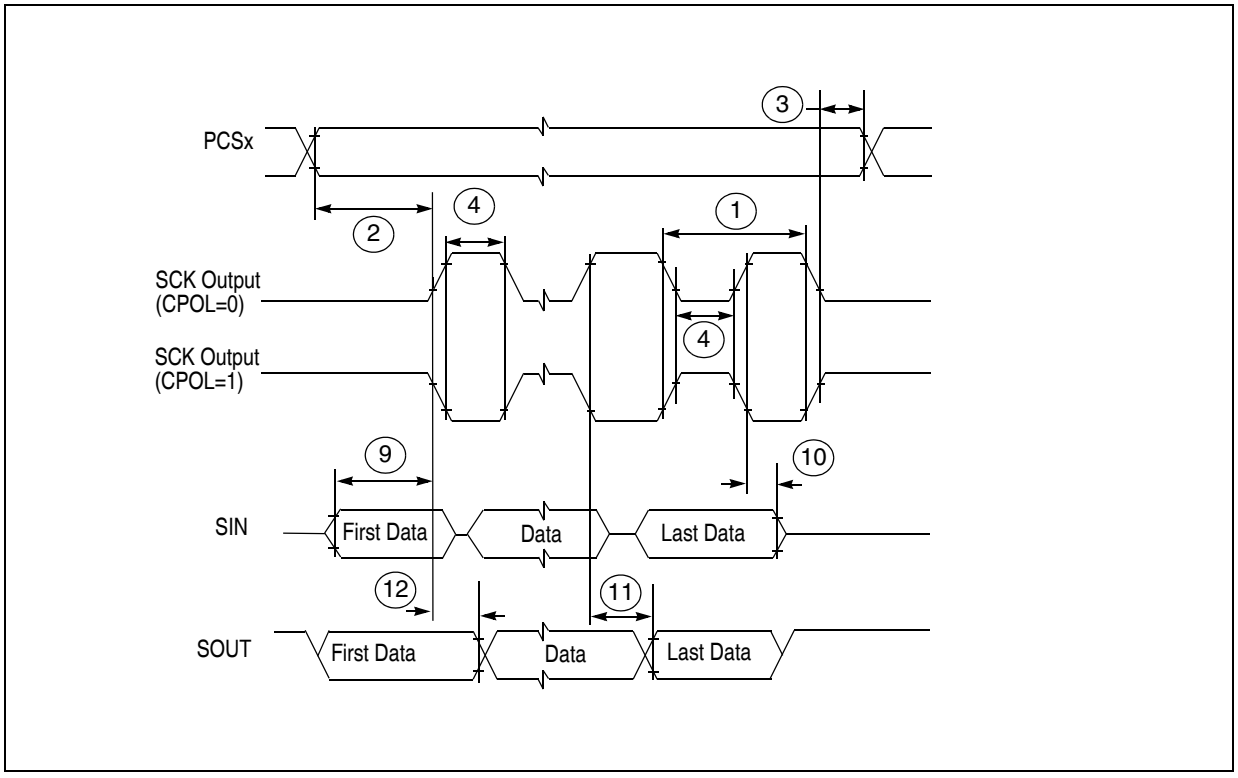


Figure 26. DSPI modified transfer format timing — Master, CPHA = 0

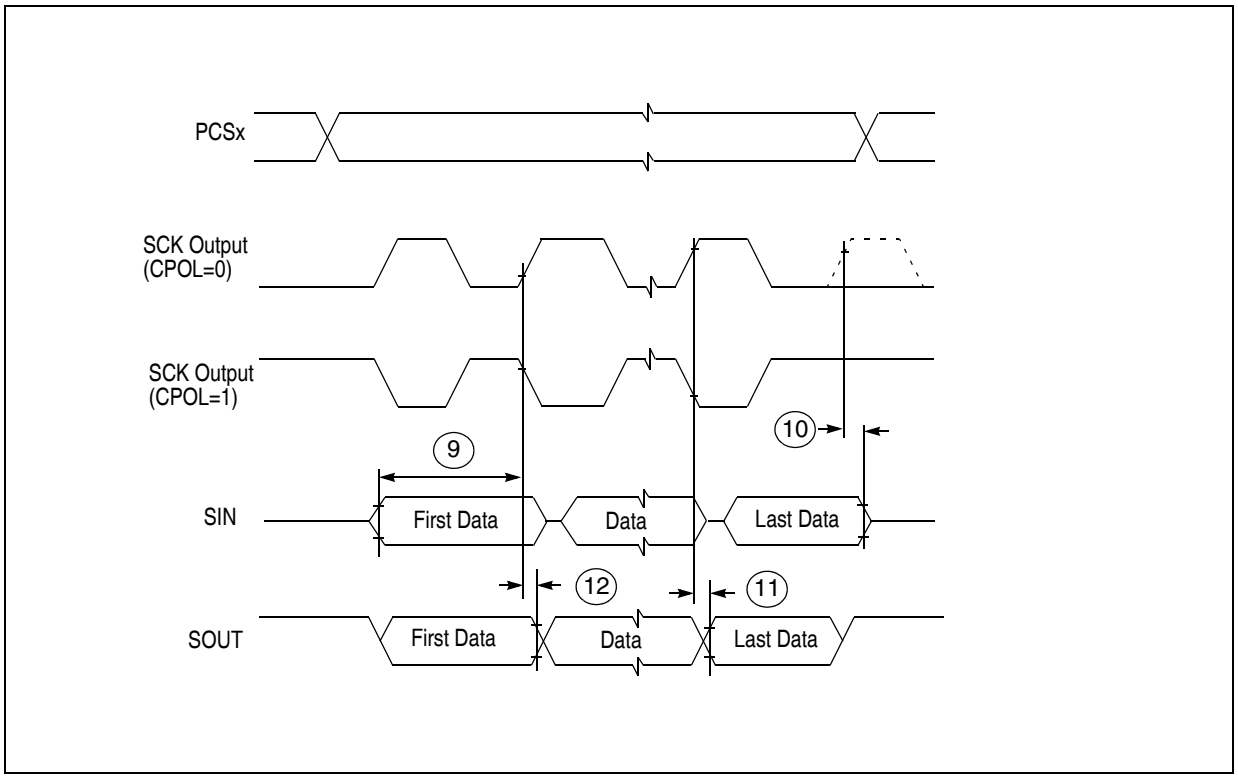


Figure 27. DSPI modified transfer format timing — Master, CPHA = 1

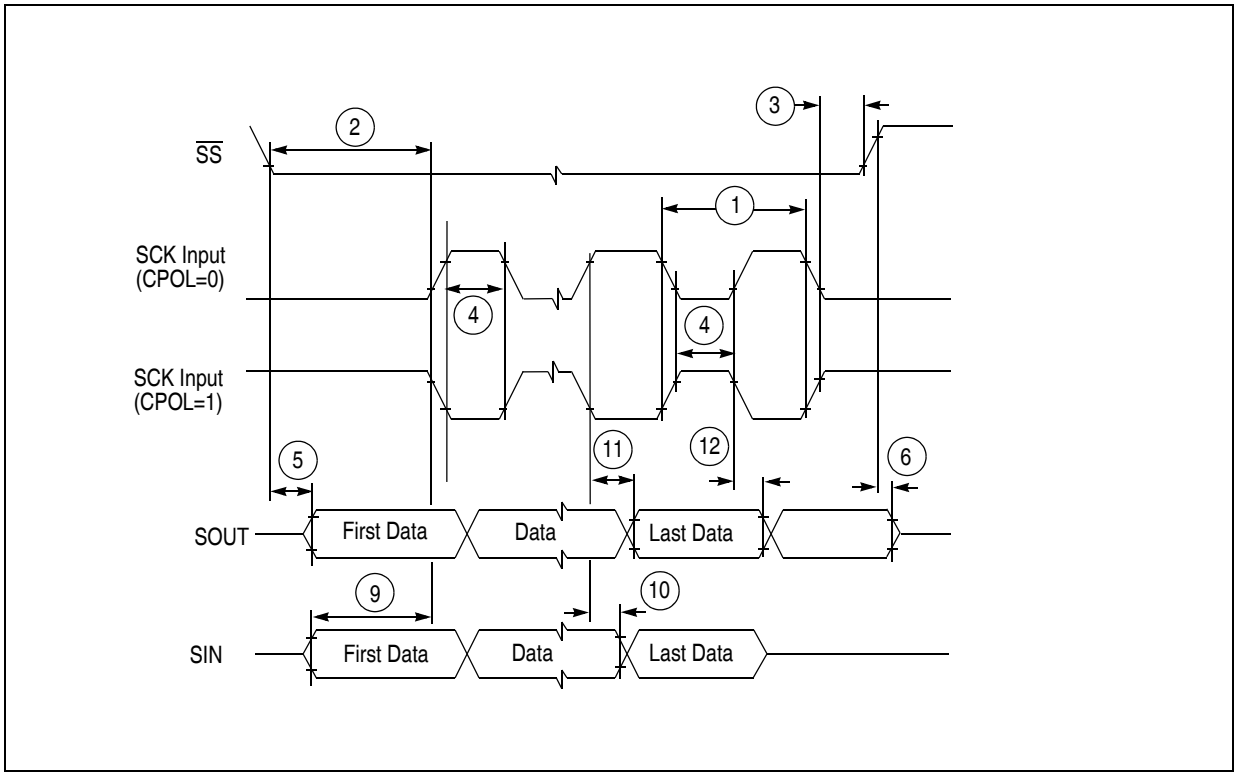


Figure 28. DSPI modified transfer format timing — Slave, CPHA = 0

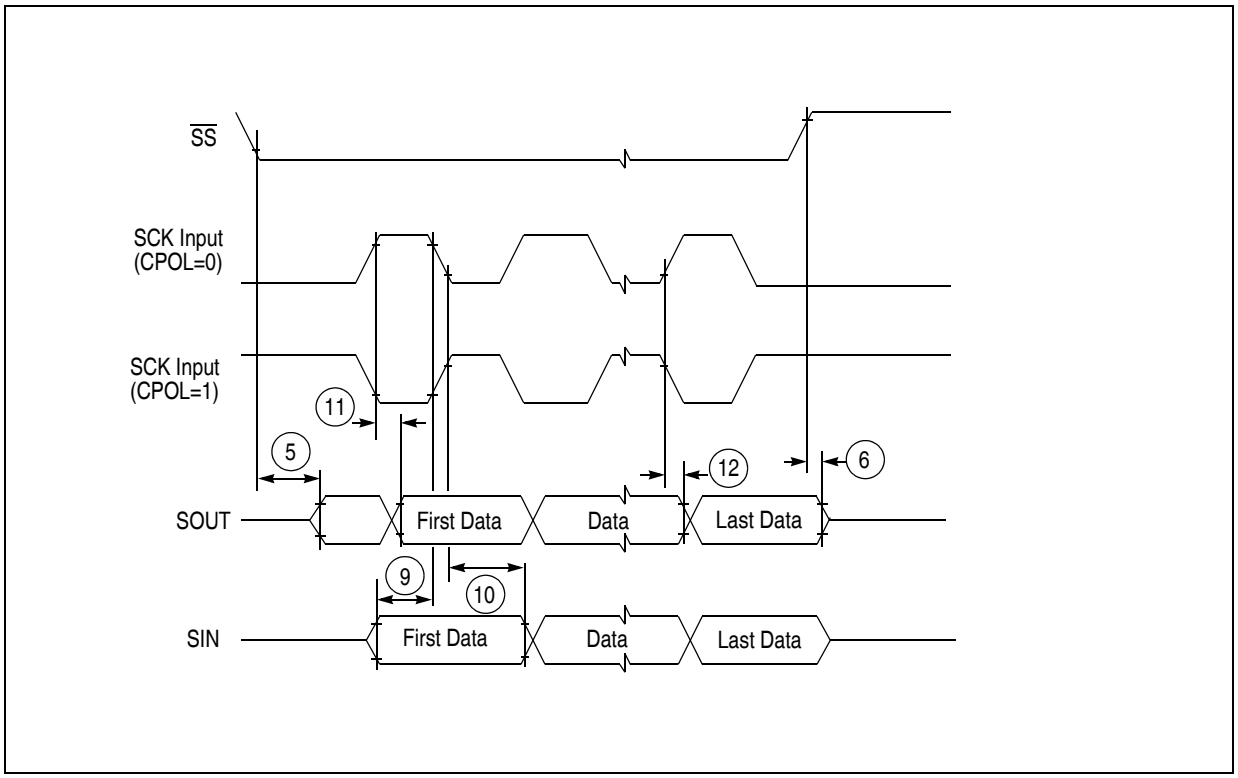


Figure 29. DSPI modified transfer format timing — Slave, CPHA = 1

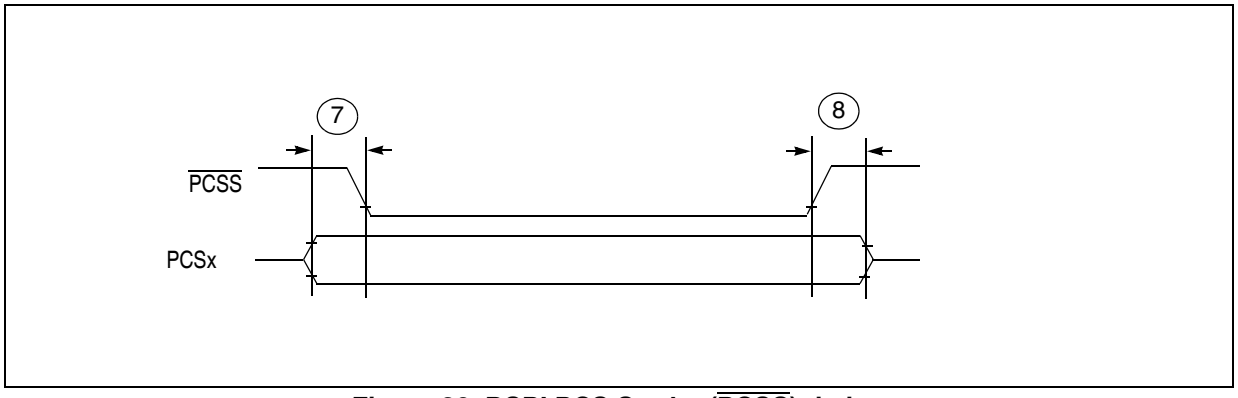


Figure 30. DSPI PCS Strobe ($\overline{\text{PCSS}}$) timing

3.18.9 Video interface timing

Table 33 details the MPC5604E's video encoder block's pixel input clocking requirement.

Table 33. Input pixel clock characteristics

No.	Parameter	Min	Max	Unit
1	PDI Clock Period	10	—	ns
2	PDI Clock Duty Cycle	50	50	%
3	Input setup time	2	—	ns
4	Input Hold Time	2	—	ns
5	Input Pixel Clock Slew Rate	—	2	ns

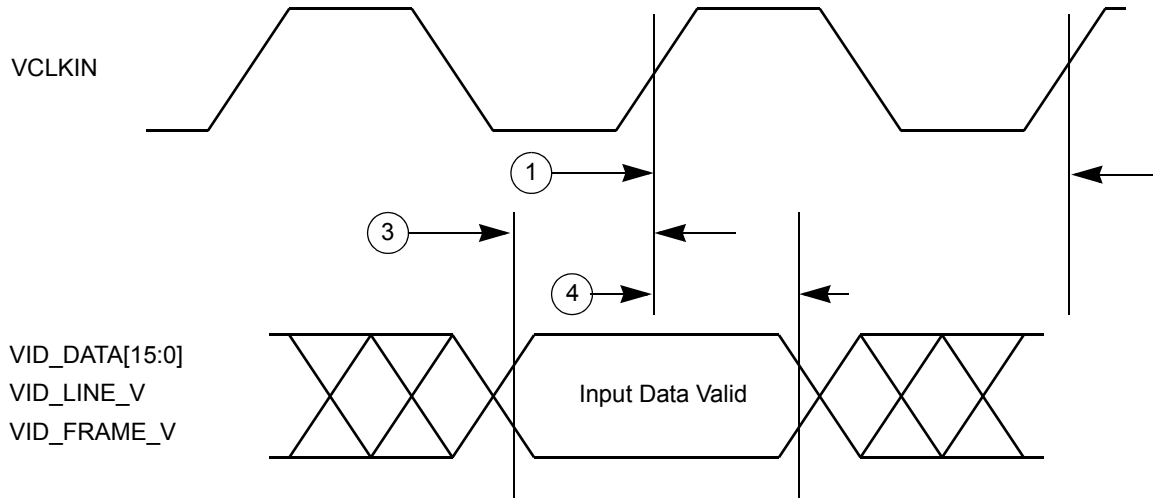


Figure 31. Video interface timing

3.18.10 Fast ethernet interface

MII signals use CMOS signal levels compatible with devices operating at either 5.0 V or 3.3 V. Signals are not TTL compatible. They follow the CMOS electrical characteristics.

3.18.10.1 MII receive signal timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the RX_CLK frequency.

Table 34. MII receive signal timing

No.	Parameter	Min	Max	Unit
1	Rx Clock Period	40	—	ns
2	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
3	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
4	Rx Clock Duty Cycle	40	60	%

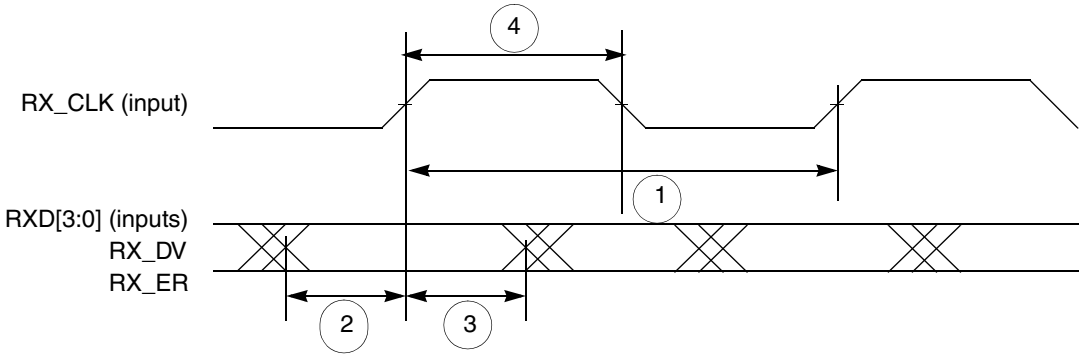


Figure 32. MII receive signal timing diagram

3.18.10.2 MII transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Ethernet chapter for details of this option and how to enable it.

Table 35. MII transmit signal timing[1]

No.	Parameter	Min	Max	Unit
5	TX Clock Period	40	—	ns
6	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
7	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
8	TX Clock Duty Cycle	40	60	%

[1] Output pads configured with SRC = 0b11.

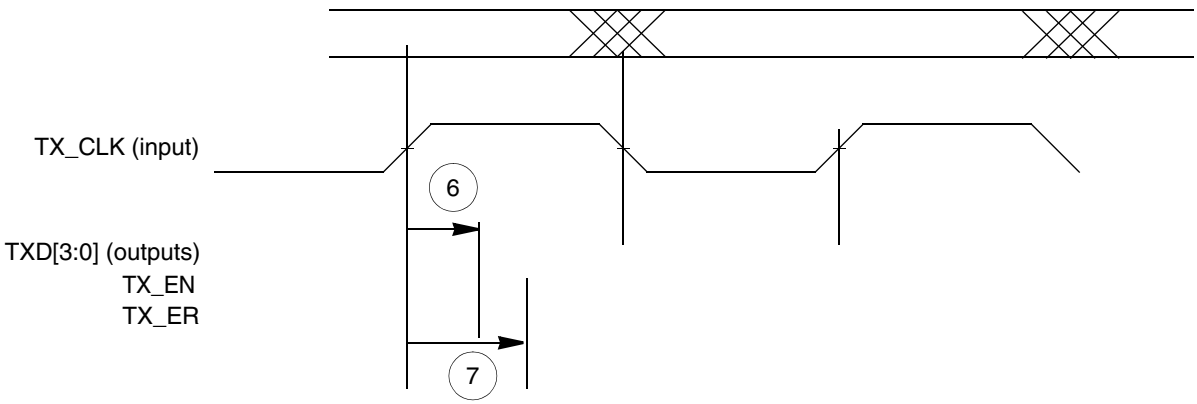


Figure 33. MII transmit signal timing diagram

3.18.10.3 MII async inputs signal timing (CRS and COL)

Table 36. MII async inputs signal timing[1]

No.	Parameter	Min	Max	Unit
9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

[1] Output pads configured with SRC = 0b11.

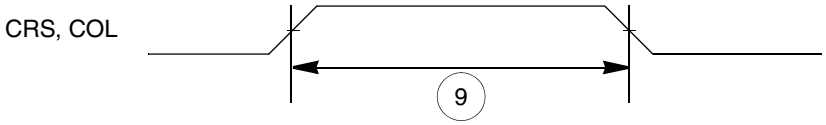


Figure 34. MII async inputs timing diagram

3.18.10.4 MII serial management channel timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 5 MHz.

Table 37. MII serial management channel timing (MDIO and MDC)

No.	Parameter	Min	Max	Unit
1	MDIO Input delay setup	28	—	ns
2	MDIO Input delay hold	0	—	ns
3	MDIO Output delay valid	—	25	ns
4	MDIO Output delay Invalid	0	—	ns
5	MDC clock period	100	—	ns
6	MDC Duty Cycle	40	60	%

3.18.11 I²C timing

Table 38. I²C SCL and SDA input timing specifications

No.	Symbol		Parameter	Value		Unit
				Min	Max	
1	—	D	Start condition hold time	2	—	IP bus cycle[1]
2	—	D	Clock low time	8	—	IP bus cycle[1]
4	—	D	Data hold time	0.0	—	ns
6	—	D	Clock high time	4	—	IP bus cycle[1]
7	—	D	Data setup time	0.0	—	ns
8	—	D	Start condition setup time (for repeated start condition only)	2	—	IP bus cycle[1]
9	—	D	Stop condition setup time	2	—	IP bus cycle[1]

1 Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device. It is equal to the system clock (Sys_clk).

Table 35. I²C SCL and SDA output timing specifications

No.	Symbol		Parameter	Value		Unit
				Min	Max	
1[1]	—	D	Start condition hold time	6	—	IP bus cycle[2]
2[1]	—	D	Clock low time	10	—	IP bus cycle[1]
3[3]	—	D	SCL/SDA rise time	—	99.6	ns
4[1]	—	D	Data hold time	7	—	IP bus cycle[1]
5[1]	—	D	SCL/SDA fall time	—	99.5	ns
6[1]	—	D	Clock high time	10	—	IP bus cycle[1]
7[1]	—	D	Data setup time	2	—	IP bus cycle[1]
8[1]	—	D	Start condition setup time (for repeated start condition only)	20	—	IP bus cycle[1]
9[1]	—	D	Stop condition setup time	10	—	IP bus cycle[1]

1 Programming IBFD (I²C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

2 Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device.

3 Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

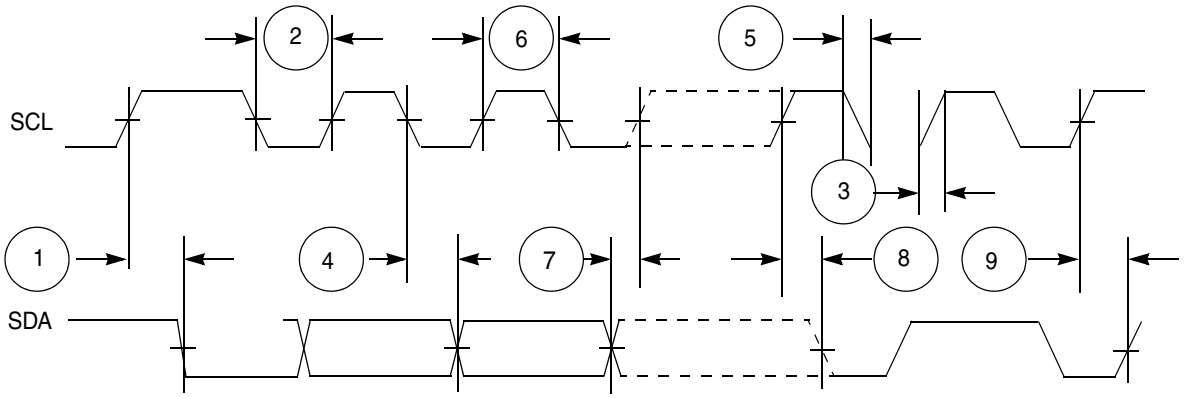


Figure 36. I²C input/output timing

3.18.12 SAI timing

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device.

Table 39. Master Mode SAI Timing

No.	Parameter	Value		Unit
		Min	Max	
	Operating voltage	2.7	3.6	V
S1	SAI_MCLK cycle time	40	—	ns
S2	SAI_MCLK pulse width high/low	45%	55%	MCLK period
S3	SAI_BCLK cycle time	80	—	BCLK period
S4	SAI_BCLK pulse width high/low	45%	55%	ns
S5	SAI_BCLK to SAI_FS output valid	—	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	28	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

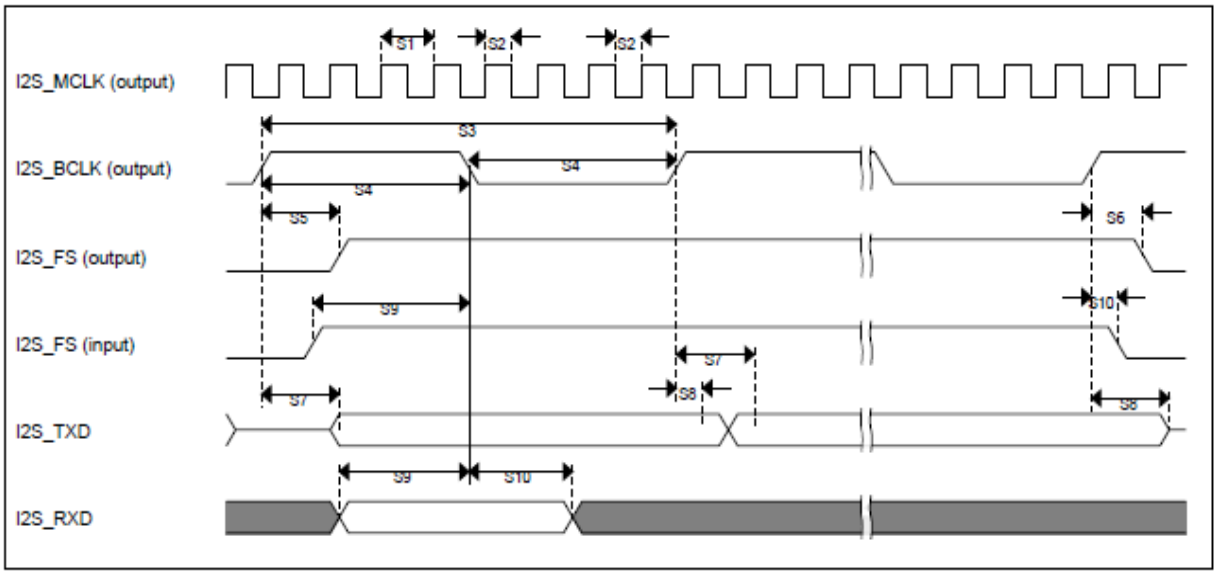


Figure 37. SAI timing master modes

Table 40. Slave Mode SAI Timing

No.	Parameter	Value		Unit
		Min	Max	
	Operating voltage	2.7	3.6	V
S11	SAI_BCLK cycle time (input)	80	—	ns
S12	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	—	ns
S14	SAI_FS input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	28	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	10	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

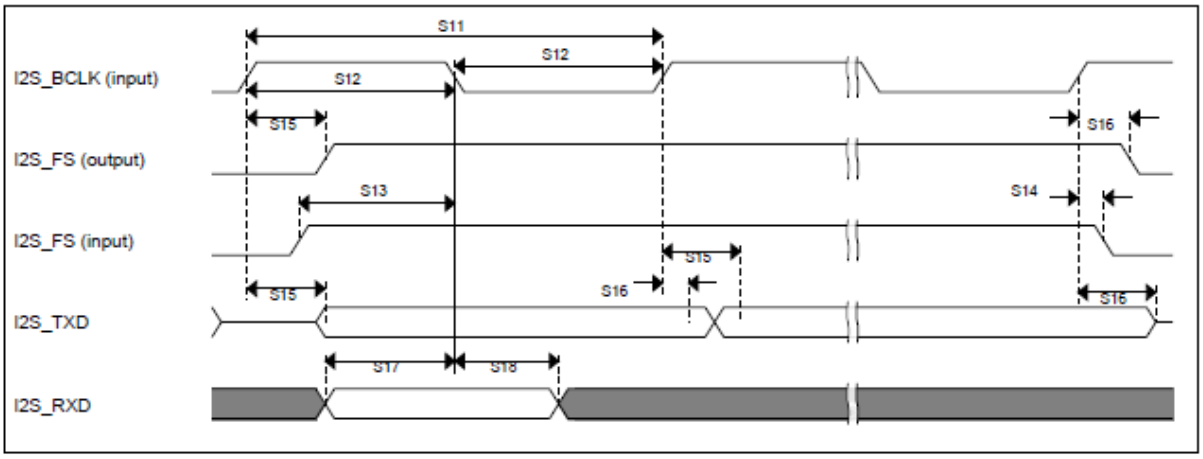


Figure 38. SAI timing slave modes

4 Package mechanical data

4.1 100 LQFP mechanical outline drawing

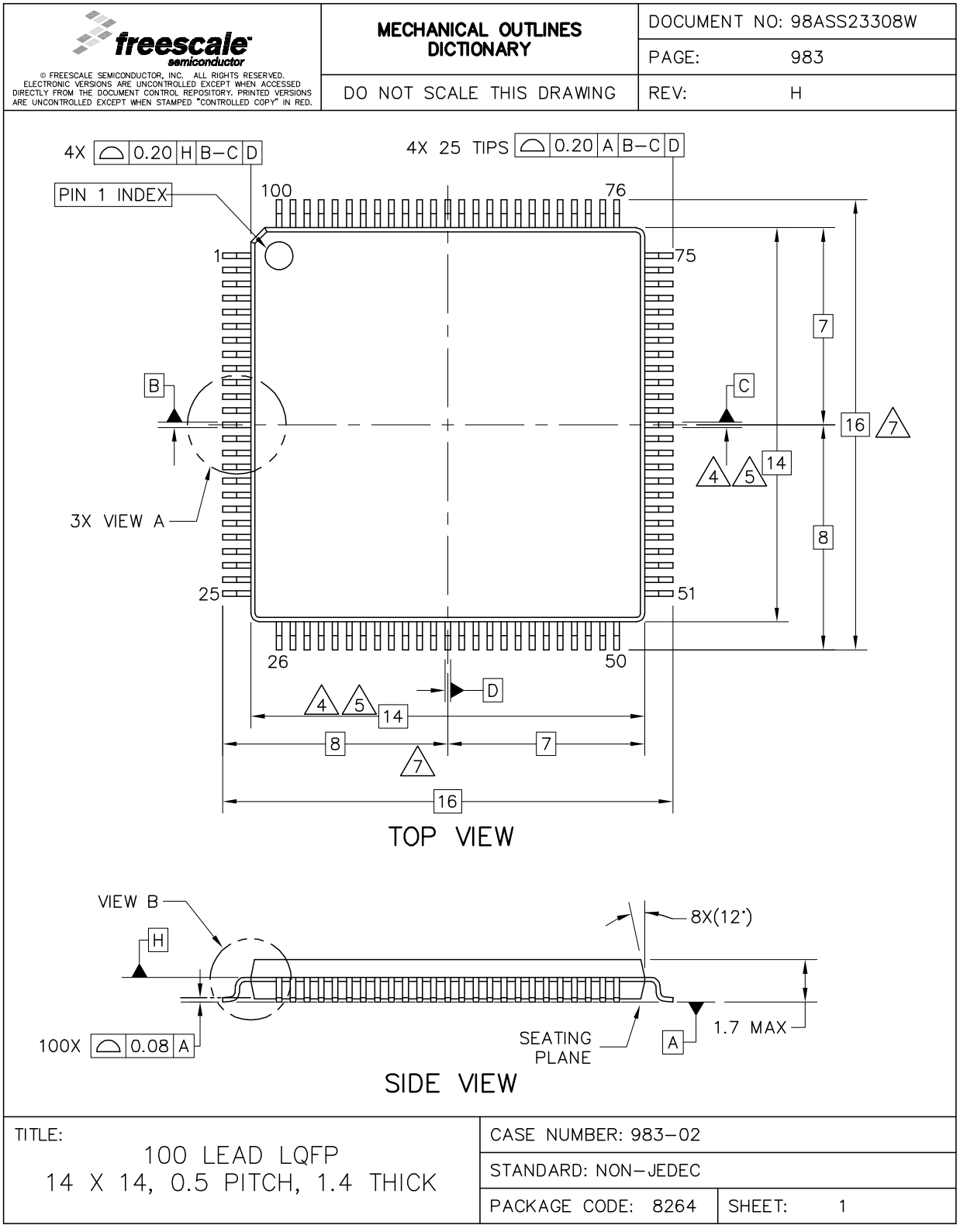


Figure 39. 100 LQFP package mechanical drawing (part 1)

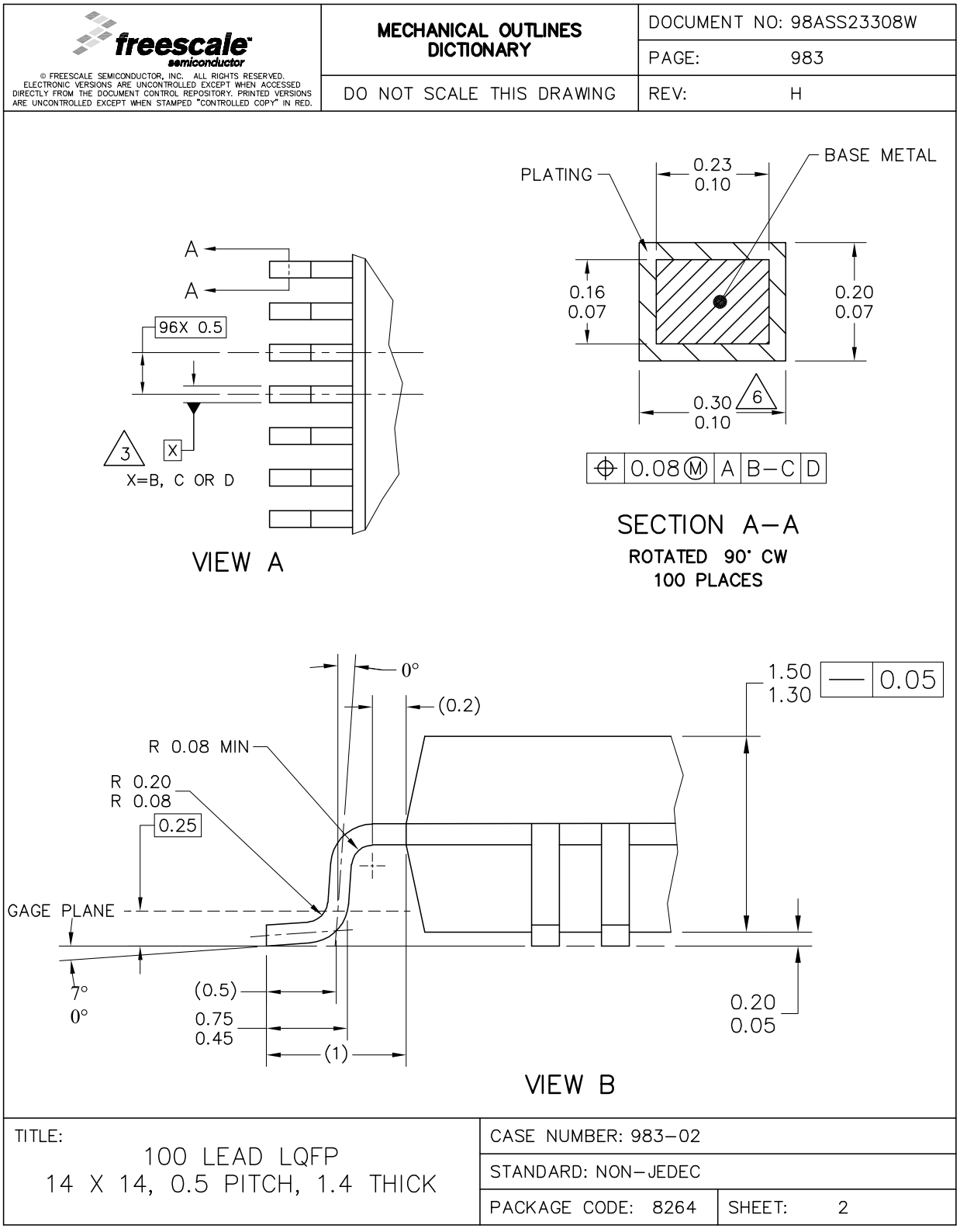


Figure 40. 100 LQFP package mechanical drawing (part 2)

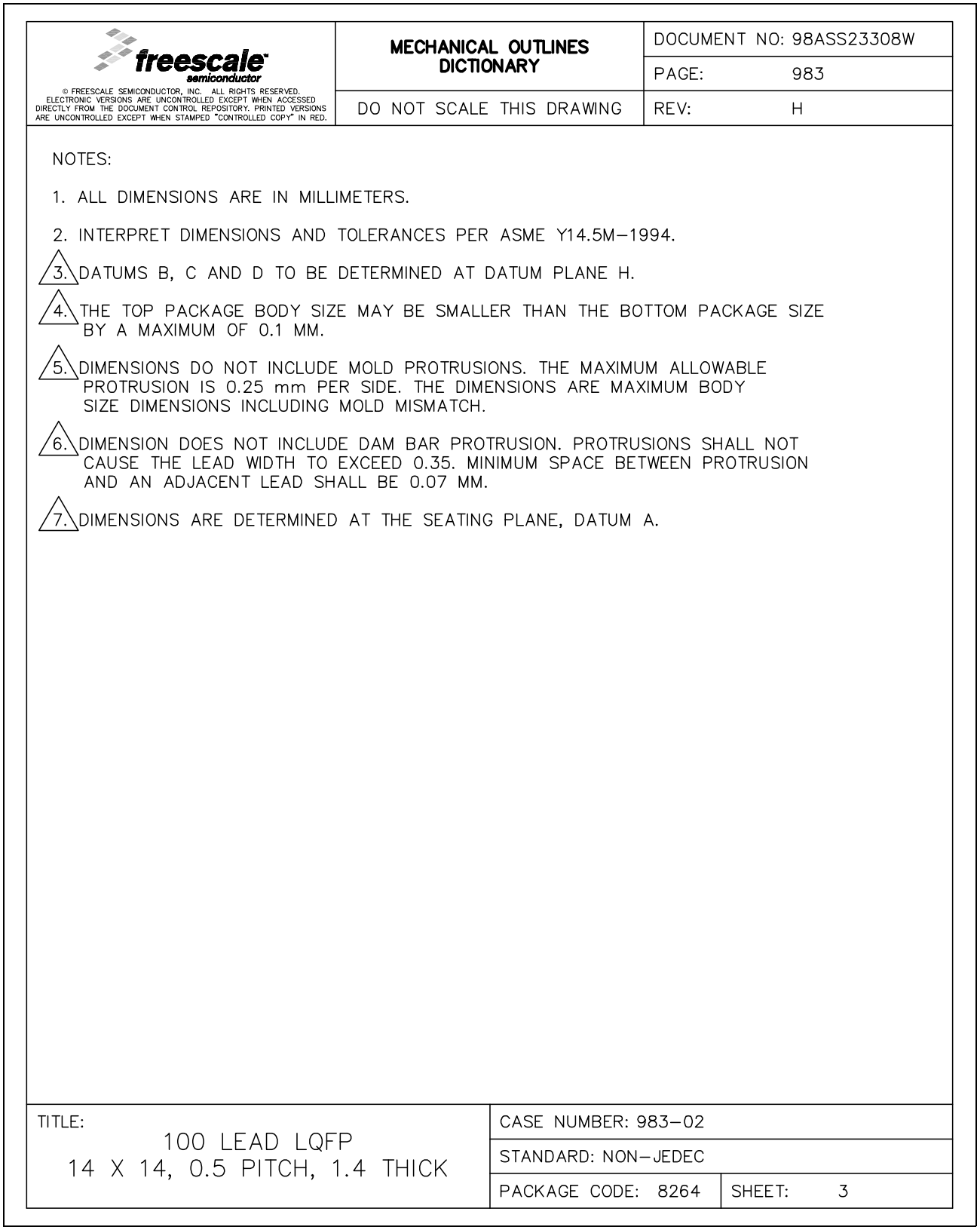


Figure 41. 100 LQFP package mechanical drawing (part 3)

4.2 64 LQFP mechanical outline drawing

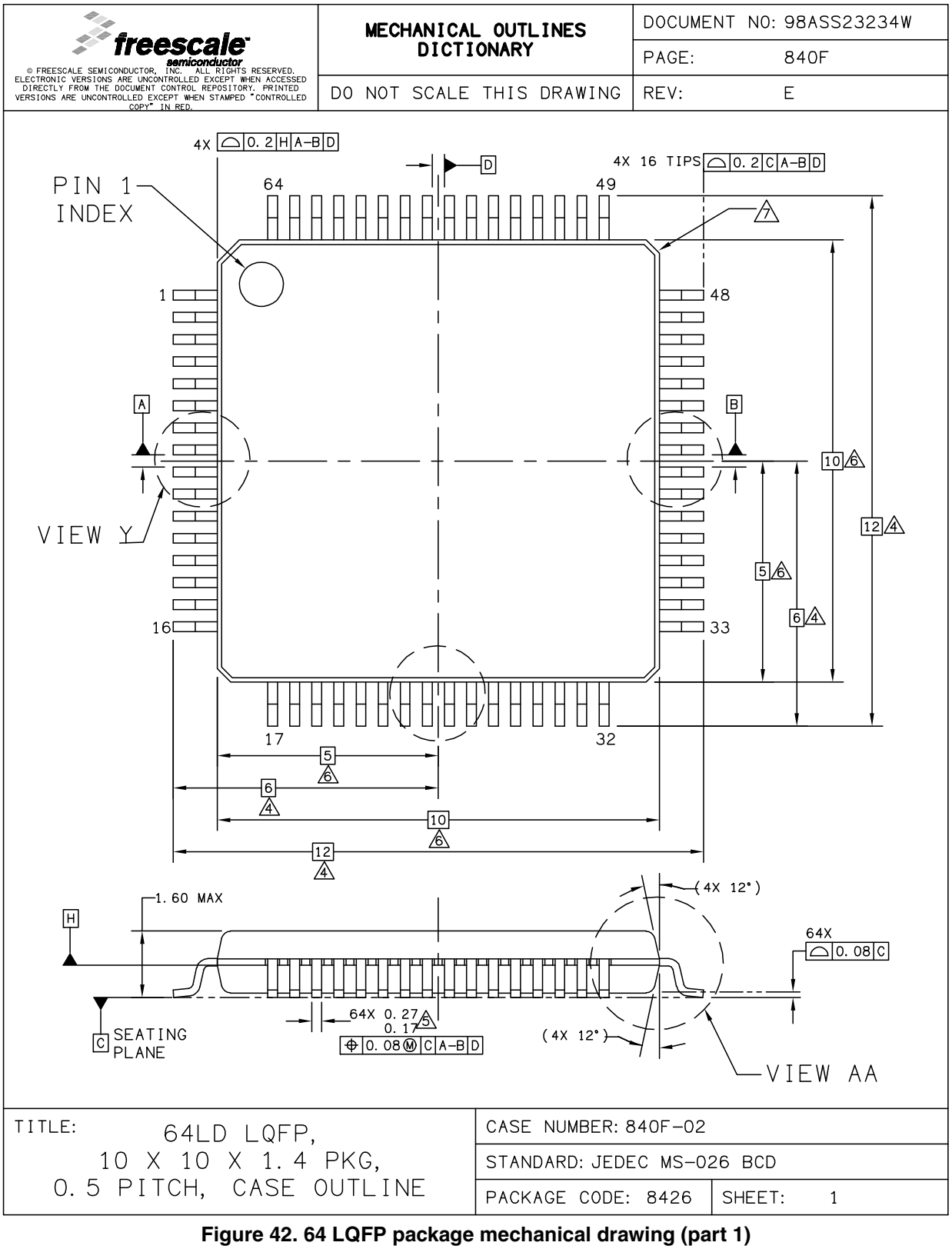


Figure 42. 64 LQFP package mechanical drawing (part 1)

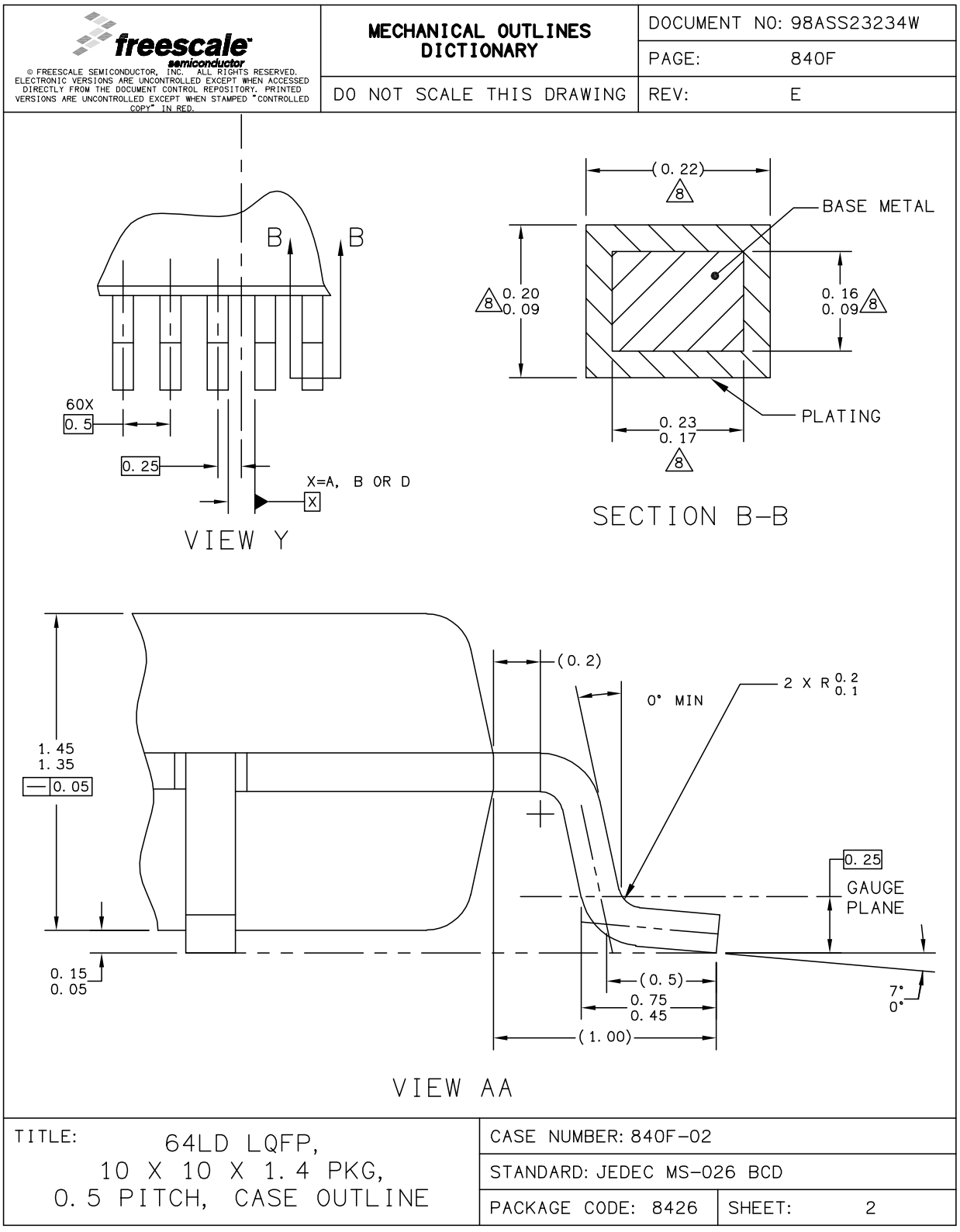
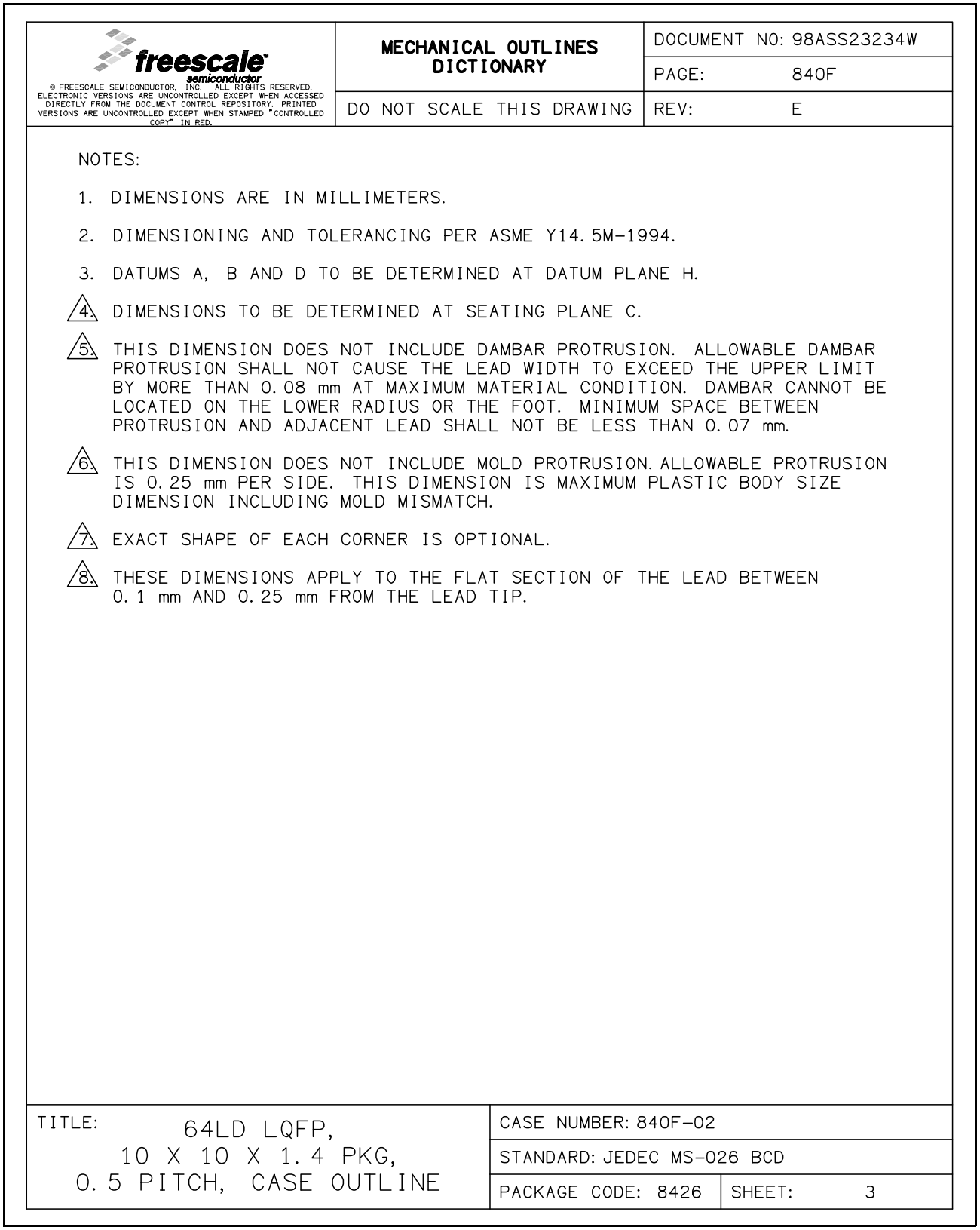


Figure 43. 64LQFP package mechanical drawing (part 2)



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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
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3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

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CASE NUMBER: 840F–02

STANDARD: JEDEC MS–026 BCD

PACKAGE CODE: 8426

SHEET: 3

Figure 44. 64LQFP package mechanical drawing (part 3)

5 Document revision history

Table 41. Revision history

Revision	Date	Substantive changes
1	15 Feb 2011	Initial Release
2	13 June 2011	• In the Recommended operating conditions table, changed the external supply voltage changed from 1.14 V to 1.15 V • Added a footnote in the Device Summary table • Changed the description of VDD_HV_S_BALLAST0 in the Supply pins table
3	1 Nov 2011	• Editorial changes and improvements • In the Low voltage monitor electrical characteristics table, changed the marking of V_{PORUP} from P to D •In the DC electrical characteristics table, changed the I_{OL} of the Medium, low level output voltage to 2 mA. From the same table, removed V_{OL_SYM} and $V_{OH\_SYM.}$ Revised the I_{PU} and I_{PD} •In the Main oscillator electrical characteristics table, changed the minimum value of transconductance to 4 mA/V • In the 16 MHz RC oscillator electrical characteristics table, changed the marking of f_{RC} from P to C and revised its minimum and value. • In the ADC conversion characteristics table, changed the minimum and maximum value of TUE from TBD to -3 and 3 •In the Pin muxing table, C5 port ABS[2] assignment changed from SIUL to MC_RGM •IRevised the 64-pin and 100-pin package pinouts and added a footnote. •In the Supply pins table, revised the description of ADC0 pins •In the Supply pins table, added a column Port Pin and renamed the Symbol column •IRemoved Power Supply segment table • In the Pin Muxing table, clarified the peripherals in the following port pins: C5, A3, A8, A10, A12, A15, C3, C4, C5, C6, C12 • In the Low voltage monitor electrical characteristics table, changed the maximum value of VMLVDDOK_H • In the ADC conversion characteristics, changed the ADC sampling time to 500 ns
3.1	2 Dec 2011	• Inserted values for TBDs in the table EMI Testing Specifications • From Supply Pins table, removed VVD_HV_ADV0 • In the PLLMRFM electrical specifications table, added the value of Self-clocked mode frequency • In the ADC conversion characteristics table, added the value of INJ
4	23 Jan 2012	• System Pin table, swapped the description of XTAL and EXTAL

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