Features

- **LDO1: 2.75V (Default) and 1.8V (Programmable by TWI), 70 mA Linear Very Low Drop Out Regulator with High PSRR and Low Noise.**
- **LDO2: 1.8V (Default) and 1.5V (Programmable by TWI), 70 mA Linear Low Drop Out Regulator with High PSRR and Low Noise.**
- **LDO3: 1.8V (Default) and 1.5V or 1.2V (Programmable by TWI), 70 mA Linear Low Drop Out Regulator with high PSRR and Low noise.**
- **LDO4: 1.8V, 2mA Linear Low Drop Out Regulator with Very Low Quiescent Current, +/- 100 mV Adjustable.**
- **Main Supply Rail from 2.8V to 5.5V**
- **Independent Auxiliary Supply for LDO4 Backup Section, 2.8V to 5.5V**
- **Internal State Machine for Startup and Delayed Reset Generation**
- **Additional External Reset Input**
- **Two Wire Interface for Independent Power Up/Power Down and Output Voltage Programming for Each LDO.**
- **LDOs Voltage Customization Possible on Request**
- **Available in 3 x 3 x 0.9 mm 16-pin QFN Package**
- **Applications: GPS Modules, WLAN Devices, Wireless Modules.**

1. Description

The AT73C237 is a four-channel Power Supply Power Management Unit (PMU) available in a small outline QFN 3 x 3mm package. It is a fully integrated, attractively priced, combined Power Management device for wireless modules, GPS and WLAN devices. It integrates 4X Linear Low Drop Out Regulators, three of which (LDO1, 2, 3) provide high-accuracy RF performance and 1X (LDO4) with very low quiescent current, that can be supplied by an external backup battery (VDD4) on a separate rail. An internal Low Power Bandgap (LPBG) requiring no external capacitor for decoupling, is used as reference voltage for LDO4 and starts when VDD4 is present. LDO4 regulates its output voltage with extremely low quiescent current, maximizing the lifetime of the backup battery.

An Internal State Machine manages the startup of the other LDOs. An economic High Precision Bandgap (HPBG) provides highly accurate, low noise voltage reference to LDOs 1, 2, 3 while operating in switching mode to optimize the quiescent current.

The AT73C237 features a Two-wire Interface (TWI) to increase the efficiency of the system by disabling individually each LDO when not needed.

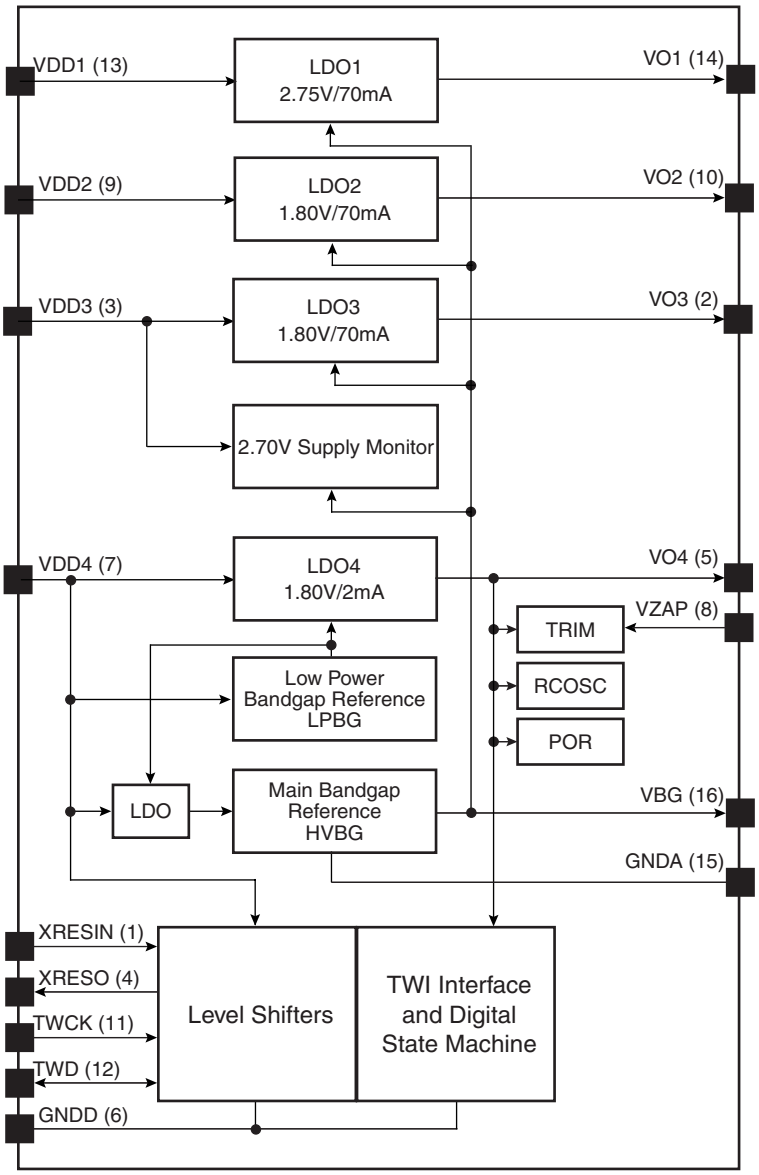
Power Management and Analog Companions (PMAAC)

AT73C237 4-channel Power Management for Wireless Modules

6362A–PMAAC–01-Jul-08

2. Block Diagram

Figure 2-1. AT73C237 Functional Block Diagram



3. Pin Description

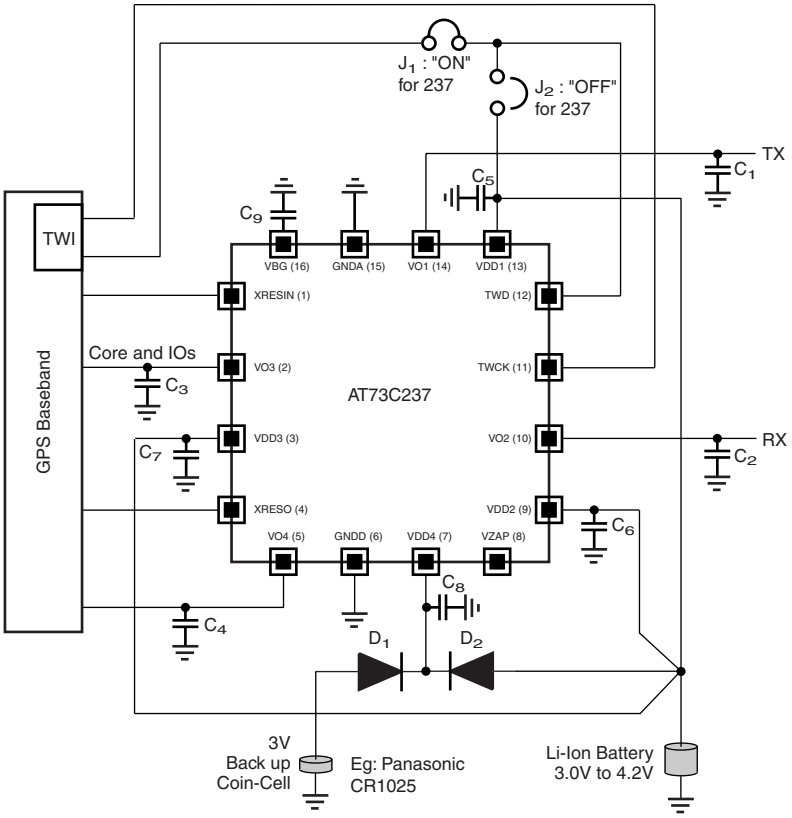
Table 3-1. Pin Description

Pin Name	I/O	Pin Number	Type	Function
XRESIN	Input	1	Digital	Reset in pin
VO3	Output	2	Analog	LDO3 output voltage
VDD3	Input	3	Power	LDO3 input voltage
XRESO	Output	4	Digital	Reset out pin
VO4	Output	5	Analog	LDO4 output voltage
GNDD	GND	6	Power	Digital ground
VDD4	Input	7	Power	LDO4 input voltage
VZAP(1)	Input	8	Digital	Reserved for manufacturing purposes.
VDD2	Input	9	Power	LDO2 input voltage
VO2	Output	10	Analog	LDO2 output voltage
TWCK(2)	Input	11	Digital	TWI input clock or LDO1,2,3 enable at logic “1“, disable at “0“
TWD(3)	Input	12	Digital	TWI input/output or tied to Vdd
VDD1(4)	Input	13	Power	LDO1 input voltage
VO1	Output	14	Analog	LDO1 output voltage
GNDA/AVSS	GND/Input	15	Analog	Analog ground and ESD ground
VBG	Output	16	Analog	Voltage reference for analog cells

Note:
1. Connect to ground (via an internal pull-down)
2. Connected to VDD1, 2 or 3 on AT73C237.
3. Connected to VDD1, 2 or 3 on AT73C237.
4. VDD1, 2, 3 should have the same input voltage.

4. Application Block Diagram

Figure 4-1. AT73C237 Application Block Diagram With GPS Module



Typical Application Components Design

Schematic Reference	Pin	Description
C1	VO1	2.2 µF ± 15% Ceramic Capacitor, X5R, 0402, 6.3V MURATA®: GRM155R60J225ME15 TDK: C1005X5R0J225MT
C2	VO2	
C3	VO3	
C4	VO4	
C5	VDD1	1 µF ± 15% Ceramic Capacitor, X5R, 0402, 6.3V MURATA: GRM155R60J105KE19 TDK: C1005X5R0J105KT
C6	VDD2	
C7	VDD3	
C8	VDD4	
C9	VBG	100 nF ± 15% Ceramic Capacitor, X5R, 0402, 10V MURATA: GRM155R61A104KA01 TDK: C1005X5R1C104KT
D1, D2		ON-Semiconductor®: BAS70-04LT1

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5-1. Absolute Maximum Ratings

Operating Temperature (Industrial).....-40°C to + 85°C
Storage Temperature.....-55°C to + 150°C
Power Supply Input on V_{DD}.....-0.3V to + 5.5V
Digital I/O Input Voltage..... -0.3V to + 5.5V
All Other Pins.....-0.3V to + 5.5V
ESD (all pins).....2 KV

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

Table 5-2. Recommended Operating Conditions

Parameter	Condition	Min	Max	Units
Operating Temperature		-40	85	°C
Power Supply Input	V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}	2.8	5.5	V

5.3 Quiescent Current In Different Operating Modes

Table 5-3. Quiescent Current In Different Operating Modes

Modes	Conditions	Quiescent [µA]	
		Typ	Max
MODE0	VDD4 not present, chip disabled, all VDDs quiescent current	0	0.1
MODE1	VDD4 present, VDD3 not present (typical mode with back-up battery on VDD4) • LDO4 • LPBG • POR • HPBG in switching mode	12	18
MODE2	VDD4 present, VDD3 present • LDO4 • LPBG • POR • Supply Monitor • Registers • Oscillator • State Machine • HPBG • LDO1 • LDO2 • LDO3	800	1000

6. Startup Procedure

6.1 At VDD4 Rising

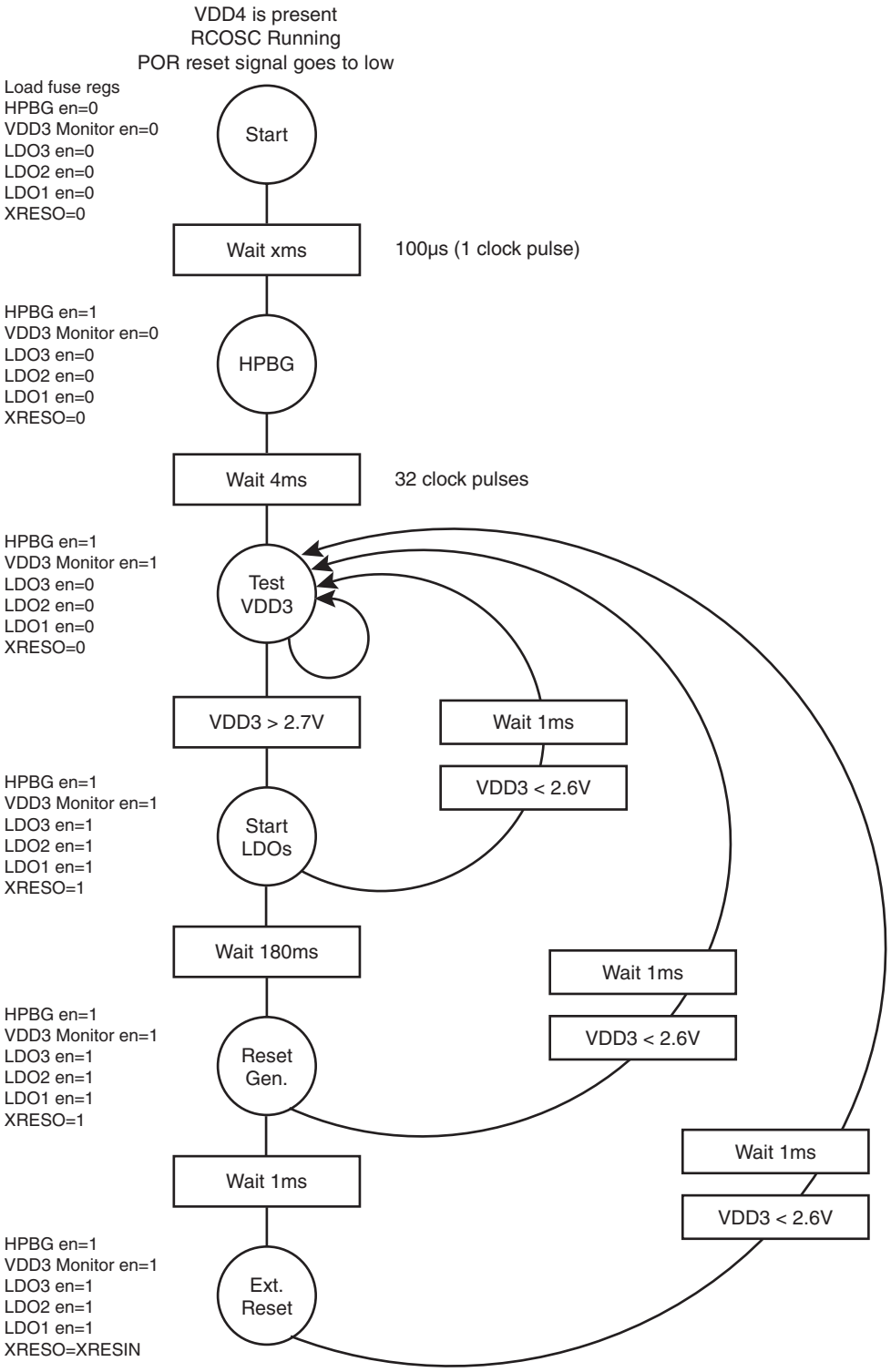
- LPBG, LDO4, RCOSC start up
- POR connected to LDO4 output VO4 resets the state machine and enables:
  - The reading of the internal fuses (TRIM cell in the application diagram) in order to set up the programmed output voltage of LDO1, LDO2, LDO3, and the correct reference voltage and oscillation frequency
  - The Two Wire Interface
  - Then under control of the state machine:
    a. HPBG is turned on
    b. After 4 ms, the Supply Monitor on VDD3 is turned on.
    c. If VDD3 is present and greater than 2.7V, LDO1, 2, 3 are turned on. During LDO regulator startup VDD3 voltage is checked.
    d. Then XRESO is kept grounded for 180 ms, and set to “1” for 1ms before following XRESIN. During that state VDD3 voltage is monitored and if lower than 2.6V, LDO regulators 1, 2 and 3 are stopped and XRESO grounded.

Both XRESIN and the Supply Monitor on VDD3 are debounced at rising and falling edges for two 10 kHz clock cycles. The debounce time is typically between 100 µs and 200 µs. Timings are defined ± 40%.

6.2 At VDD3 Falling

- The Supply monitor generates a shut down control signal when VDD3 reaches 2.6V
- The State machine sets XRESO to logic “0”.
- The State machine switches off LDO1, LDO2, LDO3. HPBG is kept enabled in order to assure a fast new startup of the LDOs.

Figure 6-1. Startup Procedure



7. Timing Diagram

Figure 7-1. AT73C237 Timings

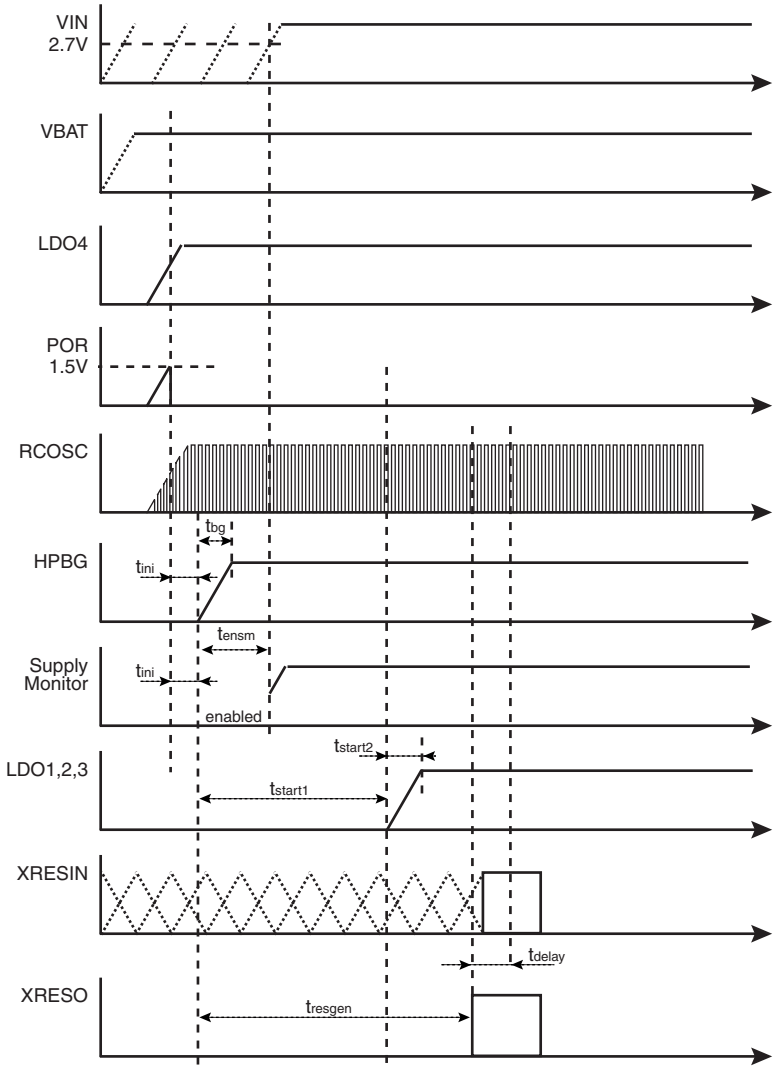


Table 7-1. Timing Parameters

Parameter	Signal	Constraint	Min	Max	Units
t_{ini}		Guard time		100	µsec
t_{bg}	HPBG	HPBG startup time		2	msec
t_{ensm}	Supply monitor	Supply monitor enable		4	msec
t_{start1}	V_{O1}, V_{O2}, V_{O3}		3	5	µsec
t_{start2}	V_{O1}, V_{O2}, V_{O3}	LDO1,2,3 Startup time	10	100	µsec
t_{resgen}	XRESO		100	500	msec
t_{delay}				1	msec

8. Electrical Specification

8.1 LDO1

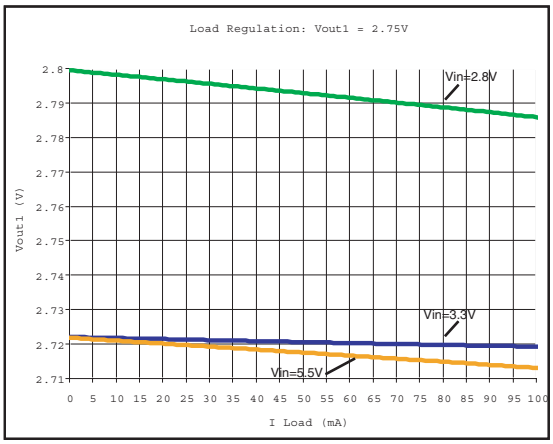
Table 8-1. LDO1 Parametric Table

Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{DD1}	Operating supply voltage	Switching Regulated	2.8	3.3	5.5	V
V_{O1}	Output voltage	Default	2.70	2.75	2.8	V
		Programmed	1.75	1.80	1.85	
I_1	Load current	With at least 300mV drop out			100	mA
		With at least 200mV drop out			70	
I_{QC}	Quiescent current			250	300	µA
I_{SC}	Shutdown current	HiZ output			1	µA
I_{SH}	Short circuit current			350		mA
t_R	Startup time		1	10	100	µsec
ΔV_{DC}	Line regulation static	From VDD=3.0V to 3.6V			5	mV
ΔV_{DC}	Load regulation static	From 10% to 100% I_1			30	mV
		From 0 to 100% I_1			40	
PSSR	Power Supply Rejection Ratio	Sine Wave, 100 kHz frequency, 3.3V mean +/- 100 m v_{PP}	65			dB
		Sine Wave, 10 kHz frequency, 3.3V mean +/- 100 m v_{PP}	60			dB
		Sine Wave, 1 kHz frequency, 3.3V mean +/- 100 m v_{PP}	45			dB
ΔV_{OUT}	Startup Overshoot				100	mV
V_{NT}	Total Output Noise	10 Hz - 100 kHz		35	100	μV_{RMS}

Table 8-2. LDO1 External Components

Schematic Reference	Description
C_1 (Input Capacitor)	2.2µF ± 15% Ceramic Capacitor, X5R, 0402, 6.3V MURATA: GRM155R60J225ME15 TDK: C1005X5R0J225MT
C_5 (Output Capacitor)	1µF ± 15% Ceramic Capacitor, X5R, 0402, 6.3V MURATA: GRM155R60J105KE19 TDK: C1005X5R0J105KT

Figure 8-1. LDO Load Regulation



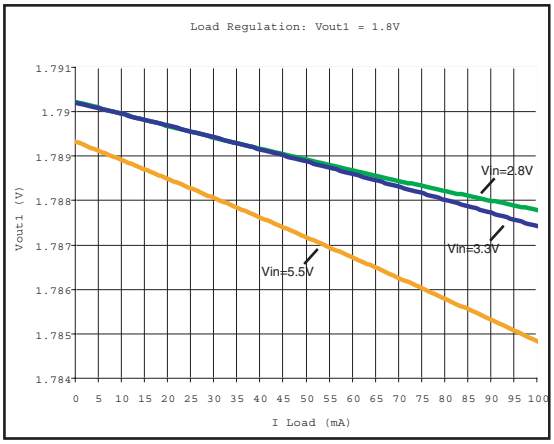
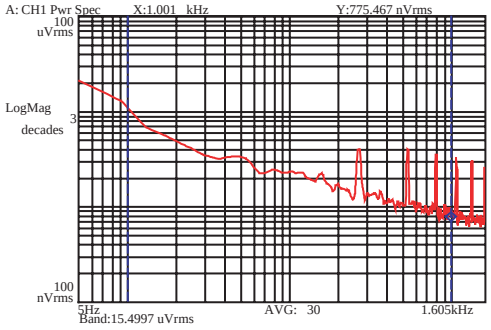
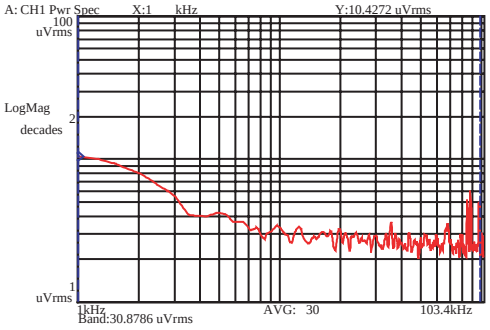


Figure 8-2. LDO1 Output Noise





8.2 LDO2

Table 8-3. LDO2 Parametric Table

Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{DD2}	Operating supply voltage	Switching Regulated	2.8	3.3	5.5	V
V_{O2}	Output voltage	Default	1.75	1.80	1.85	V
		Programmed	1.45	1.50	1.55	
I_2	Load current	With at least 300mV drop out			100	mA
		With at least 200mV drop out			70	
I_{QC}	Quiescent current			250	300	µA
I_{SC}	Shutdown current	HiZ output			1	µA
I_{SH}	Short circuit current			350		mA
t_R	Startup time		1	10	100	µsec
ΔV_{DC}	Line regulation static	From VDD=3.0V to 3.6V			5	mV
ΔV_{DC}	Load regulation static	From 10% to 100% I_2			30	mV
		From 0 to 100% I_2			40	
PSSR	Power Supply Rejection Ratio	Sine Wave, 100 kHz frequency, 3.3V mean +/- 100 m v_{PP}	70			dB
		Sine Wave, 10 kHz frequency, 3.3V mean +/- 100 m v_{PP}	65			dB
		Sine Wave, 1 kHz frequency, 3.3V mean +/- 100 m v_{PP}	45			dB
ΔV_{OUT}	Startup Overshoot				100	mV
V_{NT}	Total Output Noise	10 Hz - 100 kHz		25	50	μV_{RMS}

Table 8-4. LDO2 External Components

Schematic Reference	Description
C_2 (Input Capacitor)	2.2µF ± 15% Ceramic Capacitor, X5R, 0402, 6.3V MURATA: GRM155R60J225ME15 TDK: C1005X5R0J225MT
C_6 (Output Capacitor)	1µF ± 15% Ceramic Capacitor, X5R, 0402, 6.3V MURATA: GRM155R60J105KE19 TDK: C1005X5R0J105KT

Figure 8-3. LDO2 Load Regulation

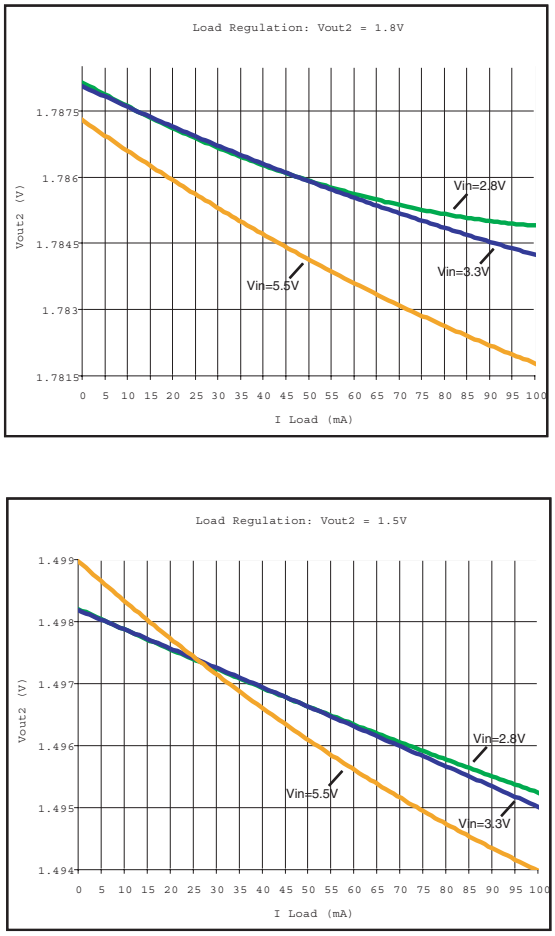
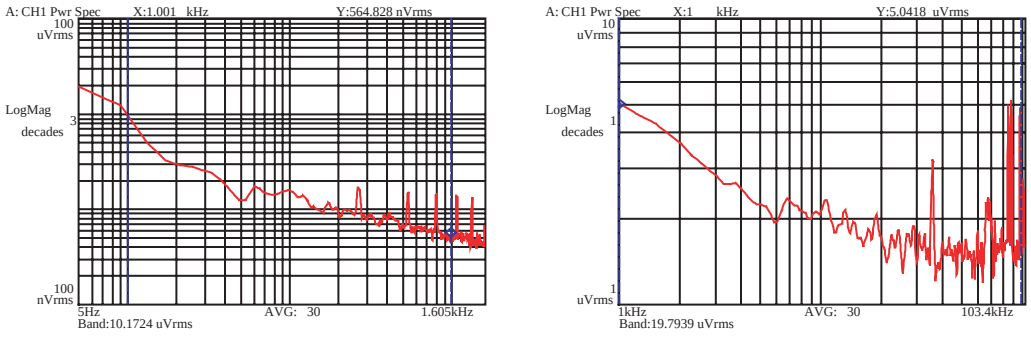


Figure 8-4. LDO2 Output Noise



8.3 LDO3

Table 8-5. LDO3 Parametric Table

Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{DD3}	Operating supply voltage	Switching Regulated	2.8	3.3	5.5	V
V_{O3}	Output voltage	Default	1.75	1.80	1.85	V
		Programmed	1.45	1.50	1.55	
		Programmed	1.18	1.23	1.28	
I_3	Load current	With at least 300mV drop out			100	mA
		With at least 200mV drop out			70	
I_{QC}	Quiescent current			250	300	µA
I_{SC}	Shutdown current	HiZ output			1	µA
I_{SH}	Short circuit current			350		mA
t_R	Startup time		1	10	100	µsec
ΔV_{DC}	Line regulation static	From VDD=3.0V to 3.6V			5	mV
ΔV_{DC}	Load regulation static	From 10% to 100% I_3			30	mV
		From 0 to 100% I_3			40	
PSSR	Power Supply Rejection Ratio	Sine Wave, 100 kHz frequency, 3.3V mean +/- 100 m v_{PP}	70			dB
		Sine Wave, 10 kHz frequency, 3.3V mean +/- 100 m v_{PP}	65			dB
		Sine Wave, 1 kHz frequency, 3.3V mean +/- 100 m v_{PP}	45			dB
ΔV_{OUT}	Startup Overshoot				100	mV
V_{NT}	Total Output Noise	10 Hz - 100 kHz		20	50	μV_{RMS}

Table 8-6. LDO3 External Components

Schematic Reference	Description
C_3 (Input Capacitor)	2.2µF ± 15% Ceramic Capacitor, X5R, 0402, 6.3V MURATA: GRM155R60J225ME15 TDK: C1005X5R0J225MT
C_7 (Output Capacitor)	1µF ± 15% Ceramic Capacitor, X5R, 0402, 6.3V MURATA: GRM155R60J105KE19 TDK: C1005X5R0J105KT

Figure 8-5. LDO3 Load Regulation

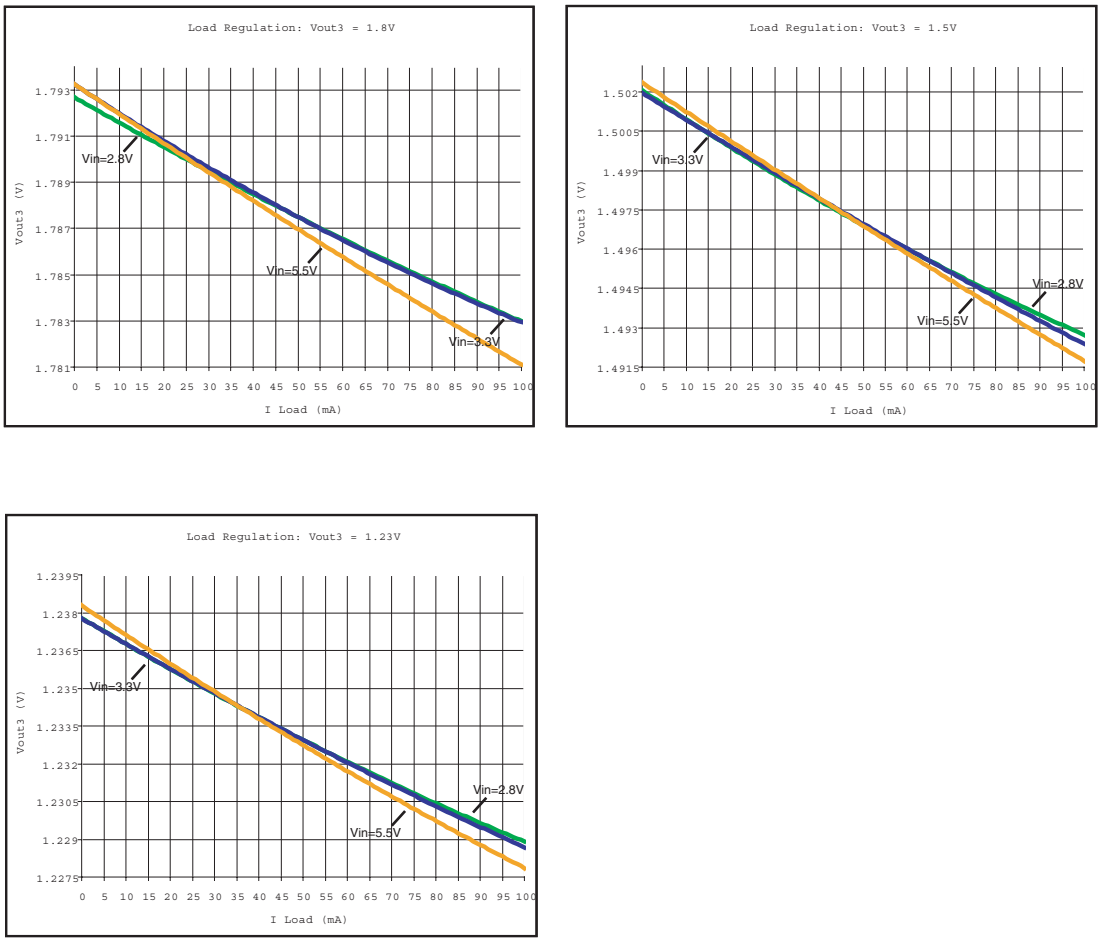
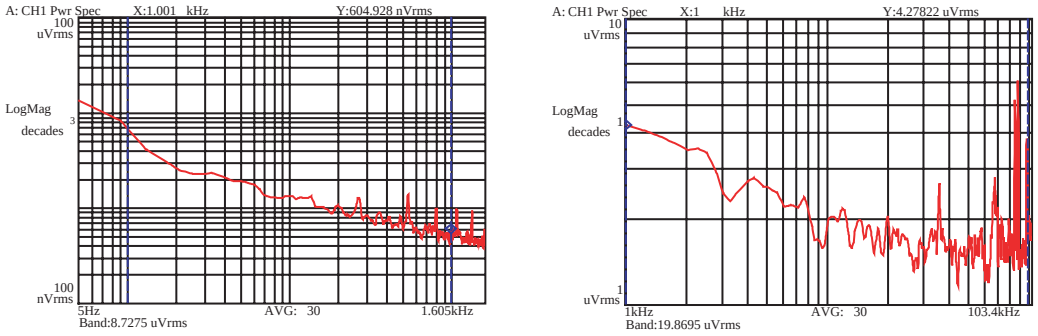


Figure 8-6. LDO3 Output Noise



8.4 LDO4

Table 8-7. LDO4 Parametric Table

Symbol	Parameter	Comments	Min	Typ	Max	Units
V_{DD4}	Operating supply voltage	Switching Regulated	2.8	3.3	5.5	V
V_{O4}	Output voltage	Default	1.7	1.8	1.9	V
I_4	Load current				2	mA
TVO4	Trimming range		-80	0	80	mV
I_{QC}	Quiescent current			1	3	µA
I_{SC}	Shutdown current	HiZ output			0.5	µA
t_R	Startup time		1	10	100	µsec
ΔV_{DC}	Line regulation static	2.8V< VDD4 <5.5V			100	mV
ΔV_{DC}	Load regulation static	0< I_4 <1.8mA			100	mV

Table 8-8. LDO4 External Components

Schematic Reference	Description
C_4 (Input Capacitor)	2.2µF ± 15% Ceramic Capacitor, X5R, 0402, 6.3V MURATA: GRM155R60J225ME15 TDK: C1005X5R0J225MT
C_8 (Output Capacitor)	1µF ± 15% Ceramic Capacitor, X5R, 0402, 6.3V MURATA: GRM155R60J105KE19 TDK: C1005X5R0J105KT

8.5 High Performance Bandgap (HPBG)

Table 8-9. HPBG Parametric Table

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_I	Operating supply voltage	Backup Battery or Supercap	2.4		3.6	V
V_{BG}	Output voltage	Factory trimmed		1.231		V
I_{SC}	Shutdown current	encore = en = 0, dcrun = 0 (1)		1	6	µA
I_{QC}	Quiescent current	Not pulsed			300	µA
		Pulsed			30	
t_S	Startup time	C_9= 100 nF		1	2	ms
V_N	Output noise	BW 10 Hz to 100 kHz		7		μV_{RMS}

Table 8-10. External Components

Schematic Reference	Description
C_9 (Output Capacitor)	100 nF ± 15% Ceramic Capacitor, X5R, 0402, 10V MURATA P/N: GRM155R61A104KA01 TDK: C1005X5R1C104KT

8.6 Low Power Bandgap (LPBG)

Table 8-11. LPBG Parametric Table

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	Operating supply voltage	Backup Battery or Supercap	2.8		5.5	V
I_{QC}	Quiescent current	At V_{BAT} 3. =V		4	7.5	µA
t_S	Startup time			50	100	µs
V_{LPBG}	Bandgap Voltage		1.15	1.2	1.25	V

8.7 Voltage Monitor

Table 8-12. Voltage Monitor Parametric Table

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{QC}	Quiescent current			5	20	µA
V_{PON}	SM on threshold		2.7		2.72	V
V_{POFF}	SM on threshold		2.6		2.62	V

8.8 XRESIN

Table 8-13. XRESIN Parametric Table

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_I	Input supply voltage range	Driven by CPU GPIO		V_{DD4}		V
		Driven by CPU open drain output		Hiz		V
		Connected to V_{DD4} when not used		V_{DD4}		V
I_{IH}	High input current				5	µA
I_{IL}	Low input current				50	µA

8.9 XRESO

Table 8-14. XRESO Parametric Table

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	Input supply voltage range			V_{DD4}		V
V_{OH}	High output voltage				200	mV
V_{OL}	Low output voltage				150	mV

8.10 TWCK

Table 8-15. TWCK Parametric Table

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	Input supply voltage range			V_{DD4}		V
I_{IH}	High input current				15	µA
I_{IL}	Low input current				13	µA

8.11 TWD

Table 8-16. TWD Parametric Table

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	Input supply voltage range			V_{DD4}		V
I_{IH}	High input current			20		µA
I_{IL}	Low input current			20		µA
V_{OH}	High output voltage				200	mV
V_{OL}	Low output voltage				150	mV

9. Functional Description

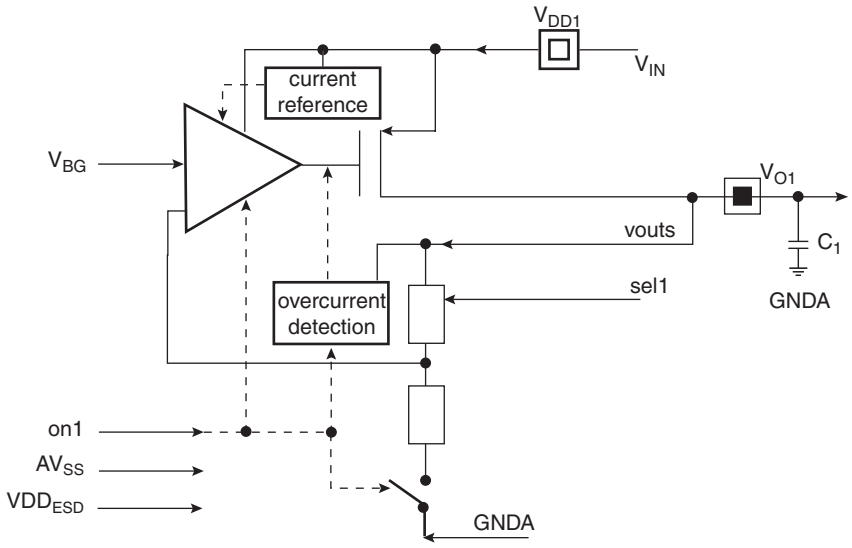
The AT73C237 is a fully integrated, attractively priced, combined Power Management. It integrates the following power supplies channels.

9.1 LDO1

LDO1 is a 2.75V/70mA LDO, compatible with RF performances. LDO1 can work with supply from 3.0V up to 5.5V and needs at least 300 mV of minimum drop-out. This LDO is designed to supply the RF section of wireless devices, showing high PSRR up to 100 kHz with very low noise on wide frequency bandwidth. LDO1 requires a 2.2 µF output capacitor.

- Additionally, 1.80V output voltages programming is possible via the TWI serial interface.

Figure 9-1. LDO1 Functional Diagram

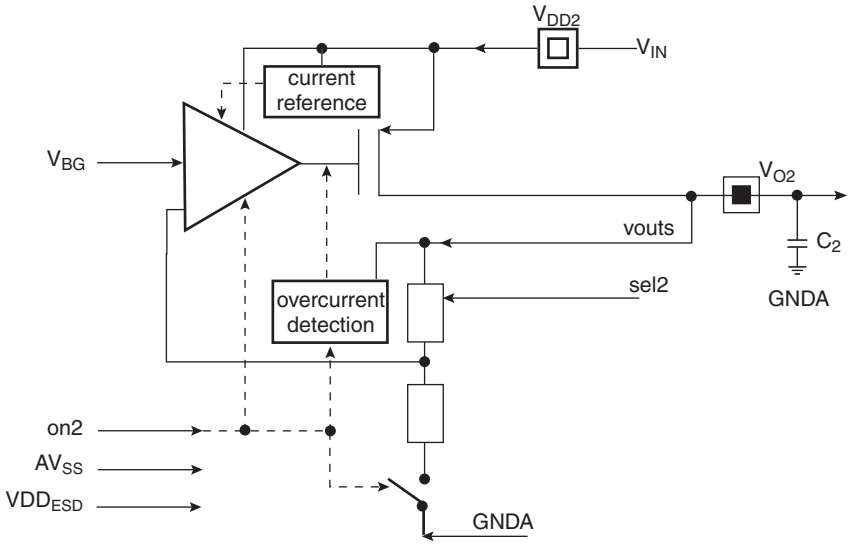


9.2 LDO2

LDO2 is a 1.80V/70mA LDO, compatible with RF performances. LDO2 can work with supply from 3.0V up to 5.5V and needs at least 300 mV of minimum drop-out. This LDO is designed to supply RF section of wireless devices, showing high PSRR up to 100kHz, very low noise on wide frequency bandwidth. LDO2 requires a 2.2 µF output capacitor.

- Additionally, 1.50V output voltages programming is possible via the TWI serial interface.

Figure 9-2. LDO2 Functional Diagram

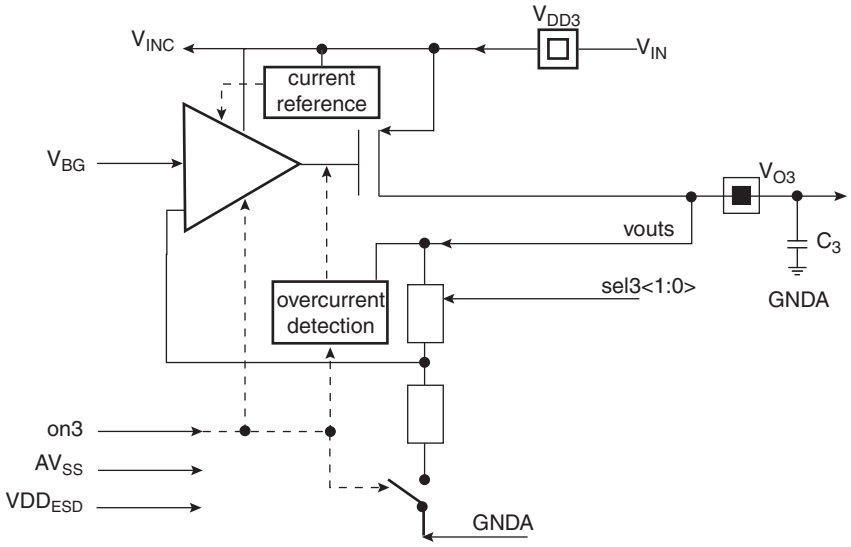


9.3 LDO3

LDO3 is a 1.80V/70mA LDO, compatible with RF performances (see electrical specifications for details). LDO3 can work with supply from 3.0V up to 5.5V and needs at least 300mV of minimum drop-out. This LDO is designed to supply RF section of wireless devices, showing high PSRR up to 100 kHz, low noise on wide frequency bandwidth. LDO3 requires a 2.2 µF output capacitor.

- Additionally, 1.50V or 1.20V output voltages programming is possible via the TWI serial interface on AT73C237.

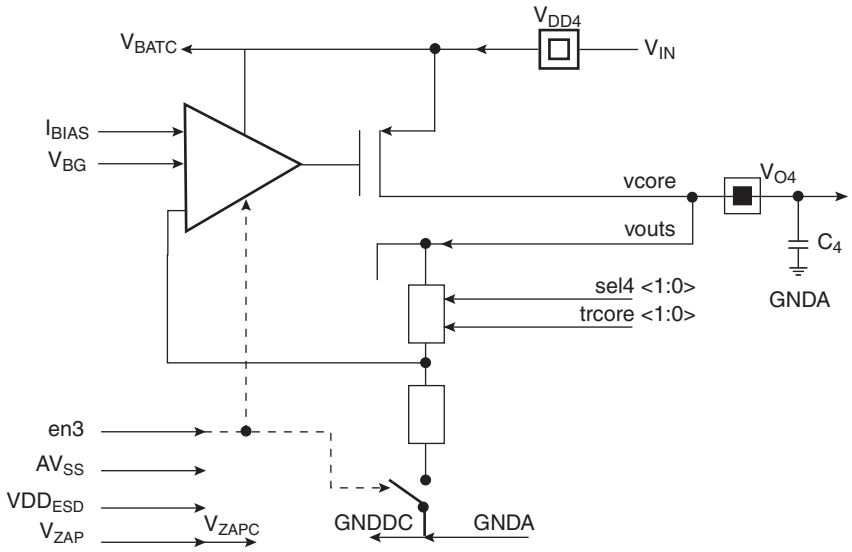
Figure 9-3. LDO3 Functional Diagram



9.4 LDO4

LDO4 is a 1.80V/2mA LDO with very low quiescent current. LDO4 can work with supply from 2.8V up to 5.5V. LDO4 requires a 1 µF output capacitor. It needs at least 300 mV of minimum drop-out. LDO4 is always active once the pin VDD4 is supplied since it is used as internal reference supply. The VDD4 rail is independent from the other input rails (VDD1, 2, 3), allowing LDO4 to be used to supply a Real Time Clock from a separate backup battery, for example.

Figure 9-4. LDO4 Functional Diagram



9.5 High Performance Bandgap (HPBG)

HPBG is a low power, low noise Band Gap circuit providing very accurate voltage reference to LDOs that then can supply RF sections. HPBG operates in switching mode decreasing its current consumption. Economic high performance Bandgap is particularly interesting when RF LDOs are in idle mode (output voltage provided with very low output current e.g. <1mA). HPBG is biased from an internal regulator supplied by VDD4, thus it is not active when only VDD3 is present. HPBG requires at least external 100nF capacitor to achieve very low noise/high accuracy voltage reference.
HPBG is trimmed to 1.231V during product test.

9.6 Low Power Bandgap (LPBG)

LPBG is a low power Bandgap circuit used as reference voltage for LDO4. LPBG starts up as soon as VDD4 is present and doesn't require any external capacitor for decoupling.

9.7 Reset Generator

A Reset Generator produces an output reset (rising from “0” to “1”), called XRESO, at least 100 ms after the input reset state is activated. The input reset state can be produced by:

- VDD3 rising up, XRESIN not used or at “1”.
- External signal rising up on XRESIN and VDD3 present.

9.8 State Machine

An Internal State Machine supervises the start up of the regulators connected to VDD1, VDD2 and VDD3. The startup configuration is in the following order LDO3 then LDO1 then LDO2.
A voltage must be present on VDD4 to supply LDO4.

9.9 Oscillator

An Internal Oscillator (RCOSC) is used to generate the internal master clock which synchronizes the state machine controlling the start up of the LDOs and HPBG.

9.10 Power-On-Reset

A Power-On-Reset (POR) monitors the output of LDO4 (VO4) and generates an internal signal to enable the trimming registers to be loaded for LDO1, LDO2, LDO3 output voltage programming, as well as for the reference voltages and internal oscillator trimming. This internal signal is released when VO4 is higher then 1.5V ± 300 mV.

9.11 Supply Monitor

A Supply Monitor is set on VDD3 and generates an internal signal to enable state machine to startup the LDOs and to generate the XRESO signal. The threshold has been set to 2.7V when rising up and 2.6V when falling down.

9.12 Digital Control

On AT73C237, the pins TWCK, TWD are respectively the clock and data lines of a true two-wire interface, allowing to activate and disable the output voltage delivered by the regulators LDO1, LDO2, LDO3 and also to change their output voltage value.

9.13 Two-wire Interface (TWI) Protocol

The two-wire interface interconnects components on a unique two-wire bus, made up of one clock line and one data line with speeds up to 400 Kbits per second, based one a byte oriented transfer format. The TWI is slave only and single byte access.

The interface adds flexibility to the power supply solution, enabling LDO regulators to be controlled depending on the instantaneous application requirements.

The AT73C237 has the following 7-bit address:1001000.

Attempting to read data from register addresses not listed in this section results in 0xFF being read out.

- TWCK is an input pin for the clock
- TWD is an open-drain pin that drives or receives the serial data

The data put on the TWD line must be 8 bits long. Data is transferred MSB first. Each byte must be followed by an acknowledgement.

Each transfer begins with a START condition and terminates with a STOP condition.

- A high-to-low transition on TWD while TWCK is high defines a START condition.
- A low-to-high transition on TWD while TWCK is high defines a STOP condition.

Figure 9-5. TWI Start/Stop Cycle

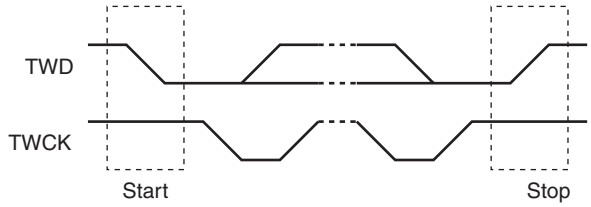
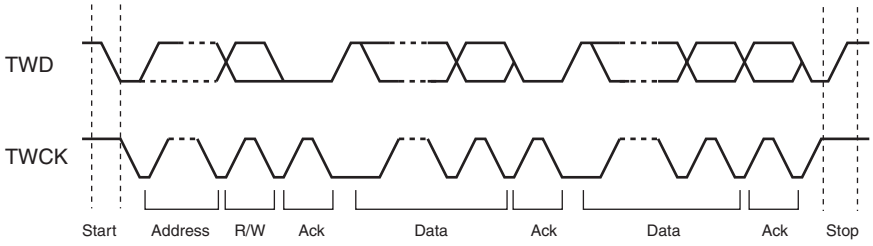


Figure 9-6. TWI Data Cycle



After the host initiates a Start condition, it sends the 7-bit slave address defined above to notify the slave device. A Read/Write bit follows (Read = 1, Write = 0).

The device acknowledges each received byte.

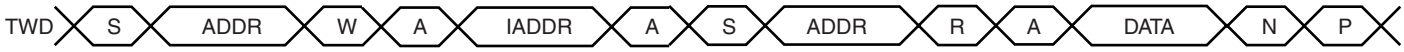
The first byte sent after device address and R/W bit is the address of the device register the host wants to read or write.

For a write operation the data follows the internal address

For a read operation a repeated Start condition needs to be generated followed by a read on the device.

Figure 9-7. TWD Write Operation

Figure 9-8. TWD Read Operation



- S = Start
- P = Stop
- W = Write
- R = Read
- A = Acknowledge
- N = Not Acknowledge
- ADDR = Device address
- IADDR = Internal address

10. Registers

Table 10-1. Registers

Address	Register	Description	Access	Reset value
0x00	LDO_CTRL	LDO control	Read / Write	0x0F
0x08	LDO_TRIM1	LDO 1,2,3 trim	Read / Write	0x00
0x0A	LDO_TRIM4	LDO4 trim	Read / Write	0x00

10.1 LDO Control: LDO_CTRL (0x00)

7	6	5	4	3	2	1	0
-	-	-	-	Onldo4	Onldo3	Onldo2	Onldo1

Table 10-2. LDO_CTRL (0x00) Structure

Bit	Name	Description	Reset value
7:4	-	Not used	-
3	Onldo4	LDO4 enable (active high, HiZ when off)	1
2	Onldo3	LDO3 enable (active high, HiZ when off)	1
1	Onldo2	LDO2 enable (active high, HiZ when off)	1
0	Onldo1	LDO1 enable (active high, HiZ when off)	1

10.2 LDO 1,2,3 trim: LDO_TRIM1 (0x08)

7	6	5	4	3	2	1	0
-	-	-	Sel1	Sel2	Sel3		-

Table 10-3. LDO_TRIM1 (0x08) Structure

Bit	Name	Description	Reset value
7:5	-	Not used	-
4	Sel1	LDO1 output voltage select	0
3	Sel2	LDO2 output voltage select	0
2:1	Sel3	LDO3 output voltage select	00
0	-	Not used	-

Table 10-4. LDO_TRIM1 (0x08) - Output Voltages Selection

Sel1	VO1	Sel2	VO2	Sel3	VO3
0	2.75V	0	1.8V	00	1.8V
1	1.8V	1	1.5V	01	1.5V
-	-	-	-	10	1.23V
-	-	-	-	11	1.8

10.3 LDO 4 trim: LDO_TRIM4 (0x0A)

7	6	5	4	3	2	1	0
-	-	-	-	Sel4		trcore1	trcore0

Table 10-5. LDO_TRIM1 (0x08) Structure

Bit	Name	Description	Reset value
7:4	-	Not used	-
3:2	Sel4	LDO4 output voltage select	00
1:0	trcore	LDO4 output voltage trimming	00

Table 10-6. LDO_TRIM1 (0x08) - Sel4

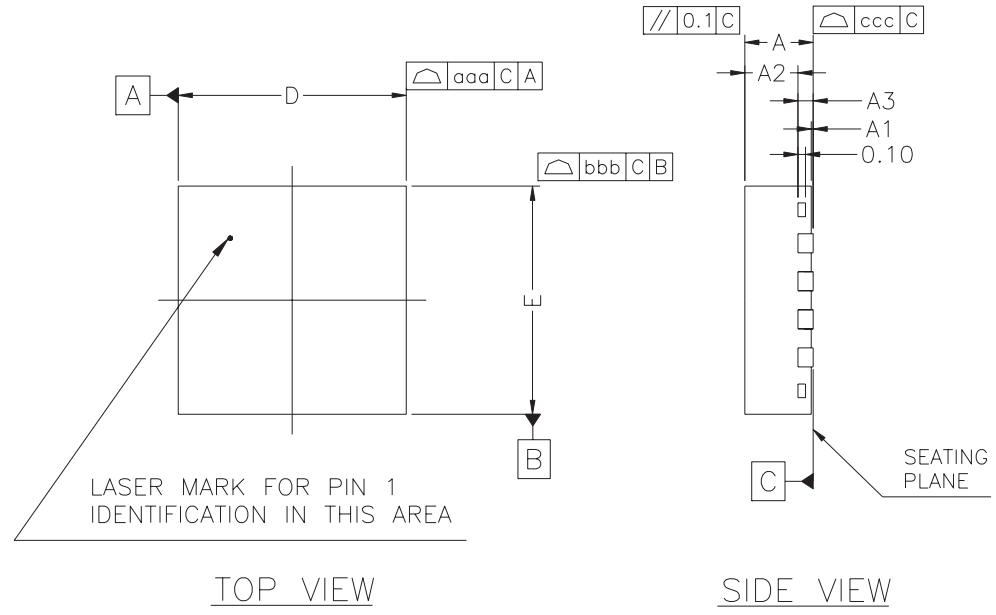
Sel4	VO4
00	1.8V
01	-
10	-
11	-

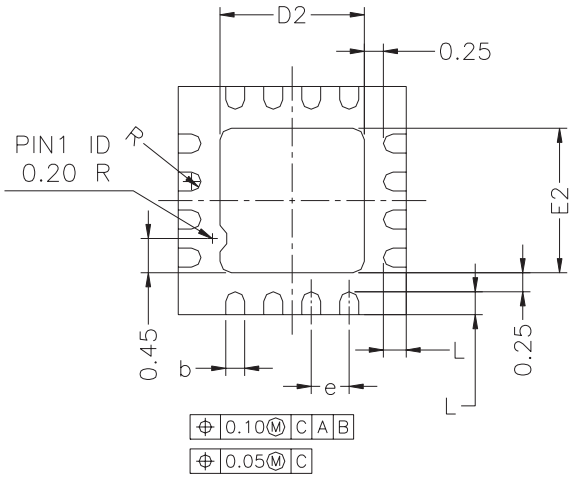
Table 10-7. LDO_TRIM1 (0x08) - trcore

trcore	VO4
00	Typ value (1.8V)
01	+80mV
10	-80mV
11	Typ value (1.8V)

11. Package Information

Figure 11-1. Mechanical Package Drawing for 16-lead Quad Flat No Lead Package





NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.PACKAGE WARPAGE MAX 0.08 mm.

* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	---	---	0.05	---	---	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	1.80	1.90	2.00	0.071	0.075	0.079
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.80	1.90	2.00	0.071	0.075	0.079
L	0.25	0.30	0.35	0.010	0.012	0.014
e	0.50 bsc			0.020 bsc		
R	0.09	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

12. Ordering Information

Table 12-1. Ordering Information

Ordering Code	Package	Package Type	Temperature Operating Range
AT73C237	QFN 3x3 mm	Green	0°C to +70°C

13. Revision History

Doc. Rev	Comments	Change Request Ref.
6362A	First issue	

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