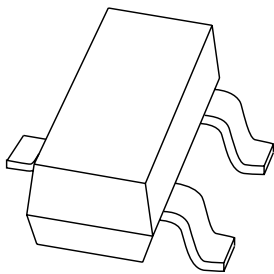


# DATA SHEET



## **PBSS4350T**

50 V; 3 A NPN low  $V_{CEsat}$   
(BISS) transistor

Product data sheet  
Supersedes data of 2002 Aug 08

2004 Jan 09

# 50 V; 3 A NPN low $V_{CEsat}$ (BISS) transistor

**PBSS4350T**

**FEATURES**

- Low collector-emitter saturation voltage  $V_{CEsat}$  and corresponding low  $R_{CEsat}$
- High collector current capability
- High collector current gain
- Improved efficiency due to reduced heat generation.

**APPLICATIONS**

- Power management applications
- Low and medium power DC/DC convertors
- Supply line switching
- Battery chargers
- Linear voltage regulation with low voltage drop-out (LDO).

**DESCRIPTION**

NPN low  $V_{CEsat}$  transistor in a SOT23 plastic package. PNP complement: PBSS5350T.

**MARKING**

| TYPE NUMBER | MARKING CODE <sup>(1)</sup> |
|-------------|-----------------------------|
| PBSS4350T   | ZC*                         |

**Note**

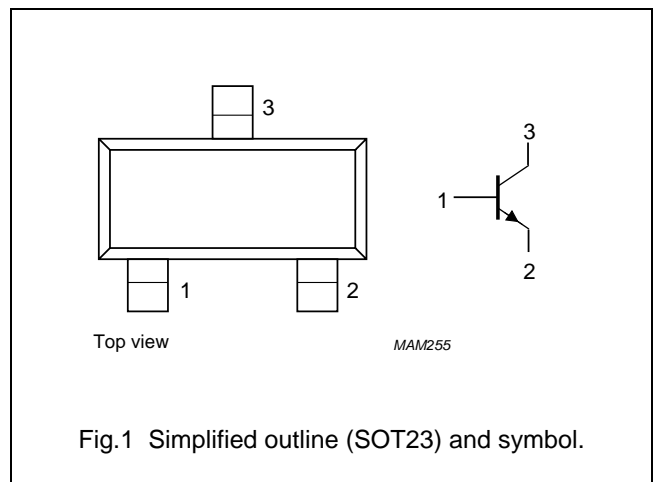
1. \* = p: Made in Hong Kong.  
 \* = t: Made in Malaysia.  
 \* = W: Made in China.

**QUICK REFERENCE DATA**

| SYMBOL      | PARAMETER                         | MAX. | UNIT |
|-------------|-----------------------------------|------|------|
| $V_{CEO}$   | collector-emitter voltage         | 50   | V    |
| $I_C$       | collector current (DC)            | 2    | A    |
| $I_{CRP}$   | repetitive peak collector current | 3    | A    |
| $R_{CEsat}$ | equivalent on-resistance          | 130  | mΩ   |

**PINNING**

| PIN | DESCRIPTION |
|-----|-------------|
| 1   | base        |
| 2   | emitter     |
| 3   | collector   |



**ORDERING INFORMATION**

| TYPE NUMBER | PACKAGE |  |         |
|-------------|---------|--|---------|
|             | NAME    | DESCRIPTION                              | VERSION |
| PBSS4350T   | –       | plastic surface mounted package; 3 leads | SOT23   |

50 V; 3 A NPN low  $V_{CEsat}$  (BISS) transistor

## PBSS4350T

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL    | PARAMETER                         | CONDITIONS                                  | MIN. | MAX. | UNIT |
|-----------|-----------------------------------|---|------|------|------|
| $V_{CBO}$ | collector-base voltage            | open emitter                                | –    | 50   | V    |
| $V_{CEO}$ | collector-emitter voltage         | open base                                   | –    | 50   | V    |
| $V_{EBO}$ | emitter-base voltage              | open collector                              | –    | 5    | V    |
| $I_C$     | collector current (DC)            |   | –    | 2    | A    |
| $I_{CRP}$ | repetitive peak collector current | note 1                                      | –    | 3    | A    |
| $I_{CM}$  | peak collector current            | single peak                                 | –    | 5    | A    |
| $I_B$     | base current (DC)                 |   | –    | 0.5  | A    |
| $P_{tot}$ | total power dissipation           | $T_{amb} \leq 25\text{ °C}$ ; note 2        | –    | 300  | mW   |
|           |                                   | $T_{amb} \leq 25\text{ °C}$ ; note 3        | –    | 480  | mW   |
|           |                                   | $T_{amb} \leq 25\text{ °C}$ ; note 4        | –    | 540  | mW   |
|           |                                   | $T_{amb} \leq 25\text{ °C}$ ; notes 1 and 2 | –    | 1.2  | W    |
| $T_{stg}$ | storage temperature               |   | –65  | +150 | °C   |
| $T_j$     | junction temperature              |   | –    | 150  | °C   |
| $T_{amb}$ | operating ambient temperature     |   | –65  | +150 | °C   |

**Notes**

- Operated under pulsed conditions: pulse width  $t_p \leq 100\text{ ms}$ ; duty cycle  $\delta \leq 0.25$ .
- Device mounted on a printed-circuit board; single sided copper; tinplated; standard footprint.
- Device mounted on a printed-circuit board; single sided copper; tinplated; mounting pad for collector  $1\text{ cm}^2$ .
- Device mounted on a printed-circuit board; single sided copper; tinplated; mounting pad for collector  $6\text{ cm}^2$ .

**THERMAL CHARACTERISTICS**

| SYMBOL        | PARAMETER                                   | CONDITIONS                 | VALUE | UNIT |
|---------------|---|----------------------------|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air; note 1        | 417   | K/W  |
|               |   | in free air; note 2        | 260   | K/W  |
|               |   | in free air; note 3        | 230   | K/W  |
|               |   | in free air; notes 1 and 4 | 104   | K/W  |

**Notes**

- Device mounted on a printed-circuit board; single sided copper; tinplated; standard footprint.
- Device mounted on a printed-circuit board; single sided copper; tinplated; mounting pad for collector  $1\text{ cm}^2$ .
- Device mounted on a printed-circuit board; single sided copper; tinplated; mounting pad for collector  $6\text{ cm}^2$ .
- Operated under pulsed conditions: pulse width  $t_p \leq 100\text{ ms}$ ; duty cycle  $\delta \leq 0.25$ .

50 V; 3 A NPN low  $V_{CEsat}$  (BISS) transistor

## PBSS4350T

**CHARACTERISTICS**

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

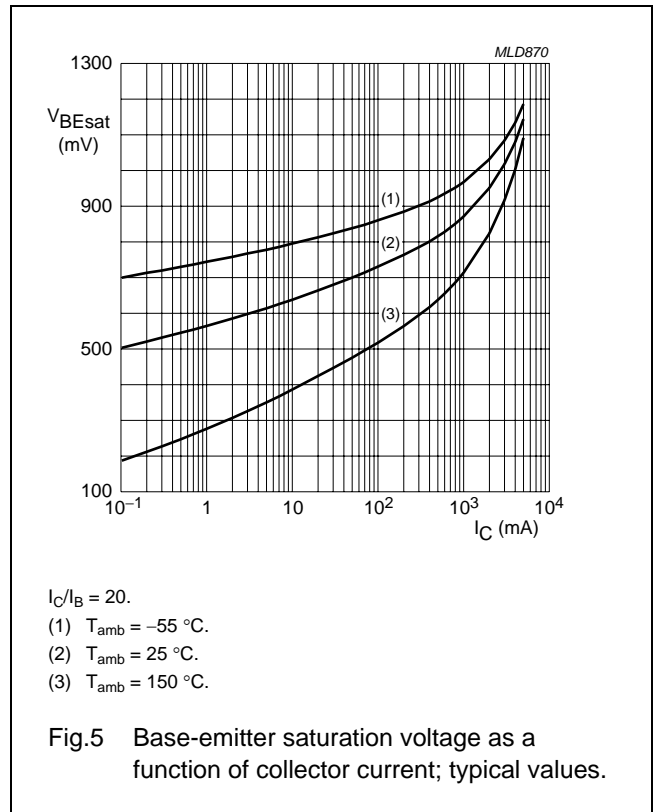
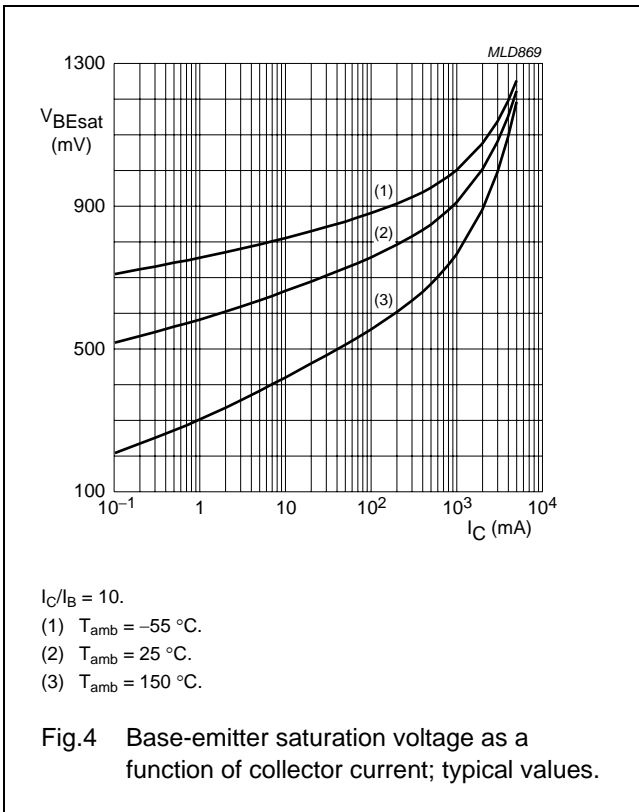
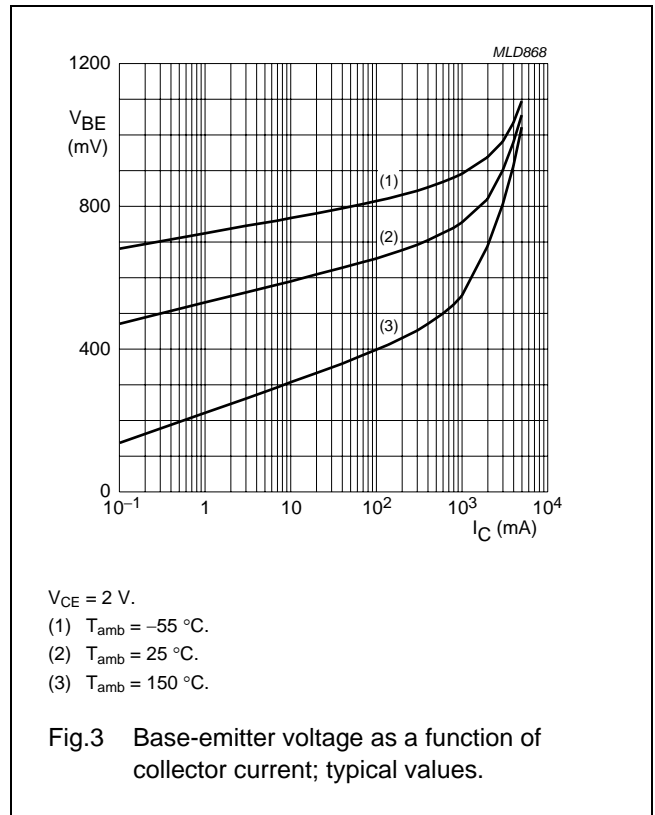
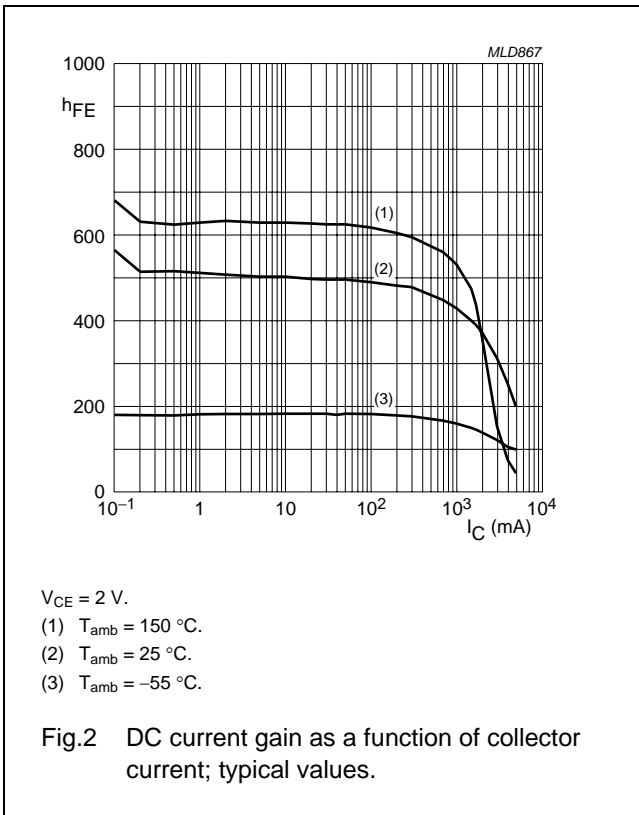
| SYMBOL      | PARAMETER                            | CONDITIONS  | MIN. | TYP. | MAX. | UNIT             |
|-------------|--------------------------------------|---|------|------|------|------------------|
| $I_{CBO}$   | collector-base cut-off current       | $I_E = 0; V_{CB} = 50\text{ V}$                                     | –    | –    | 100  | nA               |
|             |                                      | $I_E = 0; V_{CB} = 50\text{ V}; T_j = 150\text{ °C}$                | –    | –    | 50   | $\mu\text{A}$    |
| $I_{EBO}$   | emitter-base cut-off current         | $I_C = 0; V_{EB} = 5\text{ V}$                                      | –    | –    | 100  | nA               |
| $h_{FE}$    | DC current gain                      | $I_C = 100\text{ mA}; V_{CE} = 2\text{ V}$                          | 300  | –    | –    |                  |
|             |                                      | $I_C = 500\text{ mA}; V_{CE} = 2\text{ V}$                          | 300  | –    | –    |                  |
|             |                                      | $I_C = 1\text{ A}; V_{CE} = 2\text{ V}; \text{note 1}$              | 300  | –    | –    |                  |
|             |                                      | $I_C = 2\text{ A}; V_{CE} = 2\text{ V}; \text{note 1}$              | 200  | –    | –    |                  |
|             |                                      | $I_C = 3\text{ A}; V_{CE} = 2\text{ V}; \text{note 1}$              | 100  | –    | –    |                  |
| $V_{CEsat}$ | collector-emitter saturation voltage | $I_C = 500\text{ mA}; I_B = 50\text{ mA}$                           | –    | –    | 80   | mV               |
|             |                                      | $I_C = 1\text{ A}; I_B = 50\text{ mA}$                              | –    | –    | 160  | mV               |
|             |                                      | $I_C = 2\text{ A}; I_B = 100\text{ mA}; \text{note 1}$              | –    | –    | 280  | mV               |
|             |                                      | $I_C = 2\text{ A}; I_B = 200\text{ mA}; \text{note 1}$              | –    | –    | 260  | mV               |
|             |                                      | $I_C = 3\text{ A}; I_B = 300\text{ mA}; \text{note 1}$              | –    | –    | 370  | mV               |
| $R_{CEsat}$ | equivalent on-resistance             | $I_C = 2\text{ A}; I_B = 200\text{ mA}; \text{note 1}$              | –    | 100  | 130  | $\text{m}\Omega$ |
| $V_{BEsat}$ | base-emitter saturation voltage      | $I_C = 2\text{ A}; I_B = 100\text{ mA}; \text{note 1}$              | –    | –    | 1.1  | V                |
|             |                                      | $I_C = 3\text{ A}; I_B = 300\text{ mA}; \text{note 1}$              | –    | –    | 1.2  | V                |
| $V_{BEon}$  | base-emitter turn-on voltage         | $I_C = 1\text{ A}; V_{CE} = 2\text{ V}; \text{note 1}$              | 1.2  | –    | –    | V                |
| $f_T$       | transition frequency                 | $I_C = 100\text{ mA}; V_{CE} = 5\text{ V};$<br>$f = 100\text{ MHz}$ | 100  | –    | –    | MHz              |
| $C_c$       | collector capacitance                | $I_E = I_e = 0; V_{CB} = 10\text{ V}; f = 1\text{ MHz}$             | –    | –    | 25   | pF               |

**Note**

1. Pulse test:  $t_p \leq 300\text{ }\mu\text{s}$ ;  $\delta \leq 0.02$ .

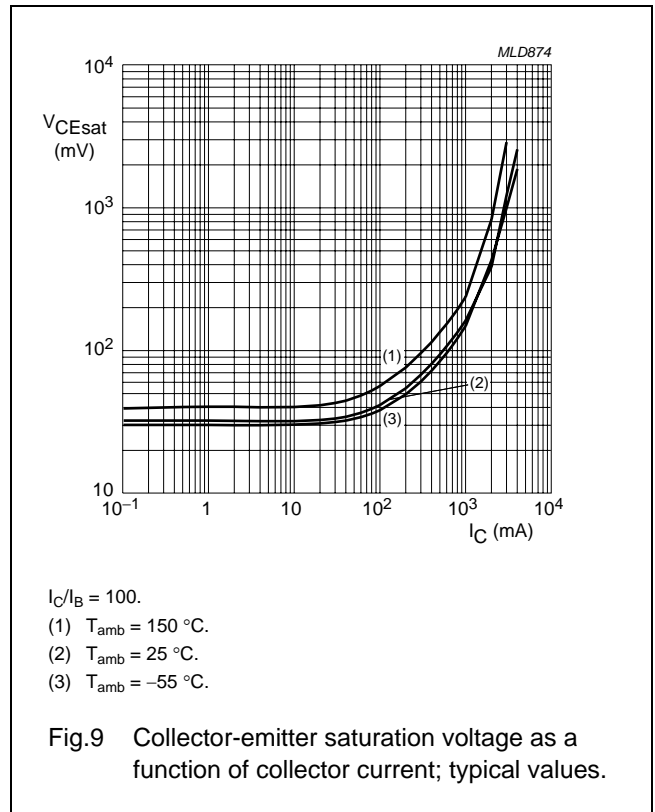
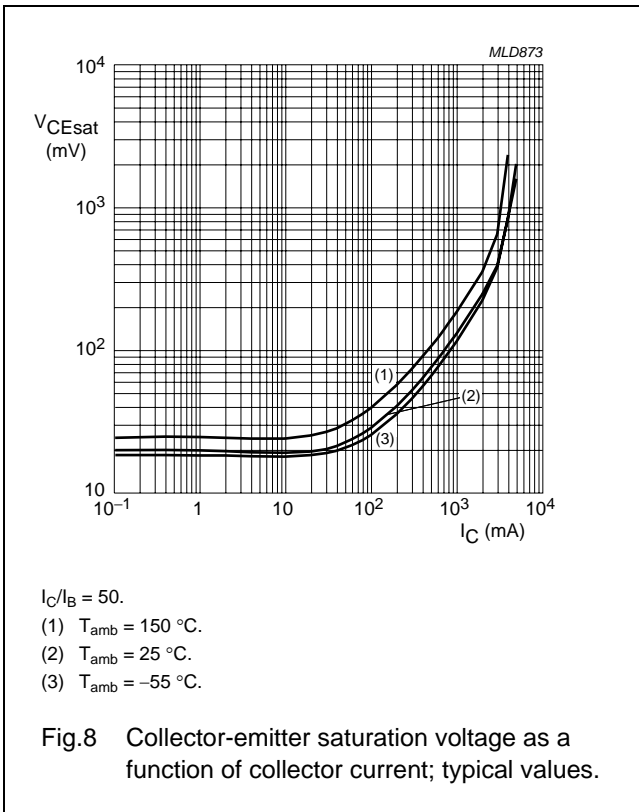
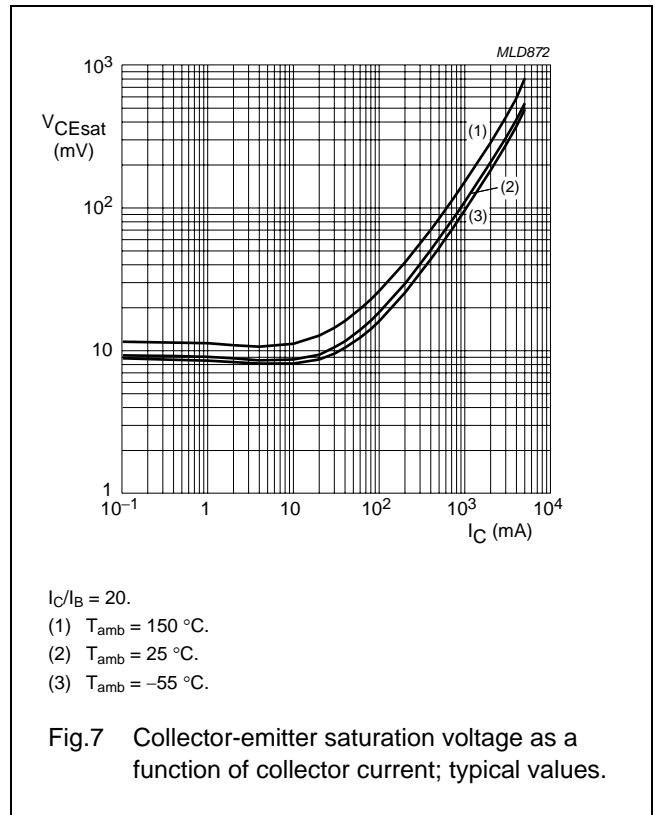
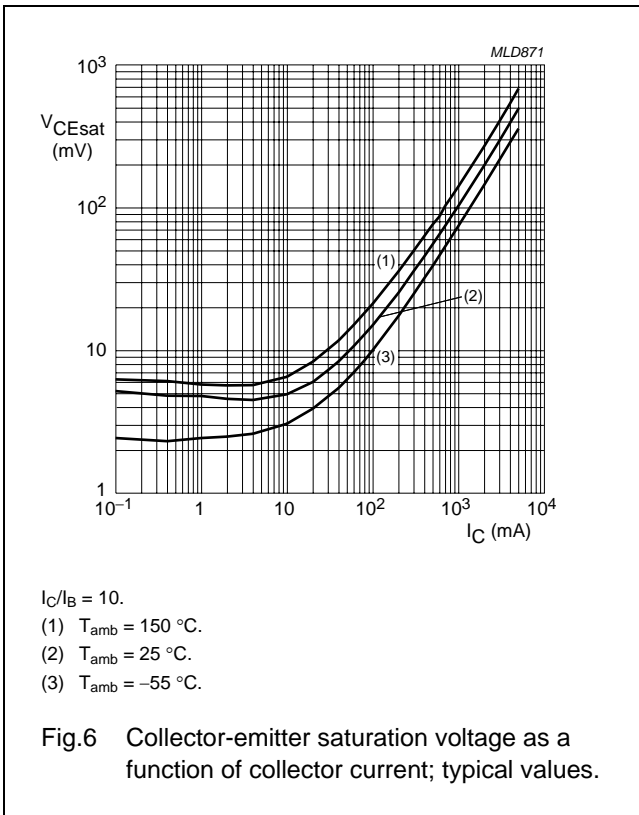
50 V; 3 A NPN low  $V_{CEsat}$  (BISS) transistor

PBSS4350T



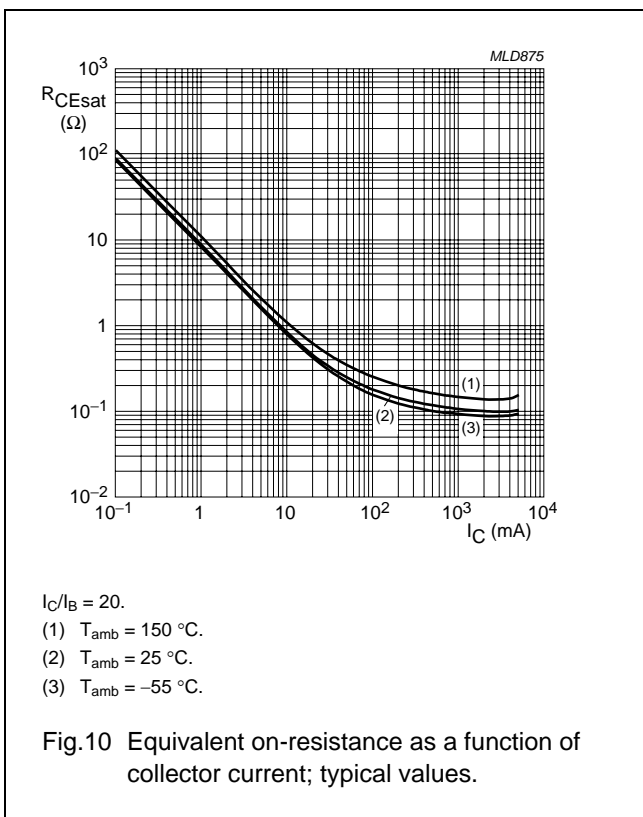
50 V; 3 A NPN low  $V_{CEsat}$  (BISS) transistor

PBSS4350T



50 V; 3 A NPN low  $V_{CEsat}$  (BISS) transistor

PBSS4350T



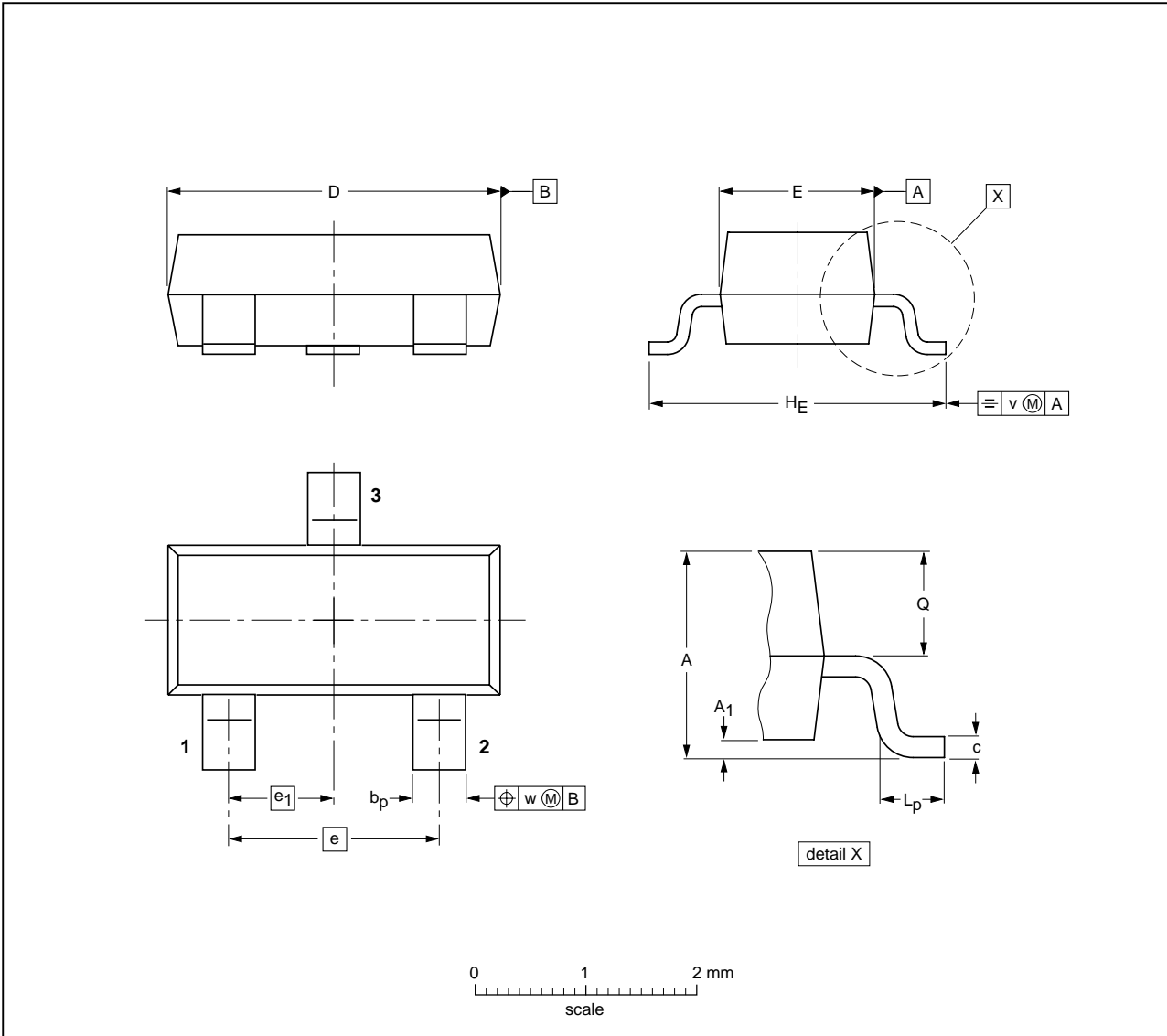
50 V; 3 A NPN low  $V_{CEsat}$  (BISS) transistor

PBSS4350T

PACKAGE OUTLINE

Plastic surface-mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

| UNIT | A          | A <sub>1</sub><br>max. | b <sub>p</sub> | c            | D          | E          | e   | e <sub>1</sub> | H <sub>E</sub> | L <sub>p</sub> | Q            | v   | w   |
|------|------------|------------------------|----------------|--------------|------------|------------|-----|----------------|----------------|----------------|--------------|-----|-----|
| mm   | 1.1<br>0.9 | 0.1                    | 0.48<br>0.38   | 0.15<br>0.09 | 3.0<br>2.8 | 1.4<br>1.2 | 1.9 | 0.95           | 2.5<br>2.1     | 0.45<br>0.15   | 0.55<br>0.45 | 0.2 | 0.1 |

| OUTLINE<br>VERSION | REFERENCES |          |       |  | EUROPEAN<br>PROJECTION | ISSUE DATE           |
|--------------------|------------|----------|-------|--|------------------------|----------------------|
|                    | IEC        | JEDEC    | JEITA |  |                        |                      |
| SOT23              |            | TO-236AB |       |  |                        | 04-11-04<br>06-03-16 |



50 V; 3 A NPN low  $V_{CEsat}$  (BISS) transistor

PBSS4350T

**DATA SHEET STATUS**

| DOCUMENT STATUS <sup>(1)</sup> | PRODUCT STATUS <sup>(2)</sup> | DEFINITION  |
|--------------------------------|-------------------------------|---|
| Objective data sheet           | Development                   | This document contains data from the objective specification for product development. |
| Preliminary data sheet         | Qualification                 | This document contains data from the preliminary specification.                       |
| Product data sheet             | Production                    | This document contains the product specification.                                     |

**Notes**

1. Please consult the most recently issued document before initiating or completing a design.
2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

**DISCLAIMERS**

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions

above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

# ***NXP Semiconductors***

## **Customer notification**

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

## **Contact information**

For additional information please visit: <http://www.nxp.com>

For sales offices addresses send e-mail to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

© NXP B.V. 2009

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

R75/02/pp10

Date of release: 2004 Jan 09

Document order number: 9397 750 12437

founded by

**PHILIPS**