High Speed, High Gain Bipolar NPN Power Transistor

with Integrated Collector–Emitter Diode and Built–in Efficient Antisaturation Network

The BUL45D2G is state–of–art High Speed High gain BiPolar transistor (H2BIP). High dynamic characteristics and lot–to–lot minimum spread (± 150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an h_{FE} window. It's characteristics make it also suitable for PFC application.

Features

- Low Base Drive Requirement
- High Peak DC Current Gain
- Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread
- Integrated Collector-Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic V_{CE(sat)}
- "6 Sigma" Process Providing Tight and Reproductible Parameter Spreads
- These Devices are Pb-Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	V _{CEO}	400	Vdc
Collector-Base Breakdown Voltage	V _{CBO}	700	Vdc
Collector-Emitter Breakdown Voltage	V _{CES}	700	Vdc
Emitter-Base Voltage	V _{EBO}	12	Vdc
Collector Current – Continuous	I _C	5	Adc
Collector Current – Peak (Note 1)	I _{CM}	10	Adc
Base Current - Continuous	I _B	2	Adc
Base Current – Peak (Note 1)	I _{BM}	4	Adc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	75 0.6	W W/°C
Operating and Storage Temperature	T _J , T _{stg}	-65 to +150	°C

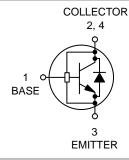
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

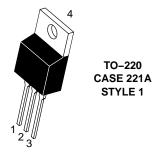


ON Semiconductor®

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POWER TRANSISTOR 5.0 AMPERES, 700 VOLTS, 75 WATTS





MARKING DIAGRAM



A = Assembly Location

Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
BUL45D2G	TO-220 (Pb-Free)	50 Units / Rail

^{1.} Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

^{*}For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.65	°C/W
Thermal Resistance, Junction-to-Ambient		62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds		260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I _C = 100 mA, L = 25 mH)	V _{CEO(sus)}	400	450	-	Vdc
Collector–Base Breakdown Voltage (I _{CBO} = 1 mA)	V _{CBO}	700	910	-	Vdc
Emitter-Base Breakdown Voltage (I _{EBO} = 1 mA)	V _{EBO}	12	14.1	_	Vdc
Collector Cutoff Current $(V_{CE} = Rated V_{CEO}, I_B = 0)$	I _{CEO}	-	_	100	μAdc
Collector Cutoff Current $(V_{CE} = Rated \ V_{CES}, \ V_{EB} = 0)$ $@\ T_C = 25^{\circ}C$ $@\ T_C = 125^{\circ}C$ $(V_{CE} = 500 \ V, \ V_{EB} = 0)$	ICES	- -	- -	100 500	μAdc
@ T _C = 125°C Emitter-Cutoff Current (V _{FB} = 10 Vdc, I _C = 0)	I _{EBO}		_	100	μAdc
ON CHARACTERISTICS					
Base–Emitter Saturation Voltage ($I_C = 0.8$ Adc, $I_B = 80$ mAdc) @ $T_C = 25^{\circ}C$ @ $T_C = 125^{\circ}C$	V _{BE(sat)}		0.8 0.7	1 0.9	Vdc
(I _C = 2 Adc, I _B = 0.4 Adc) @ T _C = 25°C @ T _C = 125°C		<u>-</u>	0.89 0.79	1 0.9	
Collector–Emitter Saturation Voltage $ \begin{aligned} &(I_C = 0.8 \text{ Adc, } I_B = 80 \text{ mAdc}) \\ & @ T_C = 25^{\circ}\text{C} \\ & @ T_C = 125^{\circ}\text{C} \end{aligned} $ $ & @ T_C = 25^{\circ}\text{C} $ $ & @ T_C = 125^{\circ}\text{C} $ $ & (I_C = 0.8 \text{ Adc, } I_B = 40 \text{ mAdc}) $ $ & @ T_C = 25^{\circ}\text{C} $	V _{CE(sat)}	- - - -	0.28 0.32 0.32 0.38 0.46	0.4 0.5 0.5 0.6 0.75	Vdc
@ $T_C = 125^{\circ}C$ DC Current Gain ($I_C = 0.8 \text{ Adc}, V_{CE} = 1 \text{ Vdc}$) @ $T_C = 25^{\circ}C$ @ $T_C = 125^{\circ}C$ ($I_C = 2 \text{ Adc}, V_{CE} = 1 \text{ Vdc}$) @ $T_C = 25^{\circ}C$ @ $T_C = 25^{\circ}C$ @ $T_C = 125^{\circ}C$	h _{FE}	22 20 10 7	0.62 34 29 14 9.5	- - -	-
DIODE CHARACTERISTICS	ļļ		Į.		
Forward Diode Voltage (I _{EC} = 1 Adc) @ T _C = 25°C @ T _C = 125°C (I _{EC} = 2 Adc)	VEC	- -	1.04 0.7	1.5 -	V
(IEC = 2 Add) @ T _C = 25°C @ T _C = 125°C (I _{EC} = 0.4 Adc) @ T _C = 25°C @ T _C = 125°C		- - -	1.2 - 0.85 0.62	1.6 - 1.2	

ELECTRICAL CHARACTERISTICS (continued) ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic				Symbol	Min	Тур	Max	Unit
DIODE CHARACTERISTIC	cs							
Forward Recovery Time (see Figure 27)				T _{fr}	-	330	-	ns
@ $T_C = 25^{\circ}C$ ($I_F = 0.4 \text{ Adc, di/dt} = 10$ @ $T_C = 25^{\circ}C$	A/μs)				-	360 320	_	
DYNAMIC CHARACTERIS	STICS							<u> </u>
Current Gain Bandwidth (I _C = 0.5 Adc, V _{CE} = 10				f _T	-	13	_	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0,	f = 1 MHz)			C _{ob}	-	50	75	pF
Input Capacitance (V _{EB} = 8 Vdc)				C _{ib}	-	340	500	pF
DYNAMIC SATURATION	VOLTAGE							
Dynamic Saturation Voltage: Determined 1 μs and	$I_C = 1 \text{ A}$ $I_{B1} = 100 \text{ mA}$	@ 1 μs	@ T _C = 25°C @ T _C = 125°C	V _{CE(dsat)}	- -	3.7 9.4	- -	V
3 μs respectively after rising I _{B1} reaches	V _{CC} = 300 V	@ 3 μs	@ T _C = 25°C @ T _C = 125°C		-	0.35 2.7	- -	V
90% of final I _{B1}	$I_C = 2 A$ $I_{B1} = 0.8 A$ $V_{CC} = 300 V$	@ 1 μs	@ T _C = 25°C @ T _C = 125°C		-	3.9 12	- -	V
		@ 3 μs	@ T _C = 25°C @ T _C = 125°C		-	0.4 1.5	- -	V
SWITCHING CHARACTE	RISTICS: Resistive	Load (D.0	C. ≤ 10%, Pulse W	idth = 20 μs)		1	I	L
Turn-on Time	$I_C = 2 \text{ Adc}, I_{B1} = 0$ $I_{B2} = 1 \text{ Add}$	0.4 Adc	@ T _C = 25°C @ T _C = 125°C	t _{on}	- -	90 105	150 –	ns
Turn-off Time	V _{CC} = 300 V	dc	@ T _C = 25°C @ T _C = 125°C	t _{off}	- -	1.15 1.5	1.3	μs
Turn-on Time	$I_C = 2 \text{ Adc}, I_{B1} = 0$ $I_{B2} = 0.4 \text{ Add}$	lc	@ T _C = 25°C @ T _C = 125°C	t _{on}	- -	90 110	150 –	ns
Turn-off Time	V _{CC} = 300 Vdc		@ T _C = 25°C @ T _C = 125°C	t _{off}	2.1	- 3.1	2.4 -	μs
SWITCHING CHARACTE	RISTICS: Inductive	Load (V _{cl}	_{amp} = 300 V, V _{CC} =	= 15 V, L = 20)0 μH)	•	•	
Fall Time	$I_C = 1 \text{ Adc}$ $I_{B1} = 100 \text{ mAdc}$ $I_{B2} = 500 \text{ mAdc}$		@ T _C = 25°C @ T _C = 125°C	t _f	-	90 93	150 -	ns
Storage Time			@ T _C = 25°C @ T _C = 125°C	t _s	-	0.72 1.05	0.9 -	μs
Crossover Time			@ T _C = 25°C @ T _C = 125°C	t _c	- -	95 95	150 –	ns
Fall Time	I _C = 2 Adc I _{B1} = 0.4 Adc - I _{B2} = 0.4 Adc		@ T _C = 25°C @ T _C = 125°C	t _f	-	80 105	150 –	ns
Storage Time			@ T _C = 25°C @ T _C = 125°C	t _s	1.95 –	- 2.9	2.25	μs
Crossover Time			@ T _C = 25°C @ T _C = 125°C	t _c		225 450	300	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL STATIC CHARACTERISTICS

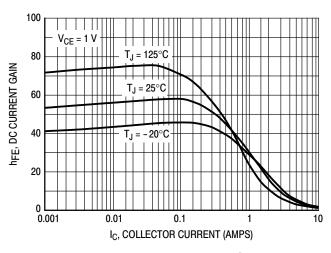


Figure 1. DC Current Gain @ 1 Volt

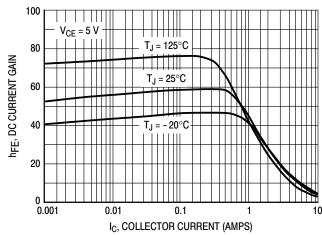


Figure 2. DC Current Gain @ 5 Volt

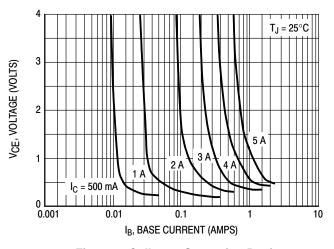


Figure 3. Collector Saturation Region

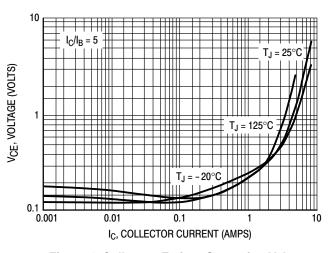


Figure 4. Collector–Emitter Saturation Voltage

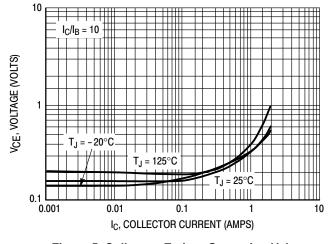


Figure 5. Collector-Emitter Saturation Voltage

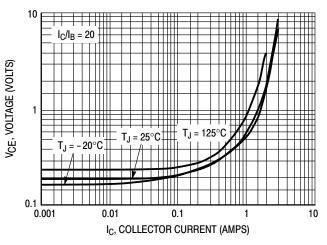


Figure 6. Collector-Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

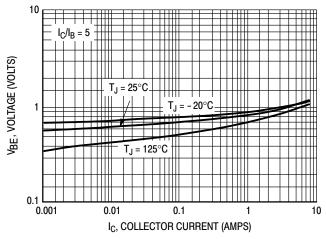


Figure 7. Base-Emitter Saturation Region

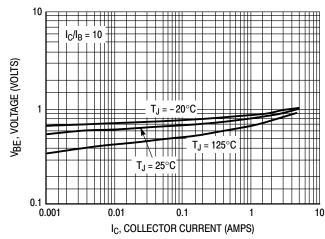


Figure 8. Base-Emitter Saturation Region

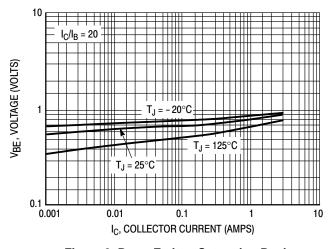


Figure 9. Base-Emitter Saturation Region

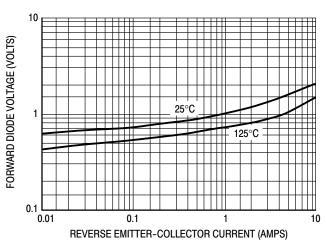


Figure 10. Forward Diode Voltage

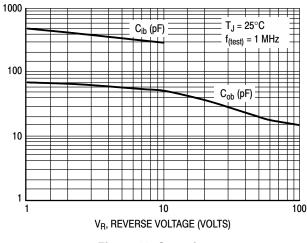


Figure 11. Capacitance

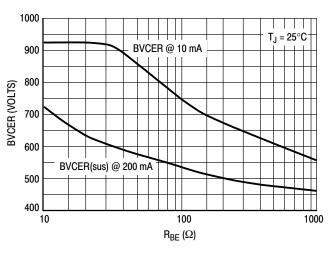


Figure 12. BVCER = f(ICER)

TYPICAL SWITCHING CHARACTERISTICS

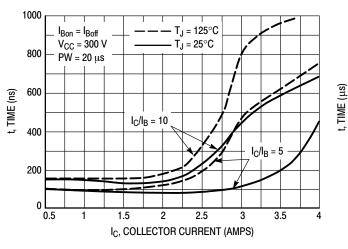


Figure 13. Resistive Switch Time, ton

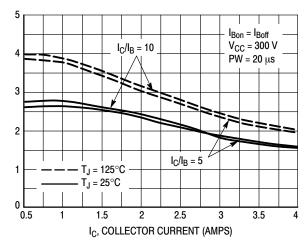


Figure 14. Resistive Switch Time, toff

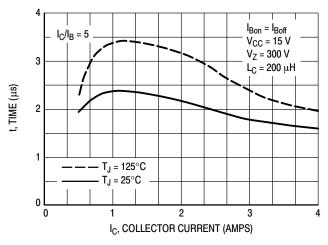


Figure 15. Inductive Storage Time, $t_{si} @ I_C/I_B = 5$

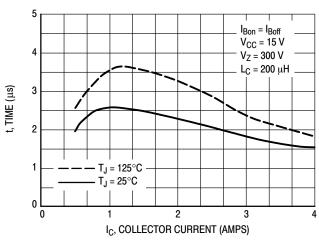


Figure 16. Inductive Storage Time, $t_{si} @ I_C/I_B = 10$

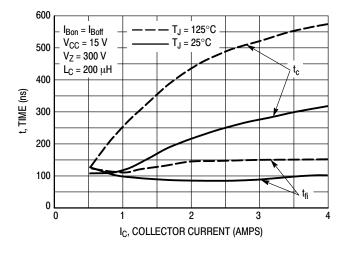


Figure 17. Inductive Switching, $t_c \& t_{fi} @ I_c/I_B = 5$

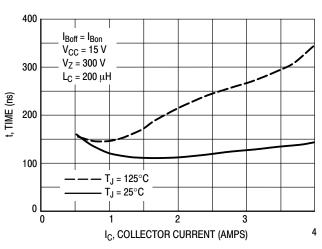


Figure 18. Inductive Switching, $t_{fi} @ l_C/l_B = 10$

TYPICAL SWITCHING CHARACTERISTICS

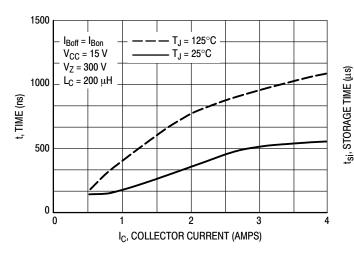
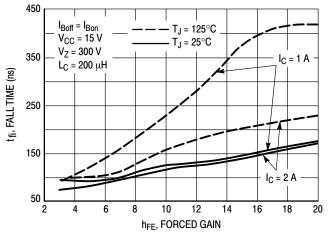


Figure 19. Inductive Switching, $t_c @ I_C/I_B = 10$

Figure 20. Inductive Storage Time



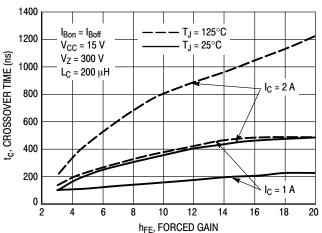
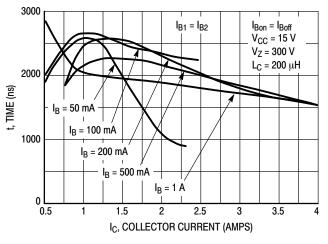


Figure 21. Inductive Fall Time

Figure 22. Inductive Crossover Time



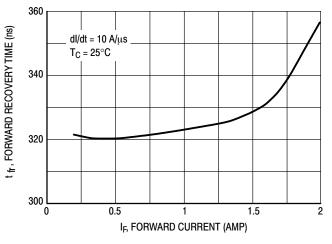


Figure 23. Inductive Storage Time, tsi

Figure 24. Forward Recovery Time tfr

TYPICAL SWITCHING CHARACTERISTICS

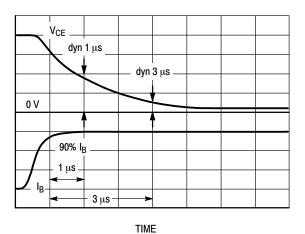


Figure 25. Dynamic Saturation Voltage Measurements

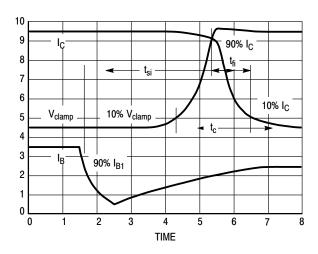


Figure 26. Inductive Switching Measurements

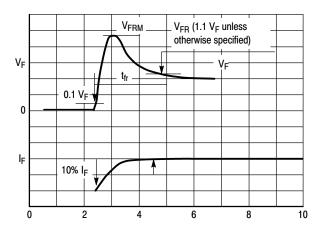
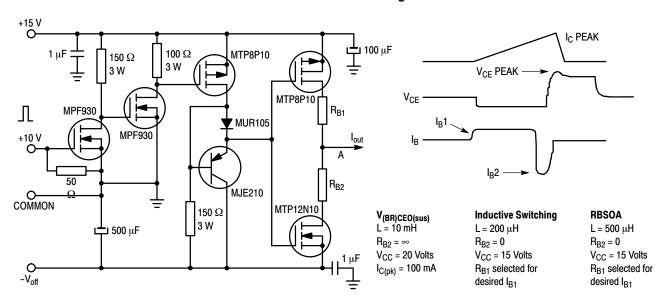


Figure 27. t_{fr} Measurements

TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit



TYPICAL CHARACTERISTICS

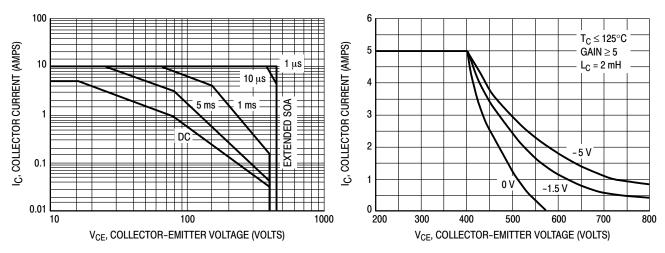


Figure 28. Forward Bias Safe Operating Area

Figure 29. Reverse Bias Safe Operating Area

TYPICAL CHARACTERISTICS

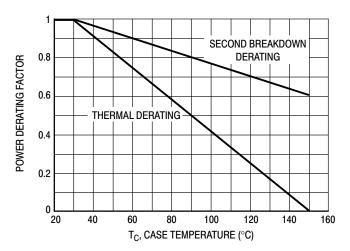


Figure 30. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on $T_C = 25$ °C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25$ °C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on

Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

 $T_{J(pk)}$ may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn—off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL THERMAL RESPONSE

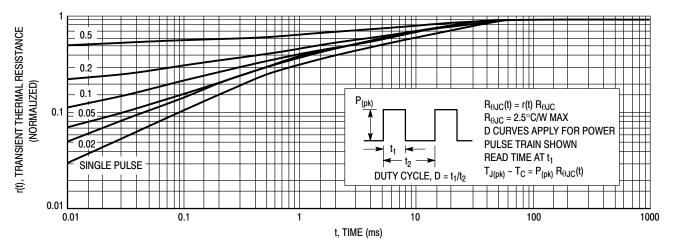
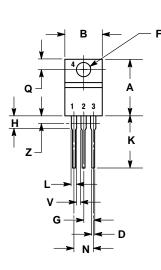
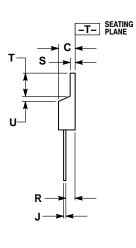


Figure 31. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL45D2

PACKAGE DIMENSIONS

TO-220 CASE 221A-09 **ISSUE AH**





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE

	INCHES		MILLIN	LIMETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.570	0.620	14.48	15.75	
В	0.380	0.415	9.66	10.53	
C	0.160	0.190	4.07	4.83	
D	0.025	0.038	0.64	0.96	
F	0.142	0.161	3.61	4.09	
G	0.095	0.105	2.42	2.66	
Н	0.110	0.161	2.80	4.10	
J	0.014	0.024	0.36	0.61	
K	0.500	0.562	12.70	14.27	
L	0.045	0.060	1.15	1.52	
N	0.190	0.210	4.83	5.33	
Q	0.100	0.120	2.54	3.04	
R	0.080	0.110	2.04	2.79	
S	0.045	0.055	1.15	1.39	
T	0.235	0.255	5.97	6.47	
U	0.000	0.050	0.00	1.27	
٧	0.045		1.15		
Z		0.080		2.04	

STYLE 1:

BASE PIN 1.

COLLECTOR

EMITTER 3 COLLECTOR

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