LV8400V

Bi-CMOS IC Forward/Reverse Motor Driver



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Overview

The LV8400V is a 1-channel motor driver IC using D-MOS FET for output stage and operates in one of the four modes under program control: forward, reverse, brake, and standby.

As the P/N-channel structure is used in the H-bridge output stage, the LV8400V features minimal number of external component and low on-resistance (0.33 Ω typical). This IC is optimal for driving motors that need large-current.

Functions

- 1-channel forward/reverse motor driver
- Low power consumption
- Low output ON resistance 0.33Ω

- Built-in constant current output circuit
- Built-in low voltage reset and thermal shutdown circuit
- Four mode function forward/reverse, brake, standby.

Specifications

Maximum Ratings at Ta = 25°C, SGND = PGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage (for load)	VM max		-0.5 to 16.0	V
Power supply voltage (for control)	V _{CC} max		-0.5 to 6.0	V
Output current	I _O max	DC	1.2	Α
	I _O peak1	t ≤ 100ms, f = 5Hz	2.0	Α
	I _O peak2	t ≤ 10ms, f = 5Hz	3.8	Α
	I _{OUT} max	DC	30	mA
Input voltage	V _{IN} max		-0.5 to V _{CC} +0.5	V
Allowable power dissipation	Pd max	Mounted on a specified board *	800	mW
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

^{*} Specified board : $30\text{mm} \times 50\text{mm} \times 1.6\text{mm}, \text{ glass epoxy board}.$

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Allowable Operating Conditions at Ta = 25°C, SGND = PGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage (for load)	VM		4.0 to 15.0	V
Power supply voltage (for control)	V _{CC}		2.7 to 5.5	V
Input signal voltage	V _{IN}		0 to V _{CC}	V
Input signal frequency	f max	Duty = 50%	200	kHz

Electrical Characteristics Ta = 25°C, V_{CC} = 5.0V, VM = 12.0V, SGND = PGND = 0V, unless otherwise specified.

D		Oh al	One distance	Damada	Ratir			Unit	
Parar	neter	Symbol	Conditions	Remarks	min	typ	max	Offic	
Standby load cur	rrent drain 1	IMO1	EN = 0V	1			1.0	μΑ	
Standby load cur	rrent drain 2	IMO2	EN = 0V, V _{CC} = 0V, Each input pin = 0V	1			1.0	μΑ	
Standby control	current drain	ICO	EN = 0V, IN1 = IN2 = 0V	2			1.0	μΑ	
Operating load c	urrent drain 1	IM1	V _{CC} = 3.3V, EN = 3.3V	3		0.35	0.70	mA	
Operating load current drain 2		IM2	V _{CC} = 5.0V, EN = 5.0V	3		0.35	0.70	mA	
Operating curren	it consumption 1	IC1	V _{CC} = 3.3V, EN = 3.3V	4		0.6	1.2	mA	
Operating current consumption 2		IC2	V _{CC} = 5.0V, EN = 5.0V	4		0.8	1.6	mA	
High-level input v	voltage	V _{IH}	2.7 ≤ V _{CC} ≤ 5.5V		0.6×V _{CC}		V _{CC}	V	
Low-level input v	roltage	V _{IL}	2.7 ≤ V _{CC} ≤ 5.5V		0		0.2×V _{CC}	V	
High-level input of (EN,IN1, IN2, IC		IH	V _{IN} = 5V	5	12.5	25	50	μА	
Low-level input of		IIL	V _{IN} = 0V	5	-1.0			μА	
Pull-down resista (EN,IN1, IN2, IC		R _{DN}			100	200	400	kΩ	
Output ON resist	tance	R _{ON}	Sum of top and bottom sides ON resistance. $2.7V \le V_{CC} \le 5.5V$	6		0.33	0.5	Ω	
Constant current current	output leakage	I _O LEAK	EN = 0V	7			1.0	μА	
Output constant	current	lout	RSET = 40Ω , Internal reference = $0.2V$	8	4.65	5.00	5.35	mA	
ISET pin voltage		VISET	RSET = 40Ω	9	0.186	0.20	0.214	V	
Constant current resistance	output ON	R _{ON} IO	RSET = 0Ω , $I_O = 5mA$	10		20	30	Ω	
Low-voltage dete	ection voltage	VCS	V _{CC} voltage	11	2.10	2.25	2.40	V	
Thermal shutdow	vn temperature	Tth	Design guarantee *	12	150	180	210	°C	
Output block	Turn-on time	TPLH		13		0.5	1.0	μs	
ļ	Turn-off time	TPHL	13 0.		0.5	1.0	μs		

^{*} Design guarantee value and no measurement is performed.

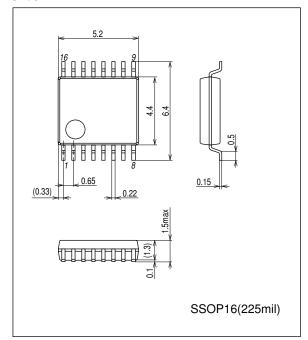
Remarks

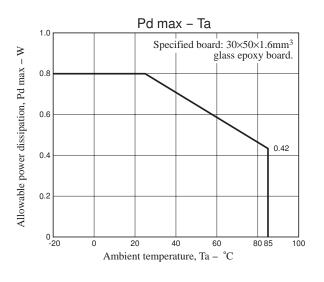
- 1. Current consumption when output at the VM pin is off.
- 2. Current consumption at the V_{CC} pin when in all function stop.
- 3. Current consumption at the VM pin when EN is high.
- 4. Current consumption at the V_{CC} pin when EN is high.
- 5. These input pins (EN, IN1, IN2, and ICTRL) have an internal pull-down resistor.
- 6. Sum of the top and bottom side output on resistance.
- 7. Leakage current when the constant current output is off.
- 8. Current value that is determined by dividing the internal reference voltage (0.2V) by RSET.
- 9. ISET pin voltage when the constant current output block is active.
- 10. ON resistance value of the constant current output block.
- 11. All output transistors are turned off if a low-voltage is detected.
- 12. All output transistors are turned off if the thermal protection circuit is activated. They are turned on again as the temperature goes down.
- 13. Rising time from 10 to 90% and falling time from 90 to 10% are specified.

Package Dimensions

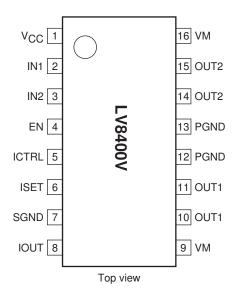
unit: mm (typ)

3178B

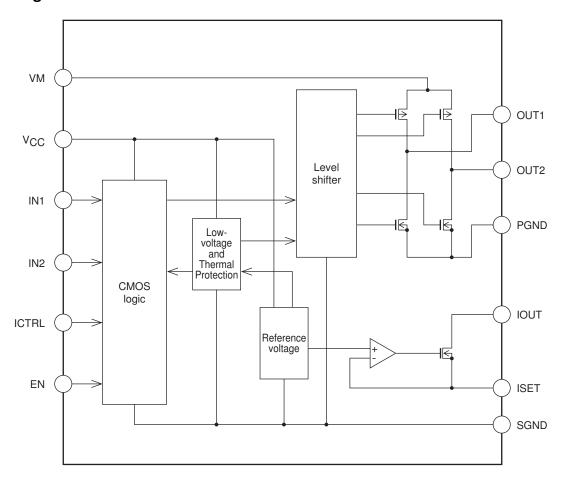




Pin Assignment



Block Diagram



Truth Table

EN	IN1	IN2	OUT1	OUT2	Mode
	Н	Н	L	L	Brake
	Н	L	Н	L	Forward
Н	L	Н	L	Н	Reverse
	L	L	Z	Z	Standby
L	-	-	Z	Z	All function stop

EN	ICTRL	IOUT	Mode
	Н	ON	Constant current ON
н	L	Z	Constant current OFF
L	-	Z	All function stop

- : denotes a don't care value. Z : High-impedance

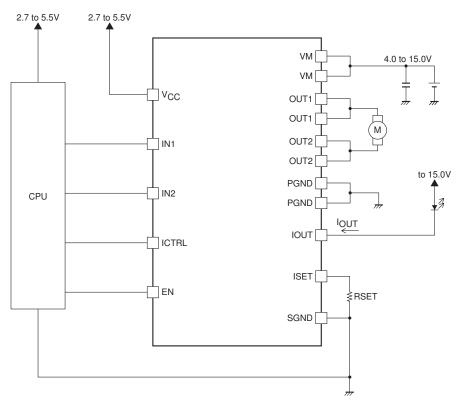
- Current drain is zero in all function stop mode. (excluding the current that flows out of the EN pin)
- * All power transistors turn off and the motor stops driving when the IC is detected in low voltage or thermal protection mode.

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Pin Functions

Pin No. Pin name Description Equivalent circuit 9 VM Motor block power supply. (Both pins must be connected) 1 V _{CC} Logic block power supply. 4 EN Logic enable pin. (Pull-down resistor incorporated) 2 IN1 3 IN2 5 ICTRL 5 ICTRL Driver output switching. (Pull-down resistor incorporated) VCC 10kΩ	Pin No. Pin na
16 (Both pins must be connected)	
4 EN Logic enable pin. (Pull-down resistor incorporated) 2 IN1 IN2 Driver output switching. (Pull-down resistor incorporated) 5 ICTRL 10kΩ VCC 10kΩ 10kΩ 10kΩ 10kΩ 10kΩ VCC VCC VCC VCC VCC VCC VCC V	
Pull-down resistor incorporated VCC 10kΩ W 200kΩ	
3 IN2 (Pull-down resistor incorporated) 10 OUT1 Driver output. 11 OUT2 15 OUT2	4 EN
11 14 OUT2 15	3 IN
11 14 15 OUT2	
	14 OU
6 ISET Constant current output.	6 ISE
8 IOUT Reference voltage 0.2V	
7 SGND Logic block ground.	7 SGN
12 PGND Driver block ground. 13 (Both pins must be connected)	

Sample Application Circuit



- *1 : Connect a kickback absorbing capacitor as close as possible to the IC. Characteristics deterioration of the IC or damage may result if an instantaneous voltage surge exceeding the maximum rated value is applied to the VM line due to coil kickback or other causes.
- *2 : The output constant current (I_{OUT}) is determined by the internal reference voltage and the sense resistor between the ISET and SGND pins.

 I_{OUT} = Internal reference voltage (0.2V) ÷ Sense resistor (RSET)

From the formula above, $I_{OUT} = 5mA$ when a sense resistor of 40Ω is connected between the ISET and SGND.

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