

# NB2305A

## 3.3 V Zero Delay Clock Buffer

The NB2305A is a versatile, 3.3 V zero delay buffer designed to distribute high-speed clocks. It accepts one reference input and drives out five low-skew clocks. It is available in a 8 pin package.

The -1H version of the NB2305A operates at up to 133 MHz, and has higher drive than the -1 devices. All parts have on-chip PLL's that lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

Multiple NB2305A devices can accept the same input clock and distribute it. In this case the skew between the outputs of the two devices is guaranteed to be less than 700 ps.

All outputs have less than 200 ps of cycle-to-cycle jitter. The input and output propagation delay is guaranteed to be less than 350 ps, and the output to output skew is guaranteed to be less than 250 ps.

The NB2305A is available in two different configurations, as shown in the ordering information table. The NB2305AI is the base part. The NB2305AI1H is the high drive version of the -1 and its rise and fall times are much faster than -1 part.

### Features

- 15 MHz to 133 MHz Operating Range, Compatible with CPU and PCI Bus Frequencies
- Zero Input – Output Propagation Delay
- Multiple Low-Skew Outputs
- Output-Output Skew Less than 250 ps
- Device-Device Skew Less than 700 ps
- One Input Drives 5 Outputs
- Less than 200 ps Cycle-to-Cycle Jitter is Compatible with Pentium® Based Systems
- Accepts Spread Spectrum Clock at the Input
- Available in 8 Pin, 150 mil SOIC Package and 8 Pin TSSOP 4.4 mm
- 3.3 V Operation, Advanced 0.35  $\mu$  CMOS Technology
- Guaranteed Across Commercial and Industrial Temperature Ranges
- These are Pb-Free Devices



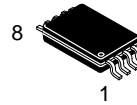
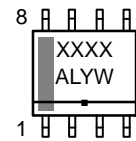
ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

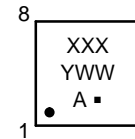
### MARKING DIAGRAMS\*



SOIC-8  
D SUFFIX  
CASE 751



TSSOP-8  
DT SUFFIX  
CASE 948S



XXXX = Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

# NB2305A

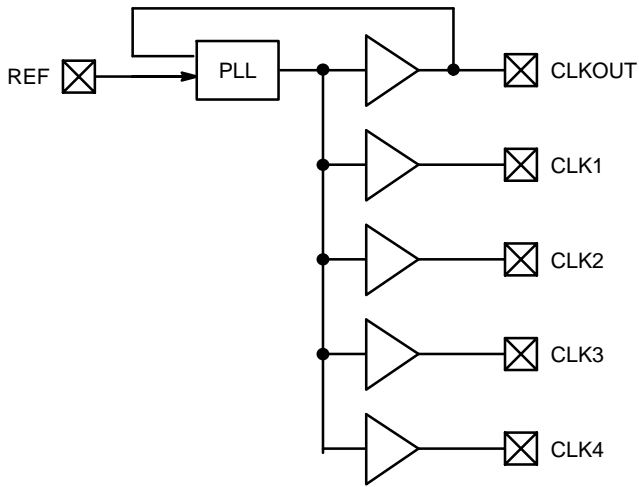


Figure 1. Block Diagram

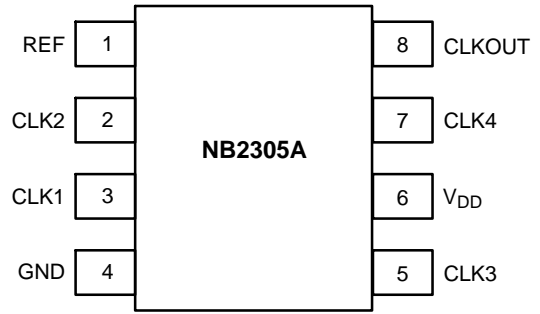


Figure 2. Pin Configuration

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Description
1	REF (Note1)	Input reference frequency, 5 V tolerant input.
2	CLK2 (Note 2)	Buffered clock output.
3	CLK1 (Note 2)	Buffered clock output.
4	GND	Ground.
5	CLK3 (Note 2)	Buffered clock output.
6	V <sub>DD</sub>	3.3 V supply.
7	CLK4 (Note 2)	Buffered clock output.
8	CLKOUT (Note 2)	Buffered clock output, internal feedback on this pin.

1. Weak pulldown.
2. Weak pulldown on all outputs.

# NB2305A

**Table 2. MAXIMUM RATINGS**

Parameter	Min	Max	Unit
Supply Voltage to Ground Potential	-0.5	+7.0	V
DC Input Voltage (Except REF)	-0.5	$V_{DD} + 0.5$	V
DC Input Voltage (REF)	-0.5	7.0	V
Storage Temperature	-65	+150	°C
Maximum Soldering Temperature (10 sec)		260	°C
Junction Temperature		150	°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)		>2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 3. RECOMMENDED OPERATING CONDITIONS FOR INDUSTRIAL TEMPERATURE DEVICES**

Parameter	Description	Min	Max	Unit
$V_{DD}$	Supply Voltage	3.0	3.6	V
$T_A$	Operating Temperature (Ambient Temperature)	Industrial Commercial	-40 85 70	°C
$C_L$	Load Capacitance, below 100 MHz		30	pF
$C_L$	Load Capacitance, from 100 MHz to 133 MHz		10	pF
$C_{IN}$	Input Capacitance		7	pF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 4. ELECTRICAL CHARACTERISTICS**  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

Parameter	Description	Test Conditions	Min	Max	Unit
$V_{IL}$	Input LOW Voltage (Note 3)			0.8	V
$V_{IH}$	Input HIGH Voltage (Note 3)		2.0		V
$I_{IL}$	Input LOW Current	$V_{IN} = 0\text{ V}$		50	$\mu\text{A}$
$I_{IH}$	Input HIGH Current	$V_{IN} = V_{DD}$		100	$\mu\text{A}$
$V_{OL}$	Output LOW Voltage	$I_{OL} = 8\text{ mA (-1)}$ $I_{OL} = 12\text{ mA (-1H)}$		0.4	V
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -8\text{ mA (-1)}$ $I_{OH} = -12\text{ mA (-1H)}$	2.4		V
$I_{DD}$	Supply Current (Commercial Temp)	Unloaded outputs at 66.67 MHz, Select inputs at $V_{DD}$		34	mA
$I_{DD}$	Supply Current (Industrial Temp)	Unloaded outputs at 100 MHz 66.67 MHz 33 MHz Select inputs at $V_{DD}$ or GND, at Room Temp		50 34 19	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. REF input has a threshold voltage of  $V_{DD}/2$ .

## NB2305A

**Table 5. SWITCHING CHARACTERISTICS**  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$  (Note 4)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
$1/t_1$	Output Frequency	30 pF load 10 pF load	15 15		100 133	MHz
$1/t_1$	Duty Cycle = $(t_2 / t_1) * 100$ (-1, -1H) (-1H)	Measured at 1.4 V, $F_{OUT} = 66.67\text{ MHz}$ < 50 MHz	40 45	50 50	60 55	%
$t_3$	Output Rise Time (-1) (-1H)	Measured between 0.8 V and 2.0 V			2.5 1.5	ns
$t_4$	Output Fall Time (-1) (-1H)	Measured between 2.0 V and 0.8 V			2.5 1.5	ns
$t_5$	Output-to-Output Skew	All outputs equally loaded			250	ps
$t_6$	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at $V_{DD}/2$		0	$\pm 350$	ps
$t_7$	Device-to-Device Skew	Measured at $V_{DD}/2$ on the CLKOUT pins of the device		0	700	ps
$t_J$	Cycle-to-Cycle Jitter	Measured at 66.67 MHz, loaded outputs			200	ps
$t_{LOCK}$	PLL Lock Time	Stable power supply, valid clock presented on REF pin			1.0	ms

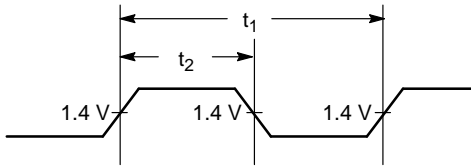
4. All parameters specified with loaded outputs.

**Zero Delay and Skew Control**

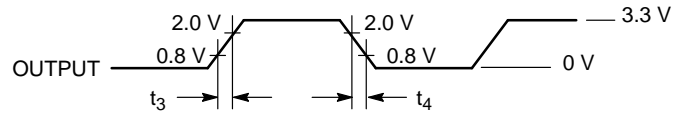
All outputs should be uniformly loaded to achieve Zero Delay between input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input–output delay.

For applications requiring zero input–output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs, for obtaining zero–input–output delay.

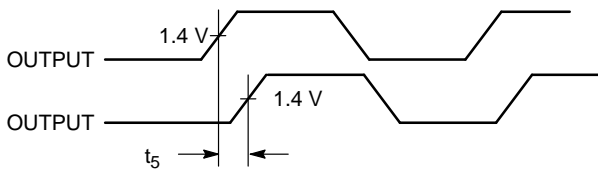
**SWITCHING WAVEFORMS**



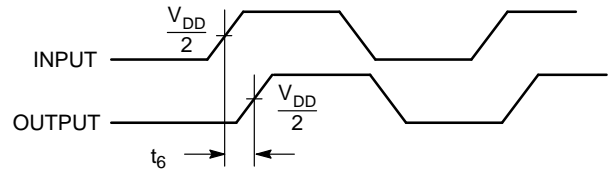
**Figure 3. Duty Cycle Timing**



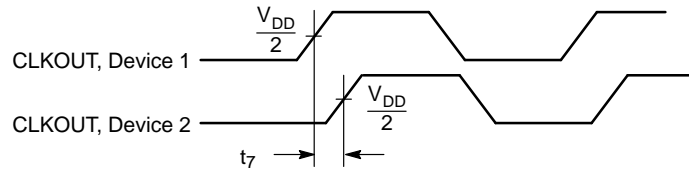
**Figure 4. All Outputs Rise/Fall Time**



**Figure 5. Output – Output Skew**



**Figure 6. Input – Output Propagation Delay**



**Figure 7. Device – Device Skew**

# NB2305A

## TEST CIRCUITS

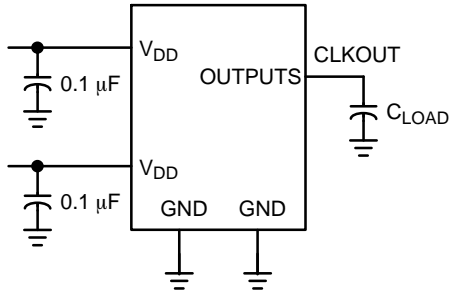


Figure 8. Test Circuit #1

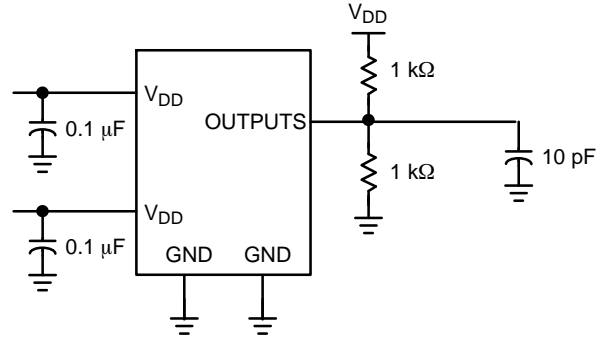


Figure 9. Test Circuit #2  
For parameter  $t_8$  (output slew rate) on -1H devices

### ORDERING INFORMATION

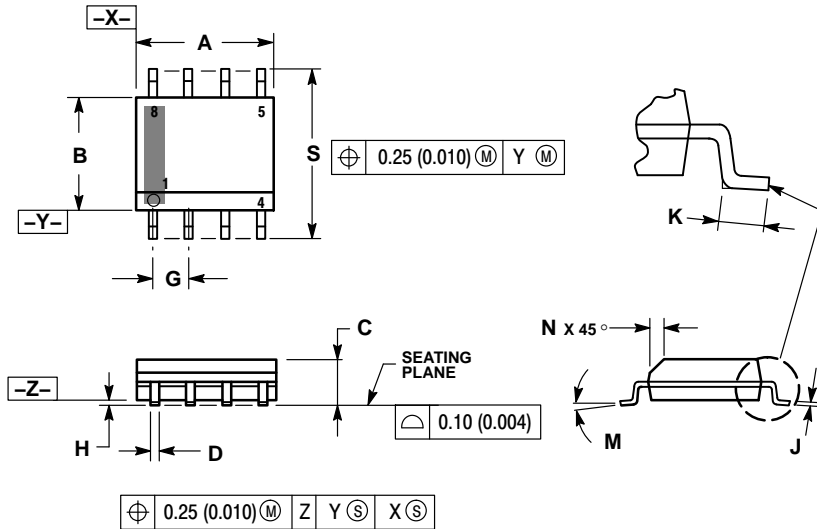
Device	Marking	Operating Range	Package	Shipping <sup>†</sup>	Availability
NB2305AI1DG	511	Industrial & Commercial	SOIC-8 (Pb-Free)	98 Units / Rail	Now
NB2305AI1DR2G	511	Industrial & Commercial	SOIC-8 (Pb-Free)	2500 Tape & Reel	Now
NB2305AI1HDG	511H	Industrial & Commercial	SOIC-8 (Pb-Free)	98 Units / Rail	Now
NB2305AI1HDR2G	511H	Industrial & Commercial	SOIC-8 (Pb-Free)	2500 Tape & Reel	Now
NB2305AI1DTG	511	Industrial & Commercial	TSSOP-8 (Pb-Free)	100 Units / Rail	Now
NB2305AI1DTR2G	511	Industrial & Commercial	TSSOP-8 (Pb-Free)	2500 Tape & Reel	Now
NB2305AI1HDTG	5IH	Industrial & Commercial	TSSOP-8 (Pb-Free)	100 Units / Rail	Now
NB2305AI1HDTR2G	5IH	Industrial & Commercial	TSSOP-8 (Pb-Free)	2500 Tape & Reel	Now

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NB2305A

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AK

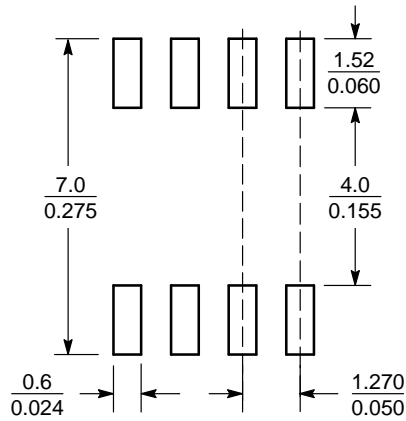


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



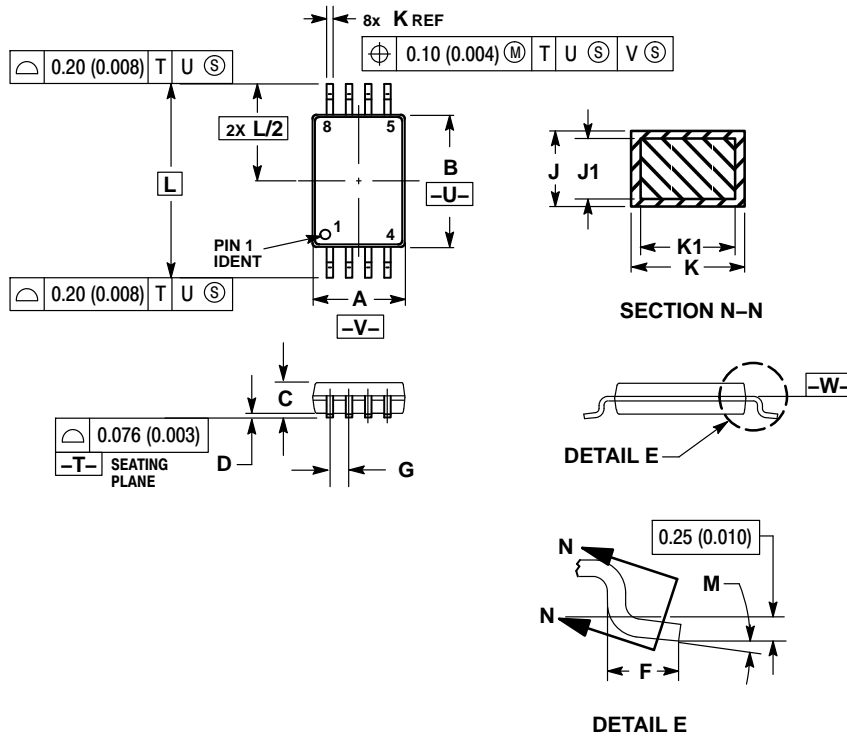
SCALE 6:1  $\left( \frac{\text{mm}}{\text{inches}} \right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NB2305A

## PACKAGE DIMENSIONS

### TSSOP-8 CASE 948S ISSUE C




#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

Pentium is a registered trademark of Intel Corporation.

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative