

MC100E310

5 V ECL Low Voltage 2:8 Differential Fanout Buffer

Description

The MC100E310 is a low voltage, low skew 2:8 differential ECL fanout buffer designed with clock distribution in mind. The device features fully differential clock paths to minimize both device and system skew. The E310 offers two selectable clock inputs to allow for redundant or test clocks to be incorporated into the system clock trees.

The lowest TPD delay time results from terminating only one output pair, and the greatest TPD delay time results from terminating all the output pairs. This shift is about 10–20 pS in TPD. The skew between any two output pairs within a device is typically about 25 nS. If other output pairs are not terminated, the lowest TPD delay time results from both output pairs and the skew is typically 25 nS. When all outputs are terminated, the greatest TPD (delay time) occurs and all outputs display about the same 10–20 ps increase in TPD, so the relative skew between any two output pairs remains about 25 ns.

For more information on using PECL, designers should refer to ON Semiconductor Application Note [AN1406/D](#).

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series Contains Temperature Compensation.

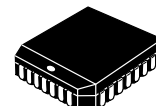
Features

- Dual Differential Fanout Buffers
- 200 ps Part-to-Part Skew
- 50 ps Output-to-Output Skew
- 28-lead PLCC Packaging
- Q Output will Default LOW with Inputs Open or at V_{EE}
- PECL Mode Operating Range: $V_{CC} = 4.2$ V to 5.7 V with $V_{EE} = 0$ V
- NECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -4.2$ V to -5.7 V
- Internal Input 50 k Ω Pulldown Resistors
- ESD Protection:
 - ◆ > 2 kV Human Body Model
 - ◆ > 200 V Machine Model
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity: Level 3 (Pb-Free)
(For Additional Information, see Application Note [AND8003/D](#))
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 212 Devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



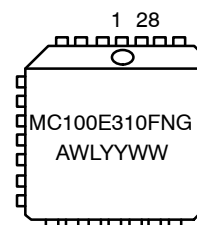
ON Semiconductor®

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PLCC-28
FN SUFFIX
CASE 776-02

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

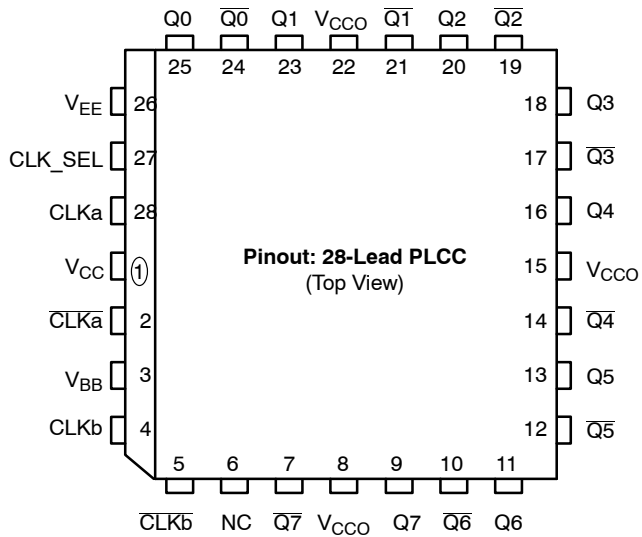
*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|-------------------|-----------------|
| MC100E310FNG | PLCC-28 (Pb-Free) | 37 Units / Tube |
| MC100E310FNR2G | PLCC-28 (Pb-Free) | 500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Logic Diagram and Pinout Assignment

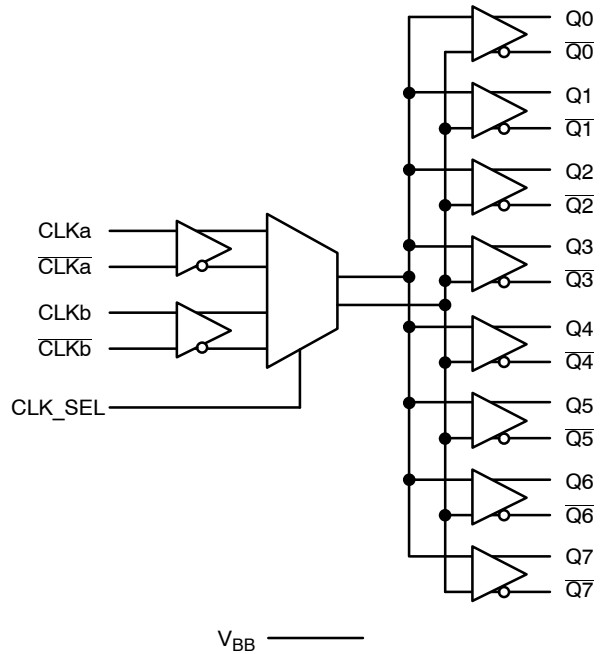


Figure 2. Logic Symbol

Table 1. PIN DESCRIPTION

| PIN | Function |
|------------------------------------|------------------------------|
| CLKa, CLKb; CLKa-bar, CLKb-bar | ECL Differential Input Pairs |
| Q0:7; Q0-bar:7 | ECL Differential Outputs |
| CLK_SEL | ECL Input Clock Select |
| V _{BB} | Reference Voltage Output |
| V _{CC} , V _{CCO} | Positive Supply |
| V _{EE} | Negative Supply |
| NC | No Connect |

Table 2. FUNCTION TABLE

| PIN | Function |
|-----|---------------|
| 0 | CLKa Selected |
| 1 | CLKb Selected |

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Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---------------|--|--|--|--------------|--|
| V_{CC} | PECL Mode Power Supply | $V_{EE} = 0\text{ V}$ | | 8 | V |
| V_I | PECL Mode Input Voltage NECL Mode Input Voltage | $V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$ | $V_I \leq V_{CC}$ $V_I \geq V_{EE}$ | 6 -6 | V V |
| I_{out} | Output Current | Continuous Surge | | 50 100 | mA mA |
| I_{BB} | V_{BB} Sink/Source | | | ± 0.5 | mA |
| T_A | Operating Temperature Range | | | -40 to +85 | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | $^{\circ}\text{C}$ |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | PLCC-28 PLCC-28 | 63.5 43.5 | $^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$ |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | PLCC-28 | 22 to 26 | $^{\circ}\text{C}/\text{W}$ |
| T_{sol} | Wave Solder (Pb-Free) | | | 265 | $^{\circ}\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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Table 4. 100E SERIES PECL DC CHARACTERISTICS ($V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|------|------|------|------|------|------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 55 | 60 | | 55 | 60 | | 65 | 70 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | 3915 | 3995 | 4120 | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | 3170 | 3305 | 3445 | 3190 | 3255 | 3380 | 3190 | 3260 | 3380 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | mV |
| V_{BB} | Output Voltage Reference | 3.62 | | 3.74 | 3.62 | | 3.74 | 3.62 | | 3.74 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.7 | | 4.6 | 2.7 | | 4.6 | 2.7 | | 4.6 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.5 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

Table 5. 100E SERIES NECL DC CHARACTERISTICS ($V_{CCx} = 0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 55 | 60 | | 55 | 60 | | 65 | 70 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | -1085 | -1005 | -880 | -1025 | -950 | -880 | -1025 | -950 | -880 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | -1830 | -1695 | -1555 | -1810 | -1745 | -1620 | -1810 | -1740 | -1620 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1165 | -1025 | -880 | -1165 | -1025 | -880 | -1165 | -1025 | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1810 | -1645 | -1475 | -1810 | -1645 | -1475 | -1810 | -1645 | -1475 | mV |
| V_{BB} | Output Voltage Reference | -1.38 | | -1.26 | -1.38 | | -1.26 | -1.38 | | -1.26 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | -2.3 | | -0.4 | -2.3 | | -0.4 | -2.3 | | -0.4 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.5 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

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Table 6. AC CHARACTERISTICS ($V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0\text{ V}$ or $V_{CCx} = 0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|------------------------|---|------------|-----|------------|------------|-----|------------|------------|-----|------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{MAX} | Maximum Toggle Frequency | 700 | 900 | | 700 | 900 | | 700 | 900 | | MHz |
| t_{PLH} t_{PHL} | Propagation Delay to Output IN (differential) (Note 2) IN (single-ended) (Note 3) | 525 500 | | 725 750 | 550 550 | | 750 800 | 575 600 | | 775 850 | ps |
| t_{skew} | Within-Device Skew (Note 4) Part-to-Part Skew (Diff) | | | 75 250 | | | 50 200 | | | 50 200 | ps |
| t_{JITTER} | Random Clock Jitter (RMS) | | < 1 | | | < 1 | | | < 1 | | ps |
| V_{PP} | Input Voltage Swing (Differential Configuration) | 500 | | | 500 | | | 500 | | | mV |
| t_r/t_f | Output Rise/Fall Time (20%–80%) | 200 | | 600 | 200 | | 600 | 200 | | 600 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. V_{EE} can vary -0.46 V / $+0.8\text{ V}$.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the ON Semiconductor High Performance ECL Data Book (DL140/D).
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.

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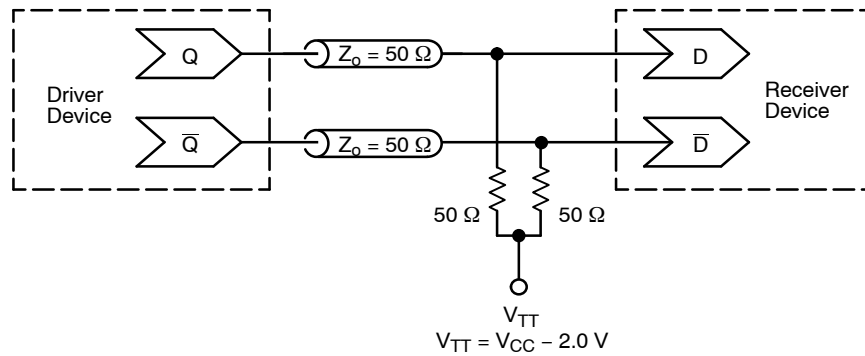


Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

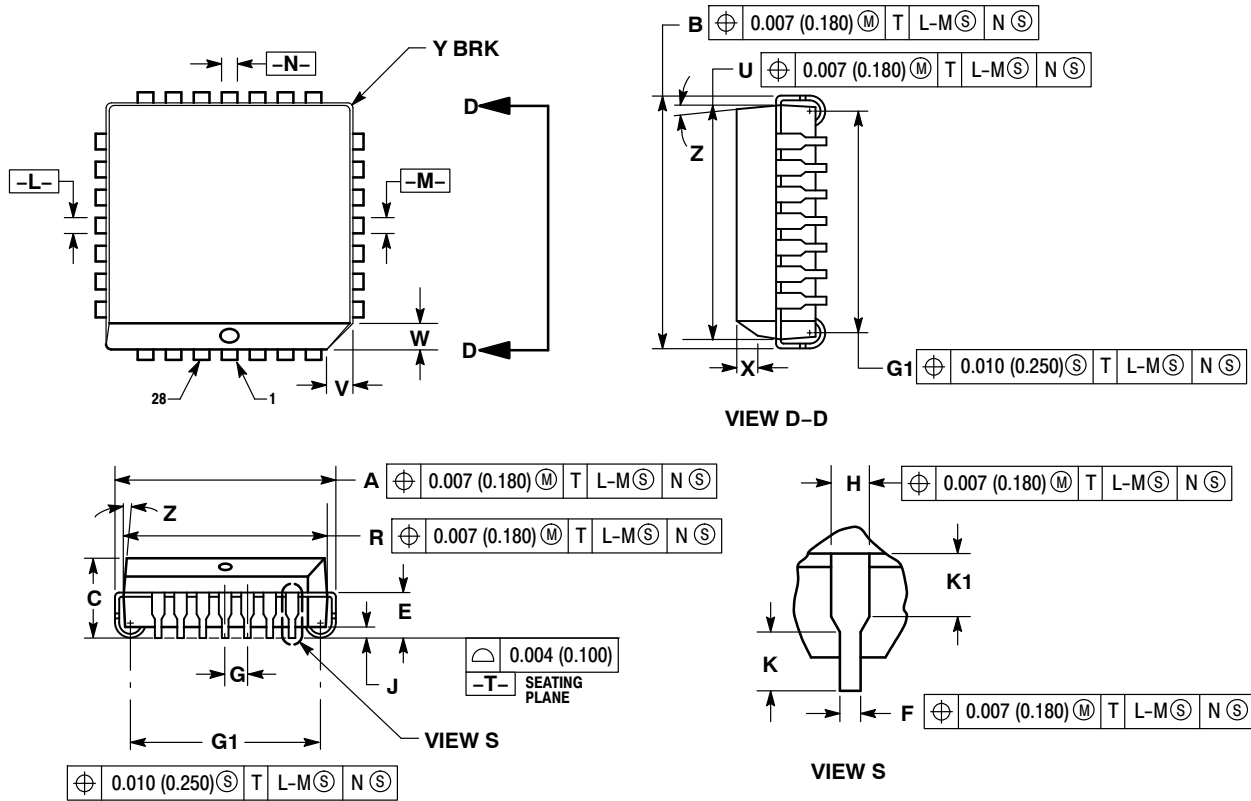
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

28 LEAD PLLC
FN SUFFIX
CASE 776-02
ISSUE F




NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.485 | 0.495 | 12.32 | 12.57 |
| B | 0.485 | 0.495 | 12.32 | 12.57 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.021 | 0.33 | 0.53 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | --- | 0.51 | --- |
| K | 0.025 | --- | 0.64 | --- |
| R | 0.450 | 0.456 | 11.43 | 11.58 |
| U | 0.450 | 0.456 | 11.43 | 11.58 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | --- | 0.020 | --- | 0.50 |
| Z | 2° | 10° | 2° | 10° |
| G1 | 0.410 | 0.430 | 10.42 | 10.92 |
| K1 | 0.040 | --- | 1.02 | --- |

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