

NB100EP223

3.3V 2:1:22 Differential HSTL/PECL to HSTL Clock Driver with LVTTTL Clock Select and Output Enable

Description

The NB100EP223 is a low skew 2:1:22 differential clock driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The part is designed for use in low voltage applications which require a large number of outputs to drive precisely aligned low skew signals to their destination. The two clock inputs are differential HSTL or LVPECL and they are selected by the CLK_SEL pin which is LVTTTL. To avoid generation of a runt clock pulse when the device is enabled/disabled, the Output Enable (OE), which is LVTTTL, is synchronous ensuring the outputs will only be enabled/disabled when they are already in LOW state (See Figure 7).

The NB100EP223 guarantees low output-to-output skew. The optimal design, layout, and processing minimize skew within a device and from lot to lot. In any differential output pair, the same bias and termination scheme is required. Unused output pairs should be left unterminated (open) to “reduce power and switching noise as much as possible.” Any unused single line of a differential pair should be terminated the same as the used line to maintain balanced loads on the differential driver outputs. The output structure uses an open emitter architecture and will be terminated with 50 Ω to ground instead of a standard HSTL configuration (See Figure 6). The wide VIHCMR specification allows both pair of CLOCK inputs to accept LVDS levels.

Features

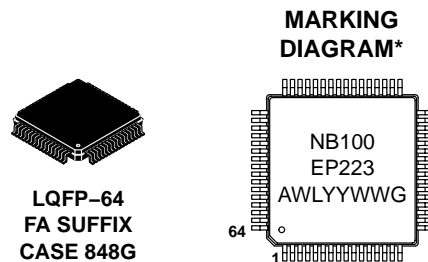
- 100 ps Typical Device-to-Device Skew
- 25 ps Typical Within Device Skew
- HSTL Compatible Outputs Drive 50 Ω to Ground With No Offset Voltage
- Maximum Frequency >500 MHz
- 1 ns Typical Propagation Delay
- LVPECL and HSTL Mode Operating Range: $V_{CC} = 3\text{ V}$ to 3.6 V with $GND = 0\text{ V}$, $V_{CCO} = 1.6\text{ V}$ to 2.0 V
- Q Output will Default Low with Inputs Open
- Thermally Enhanced 64-Lead LQFP
- CLOCK Inputs are LVDS-Compatible; Requires External 100 Ω LVDS Termination Resistor
- These are Pb-Free Devices*

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

<http://onsemi.com>



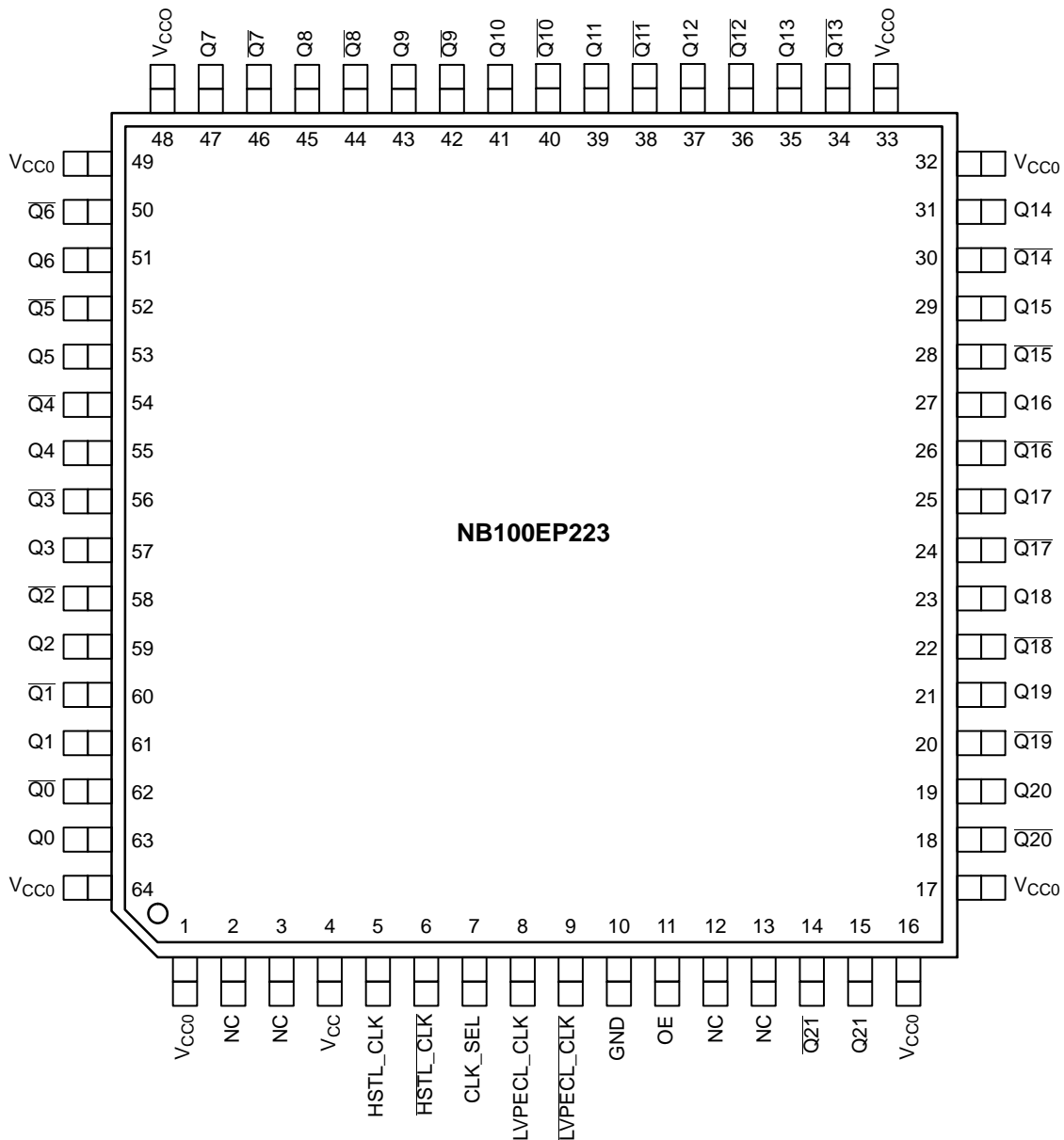
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

NB100EP223



All V_{CC}, V_{CC0}, and GND pins must be externally connected to appropriate Power Supply to guarantee proper operation (V_{CC} ≠ V_{CC0}). The thermally conductive exposed pad on package bottom (see package case drawing) is electrically connected to GND internally.

Figure 1. 64-Lead LQFP Pinout (Top View)

Table 1. PIN DESCRIPTION

| PIN | FUNCTION |
|---------------------------|--|
| HSTL_CLK*, HSTL_CLK** | HSTL, LVPECL or LVDS Differential Inputs |
| LVPECL_CLK*, LVPECL_CLK** | LVPECL Differential Inputs |
| CLK_SEL** | LVC MOS/LVTTL Input CLK Select |
| OE** | LVC MOS/LVTTL Output Enable |
| Q0–Q21, Q0–Q21 | HSTL Differential Outputs |
| V _{CC} | Positive Supply_Core (3.0 V – 3.6 V) |
| V _{CC0} | Positive Supply_HSTL Outputs(1.6V–2.0V) |
| GND*** | Ground |

Table 2. FUNCTION TABLE

| OE* | CLK_SEL | Q0–Q21 | Q0–Q21 |
|-----|---------|------------|------------|
| L | L | L | H |
| L | H | L | H |
| H | L | HSTL_CLK | HSTL_CLK |
| H | H | LVPECL_CLK | LVPECL_CLK |

* The OE (Output Enable) signal is synchronized with the rising edge of the HSTL_CLK and LVPECL_CLK signal.

* Pins will default LOW when left open.

** Pins will default HIGH when left open.

***The thermally conductive exposed pad on the bottom of the package is electrically connected to GND internally.

NB100EP223

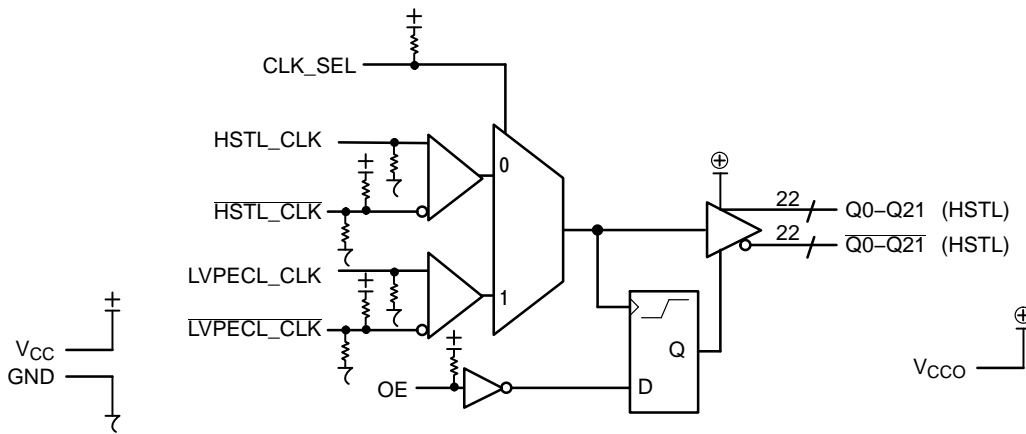


Figure 2. Logic Diagram

Table 3. ATTRIBUTES

| Characteristics | | Value | |
|--|--|---|-----------------------------|
| Internal Input Pulldown Resistor | | 75 k Ω | |
| Internal Input Pullup Resistor | | 37.5 k Ω | |
| ESD Protection | | Human Body Model Machine Model Charged Device Model | > 2 kV > 150 V > 2 kV |
| Moisture Sensitivity (Note 1) | | Pb Pkg | Pb-Free Pkg |
| | | LQFP-64 | Level 2 Level 3 |
| Flammability Rating | | Oxygen Index: 28 to 34 | |
| | | UL 94 V-0 @ 0.125 in | |
| Transistor Count | | 693 | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | | |

1. For additional information, refer to Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|---|---------------------|----------------------------------|-------------|--------------|
| V _{CC} | Core Power Supply | GND = 0 V | V _{CCO} = 1.8 V | 4 | V |
| V _{CCO} | HSTL Output Power Supply | GND = 0 V | V _{CC} = 3.3 V | 4 | V |
| V _I | PECL Mode Input Voltage | GND = 0 V | V _I ≤ V _{CC} | 4 | V |
| I _{out} | Output Current | Continuous Surge | | 50 100 | mA mA |
| T _A | Operating Temperature Range | | | 0 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) (See Application Information) | 0 lfpm 500 lfpm | 64 LQFP 64 LQFP | 35.6 30 | °C/W °C/W |
| θ_{JC} | Thermal Resistance (Junction-to-Case) (See Application Information) | 0 lfpm 500 lfpm | 64 LQFP 64 LQFP | 3.2 6.4 | °C/W °C/W |
| T _{sol} | Wave Solder | Pb Pb-Free | | 265 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NB100EP223

Table 5. LVPECL DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$; $V_{CC0} = 1.8\text{ V}$; $GND = 0\text{ V}$

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|-------------|---|------|-----|------|------|-----|------|------|-----|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{CC} | Power Supply Current V_{CC} | 82 | 100 | 130 | 82 | 100 | 130 | 82 | 100 | 130 | mA |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 1490 | | 1675 | 1490 | | 1675 | 1490 | | 1675 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential) (Note 2) (Figure 4) LVPECL_CLK/LVPECL_CLK HSTL_CLK/HSTL_CLK | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| | | 0.3 | | 1.6 | 0.3 | | 1.6 | 0.3 | | 1.6 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current CLK CLK | 0.5 | | | 0.5 | | | 0.5 | | | μA |
| | | -150 | | | -150 | | | -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. V_{IHCMR} min varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. LVTTTL/LVC MOS DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$; $V_{CC0} = 1.8\text{ V}$; $GND = 0\text{ V}$

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|----------|--------------------|------|-----|-----|------|-----|-----|------|-----|-----|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V_{IH} | Input HIGH Voltage | 2.0 | | | 2.0 | | | 2.0 | | | V |
| V_{IL} | Input LOW Voltage | | | 0.8 | | | 0.8 | | | 0.8 | V |
| I_{IH} | Input HIGH Current | -150 | | 150 | -150 | | 150 | -150 | | 150 | μA |
| I_{IL} | Input LOW Current | -300 | | 300 | -300 | | 300 | -300 | | 300 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 7. HSTL DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$; $V_{CC0} = 1.6\text{--}2.0\text{ V}$; $GND = 0\text{ V}$

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|----------|--|-----------|-----|-----------|-----------|-----|-----------|-----------|-----|-----------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V_{OH} | Output HIGH Voltage (Note 3) | 1000 | | 1200 | 1000 | | 1200 | 1000 | | 1200 | mV |
| V_{OL} | Output LOW Voltage (Note 3) | 0 | | 400 | 0 | | 400 | 0 | | 400 | mV |
| V_{IH} | Input HIGH Voltage (Differential) HSTL_CLK/HSTL_CLK | V_X+100 | | 1600 | V_X+100 | | 1600 | V_X+100 | | 1600 | mV |
| V_{IL} | Input LOW Voltage (Differential) HSTL_CLK/HSTL_CLK | -300 | | V_X-100 | -300 | | V_X-100 | -300 | | V_X-100 | mV |
| V_X | Differential Cross Point Voltage | 680 | | 900 | 680 | | 900 | 680 | | 900 | mV |
| I_{IH} | Input HIGH Current | -150 | | 150 | -150 | | 150 | -150 | | 150 | μA |
| I_{IL} | Input LOW Current | -300 | | 300 | -300 | | 300 | -300 | | 300 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. All outputs loaded with 50 Ω to GND (See Figure 6).

NB100EP223

Table 8. AC CHARACTERISTICS $V_{CC} = 3.0\text{ V to }3.6\text{ V}$; $V_{CCO} = 1.6\text{ V to }2.0\text{ V}$; $GND = 0\text{ V}$ (Note 4)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|------------------------|--|------------|------------|--------------|------------|------------|--------------|------------|--------------|--------------|----------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V_{Opp} | Differential Output Voltage (Figure 3) $f_{out} < 500\text{ MHz}$ | 600 | 750 | | 600 | 750 | | 600 | 700 | | mV |
| t_{PLH} t_{PHL} | Propagation Delay (Differential) LVPECL_CLK to Q HSTL_CLK to Q | 700 800 | 900 900 | 1000 1100 | 750 850 | 900 950 | 1100 1200 | 800 850 | 1000 1050 | 1300 1350 | ps ps |
| t_{skew} | Within-Device Skew (Note 5) Device-to-Device Skew (Note 6) | | 25 100 | 50 250 | | 30 200 | 65 450 | | 50 250 | 115 450 | ps ps |
| t_{JITTER} | Random Clock Jitter (Figure 3) (RMS) | | 0.5 | 2 | | 0.5 | 2 | | 0.5 | 2 | ps |
| V_{PP} | Input Swing (Differential Mode) (Note 8) (Figure 4) LVPECL, HSTL | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| t_S | OE Set Up Time (Note 7) | 1.0 | | | 1.0 | | | 1.0 | | | ns |
| t_H | OE Hold Time | 0.5 | | | 0.5 | | | 0.5 | | | ns |
| t_r/t_f | Output Rise/Fall Time (20%–80%) | 300 | 450 | 700 | 275 | 450 | 700 | 350 | 500 | 750 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Measured with 750 mV (LVPECL) source or 1 V (HSTL) source, 50% duty cycle clock source. All outputs loaded with 50 Ω to ground (See Figure 6).
- Skew is measured between outputs under identical transitions and conditions on any one device.
- Device-to-Device skew for identical transitions at identical V_{CC} levels.
- OE Set Up Time is defined with respect to the rising edge of the clock. OE High-to-Low transition ensures outputs remain disabled during the next clock cycle. OE Low-to-High transition enables normal operation of the next input clock (See Figure 7).
- V_{PP} is the differential input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.

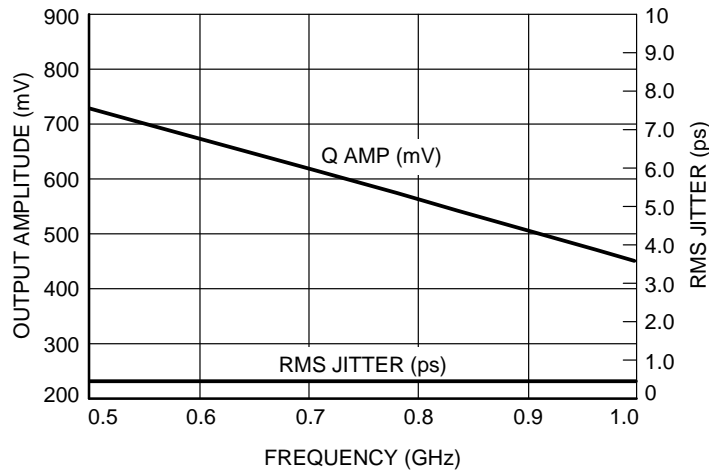


Figure 3. Output Frequency (F_{OUT}) versus Output Voltage (V_{Opp}) and Random Clock Jitter (t_{JITTER})

NB100EP223

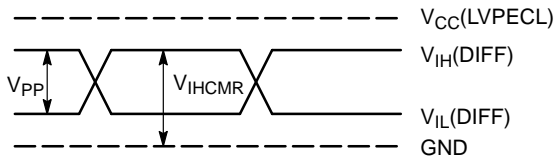


Figure 4. LVPECL Differential Input Levels

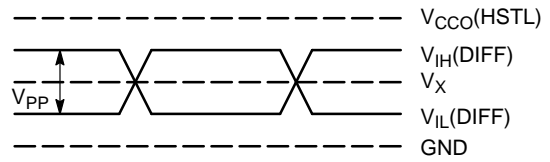


Figure 5. HSTL Differential Input Levels

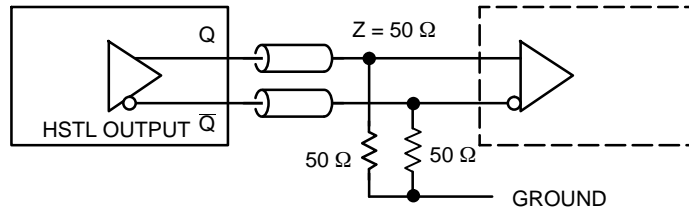


Figure 6. HSTL Output Termination and AC Test Reference

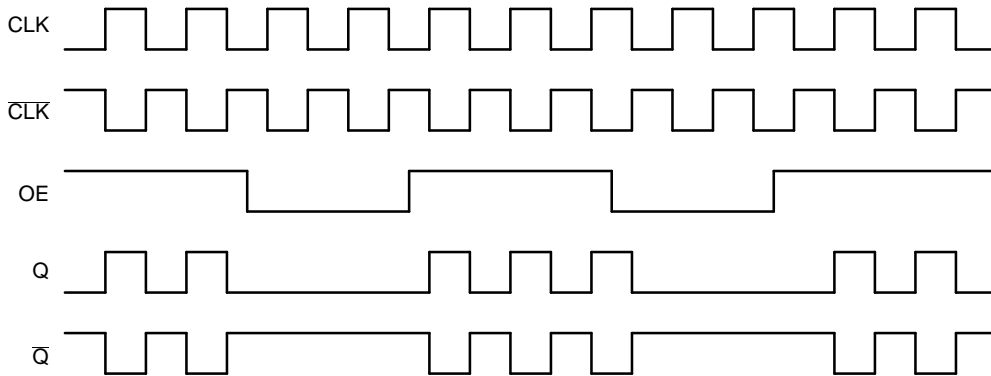


Figure 7. Output Enable (OE) Timing Diagram

APPLICATIONS INFORMATION

Using the thermally enhanced package of the NB100EP223

The NB100EP223 uses a thermally enhanced 64-lead LQFP package. The package is molded so that a portion of the leadframe is exposed at the surface of the package bottom side. This exposed metal pad will provide the low thermal impedance that supports the power consumption of the NB100EP223 high-speed bipolar integrated circuit and will ease the power management task for the system design. In multilayer board designs, a thermal land pattern on the printed circuit board and thermal vias are recommended to maximize both the removal of heat from the package and electrical performance of the NB100EP223. The size of the land pattern can be larger, smaller, or even take on a different shape than the exposed pad on the package. However, the solderable area should be at least the same size and shape as the exposed pad on the package. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal conduit. The thermal vias will connect the exposed pad of the package to internal copper planes of the board. The number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package.

Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern.

The recommended thermal land design for NB100EP223 applications on multi-layer boards comprises a 4 X 4 thermal via array using a 1.2 mm pitch as shown in Figure 8 providing an efficient heat removal path.

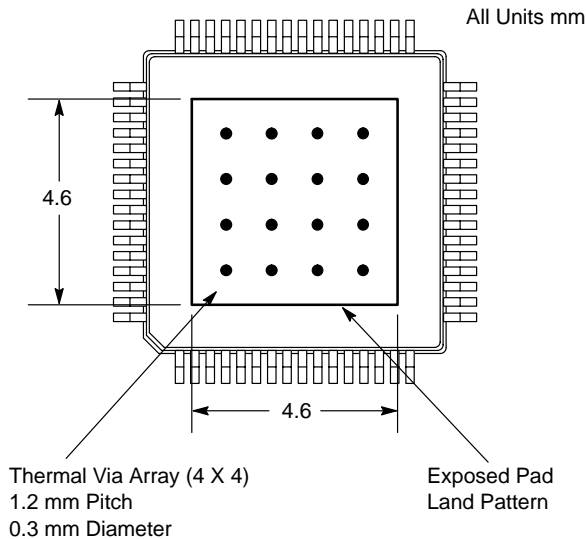


Figure 8. Recommended Thermal Land Pattern

The via diameter should be approximately 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via may result in voiding during the solder process and must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will

supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for the exposed pad package is equivalent to standard surface mount packages. Figure 9, “Recommended solder mask openings”, shows a recommended solder mask opening with respect to a 4 X 4 thermal via array. Because a large solder mask opening may result in a poor rework release, the opening should be subdivided as shown in Figure 9. For the nominal package standoff of 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

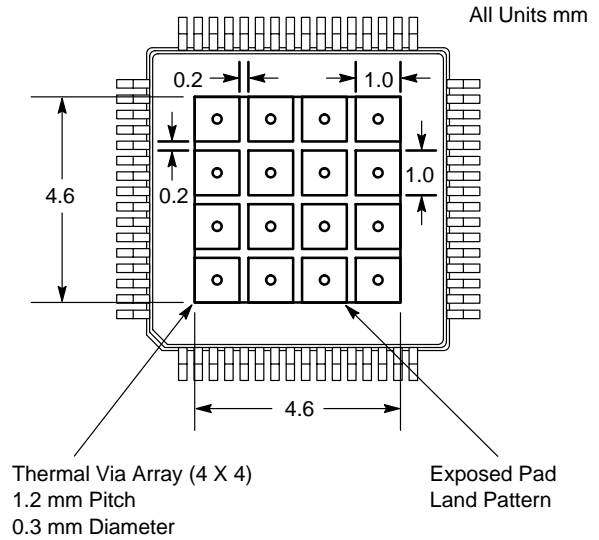


Figure 9. Recommended Solder Mask Openings

Proper thermal management is critical for reliable system operation. This is especially true for high-fanout and high output drive capability products.

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Table 9. Thermal Resistance *

| Ifpm | θ_{JA} °C/W | θ_{JC} °C/W |
|------|--------------------|--------------------|
| 0 | 35.6 | 3.2 |
| 100 | 32.8 | 4.9 |
| 500 | 30.0 | 6.4 |

* Junction to ambient and Junction to board, four-conductor layer test board (2S2P) per JESD 51-8

These recommendations are to be used as a guideline, only. It is therefore recommended that users employ sufficient thermal modeling analysis to assist in applying the general recommendations to their particular application to assure adequate thermal performance. The exposed pad of the NB100EP223 package is electrically shorted to the substrate of the integrated circuit and GND. The thermal land should be electrically connected to GND.

NB100EP223

ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------------|----------------------|--------------------|
| NB100EP223FAG | LQFP-64 (Pb-Free) | 160 Units / Tray |
| NB100EP223FAR2G | LQFP-64 (Pb-Free) | 1500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

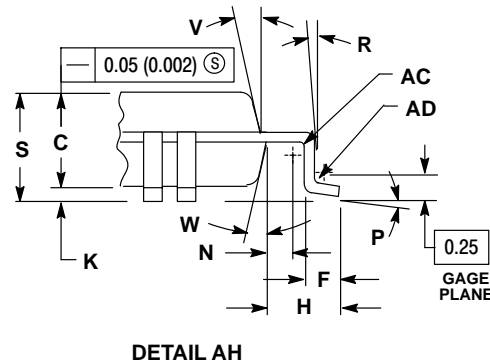
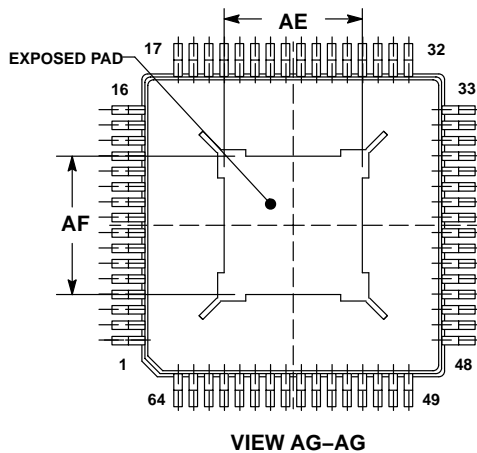
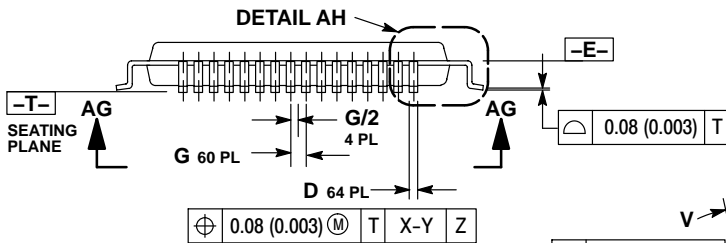
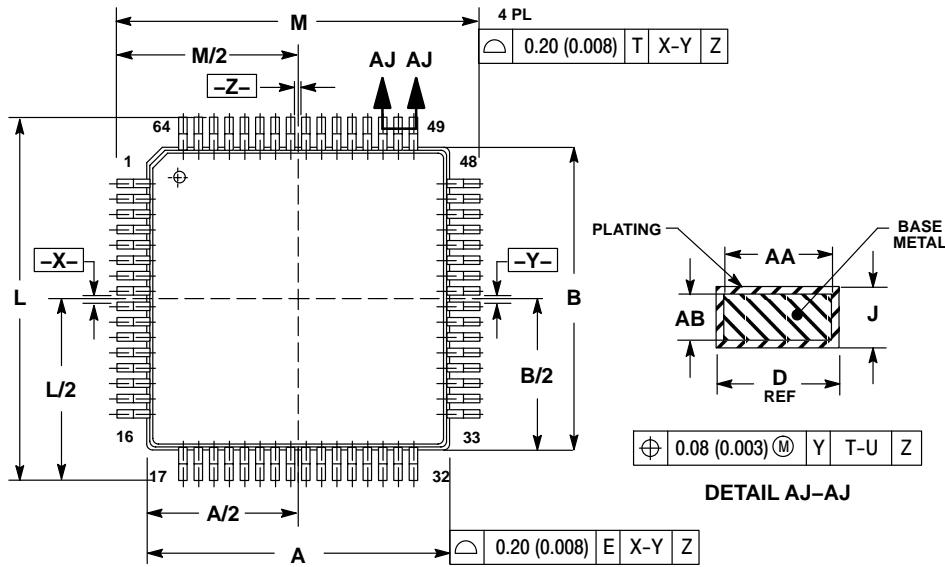
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

NB100EP223

PACKAGE DIMENSIONS

LQFP 64 LEAD EXPOSED PAD 848G-02 ISSUE A




NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MM.
- DATUM PLANE "E" IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING PLANE.
- DATUM "X", "Y" AND "Z" TO BE DETERMINED AT DATUM PLANE DATUM "E".
- DIMENSIONS M AND L TO BE DETERMINED AT SEATING PLANE DATUM "T".
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE "E".
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM D DIMENSION BY MORE THAN 0.08 (0.003). DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).
- EXACT SHAPE OF EACH CORNER IS OPTIONAL.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 10.00 BSC | --- | 0.394 BSC | --- |
| B | 10.00 BSC | --- | 0.394 BSC | --- |
| C | 1.35 | 1.45 | 0.053 | 0.057 |
| D | 0.17 | 0.27 | 0.007 | 0.011 |
| F | 0.45 | 0.75 | 0.018 | 0.030 |
| G | 0.50 BSC | --- | 0.020 BSC | --- |
| H | 1.00 REF | --- | 0.039 BSC | --- |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| K | 0.05 | 0.15 | 0.002 | 0.006 |
| L | 12.00 BSC | --- | 0.472 BSC | --- |
| M | 12.00 BSC | --- | 0.472 BSC | --- |
| N | 0.20 | --- | 0.008 | --- |
| P | 0 ° | 7 ° | 0 ° | 7 ° |
| R | 0 ° | --- | 0 ° | --- |
| S | --- | 1.60 | --- | 0.063 |
| V | 11 ° | 13 ° | 11 ° | 13 ° |
| W | 11 ° | 13 ° | 11 ° | 13 ° |
| AA | 0.17 | 0.23 | 0.007 | 0.009 |
| AB | 0.09 | 0.16 | 0.004 | 0.006 |
| AC | 0.08 | --- | 0.003 | --- |
| AD | 0.08 | --- | 0.003 | --- |
| AE | 4.50 | 4.78 | 0.180 | 0.188 |
| AF | 4.50 | 4.78 | 0.180 | 0.188 |

NB100EP223

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative