# PZT2222A

# NPN Silicon Planar Epitaxial Transistor

This NPN Silicon Epitaxial transistor is designed for use in linear and switching applications. The device is housed in the SOT−223 package which is designed for medium power surface mount applications.

### Features

- PNP Complement is PZT2907AT1
- The SOT−223 Package Can be Soldered Using Wave or Reflow
- SOT−223 Package Ensures Level Mounting, Resulting in Improved Thermal Conduction, and Allows Visual Inspection of Soldered Joints
- The Formed Leads Absorb Thermal Stress During Soldering, Eliminating the Possibility of Damage to the Die
- Available in 12 mm Tape and Reel
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant*

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector−Emitter Voltage | $V_{CEO}$ | 40 | Vdc |
| Collector−Base Voltage | $V_{CBO}$ | 75 | Vdc |
| Emitter−Base Voltage (Open Collector) | $V_{EBO}$ | 6.0 | Vdc |
| Collector Current | $I_C$ | 600 | mAdc |
| Total Power Dissipation up to $T_A$ = 25°C (Note 1) | $P_D$ | 1.5 | W |
| Storage Temperature Range | $T_{stg}$ | − 65 to +150 | °C |
| Junction Temperature | $T_J$ | 150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Device mounted on an epoxy printed circuit board 1.575 inches x 1.575 inches x 0.059 inches; mounting pad for the collector lead min. 0.93 inches$^2$.

### THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance, Junction−to−Ambient | $R_{\theta JA}$ | 83.3 | °C/W |
| Lead Temperature for Soldering, 0.0625″ from case<br>Time in Solder Bath | $T_L$ | 260<br>10 | °C<br>Sec |

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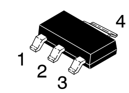
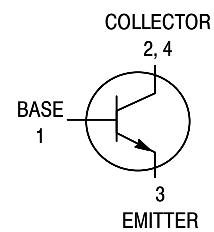
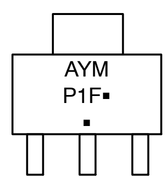
**SOT−223 PACKAGE**
**NPN SILICON TRANSISTOR**
**SURFACE MOUNT**




**SOT−223 (TO−261)**
**CASE 318E−04**
**STYLE 1**




### MARKING DIAGRAM




A = Assembly Location
Y = Year
M = Month Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| PZT2222AT1G | SOT−223 (Pb−Free) | 1,000 Tape & Reel |
| SPZT2222AT1G | SOT−223 (Pb−Free) | 1,000 Tape & Reel |
| PZT2222AT3G | SOT−223 (Pb−Free) | 4,000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



August, 2013 − Rev. 9
Publication Order Number:
PZT2222AT1/D

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector−Emitter Breakdown Voltage ($I_C$ = 10 mAdc, $I_B$ = 0) | | $V_{(BR)CEO}$ | 40 | – | Vdc |
| Collector−Base Breakdown Voltage ($I_C$ = 10 μAdc, $I_E$ = 0) | | $V_{(BR)CBO}$ | 75 | – | Vdc |
| Emitter−Base Breakdown Voltage ($I_E$ = 10 μAdc, $I_C$ = 0) | | $V_{(BR)EBO}$ | 6.0 | – | Vdc |
| Base−Emitter Cutoff Current ($V_{CE}$ = 60 Vdc, $V_{BE}$ = – 3.0 Vdc) | | $I_{BEX}$ | – | 20 | nAdc |
| Collector−Emitter Cutoff Current ($V_{CE}$ = 60 Vdc, $V_{BE}$ = – 3.0 Vdc) | | $I_{CEX}$ | – | 10 | nAdc |
| Emitter−Base Cutoff Current ($V_{EB}$ = 3.0 Vdc, $I_C$ = 0) | | $I_{EBO}$ | – | 100 | nAdc |
| Collector−Base Cutoff Current<br>($V_{CB}$ = 60 Vdc, $I_E$ = 0)<br>($V_{CB}$ = 60 Vdc, $I_E$ = 0, $T_A$ = 125°C) | | $I_{CBO}$ | <br>–<br>– | <br>10<br>10 | <br>nAdc<br>μAdc |
| **ON CHARACTERISTICS** | | | | | |
| DC Current Gain<br>($I_C$ = 0.1 mAdc, $V_{CE}$ = 10 Vdc)<br>($I_C$ = 1.0 mAdc, $V_{CE}$ = 10 Vdc)<br>($I_C$ = 10 mAdc, $V_{CE}$ = 10 Vdc)<br>($I_C$ = 10 mAdc, $V_{CE}$ = 10 Vdc, $T_A$ = – 55°C)<br>($I_C$ = 150 mAdc, $V_{CE}$ = 10 Vdc)<br>($I_C$ = 150 mAdc, $V_{CE}$ = 1.0 Vdc)<br>($I_C$ = 500 mAdc, $V_{CE}$ = 10 Vdc) | | $h_{FE}$ | <br>35<br>50<br>70<br>35<br>100<br>50<br>40 | <br>–<br>–<br>–<br>–<br>300<br>–<br>– | – |
| Collector−Emitter Saturation Voltages<br>($I_C$ = 150 mAdc, $I_B$ = 15 mAdc)<br>($I_C$ = 500 mAdc, $I_B$ = 50 mAdc) | | $V_{CE(sat)}$ | <br>–<br>– | <br>0.3<br>1.0 | Vdc |
| Base−Emitter Saturation Voltages<br>($I_C$ = 150 mAdc, $I_B$ = 15 mAdc)<br>($I_C$ = 500 mAdc, $I_B$ = 50 mAdc) | | $V_{BE(sat)}$ | <br>0.6<br>– | <br>1.2<br>2.0 | Vdc |
| Input Impedance<br>($V_{CE}$ = 10 Vdc, $I_C$ = 1.0 mAdc, f = 1.0 kHz)<br>($V_{CE}$ = 10 Vdc, $I_C$ = 10 mAdc, f = 1.0 kHz) | | $h_{ie}$ | <br>2.0<br>0.25 | <br>8.0<br>1.25 | kΩ |
| Voltage Feedback Ratio<br>($V_{CE}$ = 10 Vdc, $I_C$ = 1.0 mAdc, f = 1.0 kHz)<br>($V_{CE}$ = 10 Vdc, $I_C$ = 10 mAdc, f = 1.0 kHz) | | $h_{re}$ | <br>–<br>– | <br>$8.0x10^{-4}$<br>$4.0x10^{-4}$ | – |
| Small−Signal Current Gain<br>($V_{CE}$ = 10 Vdc, $I_C$ = 1.0 mAdc, f = 1.0 kHz)<br>($V_{CE}$ = 10 Vdc, $I_C$ = 10 mAdc, f = 1.0 kHz) | | $\|h_{fe}\|$ | <br>50<br>75 | <br>300<br>375 | – |
| Output Admittance<br>($V_{CE}$ = 10 Vdc, $I_C$ = 1.0 mAdc, f = 1.0 kHz)<br>($V_{CE}$ = 10 Vdc, $I_C$ = 10 mAdc, f = 1.0 kHz) | | $h_{oe}$ | <br>5.0<br>25 | <br>35<br>200 | μmhos |
| Noise Figure ($V_{CE}$ = 10 Vdc, $I_C$ = 100 μAdc, f = 1.0 kHz) | | F | – | 4.0 | dB |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Current−Gain – Bandwidth Product<br>($I_C$ = 20 mAdc, $V_{CE}$ = 20 Vdc, f = 100 MHz) | | $f_T$ | <br>300 | <br>– | MHz |
| Output Capacitance ($V_{CB}$ = 10 Vdc, $I_E$ = 0, f = 1.0 MHz) | | $C_c$ | – | 8.0 | pF |
| Input Capacitance ($V_{EB}$ = 0.5 Vdc, $I_C$ = 0, f = 1.0 MHz) | | $C_e$ | – | 25 | pF |
| **SWITCHING TIMES** ($T_A$ = 25°C) | | | | | |
| Delay Time | ($V_{CC}$ = 30 Vdc, $I_C$ = 150 mAdc,<br>$I_{B(on)}$ = 15 mAdc, $V_{EB(off)}$ = 0.5 Vdc)<br>Figure 1 | $t_d$ | – | 10 | ns |
| Rise Time | | $t_r$ | – | 25 | |
| Storage Time | ($V_{CC}$ = 30 Vdc, $I_C$ = 150 mAdc,<br>$I_{B(on)}$ = $I_{B(off)}$ = 15 mAdc)<br>Figure 2 | $t_s$ | – | 225 | ns |
| Fall Time | | $t_f$ | – | 60 | |

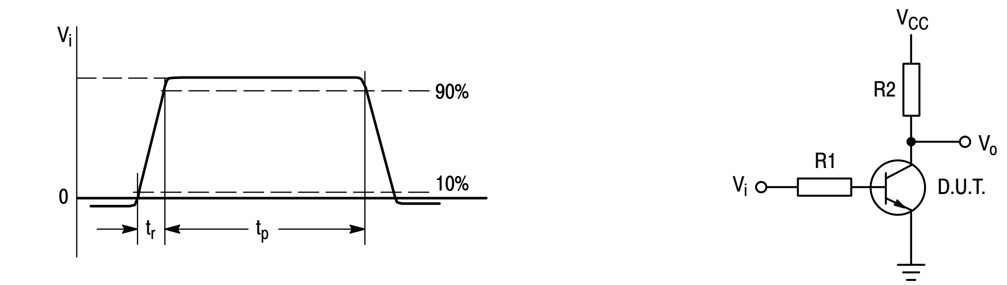



**Figure 1. Input Waveform and Test Circuit for Determining Delay Time and Rise Time**

**$V_i$ = – 0.5 V to +9.9 V, $V_{CC}$ = +30 V, R1 = 619 Ω, R2 = 200 Ω.**

| | | | | | | |
|---|---|---|---|---|---|---|
| **PULSE GENERATOR:** | | | | **OSCILLOSCOPE:** | | |
| **PULSE DURATION** | **$t_p$** | **3** | **200 ns** | **INPUT IMPEDANCE** | **$Z_i$** | **> 100 kΩ** |
| **RISE TIME** | **$t_r$** | **3** | **2 ns** | **INPUT CAPACITANCE** | **$C_i$** | **< 12 pF** |
| **DUTY FACTOR** | **δ** | **=** | **0.02** | **RISE TIME** | **$t_r$** | **< 5 ns** |

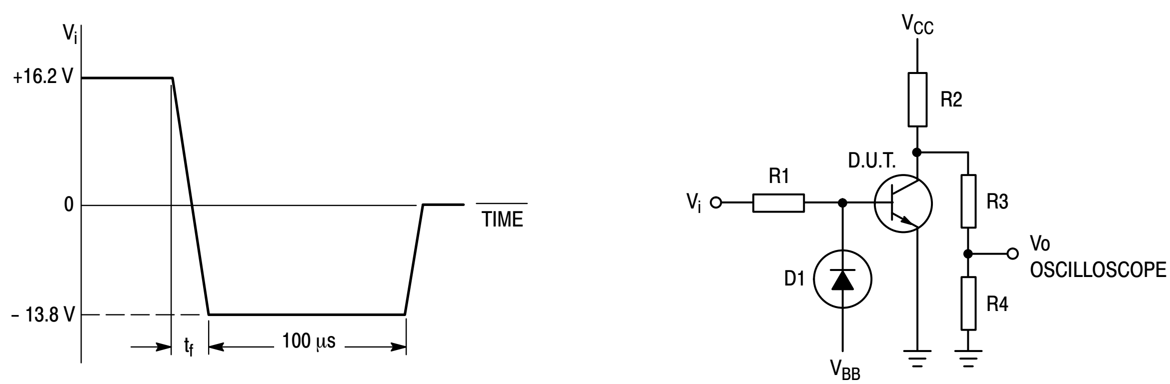



**Figure 2. Input Waveform and Test Circuit for Determining Storage Time and Fall Time**

## TYPICAL CHARACTERISTICS

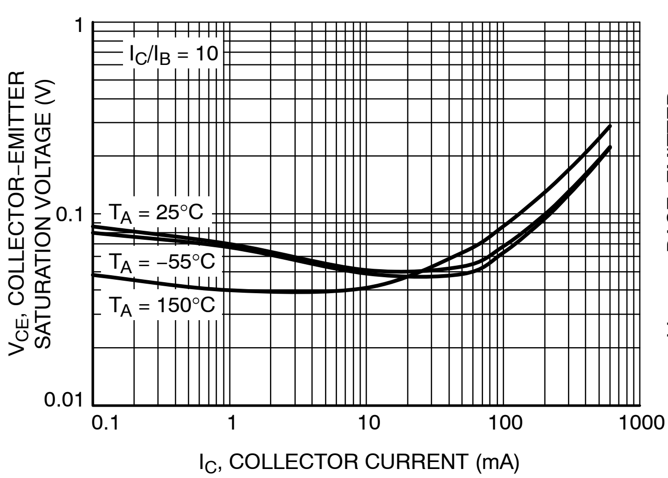



**Figure 3. Collector Emitter Saturation Voltage vs. Collector Current**

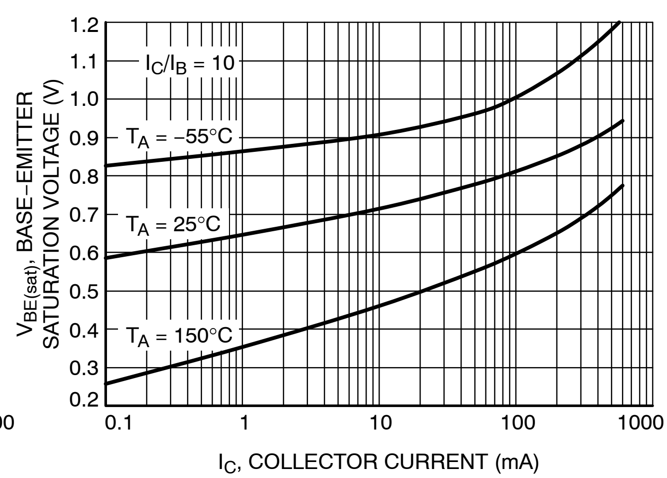



**Figure 4. Base Emitter Saturation Voltage vs. Collector Current**

## TYPICAL CHARACTERISTICS

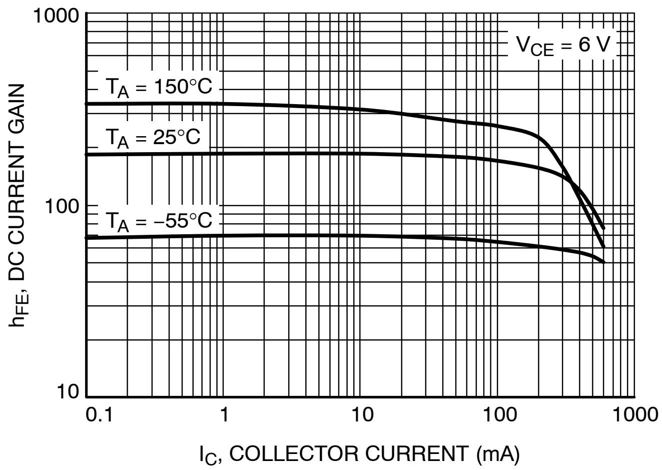



**Figure 5. DC Current Gain vs. Collector Current**

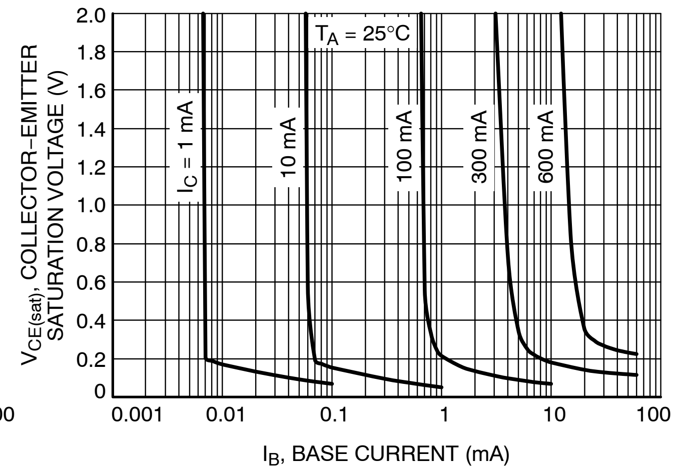



**Figure 6. Saturation Region**

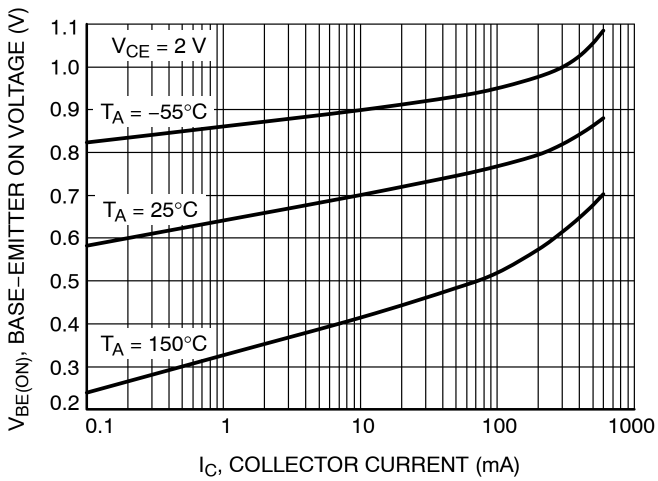



**Figure 7. Base−Emitter Turn−On Voltage vs. Collector Current**

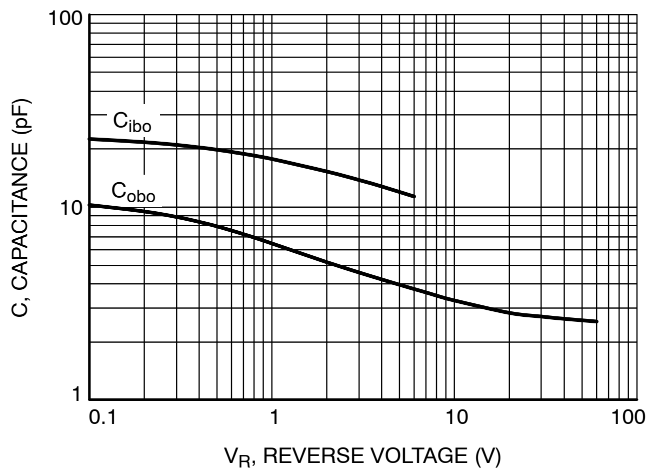



**Figure 8. Capacitance**

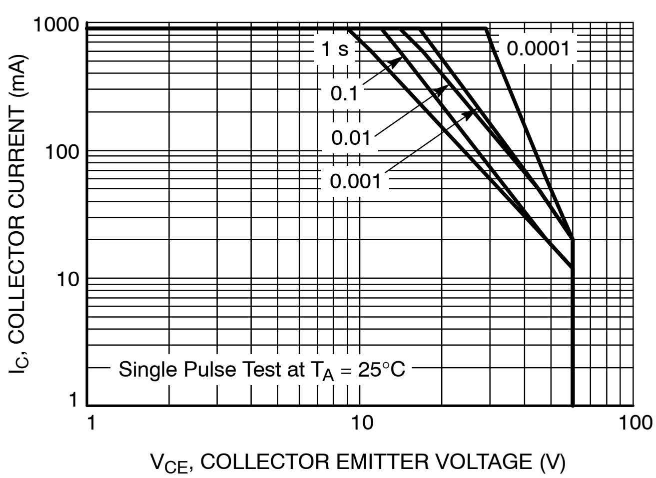
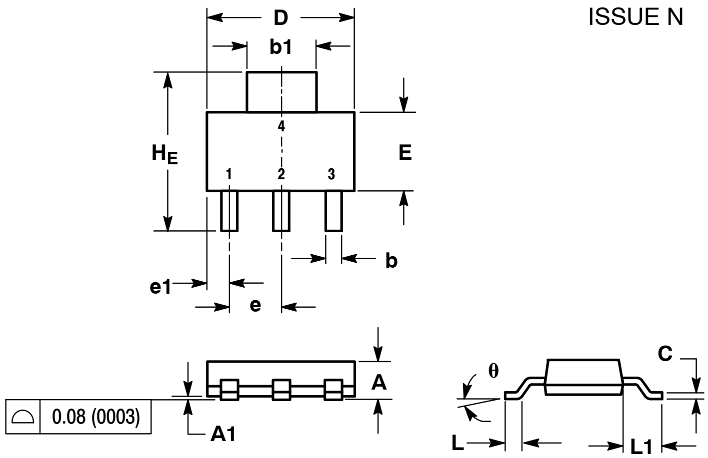



**Figure 9. Safe Operating Area**

## PACKAGE DIMENSIONS

**SOT−223 (TO−261)**
CASE 318E−04
ISSUE N

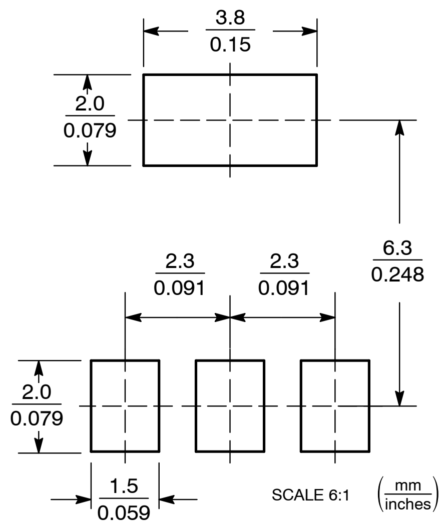



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| **DIM** | **MIN** | **NOM** | **MAX** | **MIN** | **NOM** | **MAX** |
| **A** | 1.50 | 1.63 | 1.75 | 0.060 | 0.064 | 0.068 |
| **A1** | 0.02 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| **b** | 0.60 | 0.75 | 0.89 | 0.024 | 0.030 | 0.035 |
| **b1** | 2.90 | 3.06 | 3.20 | 0.115 | 0.121 | 0.126 |
| **c** | 0.24 | 0.29 | 0.35 | 0.009 | 0.012 | 0.014 |
| **D** | 6.30 | 6.50 | 6.70 | 0.249 | 0.256 | 0.263 |
| **E** | 3.30 | 3.50 | 3.70 | 0.130 | 0.138 | 0.145 |
| **e** | 2.20 | 2.30 | 2.40 | 0.087 | 0.091 | 0.094 |
| **e1** | 0.85 | 0.94 | 1.05 | 0.033 | 0.037 | 0.041 |
| **L** | 0.20 | −−− | −−− | 0.008 | −−− | −−− |
| **L1** | 1.50 | 1.75 | 2.00 | 0.060 | 0.069 | 0.078 |
| **$H_E$** | 6.70 | 7.00 | 7.30 | 0.264 | 0.276 | 0.287 |
| **θ** | 0° | – | 10° | 0° | – | 10° |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

## SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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