# MC74LCX16244

# Low-Voltage CMOS 16-Bit Buffer

## With 5 V−Tolerant Inputs and Outputs (3−State, Non−Inverting)

The MC74LCX16244 is a high performance, non−inverting 16−bit buffer operating from a 2.3 to 3.6 V supply. The device is nibble controlled. Each nibble has separate Output Enable inputs which can be tied together for full 16−bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A $V_I$ specification of 5.5 V allows MC74LCX16244 inputs to be safely driven from 5.0 V devices. The MC74LCX16244 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

The 4.5 ns maximum propagation delays support high performance applications. Current drive capability is 24 mA at the outputs. The Output Enable ($\overline{OEn}$) inputs, when HIGH, disable the outputs by placing them in a HIGH Z condition.

The MC74LCX16244 contains sixteen non−inverting buffers with 3−state 5.0 V−tolerant outputs. The device is nibble controlled with each nibble functioning identically, but independently. The control pins may be tied together to obtain full 16−bit operation. The 3−state outputs are controlled by an Output Enable ($\overline{OEn}$) input for each nibble. When $\overline{OEn}$ is LOW, the outputs are on. When $\overline{OEn}$ is HIGH, the outputs are in the high impedance state.

### Features

- Designed for 2.3 V to 3.6 V $V_{CC}$ Operation
- 4.5 ns Maximum $t_{pd}$
- 5.0 V Tolerant − Interface Capability With 5.0 V TTL Logic
- Supports Live Insertion and Withdrawal
- $I_{OFF}$ Specification Guarantees High Impedance When $V_{CC}$ = 0 V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (20 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance:
  - Human Body Model >2000 V
  - Machine Model >200 V
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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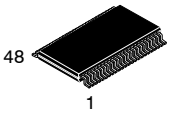
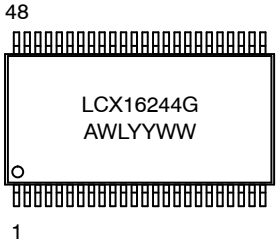



**TSSOP−48**
**DT SUFFIX**
**CASE 1201**

**MARKING DIAGRAM**




| | |
|---|---|
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

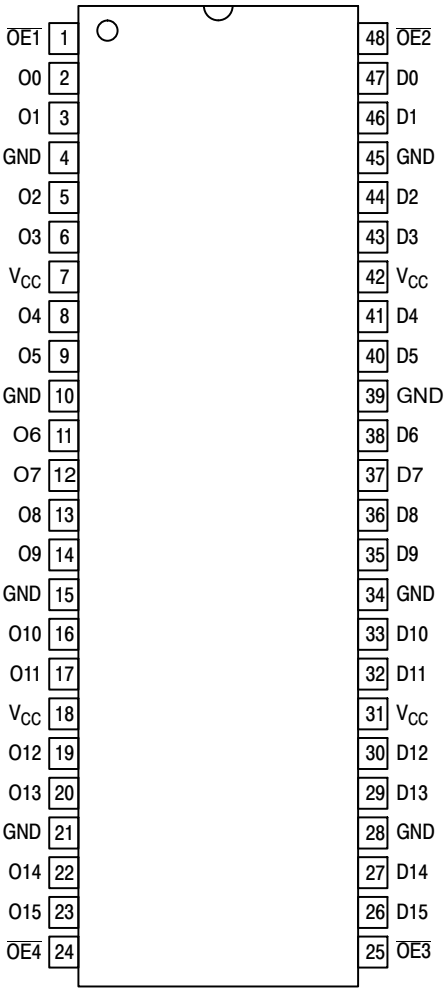



**Figure 1. Pinout: 48−Lead** (Top View)

**Table 1. PIN NAMES**

| Pins | Function |
|---|---|
| $\overline{OEn}$ | Output Enable Inputs |
| D0−D15 | Inputs |
| O0−O15 | Outputs |

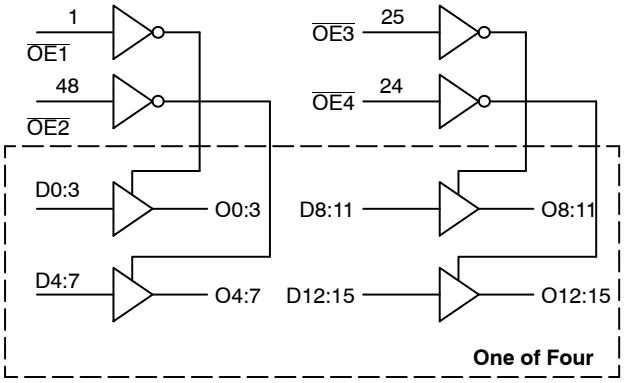



**Figure 2. Logic Diagram**

**TRUTH TABLE**

| $\overline{OE1}$ | D0:3 | O0:3 | $\overline{OE2}$ | D4:7 | O4:7 | $\overline{OE3}$ | D8:11 | O8:11 | $\overline{OE4}$ | D12:15 | O12:15 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| L | L | L | L | L | L | L | L | L | L | L | L |
| L | H | H | L | H | H | L | H | H | L | H | H |
| H | X | Z | H | X | Z | H | X | Z | H | X | Z |

H = High Voltage Level
L = Low Voltage Level
Z = High Impedance State
X = High or Low Voltage Level and Transitions Are Acceptable; for $I_{CC}$ reasons, DO NOT FLOAT Inputs.

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC74LCX16244DTG | TSSOP−48<br>(Pb−Free) | 39 Units / Rail |
| M74LCX16244DTR2G | TSSOP−48<br>(Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MAXIMUM RATINGS

| Symbol | Parameter | Value | Condition | Units |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | −0.5 to +7.0 | | V |
| $V_I$ | DC Input Voltage | $-0.5 \le V_I \le +7.0$ | | V |
| $V_O$ | DC Output Voltage | $-0.5 \le V_O \le +7.0$ | Output in 3−State | V |
| | | $-0.5 \le V_O \le V_{CC} + 0.5$ | Output in HIGH or LOW State (Note 1) | V |
| $I_{IK}$ | DC Input Diode Current | −50 | $V_I$ < GND | mA |
| $I_{OK}$ | DC Output Diode Current | −50 | $V_O$ < GND | mA |
| | | +50 | $V_O > V_{CC}$ | mA |
| $I_O$ | DC Output Source/Sink Current | ±50 | | mA |
| $I_{CC}$ | DC Supply Current Per Supply Pin | ±100 | | mA |
| $I_{GND}$ | DC Ground Current Per Ground Pin | ±100 | | mA |
| $T_{STG}$ | Storage Temperature Range | −65 to +150 | | °C |
| MSL | Moisture Sensitivity | | Level 1 | |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. $I_O$ absolute maximum rating must be observed.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage<br>Operating<br>Data Retention Only | <br>2.0<br>1.5 | <br>2.5, 3.3<br>2.5, 3.3 | <br>3.6<br>3.6 | V |
| $V_I$ | Input Voltage | 0 | | 5.5 | V |
| $V_O$ | Output Voltage<br>(HIGH or LOW State)<br>(3−State) | <br>0<br>0 | | <br>$V_{CC}$<br>5.5 | V |
| $I_{OH}$ | HIGH Level Output Current<br>$V_{CC}$ = 3.0 V − 3.6 V<br>$V_{CC}$ = 2.7 V − 3.0 V<br>$V_{CC}$ = 2.3 V − 2.7 V | | | <br>−24<br>−12<br>−8 | mA |
| $I_{OL}$ | LOW Level Output Current<br>$V_{CC}$ = 3.0 V − 3.6 V<br>$V_{CC}$ = 2.7 V − 3.0 V<br>$V_{CC}$ = 2.3 V − 2.7 V | | | <br>+24<br>+12<br>+8 | mA |
| $T_A$ | Operating Free−Air Temperature | −40 | | +85 | °C |
| $\Delta t/\Delta V$ | Input Transition Rise or Fall Rate, $V_{IN}$ from 0.8 V to 2.0 V, $V_{CC}$ = 3.0 V | 0 | | 10 | ns/V |

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Characteristic | Condition | $T_A$ = −40°C to +85°C | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage (Note 2) | 2.3 V ≤ $V_{CC}$ ≤ 2.7 V | 1.7 | | V |
| | | 2.7 V ≤ $V_{CC}$ ≤ 3.6 V | 2.0 | | |
| $V_{IL}$ | LOW Level Input Voltage (Note 2) | 2.3 V ≤ $V_{CC}$ ≤ 2.7 V | | 0.7 | V |
| | | 2.7 V ≤ $V_{CC}$ ≤ 3.6 V | | 0.8 | |
| $V_{OH}$ | HIGH Level Output Voltage | 2.3 V ≤ $V_{CC}$ ≤ 3.6 V; $I_{OL}$ = 100 μA | $V_{CC}$ − 0.2 | | V |
| | | $V_{CC}$ = 2.3 V; $I_{OH}$ = −8 mA | 1.8 | | |
| | | $V_{CC}$ = 2.7 V; $I_{OH}$ = −12 mA | 2.2 | | |
| | | $V_{CC}$ = 3.0 V; $I_{OH}$ = −18 mA | 2.4 | | |
| | | $V_{CC}$ = 3.0 V; $I_{OH}$ = −24 mA | 2.2 | | |
| $V_{OL}$ | LOW Level Output Voltage | 2.3 V ≤ $V_{CC}$ ≤ 3.6 V; $I_{OL}$ = 100 μA | | 0.2 | V |
| | | $V_{CC}$ = 2.3 V; $I_{OL}$ = 8 mA | | 0.6 | |
| | | $V_{CC}$ = 2.7 V; $I_{OL}$ = 12 mA | | 0.4 | |
| | | $V_{CC}$ = 3.0 V; $I_{OL}$ = 16 mA | | 0.4 | |
| | | $V_{CC}$ = 3.0 V; $I_{OL}$ = 24 mA | | 0.55 | |
| $I_{OZ}$ | 3−State Output Current | $V_{CC}$ = 3.6 V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{OUT}$ = 0 to 5.5 V | | ±5 | μA |
| $I_{OFF}$ | Power Off Leakage Current | $V_{CC}$ = 0, $V_{IN}$ = 5.5 V or $V_{OUT}$ = 5.5 V | | 10 | μA |
| $I_{IN}$ | Input Leakage Current | $V_{CC}$ = 3.6 V, $V_{IN}$ = 5.5 V or GND | | ±5 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_{CC}$ = 3.6 V, $V_{IN}$ = 5.5 V or GND | | 10 | μA |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | 2.3 ≤ $V_{CC}$ ≤ 3.6 V; $V_{IH}$ = $V_{CC}$ − 0.6 V | | 500 | μA |

2. These values of $V_I$ are used to test DC electrical characteristics only.

## AC CHARACTERISTICS ($t_R$ = $t_F$ = 2.5 ns; $R_L$ = 500 Ω)

| Symbol | Parameter | Waveform | $T_A$ = −40°C to +85°C | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V, $C_L$ = 50 pF | | $V_{CC}$ = 2.7 V, $C_L$ = 50 pF | | $V_{CC}$ = 2.5 V ± 0.2 V, $C_L$ = 30 pF | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Input to Output | 1 | 1.5<br>1.5 | 4.5<br>4.5 | 1.5<br>1.5 | 5.2<br>5.2 | 1.5<br>1.5 | 5.4<br>5.4 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time to<br>High and Low Level | 2 | 1.5<br>1.5 | 5.5<br>5.5 | 1.5<br>1.5 | 6.3<br>6.3 | 1.5<br>1.5 | 7.2<br>7.2 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time From<br>High and Low Level | 2 | 1.5<br>1.5 | 5.4<br>5.4 | 1.5<br>1.5 | 5.7<br>5.7 | 1.5<br>1.5 | 6.5<br>6.5 | ns |
| $t_{OSHL}$<br>$t_{OSLH}$ | Output−to−Output Skew<br>(Note 3) | | | 1.0<br>1.0 | | | | | ns |

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW ($t_{OSHL}$) or LOW−to−HIGH ($t_{OSLH}$); parameter guaranteed by design.

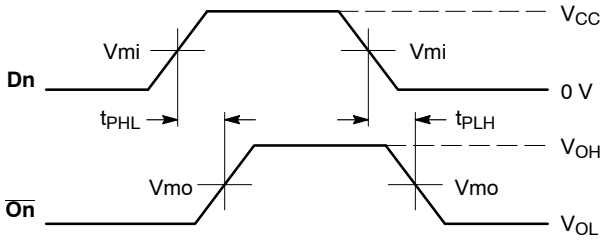
## DYNAMIC SWITCHING CHARACTERISTICS

| Symbol | Characteristic | Condition | $T_A$ = +25°C | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OLP}$ | Dynamic LOW Peak Voltage (Note 4) | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V<br>$V_{CC}$ = 2.5 V, $C_L$ = 30 pF, $V_{IH}$ = 2.5 V, $V_{IL}$ = 0 V | | 0.8<br>0.6 | | V |
| $V_{OLV}$ | Dynamic LOW Valley Voltage (Note 4) | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V<br>$V_{CC}$ = 2.5 V, $C_L$ = 30 pF, $V_{IH}$ = 2.5 V, $V_{IL}$ = 0 V | | −0.8<br>−0.6 | | V |

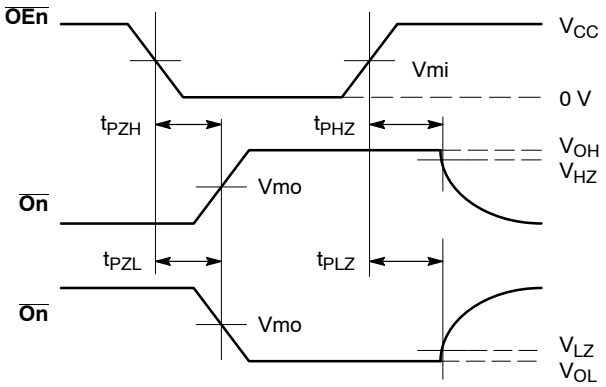
4. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the LOW state.

## CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Condition | Typical | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 8 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | 10 MHz, $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 20 | pF |




**WAVEFORM 1 – PROPAGATION DELAYS**
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; $t_W$ = 500 ns




**WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES**
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; $t_W$ = 500 ns

**Figure 3. AC Waveforms**

**Table 2. AC WAVEFORMS**

| Symbol | $V_{CC}$ | | |
|---|---|---|---|
| | **3.3 V ± 0.3 V** | **2.7 V** | **2.5 V ± 0.2 V** |
| Vmi | 1.5 V | 1.5 V | $V_{CC}$ / 2 |
| Vmo | 1.5 V | 1.5 V | $V_{CC}$ / 2 |
| $V_{HZ}$ | $V_{OL}$ + 0.3 V | $V_{OL}$ + 0.3 V | $V_{OL}$ + 0.15 V |
| $V_{LZ}$ | $V_{OH}$ − 0.3 V | $V_{OH}$ − 0.3 V | $V_{OH}$ − 015 V |

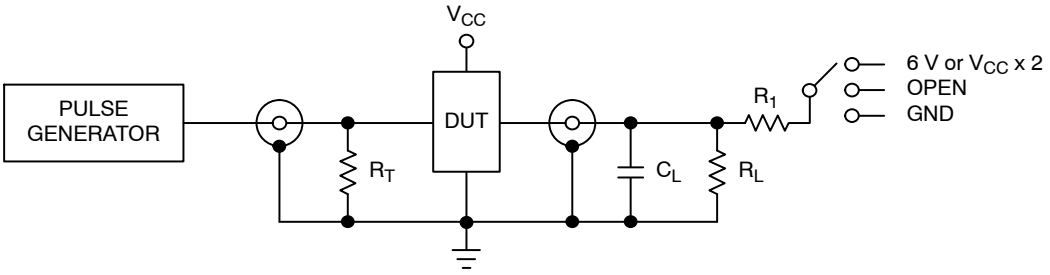



**Figure 4. Test Circuit**

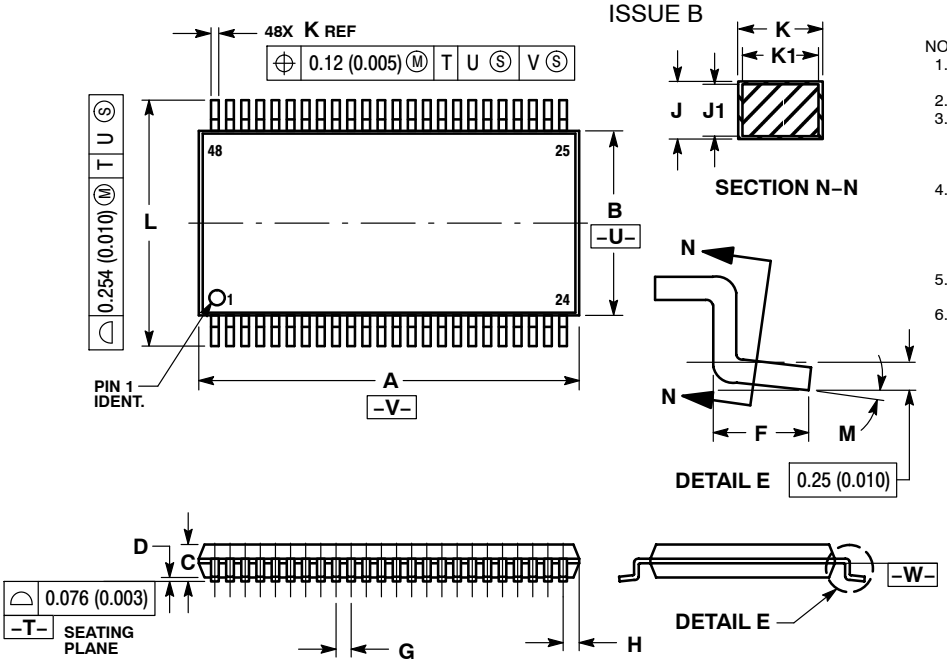
**Table 3. TEST CIRCUIT**

| Test | Switch |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | 6 V at $V_{CC}$ = 3.3 ± 0.3 V<br>6 V at $V_{CC}$ = 2.5 ± 0.2 V |
| Open Collector/Drain $t_{PLH}$ and $t_{PHL}$ | 6 V |
| $t_{PZH}$, $t_{PHZ}$ | GND |

$C_L$ = 50 pF at $V_{CC}$ = 3.3 ± 0.3 V or equivalent (includes jig and probe capacitance)
$C_L$ = 30 pF at $V_{CC}$ = 2.5 ± 0.2 V or equivalent (includes jig and probe capacitance)
$R_L$ = $R_1$ = 500 Ω or equivalent
$R_T$ = $Z_{OUT}$ of pulse generator (typically 50 Ω)

## PACKAGE DIMENSIONS

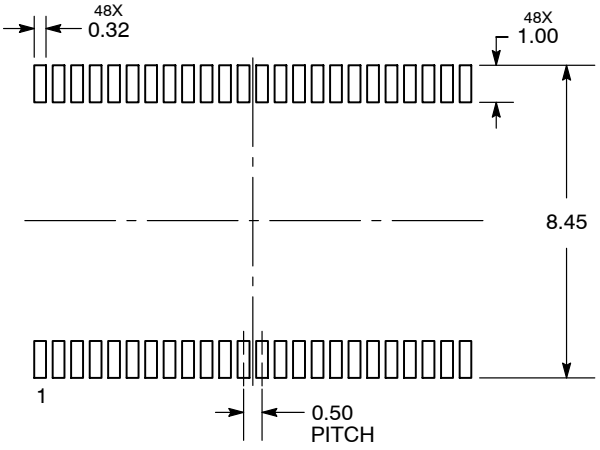
**TSSOP−48**
**DT SUFFIX**
CASE 1201
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 12.40 | 12.60 | 0.488 | 0.496 |
| B | 6.00 | 6.20 | 0.236 | 0.244 |
| C | −−− | 1.10 | −−− | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.50 BSC | | 0.0197 BSC | |
| H | 0.37 | −−− | 0.015 | −−− |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.17 | 0.27 | 0.007 | 0.011 |
| K1 | 0.17 | 0.23 | 0.007 | 0.009 |
| L | 7.95 | 8.25 | 0.313 | 0.325 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

## RECOMMENDED SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS



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