# 2-Input NAND Schmitt-Trigger

The MC74VHC1G132 is a single gate CMOS Schmitt NAND trigger fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The MC74VHC1G132 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC1G132 to be used to interface 5 V circuits to 3 V circuits.

The MC74VHC1G132 can be used to enhance noise immunity or to square up slowly changing waveforms.

#### **Features**

- High Speed:  $t_{PD} = 3.6 \text{ ns}$  (Typ) at  $V_{CC} = 5 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 1.0 \mu A$  (Max) at  $T_A = 25^{\circ}C$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 68; Equivalent Gates = 16
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

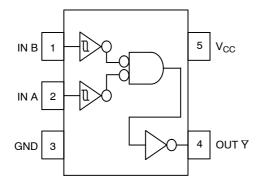


Figure 1. Pinout (Top View)



Figure 2. Logic Symbol



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# MARKING DIAGRAMS



SC-88A / SOT-353 / SC-70 DF SUFFIX CASE 419A





TSOP-5 / SOT-23 / SC-59 DT SUFFIX CASE 483



VD = Device Code
M = Date Code\*
■ = Pb-Free Package

(Note: Microdot may be in either location)
\*Date Code orientation and/or position may vary
depending upon manufacturing location.

PIN ASSIGNMENT				
1	IN B			
2	IN A			
3	GND			
4	OUT ₹			
5	V <sub>CC</sub>			

#### **FUNCTION TABLE**

Inp	uts	Output
Α	В	Y
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

#### **MAXIMUM RATINGS**

Symbol		Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage		-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage		-0.5 to +7.0	V
V <sub>OUT</sub>	DC Output Voltage		-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	DC Input Diode Current		-20	mA
lok	DC Output Diode Current		±20	mA
l <sub>OUT</sub>	DC Output Sink Current		± 12.5	mA
I <sub>CC</sub>	DC Supply Current per Supply Pin		±25	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C	
TL	Lead Temperature, 1 mm from Case	260	°C	
TJ	Junction Temperature Under Bias		+ 150	°C
θJA	Thermal Resistance	SC70-5/SC-88A (Note 1) TSOP-5	350 230	°C/W
P <sub>D</sub>	Power Dissipation in Still Air at 85°C	SC70-5/SC-88A TSOP-5	150 200	mW
MSL	Moisture Sensitivity		Level 1	
F <sub>R</sub>	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V <sub>ESD</sub>	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
I <sub>LATCHUP</sub>	Latchup Performance	Above V <sub>CC</sub> and Below GND at 125°C (Note 5)	±500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
- 2. Tested to EIA/JESD22-A114-A.
- 3. Tested to EIA/JESD22-A115-A.
- 4. Tested to JESD22-C101-A.
- 5. Tested to EIA/JESD78.

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter			Max	Unit
V <sub>CC</sub>	DC Supply Voltage		2.0	5.5	V
V <sub>IN</sub>	DC Input Voltage	0.0	5.5	V	
V <sub>OUT</sub>	DC Output Voltage		0.0	$V_{CC}$	V
T <sub>A</sub>	Operating Temperature Range		- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time $ V_{CC} = 3.5 \\ V_{CC} = 5.0 $	3 V ± 0.3 V 0 V ± 0.5 V	-	No Limit No Limit	ns/V

# Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

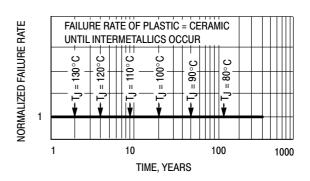


Figure 3. Failure Rate vs. Time Junction Temperature

# DC ELECTRICAL CHARACTERISTICS

			v <sub>cc</sub>	Т	A = 25°	С	<b>T</b> <sub>A</sub> ≤	85°C	-55 ≤ T <sub>A</sub>	≤ 125°C	
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V <sub>T+</sub>	Positive Threshold Voltage		3.0 4.5 5.5	1.50 2.35 2.80	1.88 2.66 3.21	2.25 3.10 3.70	1.50 2.35 2.80	2.25 3.10 3.70	1.50 2.35 2.80	2.25 3.10 3.70	٧
V <sub>T-</sub>	Negative Threshold Voltage		3.0 4.5 5.5	0.65 1.10 1.45	1.03 1.62 2.02	1.40 2.10 2.60	0.65 1.10 1.45	1.40 2.10 2.60	0.65 1.10 1.45	1.40 2.10 2.60	٧
V <sub>H</sub>	Hysteresis Voltage		3.0 4.5 5.5	0.30 0.40 0.50	0.85 1.05 1.20	1.60 2.00 2.25	0.30 0.40 0.50	1.60 2.00 2.25	0.30 0.40 0.50	1.60 2.00 2.25	V
V <sub>OH</sub>	Minimum High-Level	V <sub>IN</sub> = V <sub>CC</sub> or GND	2.0	1.9	2.0		1.9		1.9		V
	Output Voltage I <sub>OH</sub> = -50μA	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.5		
		$I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		٧
V <sub>OL</sub>	Maximum Low-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50  \mu\text{A}$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μΑ
Icc	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			1.0		20		40	μΑ

# AC ELECTRICAL CHARACTERISTICS $C_{load}$ = 50 pF, Input $t_r/t_f$ = 3.0 ns

			T	A = 25°	С	T <sub>A</sub> ≤	85°C	-55 ≤ T <sub>A</sub>	≤ 125°C	
Symbol	Parameter	Test Conditions	Min	Тур	Max	Min	Max	Min	Max	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A or B to $\overline{Y}$	$V_{CC} = 3.3 \pm 0.3 \ V  \begin{array}{c} C_L = 15 \ pF \\ C_L = 50 \ pF \end{array}$		4.6 6.1	11.9 15.4	1.0 1.0	14.0 17.5	1.0 1.0	16.1 19.6	ns
		$V_{CC} = 5.0 \pm 0.5 \text{ V}  \begin{array}{c} C_L = 15 \text{ pF} \\ C_L = 50 \text{ pF} \end{array}$		3.6 4.3	7.7 9.7	1.0 1.0	9.0 11.0	1.0 1.0	10.3 12.3	
C <sub>IN</sub>	Maximum Input Capacit- ance			5.5	10		10		10	pF

		Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
$C_{PD}$	Power Dissipation Capacitance (Note 6)	11	pF

<sup>6.</sup> C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>. C<sub>PD</sub> is used to determine the no–load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

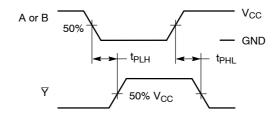
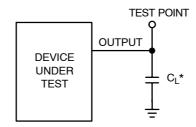


Figure 4. Switching Waveforms



<sup>\*</sup>Includes all probe and jig capacitance

Figure 5. Test Circuit

# **ORDERING INFORMATION**

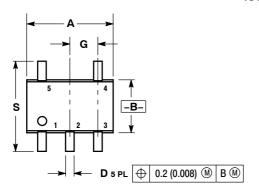
Device	Package	Shipping <sup>†</sup>
M74VHC1G132DFT1G		
NLVVHC1G132DFT1G*	SC70-5/SC-88A/SOT-353	
M74VHC1G132DFT2G	(Pb-Free)	3000 Units / Tape & Reel
NLVVHC1G132DFT2G*		3000 Offits / Tape & neer
M74VHC1G132DTT1G	SOT23-5/TSOP-5SC59-5	
NLVVHC1G132DTT1G*	(Pb-Free)	

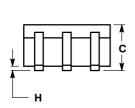
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

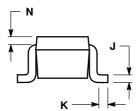
<sup>\*</sup>NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# **PACKAGE DIMENSIONS**

# SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE L



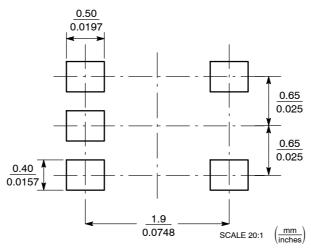




- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
  4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

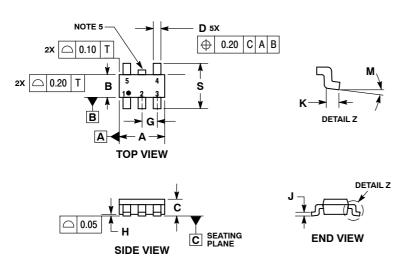
	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.071	0.087	1.80	2.20
В	0.045	0.053	1.15	1.35
С	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026	BSC	0.65	BSC
Н		0.004		0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20	REF
S	0.079	0.087	2.00	2.20

## **SOLDER FOOTPRINT**



#### PACKAGE DIMENSIONS

## TSOP-5 CASE 483-02 ISSUE K



#### NOTES

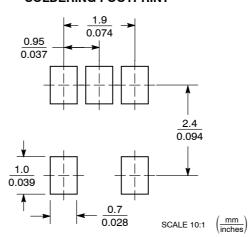
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS.
- 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
- MINIMUM THICKNESS OF BASE MATERIAL.

  4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE DIMENSION A
- EXCEED 0.15 PER SIDE. DIMENSION A.

  5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2

	MILLIMETERS				
DIM	MIN	MAX			
Α	3.00	BSC			
В	1.50	BSC			
C	0.90	1.10			
D	0.25	0.50			
G	0.95	BSC			
Ξ	0.01	0.10			
J	0.10	0.26			
K	0.20	0.60			
М	0 °	10 °			
s	2.50	3.00			

#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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