PCA9549

Octal bus switch with individually I²C-bus controlled enables

Rev. 02 — 13 July 2009 Product data sheet

1. General description

The PCA9549 provides eight bits of high speed TTL-compatible bus switching controlled by the I²C-bus. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay. Any individual A to B channel or combination of channels can be selected via the I²C-bus, determined by the contents of the programmable Control register. When the I²C-bus bit is HIGH (logic 1), the switch is on and data can flow from Port A to Port B, or vice versa. When the I²C-bus bit is LOW (logic 0), the switch is open, creating a high-impedance state between the two ports, which stops the data flow.

An active LOW reset input ($\overline{\text{RESET}}$) allows the PCA9549 to recover from a situation where the I²C-bus is stuck in a LOW state. Pulling the $\overline{\text{RESET}}$ pin LOW resets the I²C-bus state machine and causes all the bits to be open, as does the internal power-on reset function.

Three address pins allow up to eight devices on the same bus.

2. Features

- 8-bit bus switch (CBT)
- 5 Ω switch connection between two ports
- I²C-bus interface logic; compatible with SMBus standards
- Active LOW $\overline{\text{RESET}}$ input
- 3 address pins allowing up to 8 devices on the I²C-bus
- Bit selection via I²C-bus, in any combination
- Power-up with all bits deselected
- Low R_{on} switches
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO24, TSSOP24, HVQFN24

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA9549D	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
PCA9549PW	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
PCA9549BS	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-1

3.1 Ordering options

Table 2. Ordering options

Type number	Topside mark	Temperature range
PCA9549D	PCA9549D	–40 °C to +85 °C
PCA9549PW	PCA9549	–40 °C to +85 °C
PCA9549BS	9549	–40 °C to +85 °C

4. Block diagram

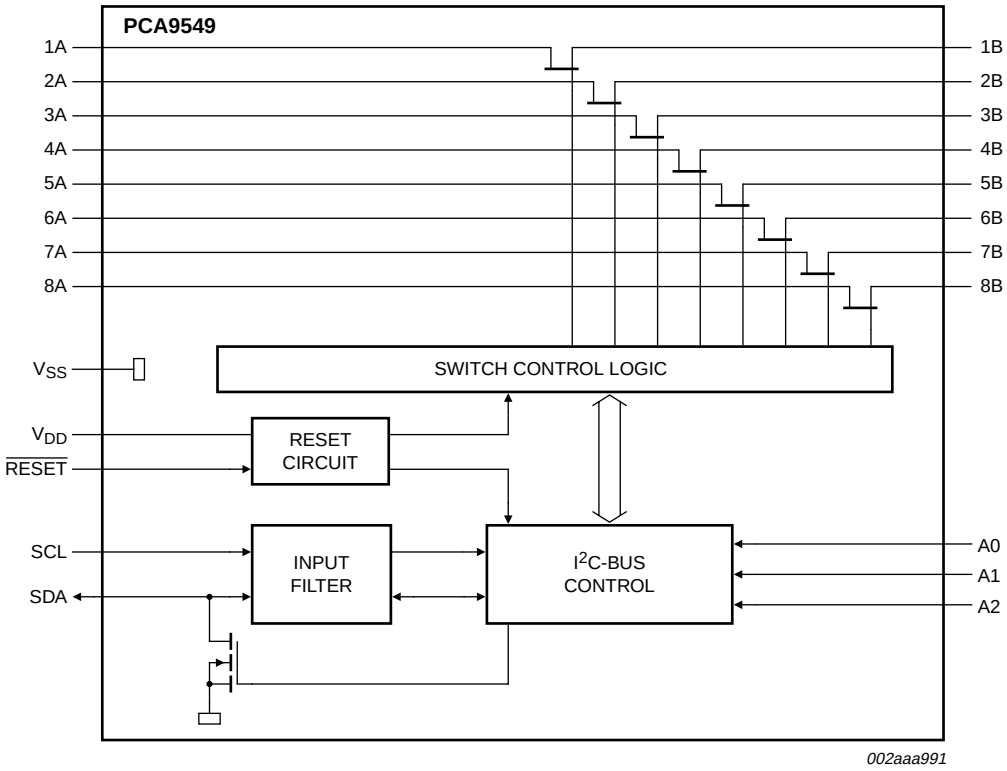


Fig 1. Block diagram

5. Pinning information

5.1 Pinning

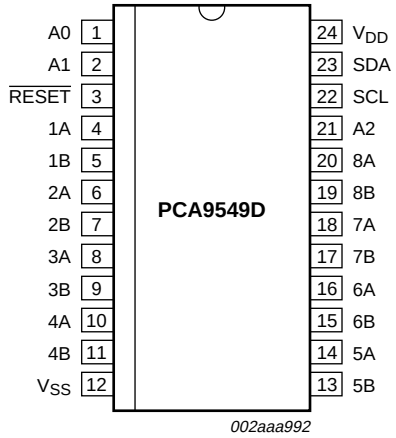


Fig 2. Pin configuration of SO24

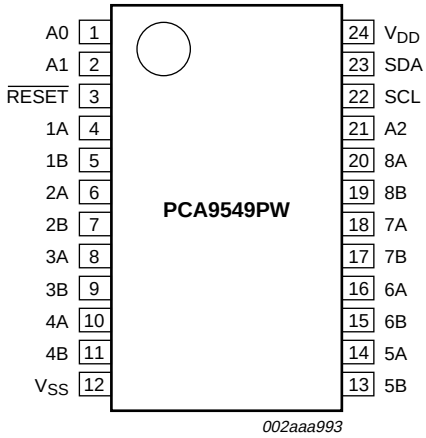
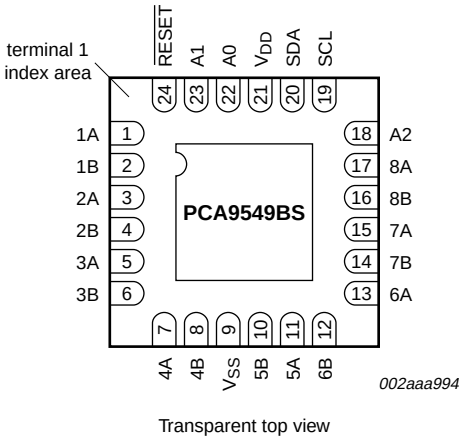


Fig 3. Pin configuration of TSSOP24



Transparent top view

Fig 4. Pin configuration of HVQFN24 (transparent top view)

5.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SO24, TSSOP24	HVQFN24	
A0	1	22	address input 0
A1	2	23	address input 1
$\overline{\text{RESET}}$	3	24	active LOW reset input
1A	4	1	input
1B	5	2	output
2A	6	3	input
2B	7	4	output
3A	8	5	input
3B	9	6	output
4A	10	7	input
4B	11	8	output
V_{SS}	12	9[1]	supply ground
5B	13	10	output
5A	14	11	input
6B	15	12	output
6A	16	13	input
7B	17	14	output
7A	18	15	input
8B	19	16	output
8A	20	17	input
A2	21	18	address input 2
SCL	22	19	serial clock line
SDA	23	20	serial data line
V_{DD}	24	21	supply voltage

[1] HVQFN24 package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

6. Functional description

6.1 Device addressing

Following a START condition, the bus master must output the address of the slave it is accessing. The address of the PCA9549 is shown in Figure 5. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

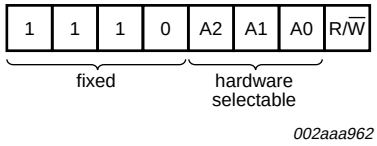


Fig 5. Slave address

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

6.2 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9549, which will be stored in the Control register. If multiple bytes are received by the PCA9549, it will save the last byte received. This register can be written and read via the I²C-bus.

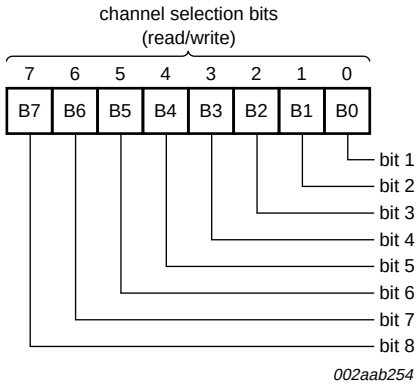


Fig 6. Control register

6.2.1 Control register definition

One or several bits are selected by the contents of the Control register. This register is written after the PCA9549 has been addressed. The entire control byte is used to determine which bit is to be selected. When a bit is selected to close, the bit will close after the Acknowledge has been placed on the I²C-bus.

Table 4. Control register

Write = channel selection; read = channel status.

B7	B6	B5	B4	B3	B2	B1	B0	Command
X	X	X	X	X	X	X	0	bit 1 disabled
							1	bit 1 enabled
X	X	X	X	X	X	0	X	bit 2 disabled
						1		bit 2 enabled
X	X	X	X	X	0	X	X	bit 3 disabled
					1			bit 3 enabled
X	X	X	X	0	X	X	X	bit 4 disabled
				1				bit 4 enabled
X	X	X	0	X	X	X	X	bit 5 disabled
			1					bit 5 enabled
X	X	0	X	X	X	X	X	bit 6 disabled
		1						bit 6 enabled
X	0	X	X	X	X	X	X	bit 7 disabled
	1							bit 7 enabled
0	X	X	X	X	X	X	X	bit 8 disabled
1								bit 8 enabled

[1] Several bits can be enabled at the same time. For example, B7 = 0, B6 = 1, B5 = 0, B4 = 0, B3 = 1, B2 = 1, B1 = 0, B0 = 0, means that bit 8, bit 6, bit 5, bit 2, and bit 1 are disabled and bit 7, bit 4, and bit 3 are enabled.

6.3 $\overline{\text{RESET}}$ input

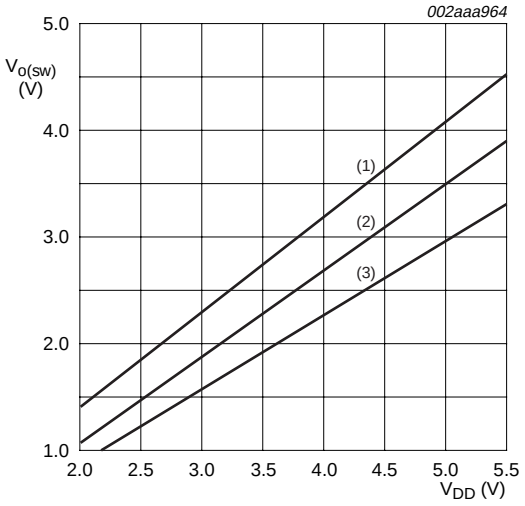
The $\overline{\text{RESET}}$ input is an active LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of $t_{w(rst)L}$, the PCA9549 will reset its registers and I²C-bus state machine and will open all bits. The $\overline{\text{RESET}}$ input must be connected to V_{DD} through a pull-up resistor.

6.4 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9549 in a reset state until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9549 registers and I²C-bus state machine are initialized to their default states, all zeroes causing all the bits to be open (high-impedance state).

6.5 CBT characteristic over V_{DD} range

The bus switch is optimized at 5.0 V but can operate over the entire supply range with lower $V_{o(sw)}$ voltage and higher gate resistance.



(1) maximum.
(2) typical.
(3) minimum.

Fig 7. $V_{o(sw)}$ voltage versus V_{DD}

Figure 7 shows the voltage characteristics of the pass gate transistors (note that the PCA9549 is only tested at the points specified in Section 9 “Static characteristics”). In order for the PCA9549 to act as a voltage translator, the $V_{o(sw)}$ voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then $V_{o(sw)}$ should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at Figure 7, we see that $V_{o(sw)}$ (maximum) will be at 2.7 V when the PCA9549 supply voltage is 3.5 V or lower so the PCA9549 supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Figure 16).

7. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 8).

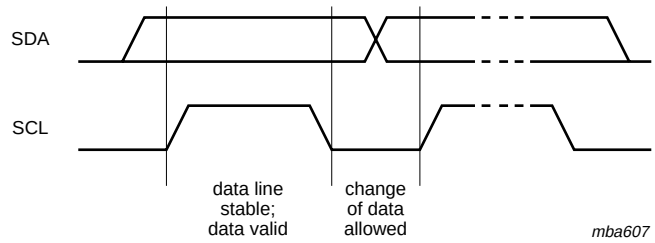


Fig 8. Bit transfer

7.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 9).

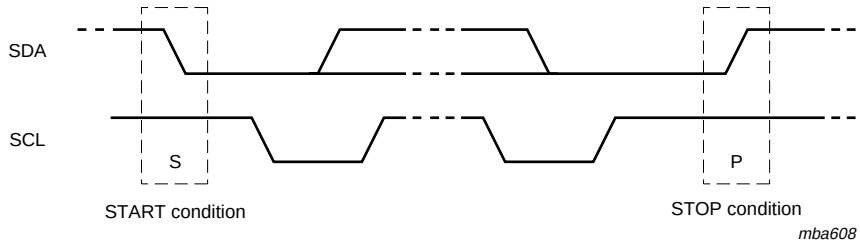


Fig 9. Definition of START and STOP conditions

7.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 10).

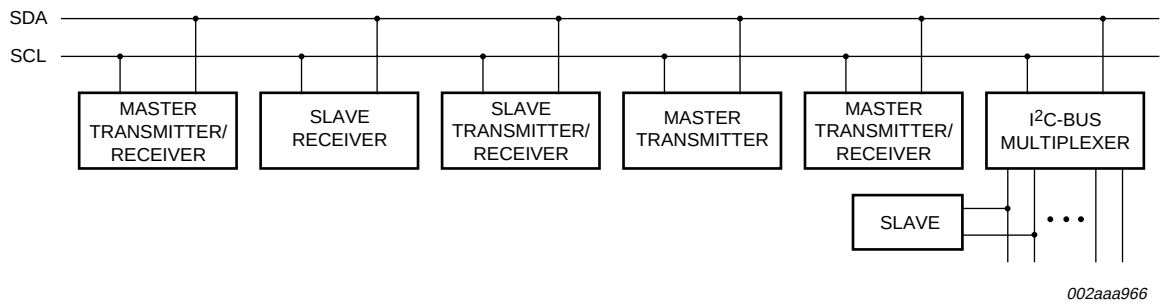


Fig 10. System configuration

7.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

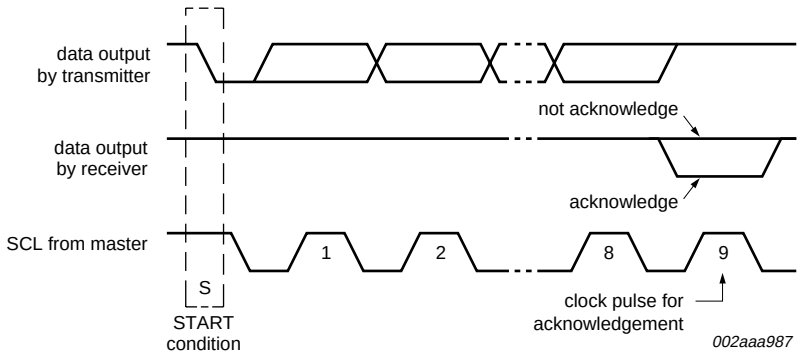


Fig 11. Acknowledgement on the I²C-bus

7.4 Bus transactions

Data is transmitted to the PCA9549 control register using the Write mode as shown in Figure 12.

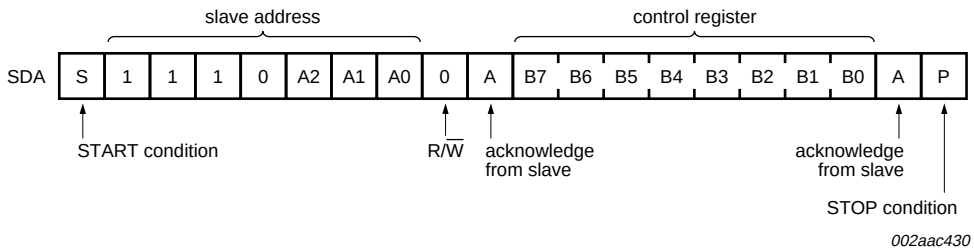


Fig 12. Write control register

Data is read from the PCA9549 using the Read mode as shown in Figure 13.

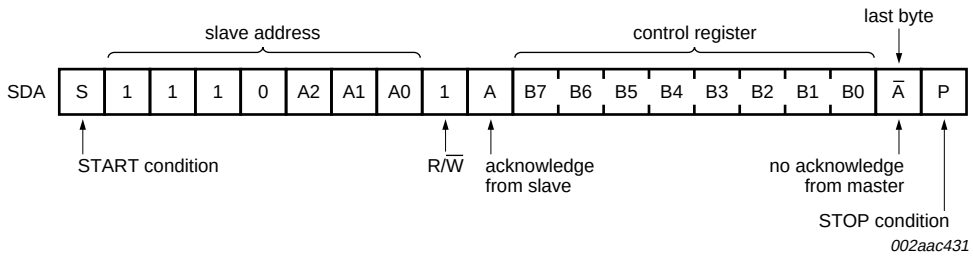


Fig 13. Read control register

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_I	input current		–20	+20	mA
I_O	output current		–25	+25	mA
I_{DD}	supply current		–100	+100	mA
I_{SS}	ground supply current		–100	+100	mA
P_{tot}	total power dissipation		-	400	mW
T_{stg}	storage temperature		–60	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 125 °C.

9. Static characteristics

Table 6. Static characteristics at V_{DD} = 2.3 V to 3.6 V

V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. See Table 7 on page 12 for V_{DD} = 4.5 V to 5.5 V[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage		2.3	-	3.6	V
I_{DD}	supply current	Operating mode; V_{DD} = 3.6 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 kHz	-	20	50	µA
I_{stb}	standby current	Standby mode; V_{DD} = 3.6 V; no load; $V_I = V_{DD}$ or V_{SS}	-	0.1	1	µA
V_{POR}	power-on reset voltage	no load; $V_I = V_{DD}$ or V_{SS} [2]	-	1.6	2.1	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		−0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	-	-	mA
		V_{OL} = 0.6 V	6	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$	-	6	21	pF
Select inputs A0 to A2, $\overline{RESET}$						
V_{IL}	LOW-level input voltage		−0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	V_{DD} + 0.5	V
I_{LI}	input leakage current	pin at V_{DD} or V_{SS}	−1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$	-	2	5	pF
Pass gate						
R_{on}	ON-state resistance	V_{DD} = 3.0 V to 3.6 V; V_O = 0.4 V; I_O = 15 mA	-	7	12	Ω
		V_{DD} = 2.3 V to 2.7 V; V_O = 0.4 V; I_O = 10 mA	-	8	15	Ω
$V_{o(sw)}$	switch output voltage	$V_{i(sw)} = V_{DD}$ = 3.3 V; $I_{o(sw)}$ = −100 µA	-	1.9	-	V
		$V_{i(sw)} = V_{DD}$ = 3.0 V to 3.6 V; $I_{o(sw)}$ = −100 µA	1.6	-	2.8	V
		$V_{i(sw)} = V_{DD}$ = 2.5 V; $I_{o(sw)}$ = −100 µA	-	1.5	-	V
		$V_{i(sw)} = V_{DD}$ = 2.3 V to 2.7 V; $I_{o(sw)}$ = −100 µA	1.0	-	2.0	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	-	+1	µA
C_{io}	input/output capacitance	$V_I = V_{SS}$	-	3	5	pF

[1] For operation between published voltage ranges, refer to the worst-case parameters in both ranges.

[2] V_{DD} must be lowered to 0.2 V in order to reset part.

Table 7. Static characteristics at V_{DD} = 4.5 V to 5.5 V

V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. See Table 6 on page 11 for V_{DD} = 2.3 V to 3.6 V[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage		4.5	-	5.5	V
I_{DD}	supply current	Operating mode; V_{DD} = 5.5 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz	-	65	100	µA
I_{stb}	standby current	Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{DD} or V_{SS}	-	0.6	2	µA
V_{POR}	power-on reset voltage	no load; V_I = V_{DD} or V_{SS} [2]	-	1.7	2.1	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	-	-	mA
		V_{OL} = 0.6 V	6	-	-	mA
I_{IL}	LOW-level input current	V_I = V_{SS}	1	-	1	µA
I_{IH}	HIGH-level input current	V_I = V_{SS}	1	-	1	µA
C_i	input capacitance	V_I = V_{SS}	-	6	21	pF
Select inputs A0 to A2, $\overline{\text{RESET}}$						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	V_{DD} + 0.5	V
I_{LI}	input leakage current	pin at V_{DD} or V_{SS}	−1	-	+50	µA
C_i	input capacitance	V_I = V_{SS}	-	2	5	pF
Pass gate						
R_{on}	ON-state resistance	V_{DD} = 4.5 V to 5.5 V; V_O = 0.4 V; I_O = 15 mA	-	5	8	Ω
$V_{o(sw)}$	switch output voltage	$V_{i(sw)}$ = V_{DD} = 5.0 V; $I_{o(sw)}$ = −100 µA	-	3.6	-	V
		$V_{i(sw)}$ = V_{DD} = 4.5 V to 5.5 V; $I_{o(sw)}$ = −100 µA	2.6	-	4.5	V
I_L	leakage current	V_I = V_{DD} or V_{SS}	−10	-	+10	µA
C_{io}	input/output capacitance	V_I = V_{SS}	-	3	5	pF

[1] For operation between published voltage ranges, refer to the worst-case parameters in both ranges.

[2] V_{DD} must be lowered to 0.2 V in order to reset part.

10. Dynamic characteristics

Table 8. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
t_{PD}	propagation delay	A to B; V_{DD} = 4.5 V to 5.5 V	-	0.25[1]	-	0.25[1]	ns
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition	[2]	4.0	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	µs
$t_{HD;DAT}$	data hold time		0[3]	3.45	0[3]	0.9	µs
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
t_r	rise time of both SDA and SCL signals		-	1000	20 + 0.1C_b[4]	300	ns
t_f	fall time of both SDA and SCL signals		-	300	20 + 0.1C_b[4]	300	ns
C_b	capacitive load for each bus line		-	400	-	400	pF
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
$t_{VD;DAT}$	data valid time	HIGH-to-LOW	-	1	-	1	µs
		LOW-to-HIGH	-	0.6	-	0.6	µs
$t_{VD;ACK}$	data valid acknowledge time		-	1	-	1	µs
$\overline{RESET}$							
$t_{w(rst)L}$	LOW-level reset time		4	-	4	-	ns
t_{rst}	reset time	SDA clear	500	-	500	-	ns
$t_{REC;STA}$	recovery time to START condition		0	-	0	-	ns

[1] Pass gate propagation delay is calculated from the 6 Ω typical R_{on} and the 50 pF load capacitance.

[2] After this period, the first clock pulse is generated.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[4] C_b = total capacitance of one bus line in pF.

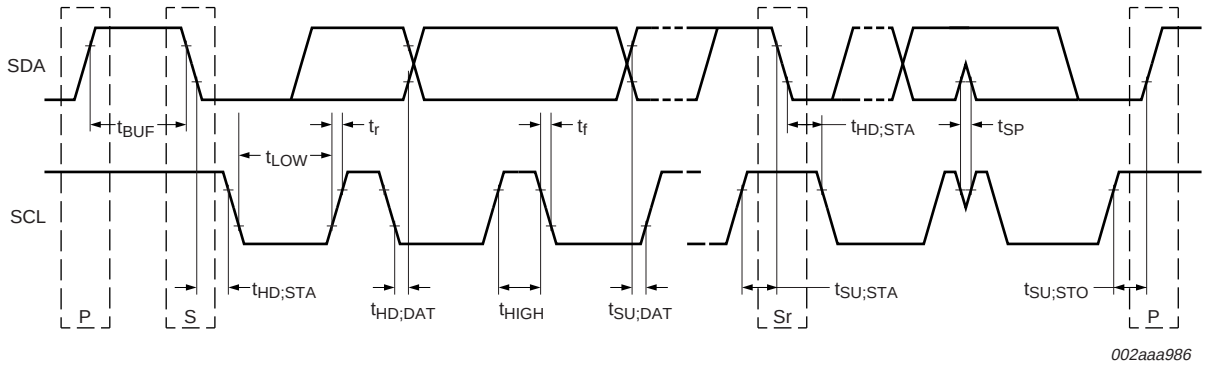


Fig 14. Definition of timing on the I²C-bus

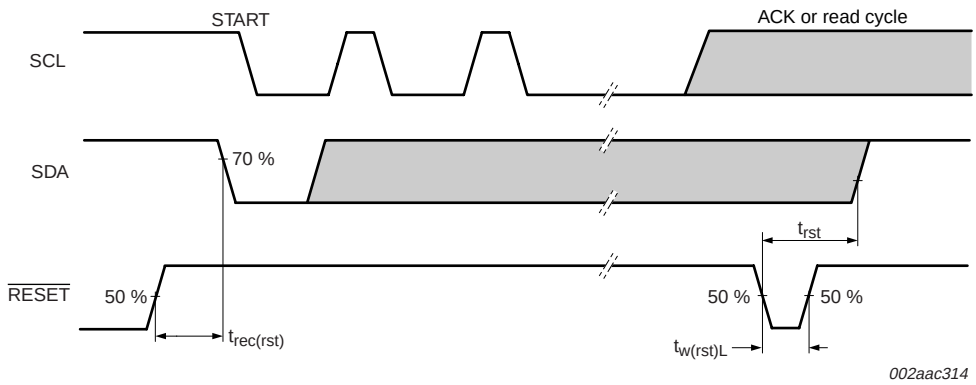
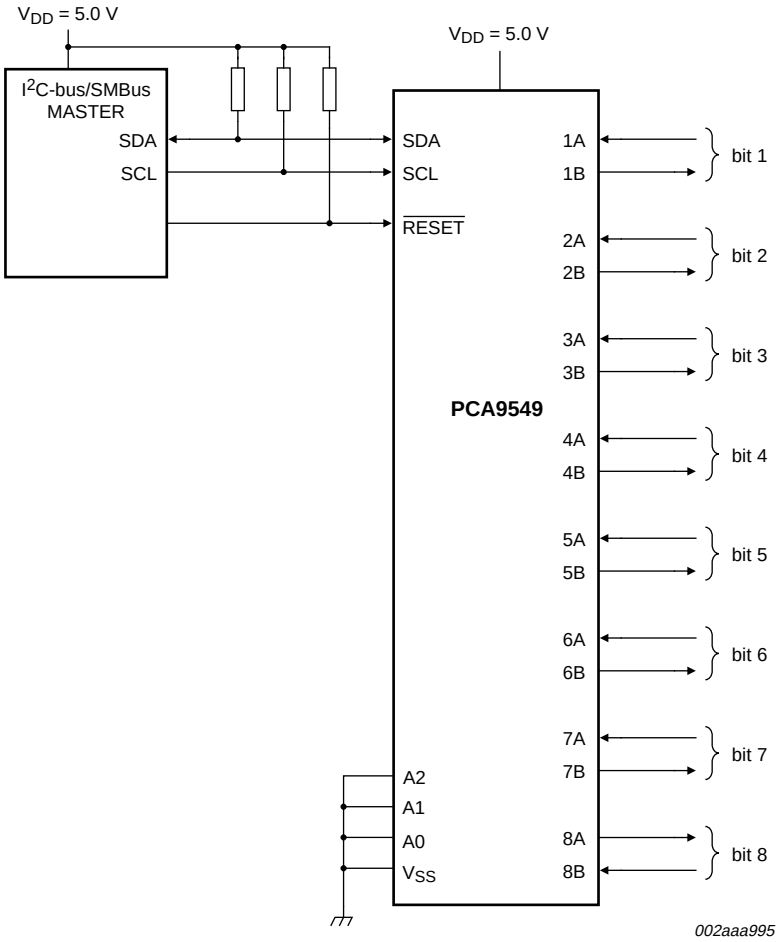


Fig 15. Definition of $\overline{\text{RESET}}$ timing

11. Application information



Remark: B can also be input and A can also be output as shown in bit 8.

Fig 16. Typical application

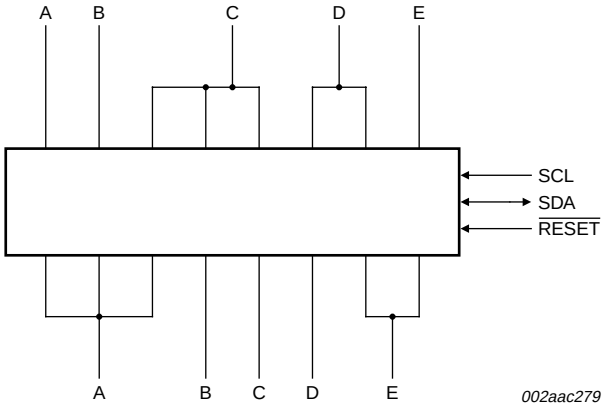


Fig 17. Custom multiplexer or demultiplexer application

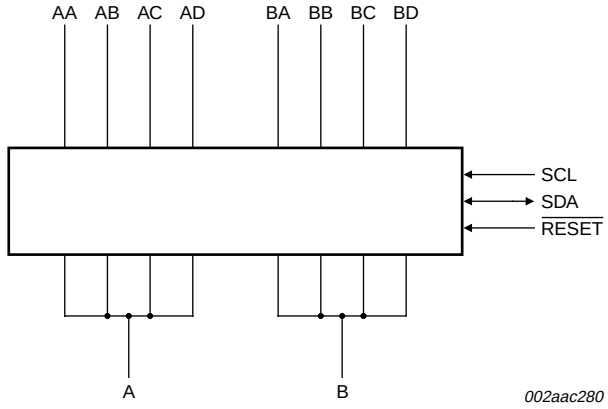
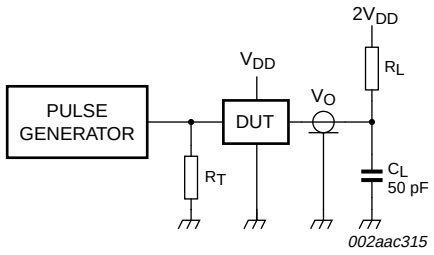


Fig 18. 2 channel 4-to-1 multiplexer or demultiplexer

12. Test information



C_L = load capacitance includes jig and probe capacitance.

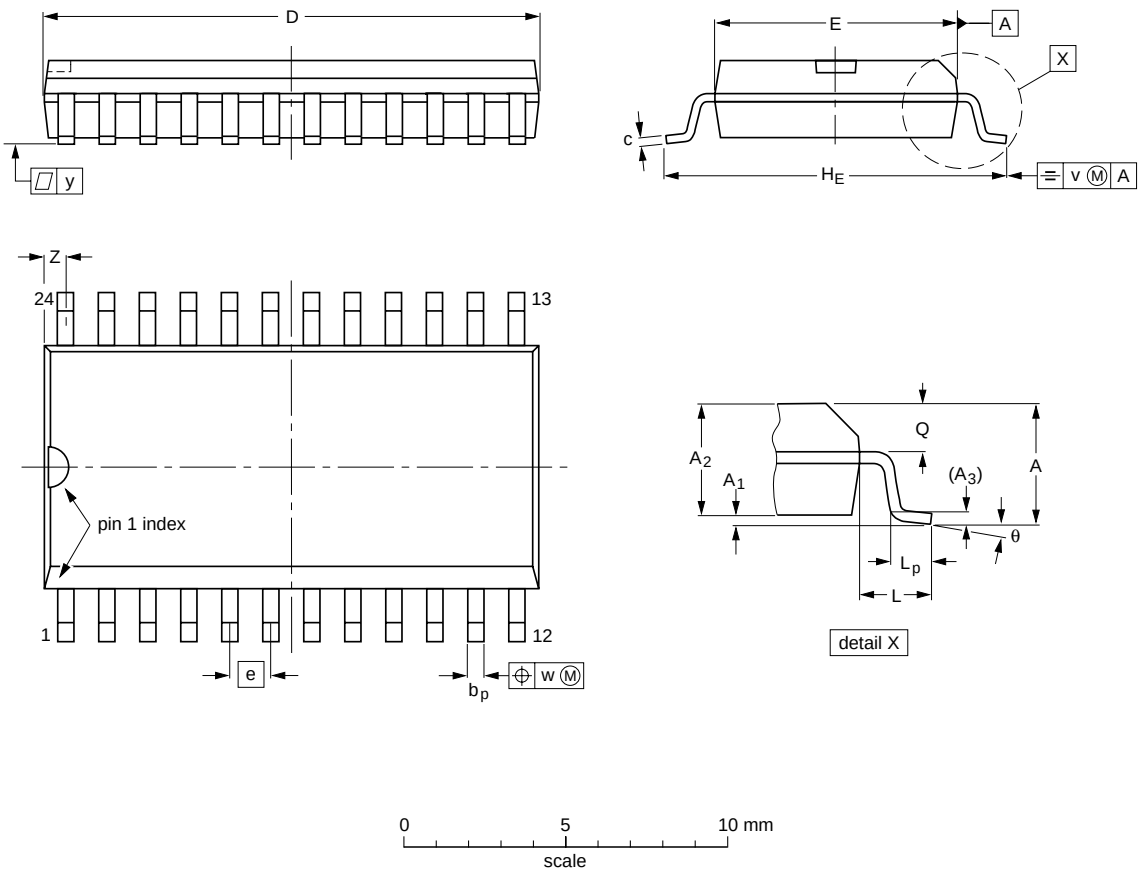
R_L = load resistance.

R_T = termination resistance; should be equal to Z_o of pulse generator.

Fig 19. Test circuit

13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

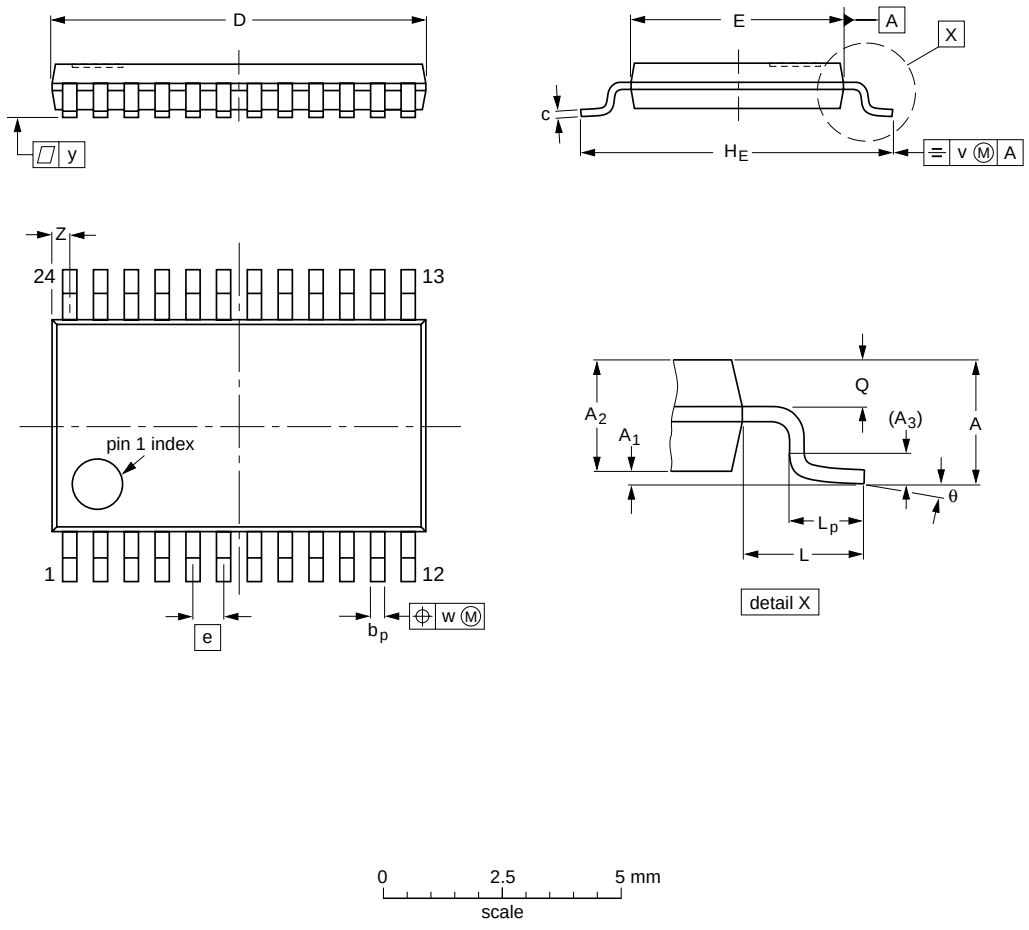
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 20. SO24 package outline (SOT137-1)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

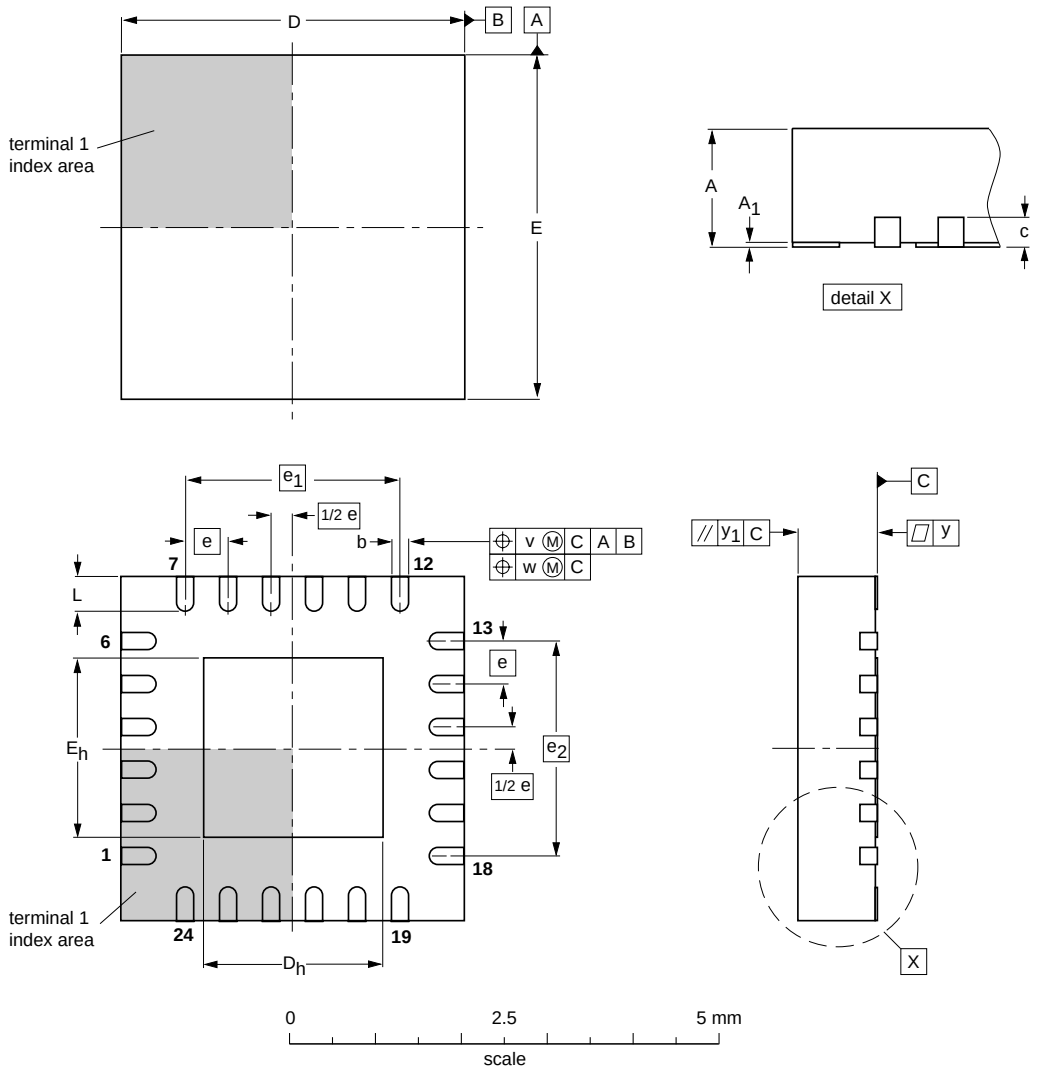
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 21. TSSOP24 package outline (SOT355-1)

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 22. HVQFN24 package outline (SOT616-1)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 23) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020C)

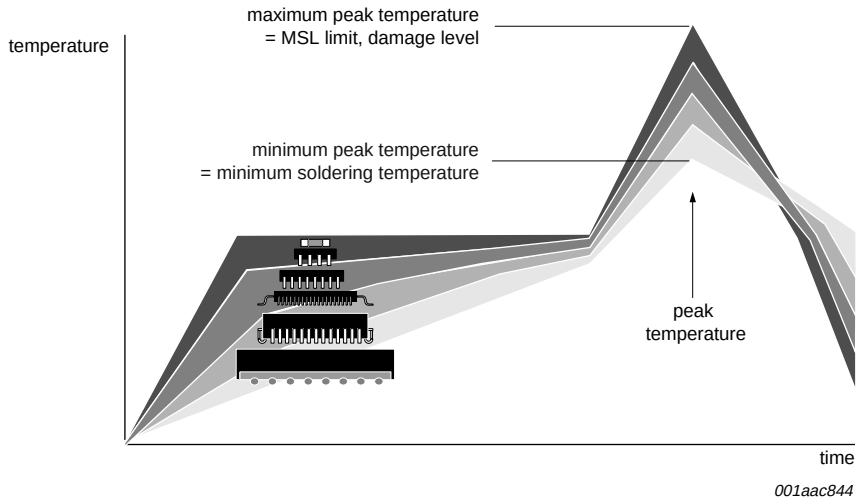
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 23.



MSL: Moisture Sensitivity Level

Fig 23. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Abbreviations

Table 11. Abbreviations

Acronym	Description
CBT	Cross Bar Technology
CDM	Charged-Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
MM	Machine Model
PCB	Printed-Circuit Board
SMBus	System Management Bus
TTL	Transistor-Transistor Logic

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9549_2	20090713	Product data sheet	-	PCA9549_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 8 “Dynamic characteristics”: – Symbol t_f: changed Unit from “µs” to “ns”. – Symbol C_b: changed Unit from “µs” to “pF”. • Updated soldering information.			
PCA9549_1	20060711	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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