UBA2017/UBA2017A

600 V fluorescent lamp driver with linear dimming function

Rev. 2 — 15 May 2012 Product data sheet

1. General description

The UBA2017/UBA2017A are high-voltage Integrated Circuits (IC) intended to drive fluorescent lamps with filaments such as Tube Lamps (TL) and Compact Fluorescent Lamps (CFL) in general lighting applications. The IC comprises a fluorescent lamp control module, half-bridge driver and several protection mechanisms. The IC drives fluorescent lamps using a half-bridge circuit made of two MOSFETs with a supply voltage of up to 600 V.

The UBA2017/UBA2017A are supplied by a start-up bleeder resistor and a dV/dt supply from the half-bridge circuit, or any other auxiliary supply derived from the half-bridge. The supply current of the IC is low. An internal clamp limits the supply voltage.

2. Features and benefits

- Half-bridge driver features:
  - Integrated level-shifter for the high-side driver of the half-bridge
  - Integrated bootstrap diode for the high-side driver supply of the half-bridge
  - Independent non-overlap time
- Fluorescent lamp controller features:
  - Linear dimming (UBA2017A only)
  - EOL (End-Of-Life) detection (both symmetrical and asymmetrical)
  - Adjustable preheat time
  - Adjustable preheat current
  - Adjustable fixed frequency preheat
  - Lamp ignition failure detection
  - Ignition detection of all lamps at multiple lamps with separate resonant tanks
  - Second ignition attempt if first failed
  - Constant output power independent of mains voltage variations
  - Automatic restart after changing lamps
  - Lamp current control
  - Enable input
- Protection
  - Hard switching/capacitive mode protection
  - Half-bridge overcurrent (coil saturation) protection
  - Lamp overvoltage (lamp removal) protection
  - Temperature protection

3. Applications

- Intended for fluorescent lamp ballasts with either a UBA2017A dimmable or a UBA2017 fixed output for AC mains voltages up to 390 V.

4. Ordering information

Table 1. Ordering information

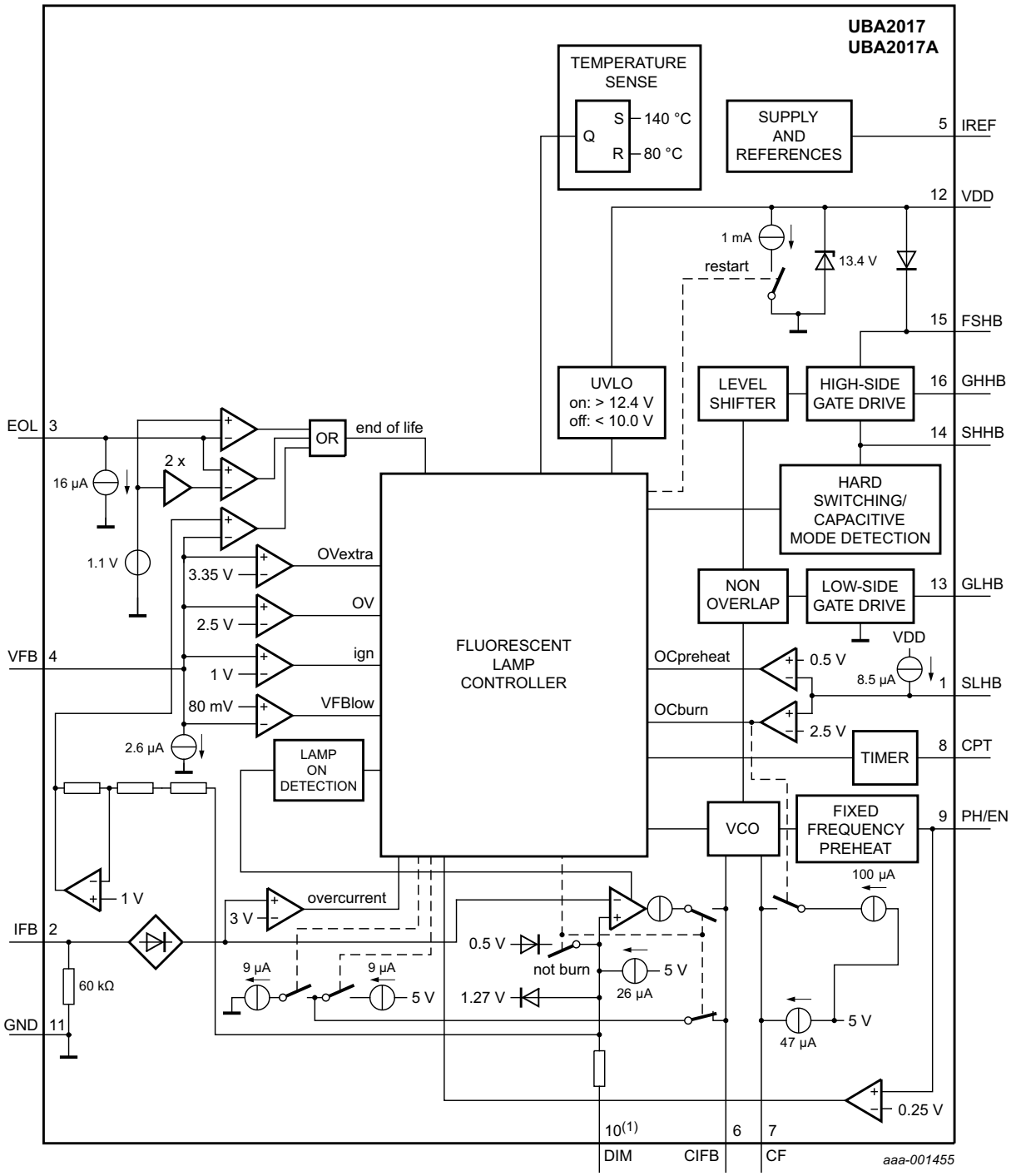
Type number	Package		
	Name	Description	Version
UBA2017T/N1	SO16	plastic small package outline package; 16 leads; body width 3.9 mm	SOT109-1
UBA2017AT/N1			
UBA2017P/N1	DIP16	plastic dual in-line package; 16 leads; (300 mil)	SOT38-4
UBA2017AP/N1			

Table 2. Functional selection

Type	PFC	Dimmable	Fixed frequency preheat
UBA2017P/T	no[1]	no	yes
UBA2017AP/AT	no[1]	yes	yes

[1] If you require PFC functionality, see the UBA2016A, UBA2015A and UBA2015.

5. Block diagram

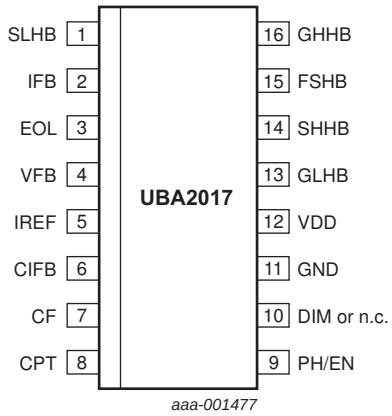


(1) Pin 10 is not connected in the UBA2017P/T.

Fig 1. Block diagram UBA2017

6. Pinning information

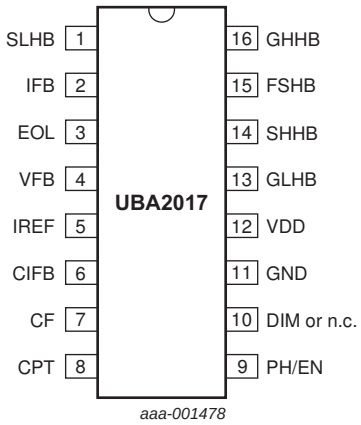
6.1 Pinning



UBA2017T: pin 10 is n.c. (not connected).

UBA2017AT: pin 10 is input pin DIM.

Fig 2. Pin configuration UBA2017T/UBA2017AT (SO16)



UBA2017P: pin 10 is n.c. (not connected).

UBA2017AP: pin 10 is input pin DIM.

Fig 3. Pin configuration UBA2017P/UBA2017AP (DIP16)

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	UBA2017AT/AP	UBA2017P/T	
SLHB	1	1	half-bridge (HB) low-side switch current sense input
IFB	2	2	lamp current feedback input
EOL	3	3	end-of-life sensing input
VFB	4	4	lamp voltage feedback input
IREF	5	5	reference current setting
CIFB	6	6	lamp current feedback compensation
CF	7	7	high frequency (HF) oscillator timing capacitor
CPT	8	8	preheat and fault timing capacitor
PH/EN	9	9	preheat frequency setting combined with enable
DIM	10	-	dimming function input (UBA2017AT/AP)
n.c.	-	10	UBA2017P/T
GND	11	11	ground
VDD	12	12	supply
GLHB	13	13	HB low-side switch gate driver output
SHHB	14	14	HB high-side source connection
FSHB	15	15	HB floating supply connection
GHHB	16	16	HB high-side switch gate driver output

7. Functional description

7.1 Introduction

The UBA2017/UBA2017A is an integrated circuit for electronically ballasted fluorescent lamps. It provides a half-bridge controller/driver with all the necessary functions for correct preheat, ignition and on-state operation of the lamp. Several protection mechanisms are incorporated to ensure the safe operation of the fluorescent lamp or a shutdown of the complete ballast under any abnormal operating conditions or lamp failure.

7.2 Half-bridge driver

The IC incorporates drivers for the half-bridge switches and all related circuits such as non-overlap, high-voltage level shifter, bootstrap circuit for the floating supply and hard switching and capacitive mode detection.

The UBA2017/UBA2017A is designed to drive a half-bridge inverter with an inductive load. The load consists typically of an inductor with a resonant capacitor and a TL or CFL. A basic half-bridge application circuit driving a TL is shown in Figure 4 which also shows a typical IC supply configuration with a start-up bleeder resistor and a dV/dt supply.

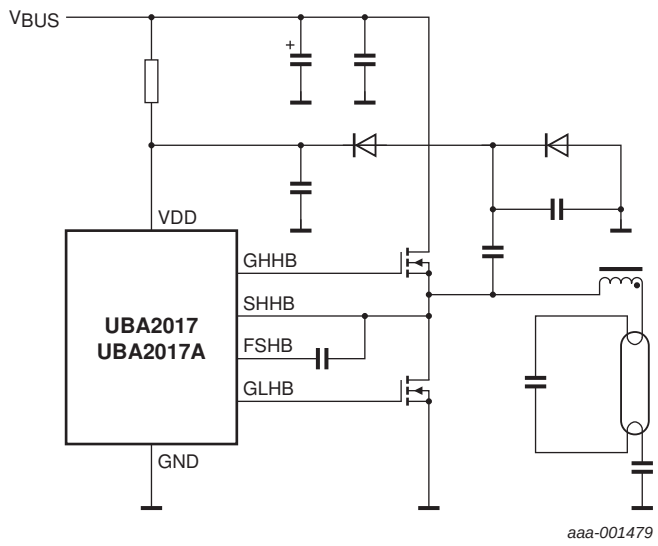


Fig 4. Basic half-bridge and IC supply connection diagram

7.2.1 VDD supply

The UBA2017/UBA2017A is intended to be supplied by a start-up bleeder resistor connected between the bus voltage V_{BUS} and VDD and a dV/dt supply from the half-bridge point at pin SHHB.

The IC starts up when the voltage at pin VDD rises above start-up voltage $V_{startup(VDD)}$ and locks out (stops oscillating) when the voltage at pin VDD drops below stop voltage $V_{stop(VDD)}$. The hysteresis between the start and stop levels allows the IC to be supplied by a buffer capacitor until the dV/dt supply is settled.

The UBA2017/UBA2017A has an internal VDD clamp. This is an internal active Zener (or shunt regulator) that limits the voltage on the VDD supply pin to clamp voltage $V_{clamp(VDD)}$. No external Zener diode is needed in the dV/dt supply circuit if the maximum current of the dV/dt supply minus the current consumption of the IC (mainly determined by the gate drivers' load) is below $I_{clamp(VDD)}$.

7.2.2 Low- and high-side drivers

The low- and high-side drivers are identical. The output of each driver is connected to the equivalent gate of an external power MOSFET. The high-side driver is supplied by the bootstrap capacitor, which is charged from the VDD supply voltage via an internal diode when the low-side power MOSFET is on. The low-side driver is directly supplied by the VDD supply voltage.

7.2.3 Non-overlap

During each transition between the two states GLHB HIGH/GHHB LOW and GLHB LOW/GHHB HIGH, GLHB and GHHB are both LOW for a fixed non-overlap time t_{no} to allow the half-bridge point to be charged or discharged by the load current (assuming the load always has an inductive behavior), and enabling zero voltage switching. See Figure 5.

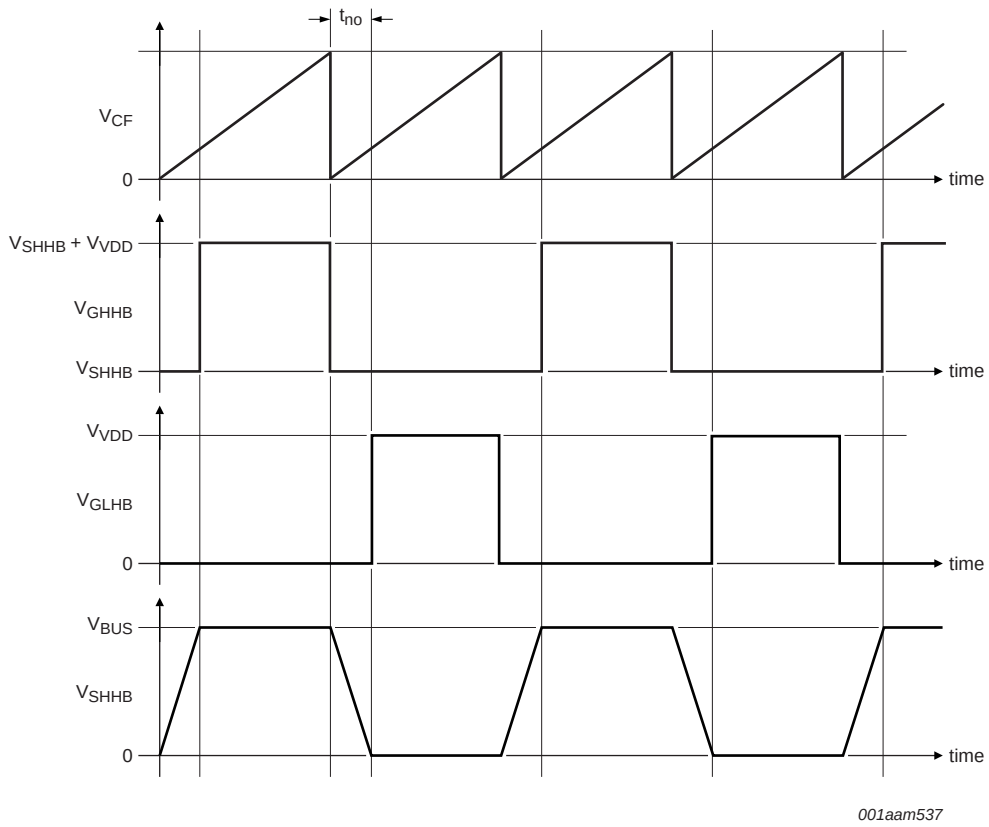


Fig 5. Oscillator, driver and half-bridge voltages

7.3 Fluorescent lamp control

The IC incorporates all the regulation and control needed for the fluorescent lamp(s), such as filament preheat, ignition frequency sweep, lamp voltage limitation, lamp current control, dimming, end-of-life detection, overcurrent protection and hard switching limiting.

In the UBA2017/UBA2017A, seven different operating states can be distinguished. In each state the IC acts in a specific way, as described in the next paragraphs. Figure 6 shows the possible transitions between the states with their conditions.

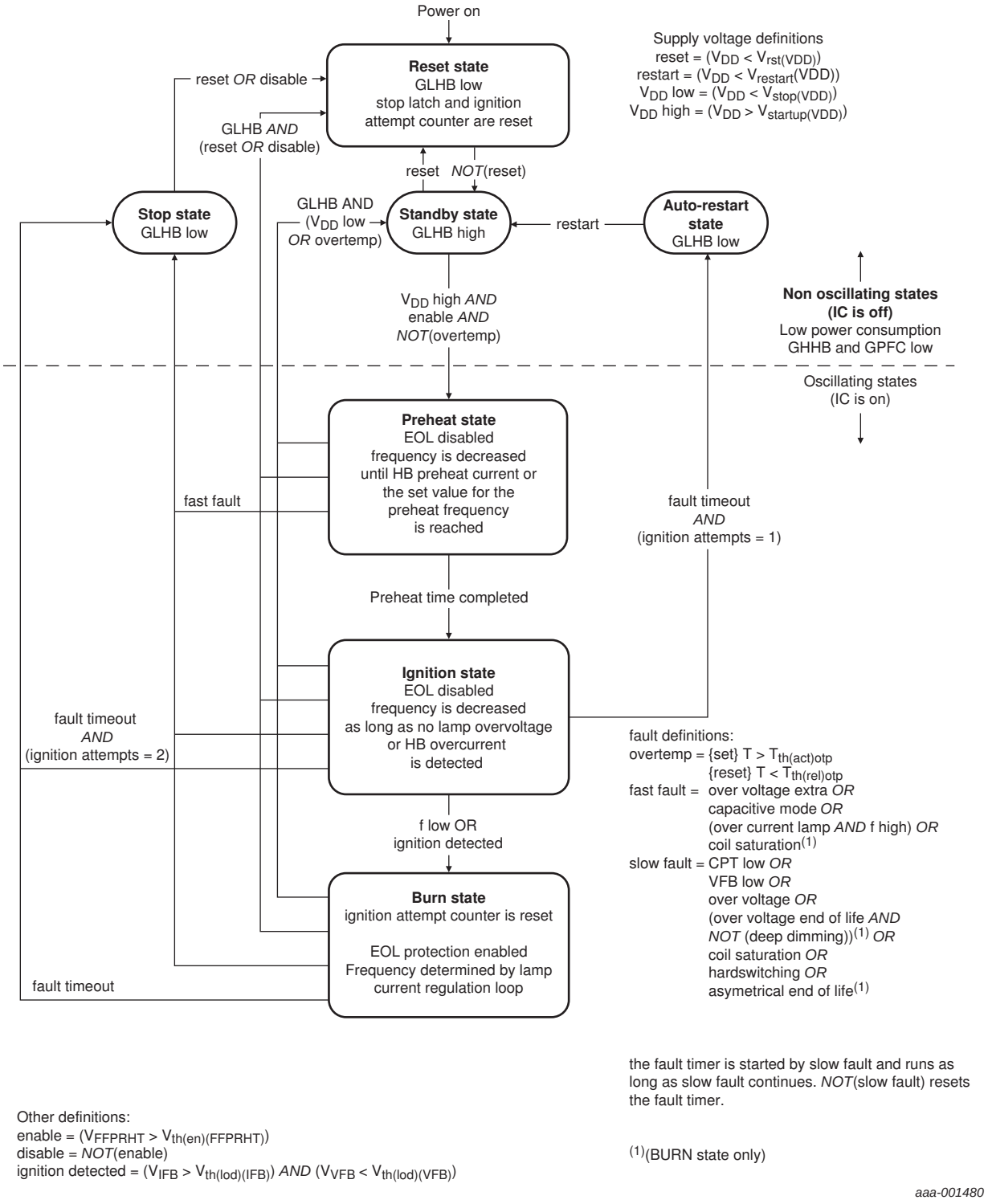


Fig 6. State diagram

7.3.1 Reset

When voltage on pin VDD is below the reset voltage $V_{rst(VDD)}$, both gates of the half-bridge driver are LOW. All internal latches are reset. When voltage on pin VDD rises above $V_{rst(VDD)}$, the IC enters the STANDBY state.

7.3.2 Standby

In the STANDBY state, the low-side gate driver is on (GLHB is HIGH). The floating supply capacitor C_{FSHB} is then charged. When the VDD voltage rises above $V_{startup(VDD)}$, the Preheat state is entered.

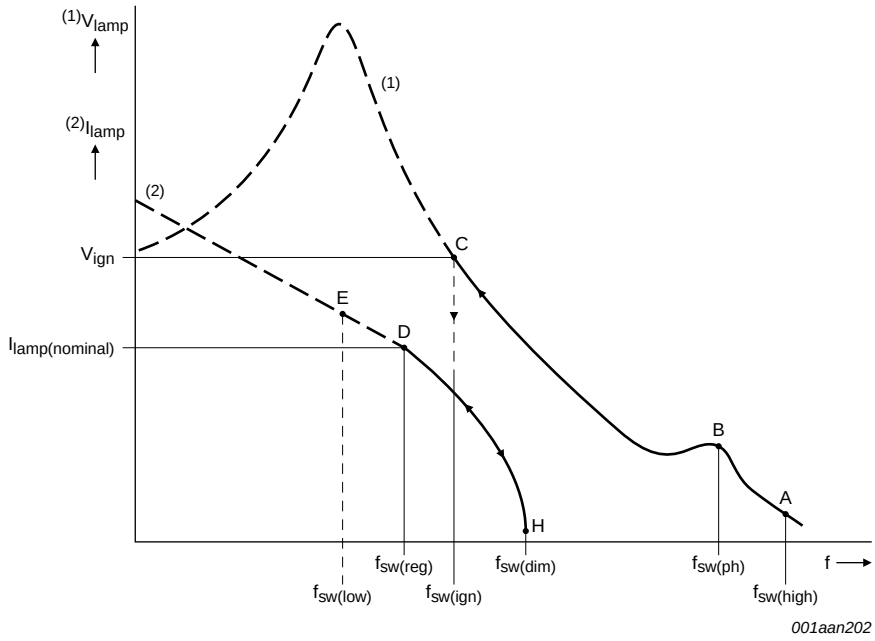
7.3.3 Oscillating states (Preheat, Ignition and Burn)

The highest and lowest oscillation frequency can be set with capacitor C_{CF} connected to the CF pin. The oscillator is implemented in such a way that the lowest frequency $f_{sw(low)}$ is the most accurate. In any oscillating state (Preheat, Ignition or Burn), when VDD voltage drops below $V_{stop(VDD)}$ or overtemperature is detected, the half-bridge stops oscillation when GLHB is HIGH and enters the STANDBY state.

7.3.4 Preheat

The oscillating frequency starts at $f_{sw(high)}$ (see Figure 7 “Resonance curve application” point A) and remains at that frequency until the voltages at pins CPT and VFB settle above their pin short protection levels ($V_{VFB} > V_{th(osp)(VFB)}$ and $V_{CPT} > V_{th(scp)(CPT)}$). The half-bridge current or frequency is regulated when in the preheat state; see Figure 7 “Resonance curve application” point B.

Pin CIFB supplies a current $I_{ch(CIFB)}$ to the externally connected compensation network on this pin and its voltage rises. This causes the switching frequency to decrease (pin CIFB is the input for the voltage controlled oscillator). This causes an increase in half-bridge current (assuming the switching frequency is higher than the load resonance frequency). This current is measured via pin SLHB using a resistor connected between the source of the low-side switch and ground. When the voltage on pin SLHB rises above the preheat current control voltage $V_{crtl(ph)SLHB}$, discharge current $I_{dch(CIFB)}$ replaces the charge current to pin CIFB and the frequency is increased. When the voltage drops below $V_{th(ocp)SLHB}$, current $I_{ch(CIFB)}$ from pin CIFB causes the frequency to decrease.



(1) Lamp voltage when lamp is off (not ignited yet).

(2) Lamp current when lamp is on.

Fig 7. Resonance curve application

The preheat frequency can also be regulated via pin PH/EN. During preheat, the output voltage of pin PH/EN is $V_{ph(PH/EN)}$. The output current that an external resistor $R_{ext(PH/EN)}$ connected to this pin sinks is compared to $^4/_5$ of the output current of the VCO (the current at pin CF with no fault condition present and the capacitor at that pin being charged minus the same current at $f_{sw(low)}$). As long as the output current of the VCO is bigger the frequency is being decreased (by charging pin CIFB with $I_{ch(CIFB)}$). If the current through the external resistor is larger, the frequency is increased (by discharging pin CIFB with $I_{dch(CIFB)}$).

Current and fixed frequency control mechanisms are active at the same time. For fixed frequency preheat using pin PH/EN, the half-bridge current sense resistor connected to pin SLHB should be small enough not the activate the current control mechanism. If current controlled preheat is used, pin PH/EN should be left open (except for the open collector or open drain that drives the enable function). The preheat time $t_{to(ph)}$ can be set with capacitor C_{CPT} on pin CPT.

7.3.5 Ignition

After the Preheat state the IC enters the Ignition state. During the Ignition state, the switching frequency is decreased by charging pin CIFB with $I_{ch(CIFB)}$. This will result in increasing lamp voltage until the lamp ignites (see point C in Figure 7 “Resonance curve application”) and lamp-on or $f_{sw(low)}$ (lowest frequency) is detected. Lamp-on detection occurs when the average absolute voltage on pin IFB is above lamp-on detection threshold $V_{th(lod)(IFB)}$ and the voltage on pin VFB is more than 50 % of each clock cycle below the lamp-on detection threshold $V_{th(lod)(VFB)}$ and after a delay $t_{d(lod)}$.

If either saturation or overvoltage is triggered, it overrules the frequency sweep-down and hold the frequency at the border where the fault appeared and start the fault timer. When the fault time-out $t_{to(fault)}$ is reached the IC enters the Auto-restart state if it was the first ignition attempt, otherwise it enters the Stop state; see Figure 6 “State diagram”.

7.3.6 Auto-restart

The Auto-restart state is entered after a fault time-out in the Ignition state during the first ignition attempt. See Figure 6 “State diagram”. When the IC is in the Auto-restart state, it draws supply current $I_{restart(VDD)}$. This slowly discharges the buffer capacitor on pin VDD until the voltage on this pin drops below $V_{restart(VDD)}$. The IC then enters the Standby state. Here the VDD capacitor is charged again to start a second ignition attempt. The bleeder current must be between standby current $I_{stb(VDD)}$ and $I_{restart(VDD)}$. A time delay can be set between the two ignition attempts with the capacitor at pin VDD to reduce stress on the HB components.

7.3.7 Burn

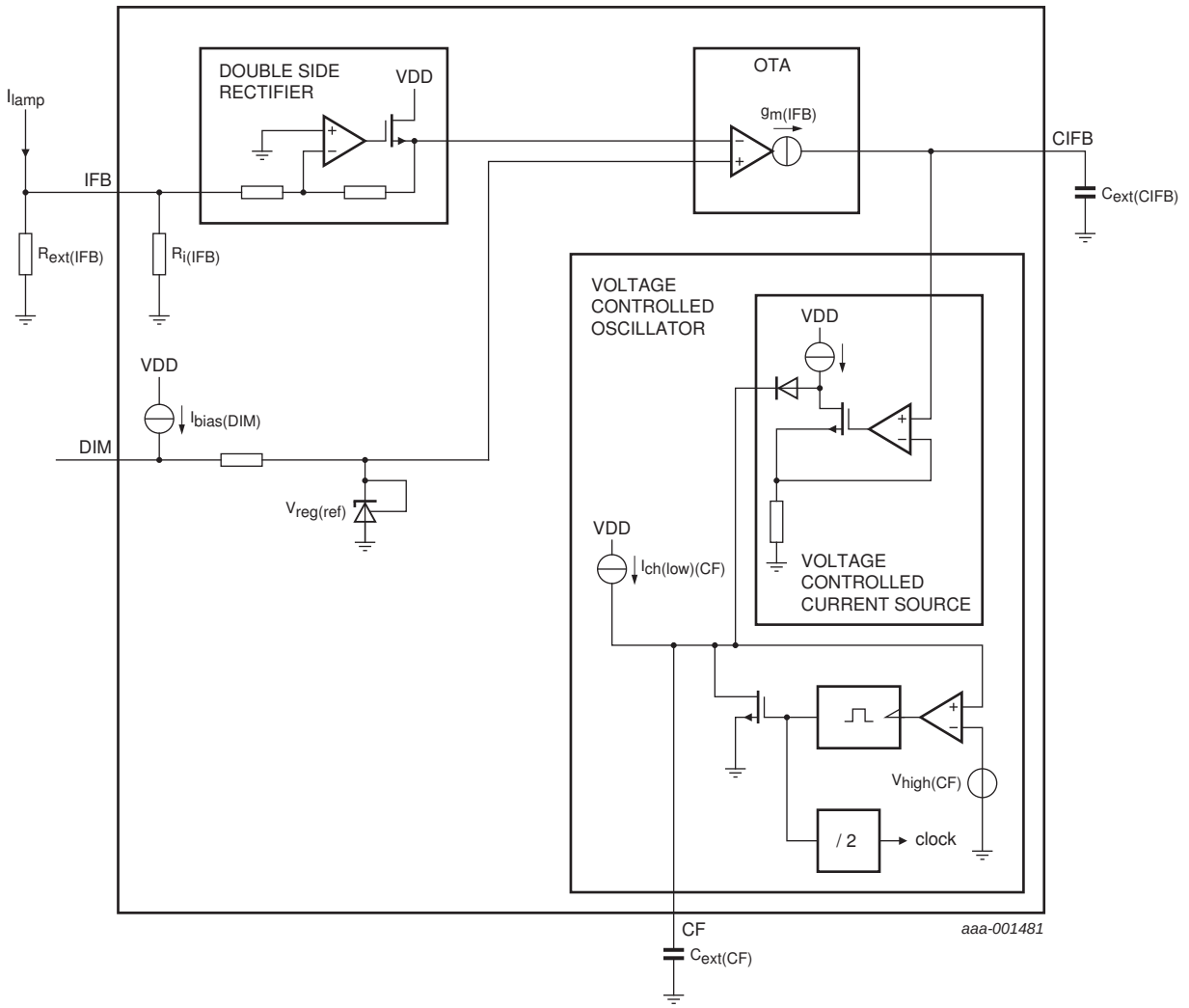
In the Burn state, the lamp current regulation and all protection circuits are active.

7.3.7.1 Lamp current control and dimming

The AC lamp current is sensed by an external resistor connected to pin IFB. The resulting AC voltage on pin IFB is internally Double-Side Rectified (DSR), and compared to a reference level by an OTA. This reference level is determined by the internal reference regulation level $V_{reg(ref)}$ and the voltage on the DIM input (UBA2017A only), as shown in Figure 8 “Lamp current control”.

Definition: the regulation voltage on pin IFB ($V_{reg(IFB)}$) is the level seen from outside the IC to which the IC tries to regulate the average absolute voltage on pin IFB.
If the DIM input is not present or not connected or $V_{DIM} > V_{reg(ref)}$ then $V_{reg(IFB)}$ is $V_{reg(ref)}$ + non-idealities from the OTA and the DSR else $V_{reg(IFB)} = V_{DIM}$ + non-idealities from OTA and DSR.

The DIM input controls the lamp current set point (UBA2017A only). The DIM input level is internally clamped to $V_{reg(ref)}$. The lowest possible DIM input level is set by the bias current on pin DIM $I_{bias(DIM)}$ and the external resistance on the pin. If no dimming is required, pin DIM can be left open or connected via a capacitor to ground. The internal current source $I_{bias(DIM)}$ will then charge the pin until it is internally clamped to $V_{reg(ref)}$.



DIM input is only present in the UBA2017A

Fig 8. Lamp current control

The output of the OTA is connected to pin CIFB. The external capacitor $C_{ext(CIFB)}$ is charged and discharged according to the voltage on the OTA inputs and the transconductance of the OTA, $g_{m(IFB)}$ according to the formula:
$I_{CIFB} = g_{m(IFB)} \times (V_{IFB} - V_{reg(IFB)})$.

More components can be connected to pin CIFB to improve the response time and stability of the lamp current control loop.

Pin CIFB is connected to the input of the VCO (Voltage Controlled Oscillator) that determines the frequency of the IC. Pin CIFB voltage is inversely proportional to the switching frequency. When the load is inductive, an increase in frequency decreases the lamp current, and a decrease in frequency increases the lamp current. With the closed loop for the lamp current in place, the IC will regulate to the required frequency for the desired lamp current. So when the IC enters the Burn state it will go to either point D or H shown in Figure 7 depending on the DIM input voltage or $V_{reg(ref)}$.

However, the switching frequency can never go below $f_{sw(low)}$. If the regulation level is not reached at $f_{sw(low)}$ the IC will stay at $f_{sw(low)}$ (point E in Figure 7).

7.3.7.2 Operation without lamp current control

To operate the lamp without current control the lamp current sense, pin IFB must be connected to ground. The lamp now operates at the lowest frequency $f_{sw(low)}$ (point E in Figure 7). Dimming is not supported in this case.

7.3.8 Stop state

When in the Stop state, the IC is off and all driver outputs are low. The IC will remain in the Stop state until the voltage on pin VDD drops below $V_{rst(VDD)}$ or it is disabled, in which case it will go to the Reset state.

The sequence of events for entering the Stop state are shown in Figure 6 “State diagram”.

7.4 Enable and Disable

The enable function works via pin PH/EN. If this pin is pulled below the enable voltage $V_{en(PH/EN)}$, the IC goes into the Standby state (immediately if GLHB is high, otherwise it will continue its normal clock cycle until GLHB is high and then go to the Standby state).

The external interface with pin PH/EN for the enable signal should be an open collector or open drain type driver. To enable the IC, the open collector or open drain should be open (high ohmic) to not disturb the fixed frequency preheat setting function of pin PH/EN.

In the Restart, Standby and Stop states, the standby pull-up current source $I_{pu(stb)(PH/EN)}$ will pull the voltage at pin PH/EN above $V_{en(PH/EN)}$. In the Preheat, Ignition and Burn states, the normal output voltage driver of the IC will pull the pin high. In those cases, the external driver must draw a current $I_{clamp(PH/EN)}$ from the pin to disable the IC.

7.5 Protection circuits

7.5.1 End-of-life rectifying lamp detection

If voltage on pin EOL is below low threshold voltage $V_{th(low)EOL}$ or above $V_{th(high)EOL}$, the fault timer will start.

A programmable end-of-life window is achieved by the internal bias current sink $I_{bias(EOL)}$. The effective relative size of the EOL window will decrease in line with the increasing series resistance connected to pin EOL.

The end-of-life lamp rectifying detection is only active during the Burn state.

7.5.2 End-of-life overvoltage detection

This protection is intended to protect against symmetrical lamp aging. When in the Burn state, the voltage on pin VFB exceeds the overvoltage end-of-life threshold voltage $V_{th(oveol)(VFB)}$ by more than 50 % of each switching cycle the fault timer will start. $V_{th(oveol)(VFB)}$ is related to the regulation voltage on pin IFB $V_{reg(IFB)}$ that itself is dependent on the voltage on pin DIM (see Section 7.3.7.1 “Lamp current control and dimming”) according to the formula $V_{th(oveol)(VFB)} = a - b \times V_{reg(IFB)}$:

Parameters a and b can be calculated from the $V_{th(oveol)(VFB)}$ values given in Table 6.

The end-of-life overvoltage protection is only active during the Burn state and (for UBA2017A) if the voltage at pin DIM is above the overvoltage end-of-life enable voltage $V_{en(oveol)(DIM)}$.

7.5.3 Capacitive mode detection

Under all normal operating conditions, the half-bridge switching frequency should be higher than the load resonance frequency. The load then shows an inductive behavior in that the load current I_{load} lags behind the half-bridge voltage V_{SHHB}. If the amplitude and the phase difference are large enough, the load current will charge any capacitance on pin SHHB during the non-overlap time $t_{no(LH)}$, and discharge it during the other non-overlap time $t_{no(HL)}$. As a result, the voltage across the switches is almost zero at the moment they turn on. This is called zero voltage switching; see Figure 9 “Switching”. Zero voltage switching provides the highest switching efficiency and the least Electromagnetic Emission (EME).

Capacitive mode switching can occur when, due to any abnormal condition, the switching frequency is below the load resonance frequency. This can happen when the lamp is removed. The load current will then keep the backgate diode of the switch that is switched off conducting during the non-overlap time, and if the other switch is turned on, a sudden step of the half-bridge voltage to the other supply rail takes place (which causes huge current spikes). Also cross conduction between the switches can occur during the reverse recovery of the backgate diode. These effects put huge stress on the power switches.

To protect against capacitive mode switching, the IC monitors pin SHHB during the non-overlap time $t_{no(LH)}$ between switching off the low-side switch and switching on of the high-side switch. If a rise of V_{SHHB} ($dV_{SHHB}/dt > V_{th(cm)(SHHB)}$) during $t_{no(LH)}$ is not detected, the IC will conclude that capacitive mode switching is occurring during the next full cycle. If capacitive mode is detected longer than the fault activation delay time $t_{det(fault)}$ then the IC will enter the Stop state.

Capacitive mode detection is active in all oscillating states.

During ignition, a situation may occur where the amplitude of the load current is high and the half-bridge is at the boundary of capacitive mode switching; see Figure 9 “Switching”. The load current crosses zero during the non-overlap time. If the amplitude of the load current is large enough, the IC might not detect capacitive mode because V_{SHHB} did rise before going down again. The backgate diode of one switch is conducting again when the other switch switches on. Since this can only happen if the load current crosses zero during the non-overlap time, the momentary value of the load current at the end of the non-overlap time will be not so significant, and is not likely to damage the switches.

Depending on the topology used, the DC blocking capacitor might be charged via the lamp(s) at the moment the lamp(s) ignite. This will cause a temporary DC current addition to the load current that might be interpreted by the IC as capacitive mode switching. If this happens, the DC blocking capacitor must be reduced or pre-charged.

7.5.4 Hard switching protection

The hard switching level $V_{step(SHHB)}$ step is measured via pin SHHB. The hard switching level is determined by measuring the voltage step on pin SHHB on the rising edge of pin GHHB; see Figure 9 “Switching”. When $V_{step(SHHB)}$ is above the hard switching protection threshold voltage on pin SHHB ($V_{th(hswp)SHHB}$), the fault timer is activated.

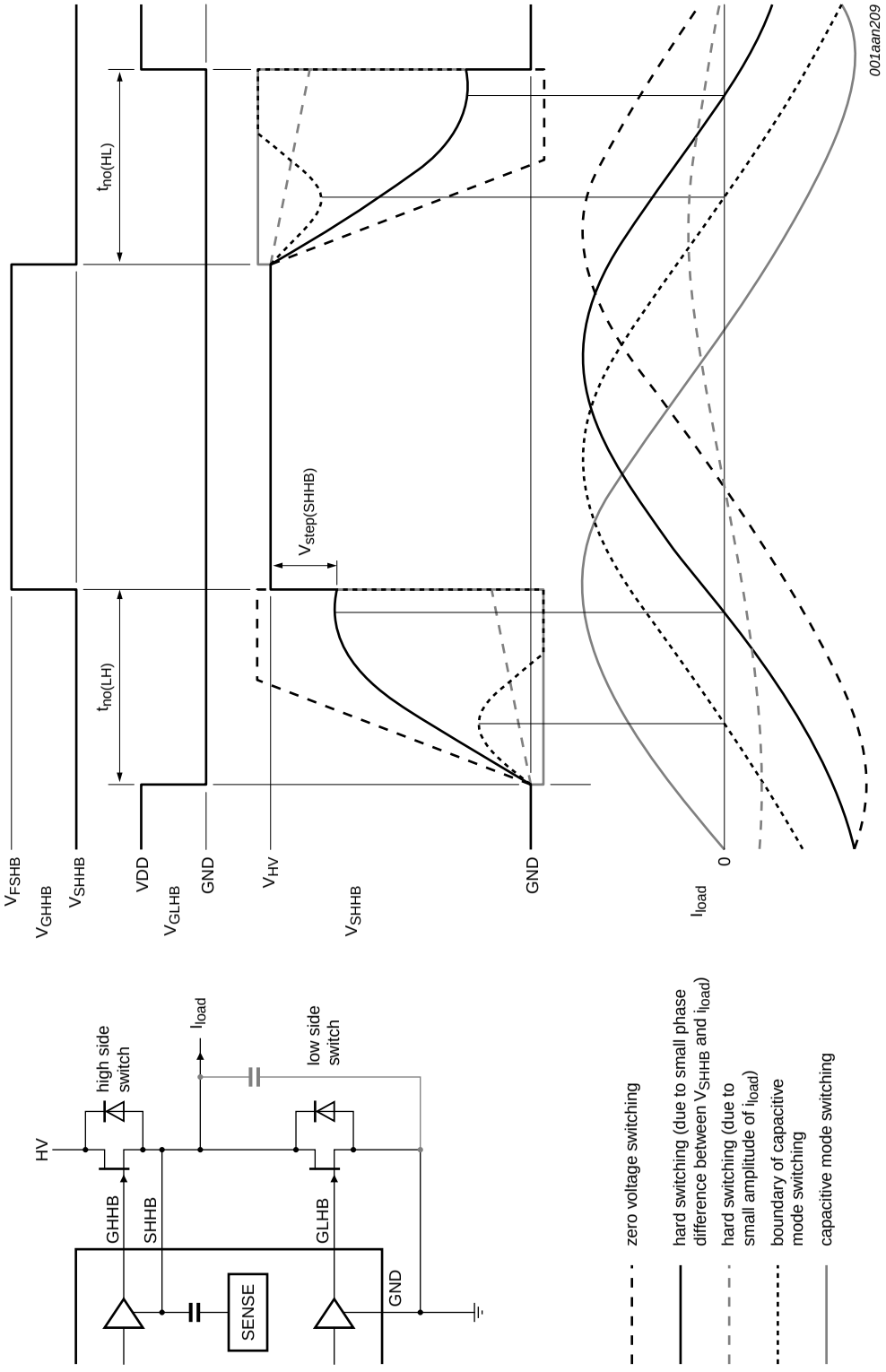


Fig 9. Switching

7.5.5 Coil saturation protection

When the peak voltage on pin SLHB exceeds saturation threshold voltage $V_{th(sat)SLHB}$, an additional current $I_{add(CF)}$ is sourced to pin CF to shorten the running oscillator cycle. In the Ignition state, the fault timer is started and a discharge current $I_{dch(CIFB)}$ is drawn from pin CIFB during the next cycle to increase the switching frequency.

In the Burn state, the IC will go to the Stop state if coil saturation is detected longer than the saturation detection delay time $t_{d(det)sat}$.

Current $I_{bias(SLHB)}$ is sourced to pin SLHB which will force the controller into coil saturation protection if pin SLHB is left open.

7.5.6 Lamp overcurrent protection

If voltage on pin IFB exceeds the overcurrent detection threshold voltage $V_{th(ocd)(IFB)}$, and the oscillator is running at $f_{sw(high)}$, an overcurrent is detected and the IC will immediately enter the Stop state.

7.5.7 Lamp overvoltage protection

When the peak voltage on pin VFB exceeds $V_{th(ov)(VFB)}$, the fault timer is started and a discharge current $I_{dch(CIFB)}$ is drawn from pin CIFB during the next cycle to increase the switching frequency.

When $V_{VFB} > V_{th(ovextra)(VFB)}$ for longer than the fault activation delay time $t_{det(fault)}$ then the IC will enter the Stop state.

7.5.8 Lamp removal detection

Removing the lamp from applications that have the resonant capacitor connected via the lamp filaments, will result in hard switching because current cannot flow through the ballast inductor.

If hard switching is detected during the Ignition or Burn state, the fault timer will be started.

For applications with the resonant capacitor connected directly to the ballast inductor, capacitive mode, coil saturation or over voltage will be detected. Capacitive mode is activated if the switching frequency ends up below the resonance frequency due to removal of the lamp. If the switching frequency is near or above the resonance frequency, the lamp (or rather the lamp socket) voltage and half-bridge current will be very high due to the unloaded resonant circuit (lamp inductor and lamp capacitor) which activates the coil saturation protection or the overvoltage protection.

7.5.9 Temperature protection

When the temperature is above $T_{th(act)otp}$ and GLHB is high, the IC enters the Standby state. The IC cannot exit the Standby state until the temperature drops below $T_{th(rel)otp}$.

7.5.10 Fault timer

Any fault that starts the fault timer must be detected for longer than the fault activation delay time $t_{d(act)fault}$ to start the timer. When the timer is started, the capacitor at pin CPT is alternately being charged and discharged. After 8 charging and 7 discharging cycles the fault time-out period $t_{to(fault)}$ is reached and the IC enters either the Stop state or the Auto-restart state, depending on the fault detected, the current state of the timer and the number of ignition attempts; see Figure 6 “State diagram”.

If the fault that started the timer is no longer detected for a period longer than the fault release delay time $t_{d(rel)fault}$, the fault timer will be reset and at any new occurrence of the fault, the timer will start from zero.

Faults which activate the fault timer are shown as SlowFault in Figure 6 “State diagram”.

The fault timer uses the same pin (CPT) to set the time with an external capacitor $C_{ext(CPT)}$ as the preheat timer. The ratio between the preheat time-out time $t_{to(ph)}$ and the fault time-out time $t_{to(fault)}$ can be changed by adding an external series resistor $R_{s(ext)(CPT)}$ or an external parallel resistor $R_{p(ext)(CPT)}$ to the external capacitor $C_{ext(CPT)}$; see Figure 10 “CPT connections”.

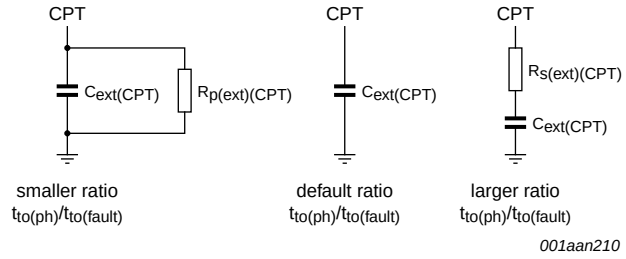


Fig 10. CPT connections

The fault timer incorporates a protection that ensures safe operation conditions if the CPT pin voltage is below $V_{th(scp)(CPT)}$ (shorted to GND) by holding the oscillation frequency at $f_{sw(high)}$.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages referenced to signal ground (GND pin 15); current flow into the IC is positive.

Symbol	Parameter	Conditions	Min	Max	Unit
General					
$R_{ref(IREF)}$	reference resistance on pin IREF		30	36	kΩ
SR	slew rate	pins FSHB, GHHB and SHHB	–4	+4	V/ns
T_{amb}	ambient temperature		–40	+125	°C
T_j	junction temperature		–40	+150	°C
T_{stg}	storage temperature		–55	+150	°C
Voltage					
V_{FSHB}	voltage on pin FSHB	continuous	0	570	V
		t < 0.5 s	0	630	V
		with respect to V_{SHHB}	–0.3	+14	V
V_{GHHB}	voltage on pin GHHB	with respect to V_{SHHB}	–0.3	+14	V
V_{GLHB}	voltage on pin GLHB		–0.3	+14	V
V_{VDD}	voltage on pin VDD		–0.3	+14	V
V_{EOL}	voltage on pin EOL		–9	+9	V
V_{SLHB}	voltage on pin SLHB		–9	+9	V
V_{IFB}	voltage on pin IFB		–5	+5	V
V_{DIM}	voltage on pin DIM		–0.1	+5	V
$V_{PH/EN}$	voltage on pin PH/EN		–0.1	+5	V
V_{VFB}	voltage on pin VFB		–0.1	+5	V
Current					
I_{VDD}	current on pin VDD		-	50	mA
I_{EOL}	current on pin EOL		–1	+1	mA
I_{SLHB}	current on pin SLHB		–1	+1	mA
ElectroStatic Discharge (ESD)					
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM):			
		JEDEC Class 2 for pins: SLHB, IFB, EOL, CIFB, CPT, IREF, VFB, CF, DIM, BOOST, PH/EN, FBPFC, COMPPFC, AUXPFC, GPFC, VDD and GLHB	–2	+2	kV
		JEDEC Class 1C for pins: GHHB, FSHB and SHHB	–1	+1	kV
		Charge Device Model (CDM):			
		JEDEC Class 3 for all pins	–500	+500	V
Latch-up					
I_{lu}		latch-up current [1]	–100	+100	mA

[1] Positive and negative latch-up currents tested at T_j = 150 °C by discharging a 22 µF capacitor though a 50 Ω series resistor with a 350 µH series inductor. Latch-up current values are in accordance with the general quality specification.

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; mounted on a single-sided PCB; SO16 package	120	K/W
		in free air; mounted on a single-sided PCB; DIP16 package	90	K/W

10. Characteristics

Table 6. Characteristics

T_{amb} = 25 °C; settings according to default setting[1]; all voltages referenced to GND; current flow into the IC is positive; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High voltage						
I_{leak}	leakage current	V_{FSHB} = 630 V; V_{GHHB} = 630 V; V_{SHHB} = 630 V; V_{VDD} = 0 V	-	-	2	µA
Start-up						
$V_{startup(VDD)}$	start-up voltage on pin VDD		11.9	12.4	12.9	V
$V_{stop(VDD)}$	stop voltage on pin VDD		9.6	10.0	10.4	V
$V_{hys(VDD)}$	hysteresis voltage on pin VDD		2.1	2.4	2.7	V
$I_{stb(VDD)}$	standby current on pin VDD	V_{VDD} = 11.5 V	0.2	0.24	0.28	mA
$I_{pu(PH/EN)}$	pull-up current on pin PH/EN	Standby or Stop state; $V_{PH/EN}$ = 0.25 V	7.7	9	10.3	µA
$V_{rst(VDD)}$	reset voltage on pin VDD		3.6	4.2	4.8	V
$V_{restart(VDD)}$	restart voltage on pin VDD		6.2	6.5	6.8	V
$I_{restart(VDD)}$	restart current on pin VDD	V_{VDD} = 9 V	0.85	1.1	1.35	mA
$V_{clamp(VDD)}$	clamp voltage on pin VDD	IC off; I_{VDD} = 0.33 mA	13.0	13.4	13.8	V
$I_{clamp(VDD)}$	clamp current on pin VDD	IC off; V_{VDD} = 14.0 V	25	45	-	mA
I_{VDD}	supply current		1.2	1.7	2.2	mA
HB preheat						
$R_{ext(PH/EN)}$	external resistance on pin PH/EN		38.6	-	-	kΩ
$t_{to(ph)}$	preheat time-out time	C_{CPT} = 100 nF	0.8	0.94	1.08	s
$V_{O(PH/EN)}$	output voltage on pin PH/EN	during preheat or ignition state	1.78	1.84	1.9	V
$V_{ctrl(ph)SLHB}$	overcurrent protection threshold voltage on pin SLHB	preheat	0.44	0.48	0.52	V
$I_{ch(CIFB)}$	charge current on pin CIFB	no fault detected; Preheat and Ignition states only; V_{CIFB} = 1.5 V	−10.3	−9.0	−7.7	µA
$I_{dch(CIFB)}$	discharge current on pin CIFB	preheat overcurrent detected; V_{CIFB} = 1.5 V	7.7	9.0	10.3	µA

Table 6. Characteristics *…continued*

T_{amb} = 25 °C; settings according to default setting[1]; all voltages referenced to GND; current flow into the IC is positive; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{sw(ph)}$	preheat switching frequency	$R_{ext(PH/EN)}$ = 40 kΩ; $C_{ext(CF)}$ = 200 pF	93	97.7	102.4	kHz
		$R_{ext(PH/EN)}$ = 100 kΩ; $C_{ext(CF)}$ = 200 pF	62	66	70	kHz
HB lamp ignition						
$f_{sw(high)}/f_{sw(low)}$	high switching frequency to low switching frequency ratio		2.2	2.4	2.6	
$V_{fsw(low)(CIFB)}$	low switching frequency voltage on pin CIFB		-	3.0	-	V
$V_{th(lod)(IFB)}$	lamp on detection threshold voltage on pin IFB		1	1.11	1.22	V
$V_{th(lod)(VFB)}$	lamp on detection threshold voltage on pin VFB		0.9	1.0	1.1	V
$V_{(Vreg-Vth(lod))}$	regulation voltage to lamp-on-detect threshold voltage difference	pin IFB	40	160	250	mV
$t_{d(lod)}$	lamp on detection delay time		2	3	4	ms
HB normal operation						
$f_{sw(low)}$	low switching frequency	C_{CF} = 200 pF	41	43	45	kHz
			20	-	80	kHz
$V_{high(CF)}$	high voltage on pin CF		-	2.5	-	V
$V_{reg(IFB)}$	regulation voltage on pin IFB	V_{CIFB} = 2 V; V_{IFB} > 0 V	1.22	1.27	1.32	V
		V_{CIFB} = 2 V; V_{DIM} = 127 mV; V_{IFB} > 0 V	77	127	177	mV
		V_{CIFB} = 2 V; V_{IFB} < 0 V	−1.34	−1.27	−1.2	V
		V_{CIFB} = 2 V; V_{DIM} = 127 mV; V_{IFB} < 0 V	−197	−127	−57	mV
$I_{ch(low)(CF)}$	low charge current on pin CF		-	47	-	µA
$V_{i(IFB)}$	input voltage on pin IFB	V_{CIFB} = 2 V	−3.1	-	+3.1	V
$R_{i(IFB)}$	input resistance on pin IFB	V_{IFB} = 1 V	-	60	-	kΩ
		V_{IFB} = −1 V	-	30	-	kΩ
$V_{en(PH/EN)}$	enable voltage on pin PH/EN		0.21	0.25	0.29	V
$V_{O(burn)(PH/EN)}$	burn state output voltage on pin PH/EN	Burn state	1.21	1.27	1.33	V
$g_{m(IFB)}$	IFB transconductance	V_{CIFB} = 2 V	14	16.5	19	µA/V
$I_{O(clamp)(PH/EN)}$	output current clamp on pin PH/EN	Preheat, Ignition or Burn states; $V_{PH/EN}$ = 0.2 V	-	-	0.16	mA
HB driver						
$I_{source(GLHB)}$	source current on pin GLHB	V_{GLHB} = 4 V	−105	−90	−75	mA
$R_{sink(GLHB)}$	sink resistance on pin GLHB	V_{GLHB} = 2 V	13.5	16	18.5	Ω
$I_{source(GHHB)}$	source current on pin GHHB	V_{SHHB} = 0 V; V_{GHHB} = 4 V	−105	−90	−75	mA
$R_{sink(GHHB)}$	sink resistance on pin GHHB	V_{SHHB} = 0 V; V_{GHHB} = 2 V	13.5	16	18.5	Ω
t_{no}	non-overlap time		1.25	1.5	1.75	µs
$V_{Fd(bs)}$	bootstrap diode forward voltage	I_{FS} = 5 mA	1.0	1.5	2.0	V

Table 6. Characteristics *…continued*

T_{amb} = 25 °C; settings according to default setting[1]; all voltages referenced to GND; current flow into the IC is positive; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dimming						
$I_{bias(DIM)}$	bias current on pin DIM	V_{DIM} = 1 V	–28	–26	–24	µA
$R_{i(DIM)}$	input resistance on pin DIM	V_{DIM} = 2.5 V	-	30	-	kΩ
HB protection						
$V_{th(sat)(SLHB)}$	saturation threshold voltage on pin SLHB		2.35	2.5	2.65	V
$t_{d(det)sat}$	saturation detection delay time	Burn state	-	0.3	-	µs
$t_{leb(SLHB)}$	leading edge blanking time on pin SLHB		260	340	420	ns
$I_{add(CF)}$	additional current on pin CF	$V_{SLHB} > V_{th(sat)SLHB}$; V_{CF} = 2 V	–107	–96	–85	µA
$I_{bias(SLHB)}$	bias current on pin SLHB	V_{SLHB} = 2.5 V	–10	–8.5	–7	µA
$V_{th(ocd)(IFB)}$	overcurrent detection threshold voltage on pin IFB		2.8	3.0	3.2	V
$V_{th(osp)(VFB)}$	open/short protection threshold voltage on pin VFB		40	80	120	mV
$V_{th(ov)(VFB)}$	overvoltage threshold voltage on pin VFB		2.4	2.5	2.6	V
$t_{det(fault)}$	fault detection time		-	125	-	µs
		overvoltage extra or capacitive mode during burn state	-	50	-	µs
$t_{rel(fault)}$	fault release time		-	1	-	ms
$V_{th(ovextra)(VFB)}$	overvoltage extra threshold voltage on pin VFB		3.2	3.35	3.5	V
$I_{bias(VFB)}$	bias current on pin VFB		2.3	2.6	2.9	µA
$V_{th(low)EOL}$	low threshold voltage on pin EOL		1	1.1	1.2	V
$V_{th(high)EOL}$	high threshold voltage on pin EOL		2	2.25	2.5	V
$I_{bias(EOL)}$	bias current on pin EOL	V_{EOL} = 1.65 V	15.4	16.2	17	µA
$V_{th(oveol)(VFB)}$	overvoltage end-of-life threshold voltage on pin VFB	UBA2017 or UBA2017A pin DIM open	0.8	0.88	0.96	V
		UBA2017A				
		V_{DIM} = 1.0 V	0.92	1.0	1.08	V
		V_{DIM} = 0.5 V	1.15	1.23	1.31	V
$V_{en(oveol)(DIM)}$	overvoltage end-of-life enable voltage on pin DIM	UBA2017A	0.21	0.25	0.29	V
$V_{th(hswp)SHHB}$	hard switching protection threshold voltage on pin SHHB	f_{sw} = 50 kHz	-	100	-	V
$V_{th(cm)SHHB}$	capacitive mode detection threshold voltage on pin SHHB	$t_{no(LH)}$	-	30	-	V/µs
$V_{th(scp)(CPT)}$	short-circuit protection threshold voltage on pin CPT		80	120	160	mV
$R_{par(ext)(CPT)}$	external parallel resistance on pin CPT		700	-	-	kΩ
$R_{s(ext)(CPT)}$	external series resistance on pin CPT		-	-	40	kΩ
$t_{to(fault)}$	fault time-out time	C_{CPT} = 100 nF	0.16	0.19	0.22	s

Table 6. Characteristics *...continued*

T_{amb} = 25 °C; settings according to default setting[1]; all voltages referenced to GND; current flow into the IC is positive; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{to(ph)}/t_{to(fault)}$	ratio between preheat time-out time and fault time-out time	$R_{par(ext)}$ = 700 kΩ; $R_{s(ext)}$ not connected (short)	3	3.4	3.8	
		$R_{par(ext)}$ not connected (open); $R_{s(ext)}$ not connected (short)	4.7	5.2	5.7	
		$R_{par(ext)}$ not connected (open); $R_{s(ext)}$ = 40 kΩ	9	11.5	14	
Temperature protection						
$T_{th(act)otp}$	overtemperature protection activation threshold temperature		120	140	160	°C
$T_{th(rel)otp}$	overtemperature protection release threshold temperature		65	80	95	°C

[1] Default setting; see Table 7.

Table 7. Default settings for characteristics

Pin name	Pin	Application
SLHB	1	connected to ground
IFB	2	connected to ground
EOL	3	connected to a 1.6 V test supply
VFB	4	connected to a 0.5 V test supply
IREF	5	connected via a 33 kΩ resistor to ground
CIFB	6	connected via a 100 nF capacitor to ground
CF	7	connected via a 200 pF C0G (NP0) capacitor to ground
CPT	8	connected via a 100 nF capacitor to ground
DIM	9	connected via a 100 pF capacitor to ground
PH/EN	10	not connected
GND	11	connected to ground
VDD	12	connected to a 13 V test supply
GLHB	13	not connected (open)
SHHB	14	connected to ground
FSHB	15	connected to a 13 V test supply
GHHB	16	not connected (open)

11. Application information

11.1 Connecting the IC in an application

A 33 kΩ resistor must be connected between pin IREF and GND. The tolerance of this resistor adds to any current related tolerances of the IC, including $f_{sw(low)}$. No other components can be connected to pin IREF.

The tolerance and temperature dependency of the capacitor connected between pin CF and GND will add to the tolerance on $f_{sw(low)}$.

A Small decoupling capacitor (about 100 pF) is recommended on pin IFB close to the IC.

Normal sized decoupling capacitors (about 10 nF) are recommended on pins DIM and EOL.

The capacitors at pins CF, CPT, FSHB and VDD should also be placed close to the IC.

A capacitor between pin CIFB and GND of at least 470 pF is needed for stability of the low switching frequency.

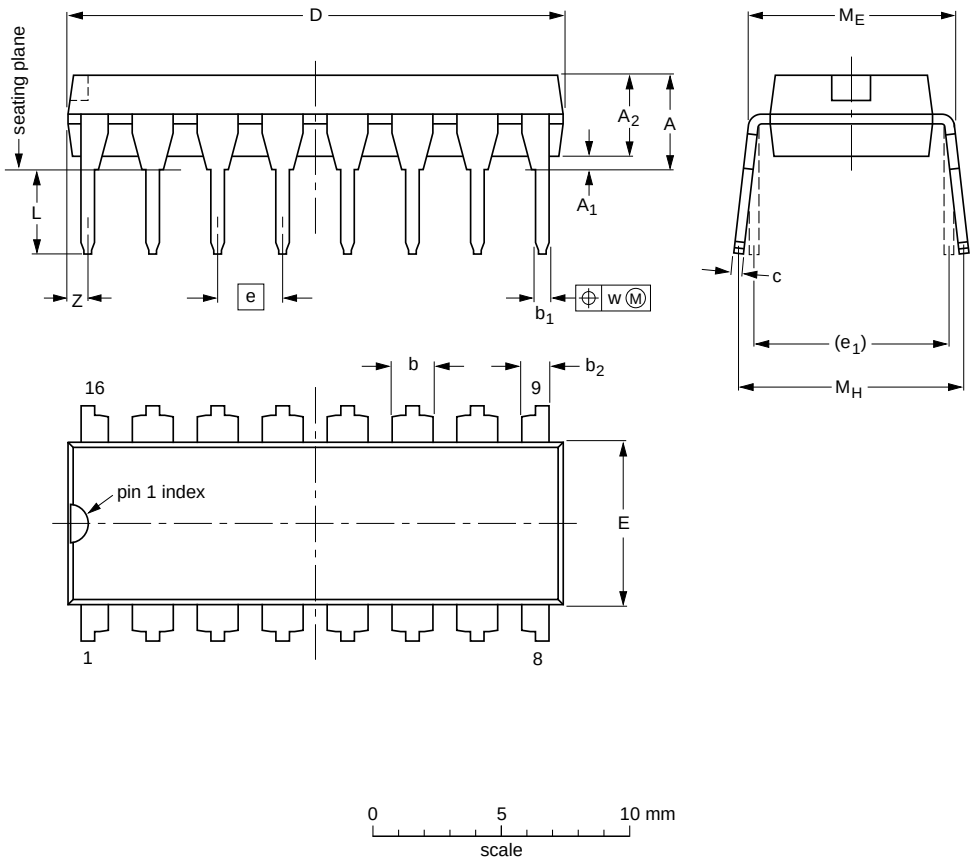
A capacitor between pin VDD and GND of at least 10 nF is needed for stability of the internal VDD voltage clamp. However, for reliable operation of the IC a low ESR type of at least 470 nF is recommended.

A capacitor between pin FSHB and SHHB is needed to supply the high-side driver. The recommended value for this capacitor is $\frac{1}{5}$ of the value of the capacitor at VDD.

A series resistor of at least 1 kΩ is recommended on pin SLHB.

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

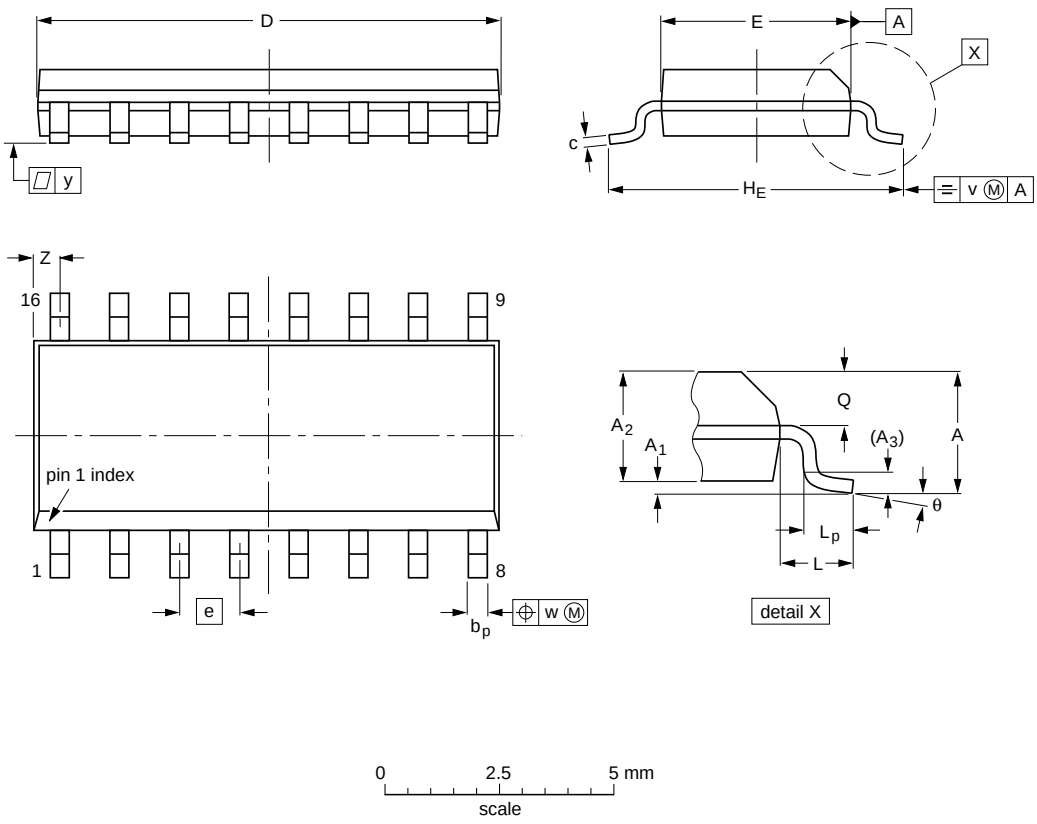
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 11. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT109-1 (SO16)

13. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UBA2017 v.2	20120515	Product data sheet	-	UBA2017 v.1
UBA2017 v.1	20120330	Preliminary data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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16. Contents

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