

PEMD2; PIMD2; PUMD2

NPN/PNP resistor-equipped transistors;
R1 = 22 k Ω , R2 = 22 k Ω

Rev. 07 — 24 September 2008

Product data sheet

1. Product profile

1.1 General description

NPN/PNP Resistor-Equipped Transistors (RET).

Table 1. Product overview

Type number	Package		PNP/PNP complement	NPN/PNP complement
	NXP	JEITA		
PEMD2	SOT666	-	PEMB1	PEMH1
PIMD2	SOT457	SC-74	-	-
PUMD2	SOT363	SC-88	PUMB1	PUMH1

1.2 Features

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

1.3 Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current		-	-	100	mA
R1	bias resistor 1 (input)		15.4	22	28.6	k Ω
R2/R1	bias resistor ratio		0.8	1	1.2	

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
PEMD2; PUMD2			
1	GND (emitter) TR1	<p>001aab555</p>	<p>006aaa143</p>
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		
PIMD2			
1	GND (emitter) TR2	<p>006aab235</p>	<p>006aab235</p>
2	input (base) TR2		
3	output (collector) TR1		
4	GND (emitter) TR1		
5	input (base) TR1		
6	output (collector) TR2		

3. Ordering information

Table 4. Ordering information

Type number	Package		Version
	Name	Description	
PEMD2	-	plastic surface-mounted package; 6 leads	SOT666
PIMD2	SC-74	plastic surface-mounted package (TSOP6); 6 leads	SOT457
PUMD2	SC-88	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 5. Marking codes

Type number	Marking code ^[1]
PEMD2	D4
PIMD2	M5
PUMD2	D*2

- [1] * = -: made in Hong Kong
 * = p: made in Hong Kong
 * = t: made in Malaysia
 * = W: made in China

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity					
V _{CBO}	collector-base voltage	open emitter	-	50	V
V _{CEO}	collector-emitter voltage	open base	-	50	V
V _{EBO}	emitter-base voltage	open collector	-	10	V
V _I	input voltage TR1				
	positive		-	+40	V
	negative		-	-10	V
	input voltage TR2				
	positive		-	+10	V
	negative		-	-40	V
I _O	output current		-	100	mA
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms	-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]		
	PEMD2 (SOT666)		[2]	200	mW
	PIMD2 (SOT457)		-	300	mW
	PUMD2 (SOT363)		-	200	mW
T _j	junction temperature		-	150	°C
T _{amb}	ambient temperature		-65	+150	°C
T _{stg}	storage temperature		-65	+150	°C

Table 6. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per device					
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]		
	PEMD2 (SOT666)		[2] -	300	mW
	PIMD2 (SOT457)		-	600	mW
	PUMD2 (SOT363)		-	300	mW

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]			
	PEMD2 (SOT666)		[2] -	-	625	K/W
	PIMD2 (SOT457)		-	-	417	K/W
	PUMD2 (SOT363)		-	-	625	K/W
Per device						
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]			
	PEMD2 (SOT666)		[2] -	-	416	K/W
	PIMD2 (SOT457)		-	-	208	K/W
	PUMD2 (SOT363)		-	-	416	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

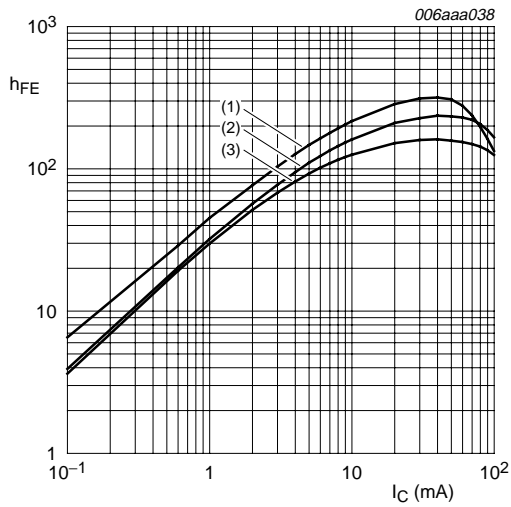
[2] Reflow soldering is the only recommended soldering method.

7. Characteristics

Table 8. Characteristics

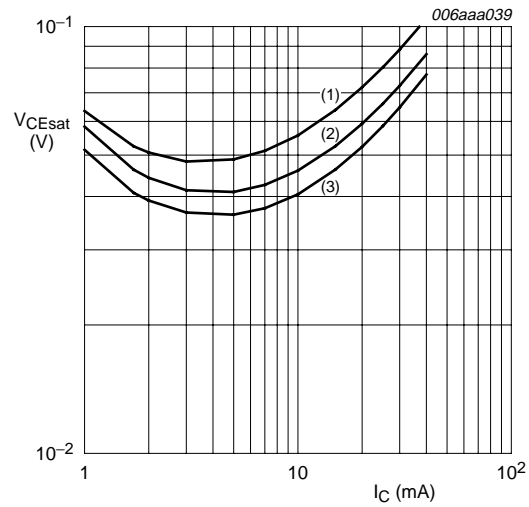
$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; I_B = 0\text{ A}$	-	-	1	μA
		$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	-	-	180	μA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 5\text{ mA}$	60	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}$	-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}; I_C = 100\text{ }\mu\text{A}$	-	1.1	0.8	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}; I_C = 5\text{ mA}$	2.5	1.7	-	V
R1	bias resistor 1 (input)		15.4	22	28.6	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$V_{CB} = 10\text{ V}; I_E = i_e = 0\text{ A}; f = 1\text{ MHz}$				
	TR1 (NPN)		-	-	2.5	pF
	TR2 (PNP)		-	-	3	pF



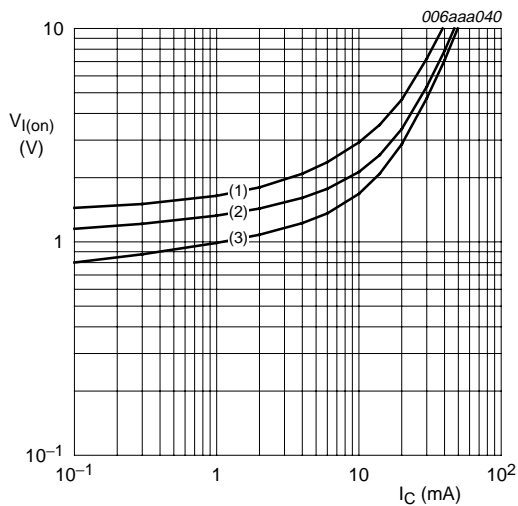
$V_{CE} = 5 \text{ V}$
 (1) $T_{amb} = 150 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig 1. TR1 (NPN): DC current gain as a function of collector current; typical values



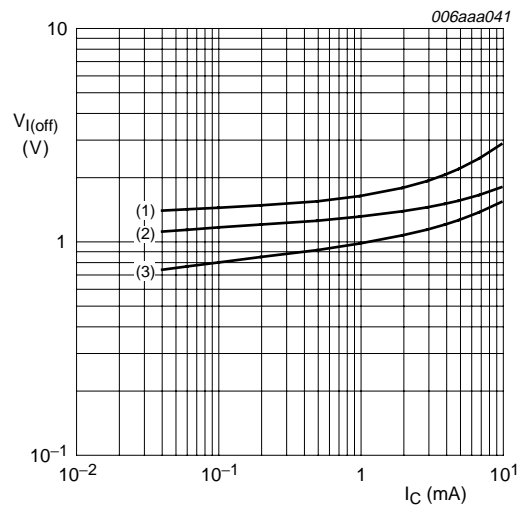
$I_C/I_B = 20$
 (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig 2. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



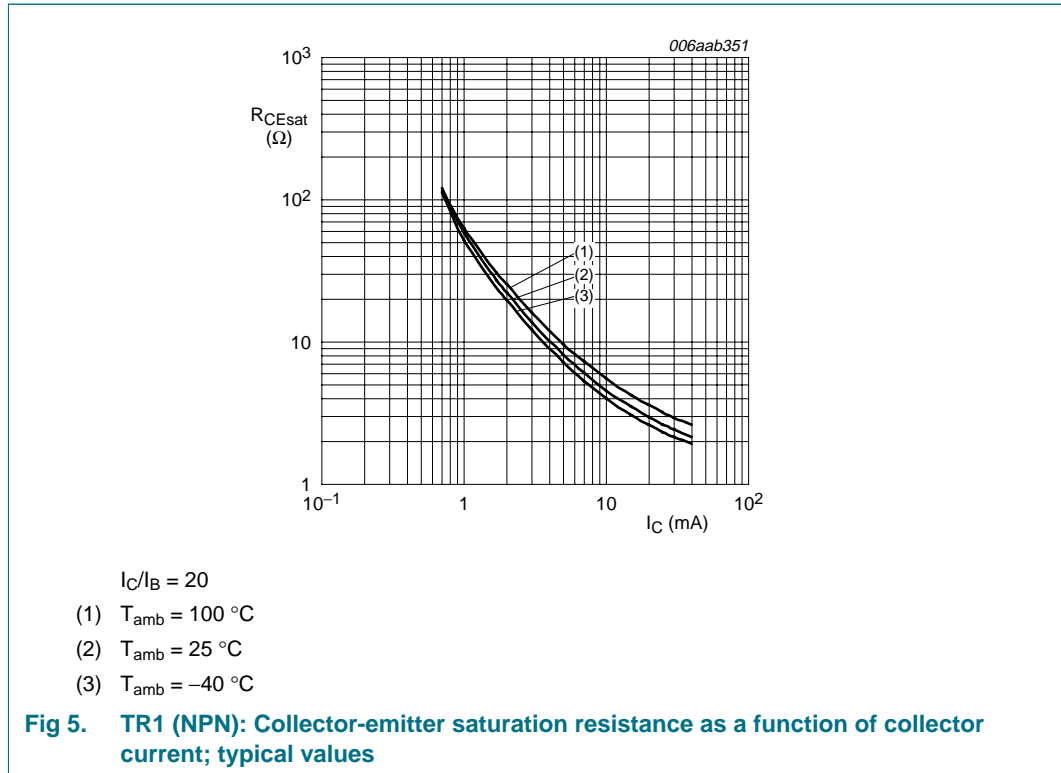
$V_{CE} = 0.3 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

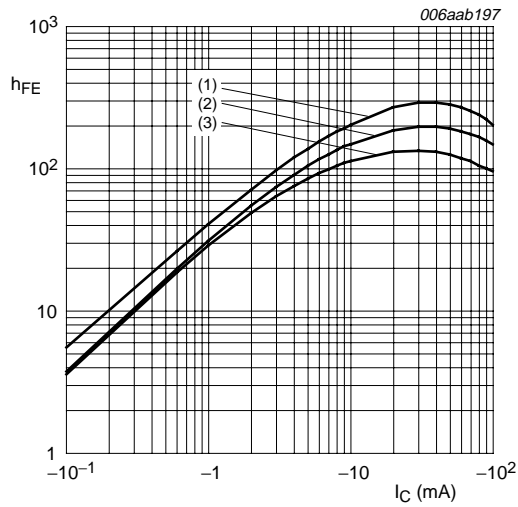
Fig 3. TR1 (NPN): On-state input voltage as a function of collector current; typical values



$V_{CE} = 5 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

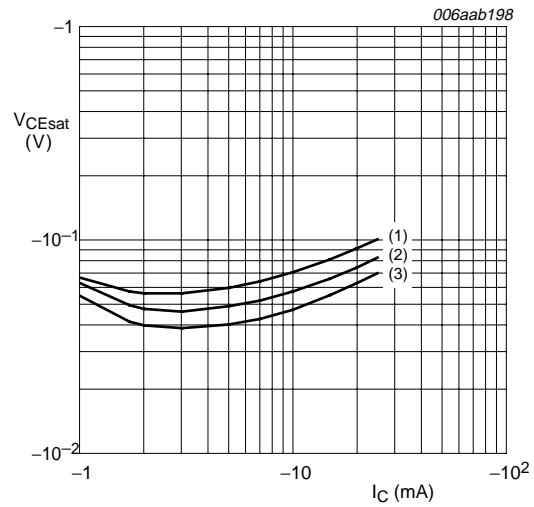
Fig 4. TR1 (NPN): Off-state input voltage as a function of collector current; typical values





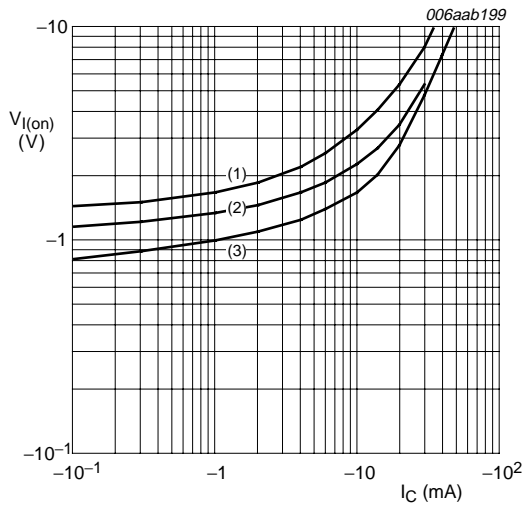
- $V_{CE} = -5\text{ V}$
- (1) $T_{amb} = 150\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = -40\text{ °C}$

Fig 6. TR2 (PNP): DC current gain as a function of collector current; typical values



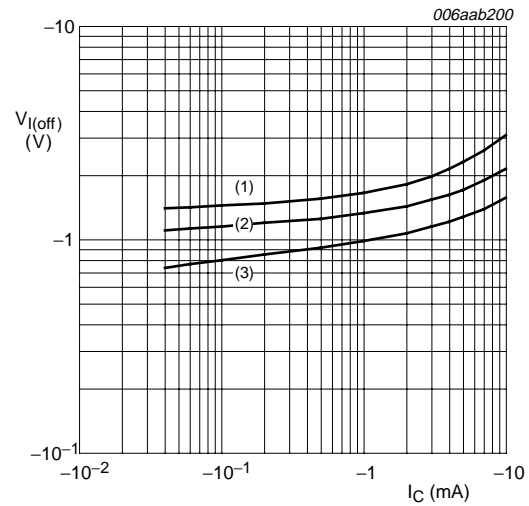
- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = -40\text{ °C}$

Fig 7. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



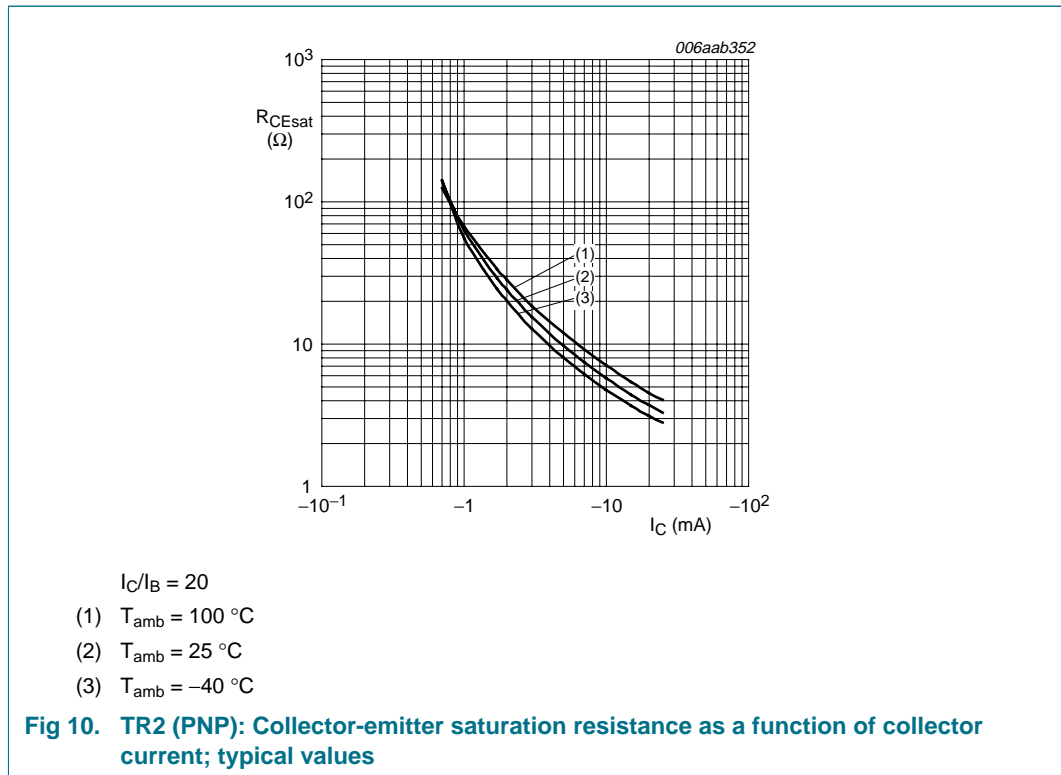
- $V_{CE} = -0.3\text{ V}$
- (1) $T_{amb} = -40\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = 100\text{ °C}$

Fig 8. TR2 (PNP): On-state input voltage as a function of collector current; typical values

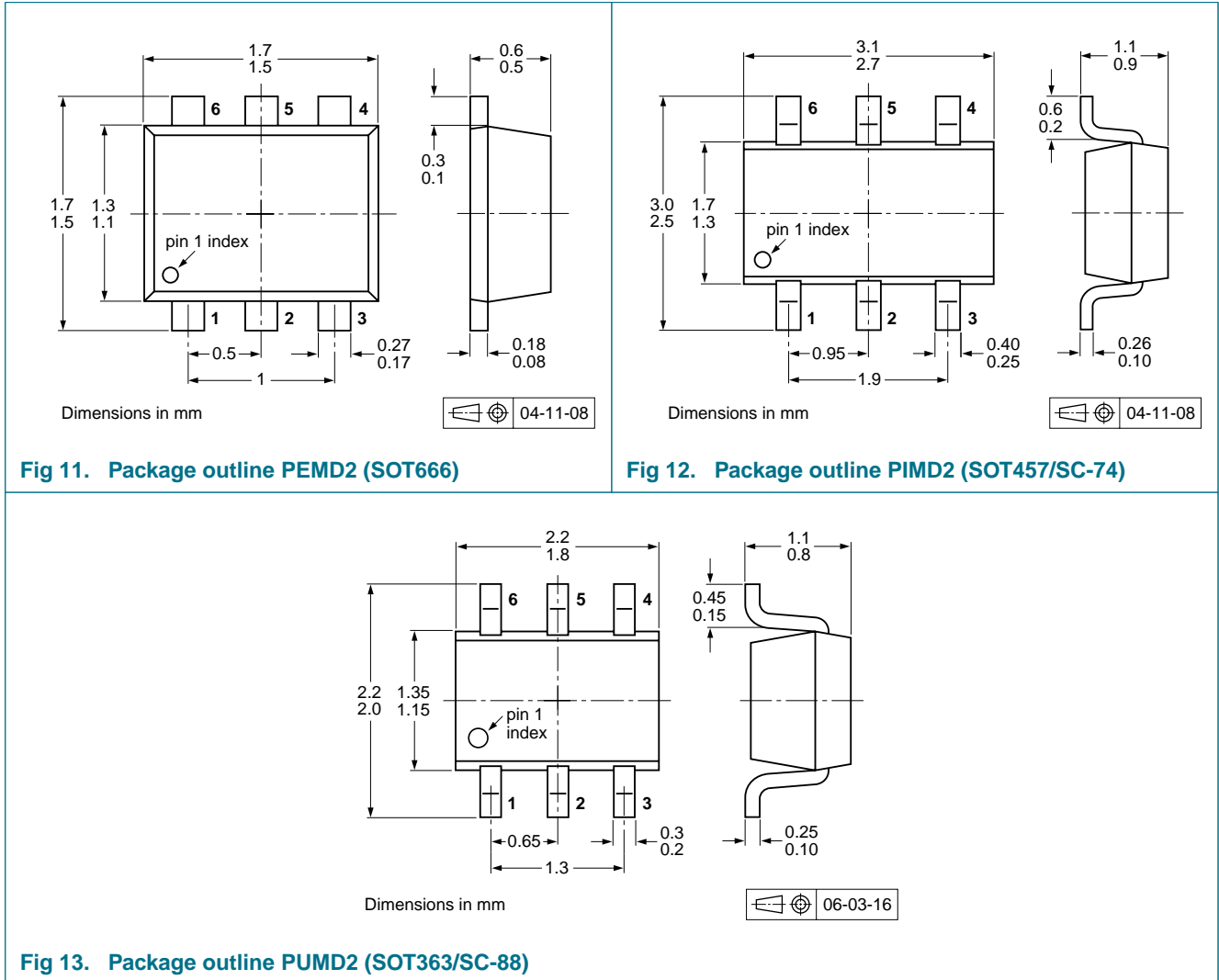


- $V_{CE} = -5\text{ V}$
- (1) $T_{amb} = -40\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = 100\text{ °C}$

Fig 9. TR2 (PNP): Off-state input voltage as a function of collector current; typical values



8. Package outline



9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

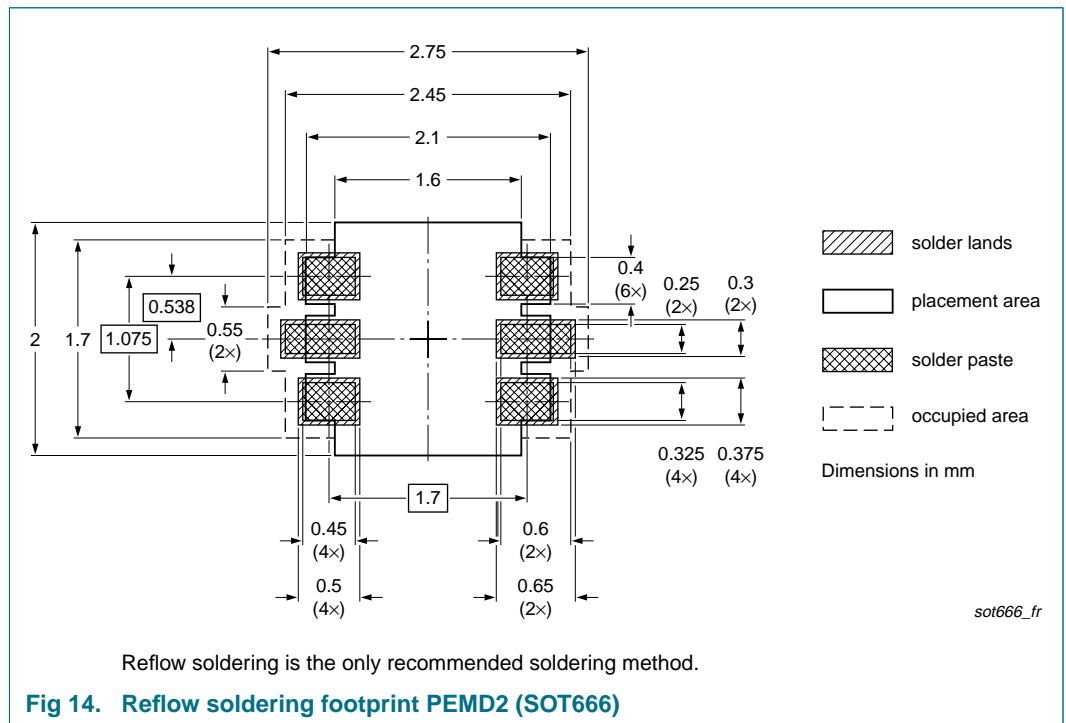
Type number	Package	Description	Packing quantity			
			3000	4000	8000	10000
PEMD2	SOT666	2 mm pitch, 8 mm tape and reel	-	-	-315	-
		4 mm pitch, 8 mm tape and reel	-	-115	-	-
PIMD2	SOT457	4 mm pitch, 8 mm tape and reel; T1 ^[2]	-115	-	-	-135
		4 mm pitch, 8 mm tape and reel; T2 ^[3]	-125	-	-	-165
PUMD2	SOT363	4 mm pitch, 8 mm tape and reel; T1 ^[2]	-115	-	-	-135
		4 mm pitch, 8 mm tape and reel; T2 ^[3]	-125	-	-	-165

[1] For further information and the availability of packing methods, see [Section 13](#).

[2] T1: normal taping

[3] T2: reverse taping

10. Soldering



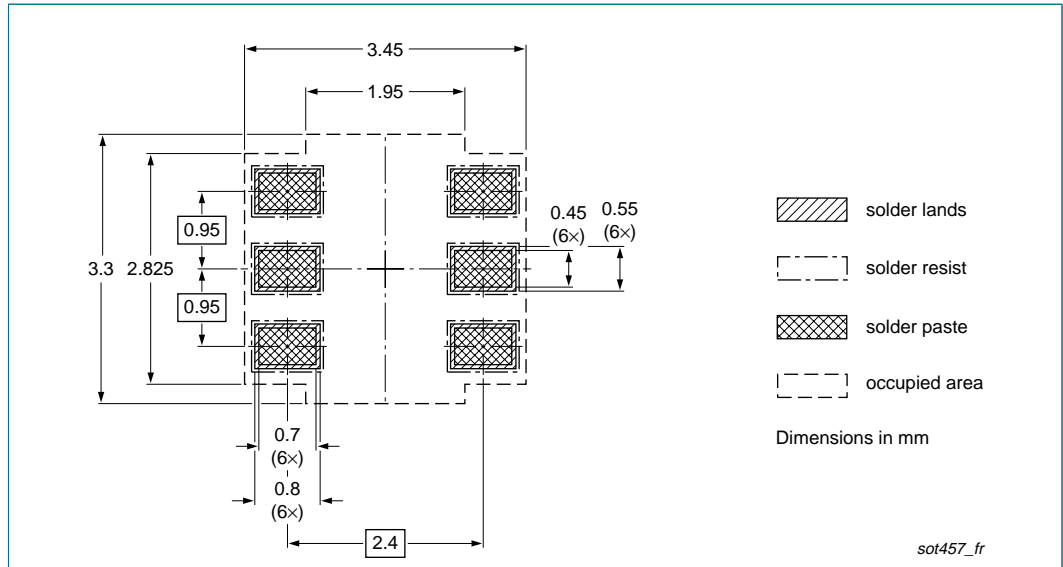


Fig 15. Reflow soldering footprint PIMD2 (SOT457/SC-74)

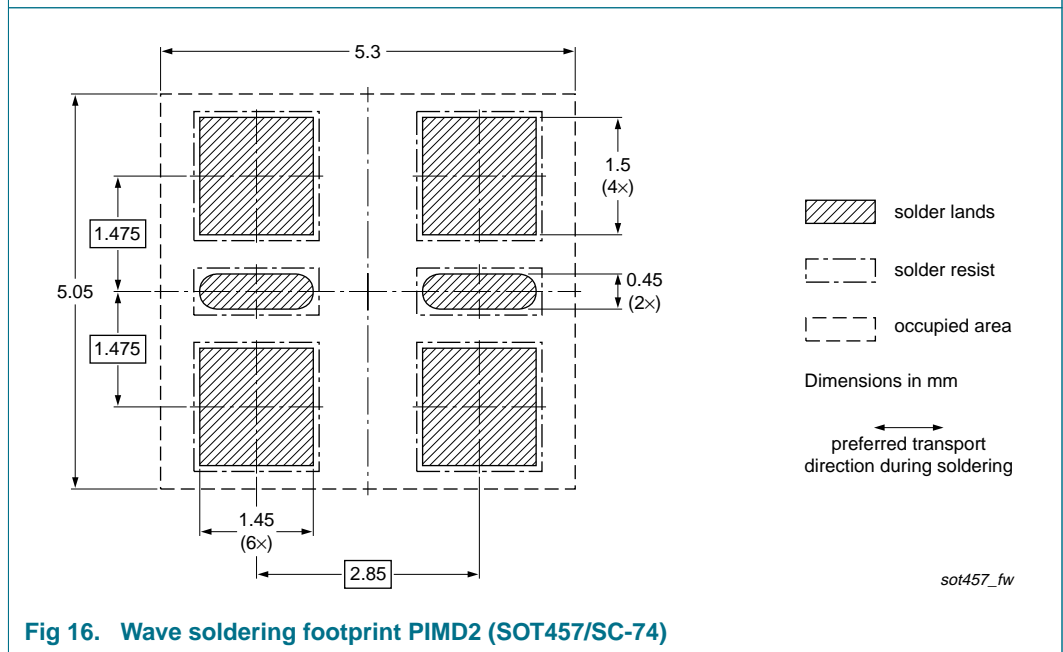


Fig 16. Wave soldering footprint PIMD2 (SOT457/SC-74)

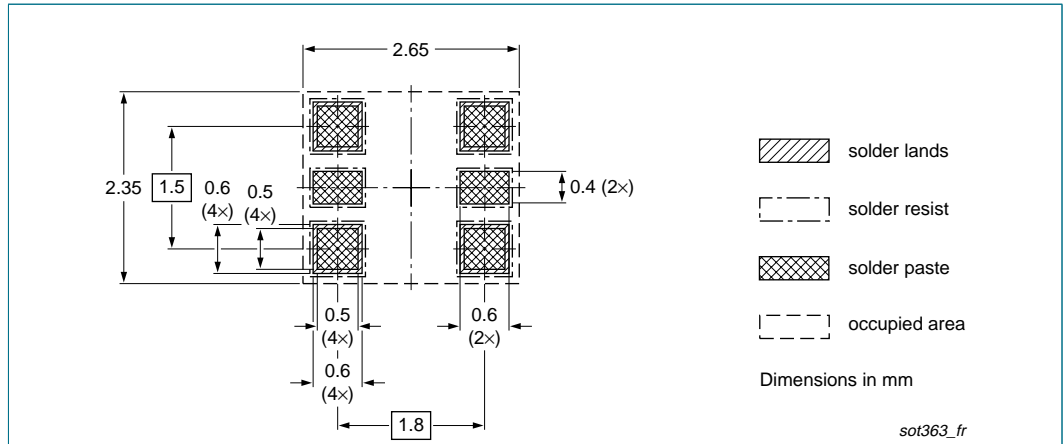


Fig 17. Reflow soldering footprint PUMD2 (SOT363/SC-88)

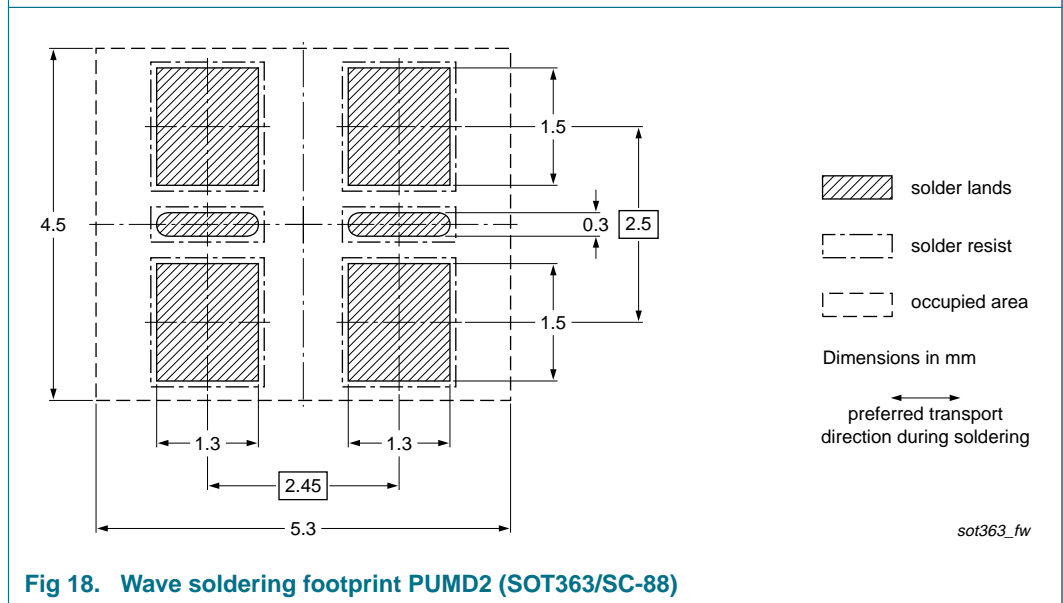


Fig 18. Wave soldering footprint PUMD2 (SOT363/SC-88)

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PEMD2_PIMD2_PUMD2_7	20080924	Product data sheet	-	PEMD2_PIMD2_PUMD2_6
Modifications: <ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 8 "Characteristics": V_{CEsat} unit corrected • Figure 1, 2, 3, 4, 5, 6, 7, 8, 9 and 10: added • Section 12 "Legal information": updated 				
PEMD2_PIMD2_PUMD2_6	20040421	Product specification	-	PEMD2_PIMD2_PUMD2_5

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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