Zynq-7000 All Programmable SoC (XC7Z010 and XC7Z020): DC and AC Switching Characteristics

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Introduction

The Zynq®-7000 All Programmable SoCs are available in -3, -2, and -1 speed grades, with -3 having the highest performance. Zynq-7000 device DC and AC characteristics are specified in commercial, extended, and industrial temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices are available in the commercial, extended, or industrial temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Zynq-7000 AP SoC (XC7Z010 and XC7Z020) data sheet, part of an overall set of documentation on the Zynq-7000 AP SoCs, is available on the Xilinx website at www.xilinx.com/zynq. All specifications are subject to change without notice.

DC Characteristics

Table 1: **Absolute Maximum Ratings(1)**

Symbol	Description	Min	Max	Units
Processing System (PS)				
V_{CCPINT}	PS internal logic supply	–0.5	1.1	V
V_{CCPAUX}	PS auxiliary supply voltage	–0.5	2.0	V
V_{CCPLL}	PS PLL supply	–0.5	2.0	V
V_{CCO_DDR}	PS DDR I/O supply voltage	–0.5	2.0	V
V_{CCO_MIO}(2)	PS MIO I/O supply voltage	–0.5	3.6	V
V_{PREF}	PS input reference voltage	–0.5	2.0	V
V_{PIN}(2)(3)(4)(5)	PS MIO I/O input voltage	–0.40	V_{CCO_MIO} + 0.55	V
	PS DDR I/O input voltage	–0.55	V_{CCO_DDR} + 0.55	V
Programmable Logic (PL)				
V_{CCINT}	PL internal supply voltage	–0.5	1.1	V
V_{CCAUX}	PL auxiliary supply voltage	–0.5	2.0	V
V_{CCBRAM}	PL supply voltage for the block RAM memories	–0.5	1.1	V
V_{CCO}	PL supply voltage for 3.3V HR I/O banks	–0.5	3.6	V
V_{REF}	Input reference voltage	–0.5	2.0	V
V_{IN}(3)(4)(5)	I/O input voltage for 3.3V HR I/O banks	–0.40	V_{CCO} + 0.55	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(6)	–0.40	2.625	V
V_{CCBATT}	Key memory battery backup supply	–0.5	2.0	V

Table 1: **Absolute Maximum Ratings(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
XADC				
V_{CCADC}	XADC supply relative to GNDADC	–0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC	–0.5	2.0	V
Temperature				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies(7)	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies(7)	–	+260	°C
T_j	Maximum junction temperature(7)	–	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. Applies to both MIO supply banks V_{CCO_MIO0} and V_{CCO_MIO1}.
3. The lower absolute voltage specification always applies.
4. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471) or the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585).
5. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4.
6. See Table 11 for TMDS_33 specifications.
7. For soldering guidelines and thermal considerations, see the *Zynq-7000 All Programmable SoC Packaging and Pinout Specification* (UG865).

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
PS					
V_{CCPINT}	PS internal supply voltage	0.95	1.00	1.05	V
V_{CCPAUX}	PS auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCPLL}	PS PLL supply	1.71	1.80	1.89	V
V_{CCO_DDR}	PS DDR I/O supply voltage	1.14	–	1.89	V
V_{CCO_MIO}(3)	PS MIO I/O supply voltage for MIO banks	1.71	–	3.465	V
V_{PIN}(4)	PS DDR and MIO I/O input voltage	–0.20	–	V_{CCO_DDR} + 0.20 V_{CCO_MIO} + 0.20	V
PL					
V_{CCINT}	PL internal supply voltage	0.95	1.00	1.05	V
V_{CCAUX}	PL auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCBRAM}	PL block RAM supply voltage	0.95	1.00	1.05	V
V_{CCO}(5)(6)	PL supply voltage for 3.3V HR I/O banks	1.14	–	3.465	V
V_{IN}(4)	I/O input voltage	–0.20	–	V_{CCO} + 0.20	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(7)	–0.20	–	2.625	V
I_{IN}(8)	Maximum current through any (PS or PL) pin in a powered or unpowered bank when forward biasing the clamp diode	–	–	10	mA
V_{CCBATT}(9)	Battery voltage	1.0	–	1.89	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C

Notes:

1. All voltages are relative to ground. The PL and PS share a common ground.
2. For the design of the power distribution system consult the *Zynq-7000 All Programmable SoC PCB Design and Pin Planning Guide* (UG933).
3. Applies to both MIO supply banks V_{CCO_MIO0} and V_{CCO_MIO1}.
4. The lower absolute voltage specification always applies.
5. Configuration data is retained even if V_{CCO} drops to 0V.
6. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
7. See Table 11 for TMDS_33 specifications.
8. A total of 200 mA per PS or PL bank should not be exceeded.
9. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ(1)	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	15	µA
C_{IN}(2)	PL die input capacitance at the pad	–	–	8	pF
C_{PIN}(2)	PS die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V	90	–	330	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	68	–	250	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	34	–	220	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	23	–	150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	12	–	120	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V	68	–	330	µA
	Pad pull-down (when selected) @ V_{IN} = 1.8V	45	–	180	µA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT}(3)	Battery supply current	–	–	150	nA
R_{IN_TERM}(4)	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices.	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices.	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices.	44	60	83	Ω

Table 3: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ(1)	Max	Units
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O and 3.3V HR I/O Banks(1)**

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
V_{CCO} + 0.55	100	–0.40	100
		–0.45	61.7
		–0.50	25.8
		–0.55	11.0
V_{CCO} + 0.60	46.6	–0.60	4.77
V_{CCO} + 0.65	21.2	–0.65	2.10
V_{CCO} + 0.70	9.75	–0.70	0.94
V_{CCO} + 0.75	4.55	–0.75	0.43
V_{CCO} + 0.80	2.15	–0.80	0.20
V_{CCO} + 0.85	1.02	–0.85	0.09
V_{CCO} + 0.90	0.49	–0.90	0.04
V_{CCO} + 0.95	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 5: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
$I_{CCPINTQ}$	PS quiescent V_{CCPINT} supply current	XC7Z010	122	122	122	mA
		XC7Z020	122	122	122	mA
$I_{CCPAUXQ}$	PS quiescent V_{CCPAUX} supply current	XC7Z010	13	13	13	mA
		XC7Z020	13	13	13	mA
I_{CCDDRQ}	PS quiescent V_{CCO_DDR} supply current	XC7Z010	4	4	4	mA
		XC7Z020	4	4	4	mA
I_{CCINTQ}	PL quiescent V_{CCINT} supply current	XC7Z010	34	34	34	mA
		XC7Z020	78	78	78	mA
I_{CCAUXQ}	PL quiescent V_{CCAUX} supply current	XC7Z010	18	18	18	mA
		XC7Z020	38	38	38	mA
I_{CCOQ}	PL quiescent V_{CCO} supply current	XC7Z010	3	3	3	mA
		XC7Z020	3	3	3	mA
$I_{CCBRAMQ}$	PL quiescent V_{CCBRAM} supply current	XC7Z010	3	3	3	mA
		XC7Z020	6	6	6	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

PS Power-On/Off Power Supply Requirements

The recommended power-on sequence is V_{CCPINT}, V_{CCPAUX} and V_{CCPLL} together, then the PS V_{CCO} supplies (V_{CCO_MIO0}, V_{CCO_MIO1}, and V_{CCO_DDR}) to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCPAUX}, V_{CCPLL} and the PS V_{CCO} supplies (V_{CCO_MIO0}, V_{CCO_MIO1}, and V_{CCO_DDR}) have the same recommended voltage levels, then they can be powered by the same supply and ramped simultaneously. Xilinx recommends powering V_{CCPLL} with the same supply as V_{CCPAUX}, with an optional ferrite bead filter.

For V_{CCO_MIO0} and V_{CCO_MIO1} voltages of 3.3V:

- The voltage difference between V_{CCO_MIO0} /V_{CCO_MIO1} and V_{CCPAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence for the PL is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

PS—PL Power Sequencing

The PS and PL power supplies are fully independent. PS power supplies (V_{CCPINT}, V_{CCPAUX}, V_{CCPLL}, V_{CCO_DDR}, V_{CCO_MIO0}, and V_{CCO_MIO1}) can be powered before or after the PL power supplies (V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCO}, and V_{CCADC}). The PS and PL power regions are isolated to prevent damage.

Power Supply Requirements

Table 6 shows the minimum current, in addition to I_{CCQ}, that is required by Zynq-7000 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four PL supplies have passed through their power-on reset threshold voltages. The Zynq-7000 device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 6: **Power-On Current for Zynq-7000 Devices(1)**

Device	$I_{CCPINTMIN}$ Typ(2)	$I_{CCPAUXMIN}$ Typ(2)	$I_{CCDDRMIN}$ Typ(2)	$I_{CCINTMIN}$ Typ(2)	$I_{CCAUXMIN}$ Typ(2)	I_{CCOMIN} Typ(2)	$I_{CCBRAMMIN}$ Typ(2)	Units
XC7Z010	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +40	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA
XC7Z020	$I_{CCPINTQ}$ +70	$I_{CCPAUXQ}$ +40	I_{CCDDRQ} + 100 mA per bank	I_{CCINTQ} +70	I_{CCAUXQ} +60	I_{CCOQ} + 90 mA per bank	$I_{CCBRAMQ}$ +40	mA

Notes:

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.
2. Typical values are specified at nominal voltage, 25°C.

Table 7: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
$T_{VCCPINT}$	Ramp time from GND to 90% of V_{CCPINT}		0.2	50	ms
$T_{VCCPAUX}$	Ramp time from GND to 90% of V_{CCPAUX}		0.2	50	ms
T_{VCCO_DDR}	Ramp time from GND to 90% of V_{CCO_DDR}		0.2	50	ms
T_{VCCO_MIO}	Ramp time from GND to 90% of V_{CCO_MIO}		0.2	50	ms
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$ and $V_{CCO\_MIO} - V_{CCPAUX} > 2.625V$	$T_j = 100°C$(1)	–	500	ms
		$T_j = 85°C$(1)	–	800	

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with worst case V_{CCO} of 3.465V.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 8: **PS DC Input and Output Levels(1)**

Bank	I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
		V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
MIO	LVCMOS18	–0.300	35% V_{CCO_MIO}	65% V_{CCO_MIO}	V_{CCO_MIO} + 0.300	0.450	V_{CCO_MIO} – 0.450	8	–8
MIO	LVCMOS25	–0.300	0.700	1.700	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} – 0.400	8	–8
MIO	LVCMOS33	–0.300	0.800	2.000	3.450	0.400	V_{CCO_MIO} – 0.400	8	–8
MIO	HSTL_I_18	–0.300	V_{PREF} – 0.100	V_{PREF} + 0.100	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} – 0.400	8	–8
DDR	SSTL18_I	–0.300	V_{PREF} – 0.125	V_{PREF} + 0.125	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.470	V_{CCO_DDR}/2 + 0.470	8	–8
DDR	SSTL15	–0.300	V_{PREF} – 0.100	V_{PREF} + 0.100	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.175	V_{CCO_DDR}/2 + 0.175	13.0	–13.0
DDR	SSTL135	–0.300	V_{PREF} – 0.090	V_{PREF} + 0.090	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 – 0.150	V_{CCO_DDR}/2 + 0.150	13.0	–13.0
DDR	HSUL_12	–0.300	V_{PREF} – 0.130	V_{PREF} + 0.130	V_{CCO_DDR} + 0.300	20% V_{CCO_DDR}	80% V_{CCO_DDR}	0.1	–0.1

Notes:

1. Tested according to relevant specifications.

Table 9: **PS Complementary Differential DC Input and Output Levels**

Bank	I/O Standard	V_{ICM}(1)			V_{ID}(2)		V_{OL}(3)	V_{OH}(4)	I_{OL}	I_{OH}
		V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DDR	DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DDR	DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO_DDR}/2) – 0.150	(V_{CCO_DDR}/2) + 0.150	13.0	–13.0
DDR	DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO_DDR}/2) – 0.175	(V_{CCO_DDR}/2) + 0.175	13.0	–13.0
DDR	DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO_DDR}/2) – 0.470	(V_{CCO_DDR}/2) + 0.470	8.00	–8.00

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q–$\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

PL I/O Levels

Table 10: **SelectIO DC Input and Output Levels**[1][2]

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.00	–8.00
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.00	–8.00
HSTL_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16.00	–16.00
HSTL_II_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16.00	–16.00
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.10	–0.10
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.7	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS33	–0.300	0.8	2.000	3.450	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVTTL	–0.300	0.8	2.000	3.450	0.400	2.400	Note 5	Note 5
MOBILE_DDR	–0.300	20% V_{CCO}	80% V_{CCO}	V_{CCO} + 0.300	10% V_{CCO}	90% V_{CCO}	0.10	–0.10
PCI33_3	–0.400	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.500	10% V_{CCO}	90% V_{CCO}	1.50	–0.50
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	13.00	–13.00
SSTL135_R	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.90	–8.90
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	13.00	–13.00
SSTL15_R	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	8.90	–8.90
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	8.00	–8.00
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.600	V_{CCO}/2 + 0.600	13.40	–13.40

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* (UG471).

Table 11: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]			V_{OCM}[3]			V_{OD}[4]		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO}–0.405	V_{CCO}–0.300	V_{CCO}–0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q–$\overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q–$\overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.

Table 12: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]		V_{OL}[3]	V_{OH}[4]	I_{OL}	I_{OH}
	V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q–$\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 13: **LVDS_25 DC Specifications**[1]

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.5	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.00	1.25	1.425	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input common-mode voltage		0.3	1.2	1.425	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the ISE® Design Suite 14.5 v1.06 and Vivado® Design Suite 2013.1 v1.06 for the -3, -2, and -1 speed grades.

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq-7000 devices.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 14 correlates the current status of each Zynq-7000 device on a per speed grade basis.

Table 14: **Zynq-7000 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7Z010			-3, -2, -1
XC7Z020			-3, -2, -1

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 15 lists the production released Zynq-7000 device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 15: **Zynq-7000 Device Production Software and Speed Specification Release**

Device	Speed Grade Designations		
	-3	-2	-1
XC7Z010	ISE 14.5 v1.06 and Vivado 2013.1 v1.06	ISE 14.4 and the 14.4 device pack v1.05	
XC7Z020	ISE 14.5 v1.06 and Vivado 2013.1 v1.06	ISE 14.4 and the 14.4 device pack v1.05	

PS Performance Characteristics

For further design requirement details, refer to the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585).

Table 16: **CPU Clock Domains Performance**

Symbol	Clock Ratio	Description	Speed Grade			Units
			-3	-2	-1	
$F_{CPU\_6X4X\_621\_MAX}$(1)	6:2:1	Maximum CPU clock frequency	800	733	667	MHz
$F_{CPU\_3X2X\_621\_MAX}$		Maximum CPU_3X clock frequency	400	367	333	MHz
$F_{CPU\_2X\_621\_MAX}$		Maximum CPU_2X clock frequency	267	244	222	MHz
$F_{CPU\_1X\_621\_MAX}$		Maximum CPU_1X clock frequency	133	122	111	MHz
$F_{CPU\_6X4X\_421\_MAX}$(1)	4:2:1	Maximum CPU clock frequency	710	600	533	MHz
$F_{CPU\_3X2X\_421\_MAX}$		Maximum CPU_3X clock frequency	355	300	267	MHz
$F_{CPU\_2X\_421\_MAX}$		Maximum CPU_2X clock frequency	355	300	267	MHz
$F_{CPU\_1X\_421\_MAX}$		Maximum CPU_1X clock frequency	178	150	133	MHz

Notes:

1. The maximum frequency during BootROM execution is 500 MHz across all speed specifications.

Table 17: **PS DDR Clock Domains Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{DDR3_MAX}	Maximum DDR3 interface performance	1066	1066	1066	Mb/s
F_{DDR3L_MAX}	Maximum DDR3L interface performance	800	800	800	Mb/s
F_{DDR2_MAX}	Maximum DDR2 interface performance	800	800	800	Mb/s
F_{LPDDR2_MAX}	Maximum LPDDR2 interface performance	800	800	800	Mb/s
F_{DDRCLK_2XMAX}	Maximum DDR_2X clock frequency	444	408	355	MHz

Notes:

1. All performance numbers apply to both internal and external V_{REF} configurations.

PS Switching Characteristics

Clocks

Table 18: **System Reference Clock Requirements**

Symbol	Description	Min	Typ	Max	Units
$T_{JTPSCLK}$	PS_CLK RMS clock jitter tolerance	–	–	±0.5	%
$T_{DCPSCLK}$	PS_CLK duty cycle	40	–	60	%
$T_{RFPSCLK}$	PS_CLK rise and fall time	–	4	–	ns
F_{PSCLK}	PS_CLK frequency	30	–	60	MHz

Table 19: **PS PLL Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
T_{LOCK_PSPLL}	PLL maximum lock time	60	60	60	µs
F_{PSPLL_MAX}	PLL maximum output frequency	2000	1800	1600	MHz
F_{PSPLL_MIN}	PLL minimum output frequency	780	780	780	MHz

Resets

Table 20: **PS Reset Requirements**

Symbol	Description	Min	Typ	Max	Units
T_{PSPOR}	Required PS_POR_B assertion time(1)	100	–	–	µs
T_{PSRST}	Required PS_SRST_B assertion time	3	–	–	PS_CLK Clock Cycles

Notes:

1. PS_POR_B needs to be asserted low until PS supply voltages reach minimum levels.

PS Configuration

Table 21: **Processor Configuration Access Port Switching Characteristics**

Symbol	Description	Min	Typ	Max	Units
F_{PCAPCK}	Maximum processor configuration access port (PCAP) frequency	–	–	100	MHz

DDR Memory Interfaces

Table 22: **DDR3 Interface Switching Characteristics (1066 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$	Input data valid window	500	–	ps
T_{DQDS}(2)	Output DQ to DQS skew	131	–	ps
T_{DQDH}(3)	Output DQS to DQ skew	288	–	ps
T_{DQSS}	Output clock to DQS skew	–0.11	0.09	T_{CK}
T_{CACK}(4)	Command/address output setup time with respect to CLK	532	–	ps
T_{CKCA}(5)	Command/address output hold time with respect to CLK	637	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.5V ±5%.
2. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 23: **DDR3 Interface Switching Characteristics (800 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$	Input data valid window	500	–	ps
T_{DQDS}(2)	Output DQ to DQS skew	232	–	ps
T_{DQDH}(3)	Output DQS to DQ skew	401	–	ps
T_{DQSS}	Output clock to DQS skew	–0.10	0.06	T_{CK}
T_{CACK}(4)	Command/address output setup time with respect to CLK	722	–	ps
T_{CKCA}(5)	Command/address output hold time with respect to CLK	882	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.5V ±5%.
2. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 24: **DDR3L Interface Switching Characteristics (800 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$	Input data valid window	500	–	ps
T_{DQDS}(2)	Output DQ to DQS skew	321	–	ps
T_{DQDH}(3)	Output DQS to DQ skew	380	–	ps
T_{DQSS}	Output clock to DQS skew	–0.12	0.04	T_{CK}
T_{CACK}(4)	Command/address output setup time with respect to CLK	636	–	ps
T_{CKCA}(5)	Command/address output hold time with respect to CLK	853	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.35V ±5%.
2. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 25: **LPDDR2 Interface Switching Characteristics (800 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$	Input data valid window	500	–	ps
T_{DQDS}(2)	Output DQ to DQS skew	196	–	ps
T_{DQDH}(3)	Output DQS to DQ skew	328	–	ps
T_{DQSS}	Output clock to DQS skew	0.90	1.06	T_{CK}
T_{CACK}(4)	Command/address output setup time with respect to CLK	202	–	ps
T_{CKCA}(5)	Command/address output hold time with respect to CLK	353	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.2V ±5%.
2. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 26: **LPDDR2 Interface Switching Characteristics (400 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$	Input data valid window	500	–	ps
T_{DQDS}(2)	Output DQ to DQS skew	664	–	ps
T_{DQDH}(3)	Output DQS to DQ skew	766	–	ps
T_{DQSS}	Output clock to DQS skew	0.90	1.06	T_{CK}
T_{CACK}(4)	Command/address output setup time with respect to CLK	731	–	ps
T_{CKCA}(5)	Command/address output hold time with respect to CLK	907	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.2V ±5%.
2. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 27: **DDR2 Interface Switching Characteristics (800 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$	Input data valid window	500	–	ps
T_{DQDS}(2)	Output DQ to DQS skew	147	–	ps
T_{DQDH}(3)	Output DQS to DQ skew	376	–	ps
T_{DQSS}	Output clock to DQS skew	–0.07	0.08	T_{CK}
T_{CACK}(4)	Command/address output setup time with respect to CLK	732	–	ps
T_{CKCA}(5)	Command/address output hold time with respect to CLK	938	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.8V ±5%.
2. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 28: **DDR2 Interface Switching Characteristics (400 Mb/s)(1)**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$	Input data valid window	500	–	ps
T_{DQDS}(2)	Output DQ to DQS skew	385	–	ps
T_{DQDH}(3)	Output DQS to DQ skew	662	–	ps
T_{DQSS}	Output clock to DQS skew	–0.11	0.06	T_{CK}
T_{CACK}(4)	Command/address output setup time with respect to CLK	1760	–	ps
T_{CKCA}(5)	Command/address output hold time with respect to CLK	1739	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.8V ±5%.
2. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

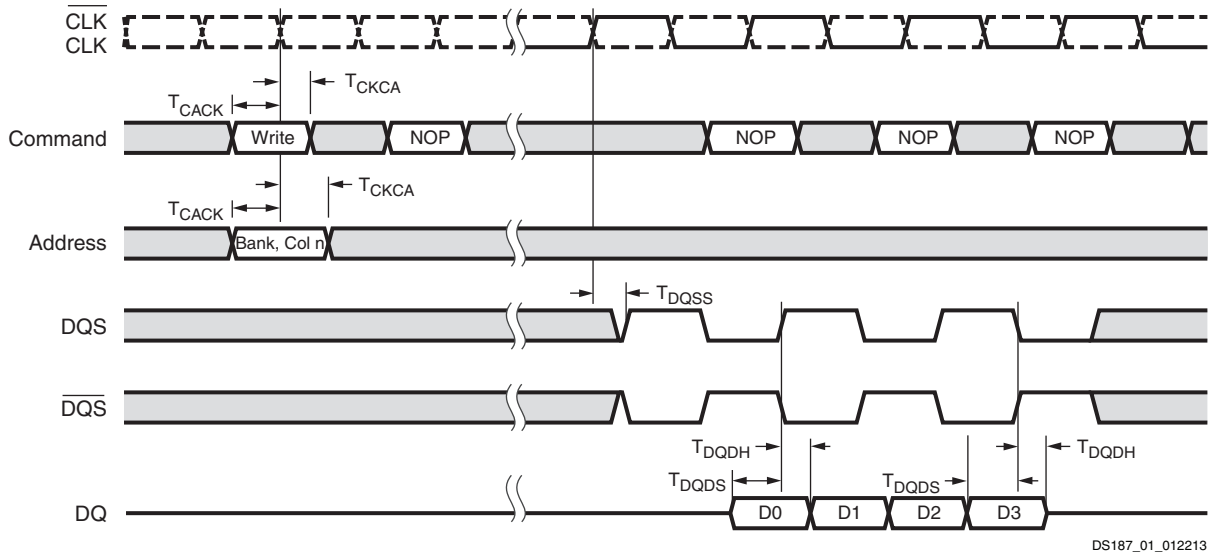

Figure 1: **DDR Output Timing Diagram**

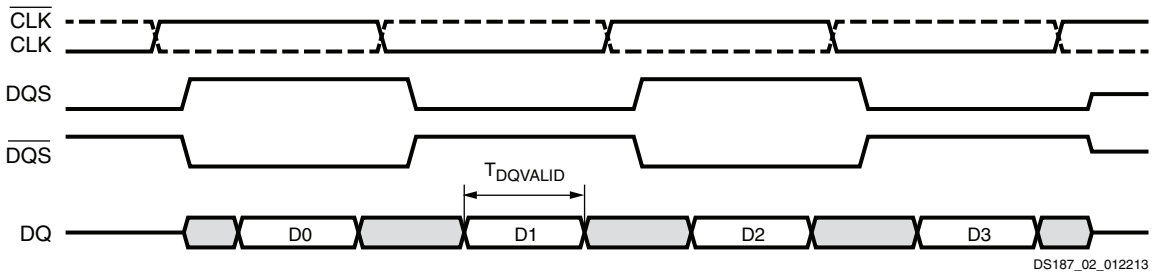

Figure 2: **DDR Input Timing Diagram**

Static Memory Controller

Table 29: **SMC Interface Delay Characteristics(1)(2)**

Symbol	Description	Min	Max	Units
$T_{NANDDOUT}$	NAND_IO output delay from last register to pad	4.12	6.45	ns
$T_{NANDALE}$	NAND_ALE output delay from last register to pad	5.08	6.33	ns
$T_{NANDCLE}$	NAND_CLE output delay from last register to pad	4.87	6.40	ns
T_{NANDWE}	NAND_WE_B output delay from last register to pad	4.69	5.89	ns
T_{NANDRE}	NAND_RE_B output delay from last register to pad	5.12	6.44	ns
T_{NANDCE}	NAND_CE_B output delay from last register to pad	4.68	5.89	ns
$T_{NANDDIN}$	NAND_IO setup time and input delay from pad to first register	1.48	3.09	ns
$T_{NANDBUSY}$	NAND_BUSY setup time and input delay from pad to first register	2.48	3.33	ns
T_{SRAMA}	SRAM_A output delay from last register to pad	3.94	5.73	ns
$T_{SRAMDOUT}$	SRAM_DQ output delay from last register to pad	4.66	6.45	ns
T_{SRAMCE}	SRAM_CE output delay from last register to pad	4.57	5.95	ns
T_{SRAMOE}	SRAM_OE_B output delay from last register to pad	4.79	6.13	ns
$T_{SRAMBLS}$	SRAM_BLS_B output delay from last register to pad	5.25	6.74	ns
T_{SRAMWE}	SRAM_WE_B output delay from last register to pad	5.12	6.48	ns
$T_{SRAMDIN}$	SRAM_DQ setup time and input delay from pad to first register	1.93	3.05	ns
$T_{SRAMWAIT}$	SRAM_WAIT setup time and input delay from pad to first register	2.26	3.15	ns

Notes:

1. All parameters do not include the package flight time and register controlled delays.
2. Refer to the ARM® PrimeCell® Static Memory Controller (PL350 series) Technical Reference Manual for more SMC timing details.

Quad-SPI Interfaces

Table 30: **Quad-SPI Interface Switching Characteristics**

Symbol	Description	Load Conditions	Min	Max	Units
Feedback Clock Enabled					
$T_{DCQSPICLK1}$	Quad-SPI clock duty cycle	All(1)(2)	44	56	%
$T_{QSPICKO1}$	Data and slave select output delay	15 pF(1)	–0.10	3.40	ns
		30 pF(2)	–1.00	3.80	
$T_{QSPIDCK1}$	Input data setup time	15 pF(1)	2.00	–	ns
		30 pF(2)	3.30	–	
$T_{QSPICKD1}$	Input data hold time	15 pF(1)	1.30	–	ns
		30 pF(2)	1.50	–	
$T_{QSPISSCLK1}$	Slave select asserted to next clock edge	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$T_{QSPICLKSS1}$	Clock edge to slave select deasserted	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$F_{QSPICLK1}$	Quad-SPI device clock frequency	15 pF(1)	–	100(3)	MHz
		30 pF(2)	–	70(3)	
Feedback Clock Disabled					
$T_{DCQSPICLK2}$	Quad-SPI clock duty cycle	All(1)(2)	44	56	%
$T_{QSPICKO2}$	Data and slave select output delay	15 pF(1)	–0.10	3.80	ns
		30 pF(2)	–1.00	3.80	ns
$T_{QSPIDCK2}$	Input data setup time(4)	All(1)(2)	$11 - \frac{1}{F_{QSPI\_REF\_CLK}}$	–	ns
$T_{QSPICKD2}$	Input data hold time	All(1)(2)	$\frac{1}{2 \times F_{QSPICLK2}}$	–	ns
$T_{QSPISSCLK2}$	Slave select asserted to next clock edge	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$T_{QSPICLKSS2}$	Clock edge to slave select deasserted	All(1)(2)	1	–	$F_{QSPI\_REF\_CLK}$ cycle
$F_{QSPICLK2}$	Quad-SPI device clock frequency	All(1)(2)	–	40	MHz
Feedback Clock Enabled or Disabled					
$F_{QSPI\_REF\_CLK}$	Quad-SPI reference clock frequency	All(1)(2)	–	200	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
2. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 30 pF loads in 4-bit stacked I/O configuration, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
3. Requires appropriate component selection/board design.
4. Use 0 ns as the input data setup time when the calculated $T_{QSPIDCK2}$ value is negative.

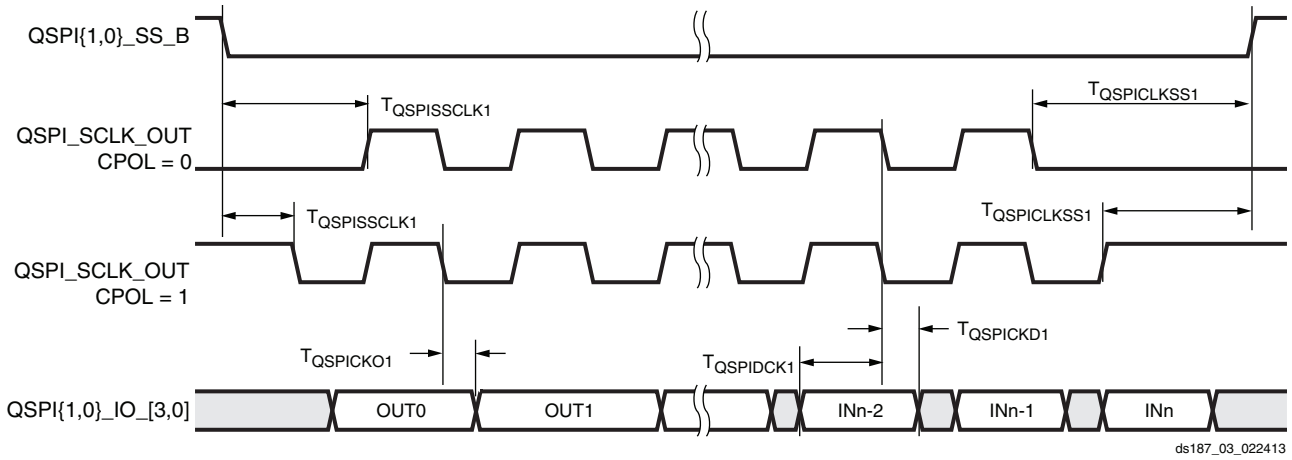

Figure 3: **Quad-SPI Interface (Feedback Clock Enabled) Timing Diagram**

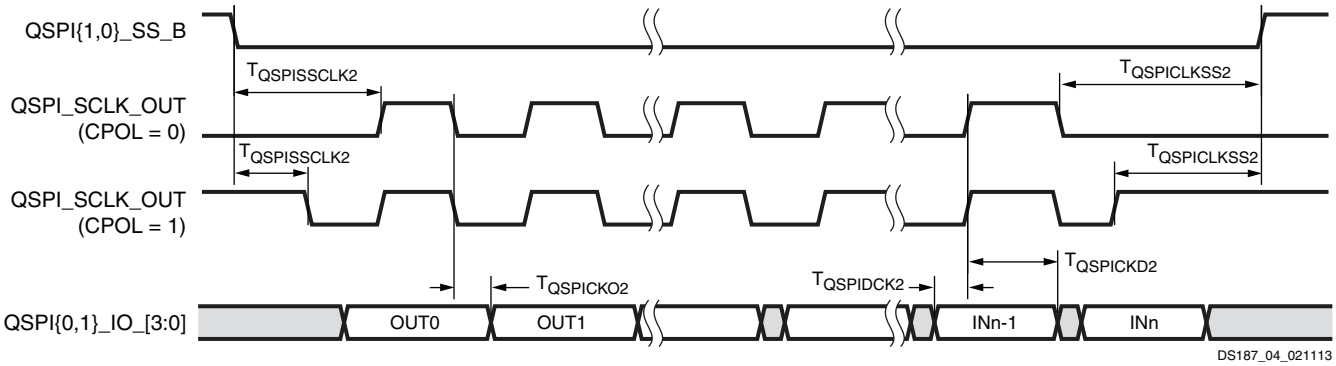

Figure 4: **Quad-SPI Interface (Feedback Clock Disabled) Timing Diagram**

ULPI Interfaces

Table 31: **ULPI Interface Clock Receiving Mode Switching Characteristics**(1)(2)

Symbol	Description	Min	Typ	Max	Units
$T_{ULPIDCK}$	Input setup to ULPI clock, all inputs	3.00	–	–	ns
$T_{ULPICKD}$	Input hold to ULPI clock, all inputs	1.00	–	–	ns
$T_{ULPICKO}$	ULPI clock to output valid, all outputs	1.70	–	8.86	ns
$F_{ULPICLK}$	ULPI device clock frequency	–	60	–	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, 60 MHz device clock frequency.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

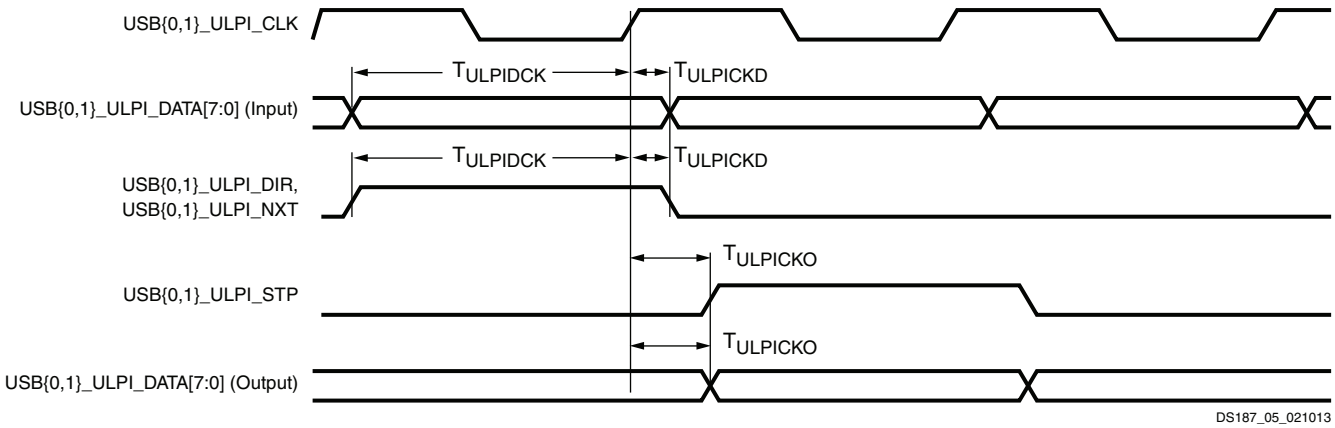

Figure 5: **ULPI Interface Timing Diagram**

RGMII and MDIO Interfaces

Table 32: **RGMII and MDIO Interface Switching Characteristics(1)(2)(3)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCGETXCLK}$	Transmit clock duty cycle	45	–	55	%
$T_{GEMTXCKO}$	RGMII_TX_D[3:0], RGMII_TX_CTL output clock to out time	–0.50	–	0.50	ns
$T_{GEMRXDCK}$	RGMII_RX_D[3:0], RGMII_RX_CTL input setup time	0.80	–	–	ns
$T_{GEMRXCKD}$	RGMII_RX_D[3:0], RGMII_RX_CTL input hold time	0.80	–	–	ns
$T_{MDIOCLK}$	MDC output clock period	400	–	–	ns
$T_{MDIOCKH}$	MDC clock High time	160	–	–	ns
$T_{MDIOCKL}$	MDC clock Low time	160	–	–	ns
$T_{MDIODCK}$	MDIO input data setup time	80	–	–	ns
$T_{MDIOCKD}$	MDIO input data hold time	0	–	–	ns
$T_{MDIOCKO}$	MDIO data output delay	–	–	170	ns
$F_{GETXCLK}$	RGMII_TX_CLK transmit clock frequency	–	125	–	MHz
$F_{GERXCLK}$	RGMII_RX_CLK receive clock frequency	–	125	–	MHz
$F_{ENET\_REF\_CLK}$	Ethernet reference clock frequency	–	125	–	MHz

Notes:

1. Test conditions: LVCMOS25, fast slew rate, 8 mA drive strength, 15 pF loads. Values in this table are specified during 1000 Mb/s operation.
2. LVCMOS25 slow slew rate and LVCMOS33 are not supported.
3. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

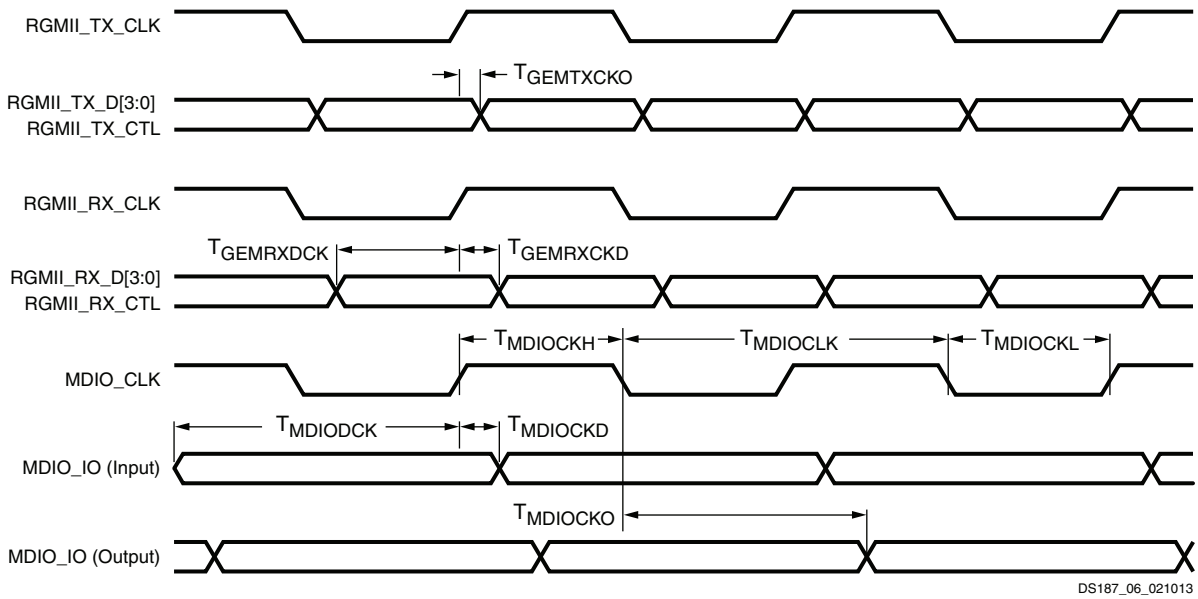

Figure 6: **RGMII Interface Timing Diagram**

SD/SDIO Interfaces

Table 33: **SD/SDIO Interface High Speed Mode Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCSDHSCLK}$	SD device clock duty cycle	–	50	–	%
$T_{SDHSCKO}$	Clock to output delay, all outputs	2.00	–	12.00	ns
$T_{SDHSDCK}$	Input setup time, all inputs	3.00	–	–	ns
$T_{SDHSCKD}$	Input hold time, all inputs	1.05	–	–	ns
$F_{SD\_REF\_CLK}$	SD reference clock frequency	–	–	100	MHz
$F_{SDHSCLK}$	High speed mode SD device clock frequency	0	–	50	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

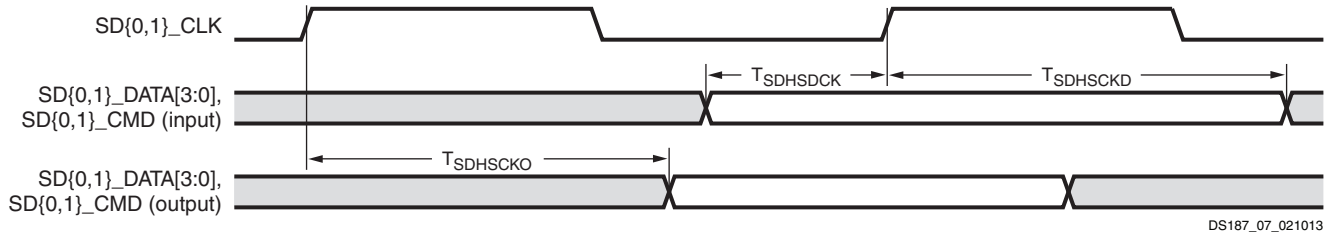

Figure 7: **SD/SDIO Interface High Speed Mode Timing Diagram**

Table 34: **SD/SDIO Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCSDSCLK}$	SD device clock duty cycle	–	50	–	%
T_{SDSCKO}	Clock to output delay, all outputs	2.00	–	12.00	ns
T_{SDSDCK}	Input setup time, all inputs	4.00	–	–	ns
T_{SDSCKD}	Input hold time, all inputs	3.00	–	–	ns
$F_{SD\_REF\_CLK}$	SD reference clock frequency	–	–	125	MHz
$F_{SDIDCLK}$	Clock frequency in identification mode	–	–	400	MHz
F_{SDSCLK}	Standard mode SD device clock frequency	0	–	50	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

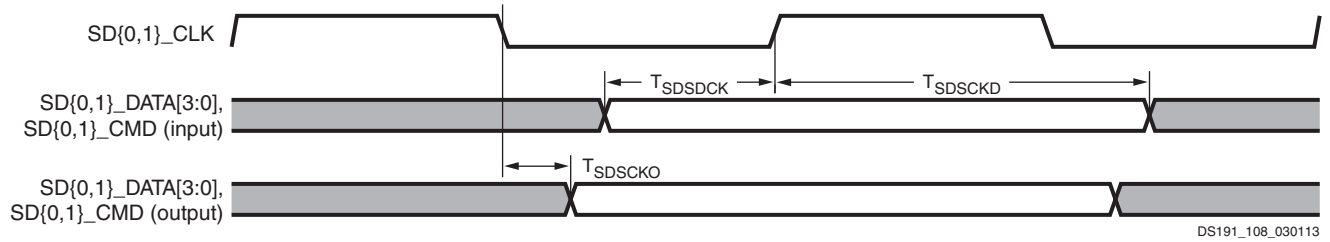

Figure 8: **SD/SDIO Interface Standard Mode Timing Diagram**

I2C Interfaces

Table 35: **I2C Fast Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCI2CFCLK}$	I2C{0,1}SCL duty cycle	–	50	–	%
$T_{I2CFCKO}$	I2C{0,1}SDAO clock to out delay	–	–	900	ns
$T_{I2CFDCK}$	I2C{0,1}SDAI setup time	100	–	–	ns
$F_{I2CFCLK}$	I2C{0,1}SCL clock frequency	–	–	400	KHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

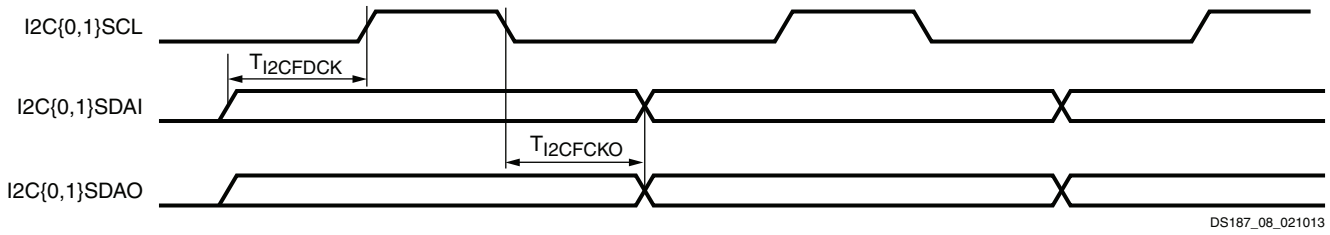

Figure 9: **I2C Fast Mode Interface Timing Diagram**

Table 36: **I2C Standard Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCI2CSCLK}$	I2C{0,1}SCL duty cycle	–	50	–	%
$T_{I2CSCKO}$	I2C{0,1}SDAO clock to out delay	–	–	3450	ns
$T_{I2CSDCK}$	I2C{0,1}SDAI setup time	250	–	–	ns
$F_{I2CSCLK}$	I2C{0,1}SCL clock frequency	–	–	100	KHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

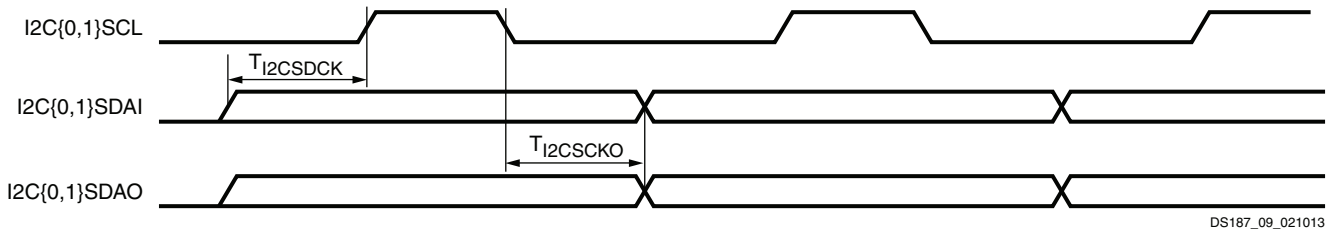

Figure 10: **I2C Standard Mode Interface Timing Diagram**

SPI Interfaces

Table 37: **SPI Master Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
$T_{DCMSPICLK}$	SPI master mode clock duty cycle	–	50	–	%
$T_{MSPIDCK}$	Input setup time for SPI{0,1}_MISO	2.00	–	–	ns
$T_{MSPICKD}$	Input hold time for SPI{0,1}_MISO	8.20	–	–	ns
$T_{MSPICKO}$	Output delay for SPI{0,1}_MOSI and SPI{0,1}_SS	–3.10	–	3.90	ns
$T_{MSPISSCLK}$	Slave select asserted to first active clock edge	1	–	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{MSPICLKSS}$	Last active clock edge to slave select deasserted	0.5	–	–	$F_{SPI\_REF\_CLK}$ cycles
$F_{MSPICLK}$	SPI master mode device clock frequency	–	–	50.00	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency	–	–	200.00	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

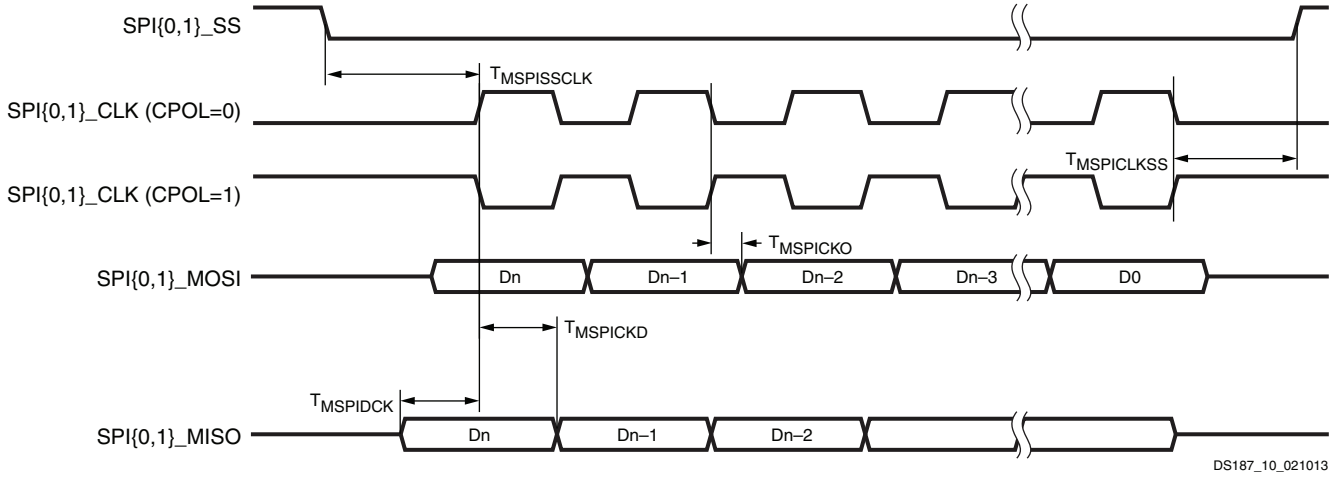

Figure 11: **SPI Master (CPHA = 0) Interface Timing Diagram**

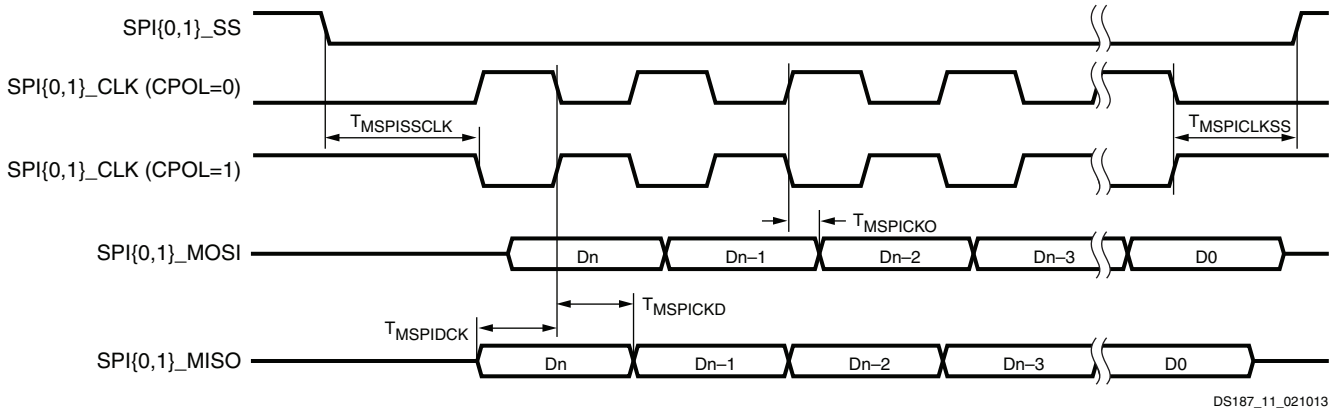

Figure 12: **SPI Master (CPHA = 1) Interface Timing Diagram**

Table 38: **SPI Slave Mode Interface Switching Characteristics(1)(2)**

Symbol	Description	Min	Max	Units
$T_{SSPIDCK}$	Input setup time for SPI{0,1}_MOSI and SPI{0,1}_SS	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICKD}$	Input hold time for SPI{0,1}_MOSI and SPI{0,1}_SS	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICKO}$	Output delay for SPI{0,1}_MISO	0	2.6	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPISSCLK}$	Slave select asserted to first active clock edge	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICLKSS}$	Last active clock edge to slave select deasserted	1	–	$F_{SPI\_REF\_CLK}$ cycles
$F_{SSPICLK}$	SPI slave mode device clock frequency	–	25	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency	–	200	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

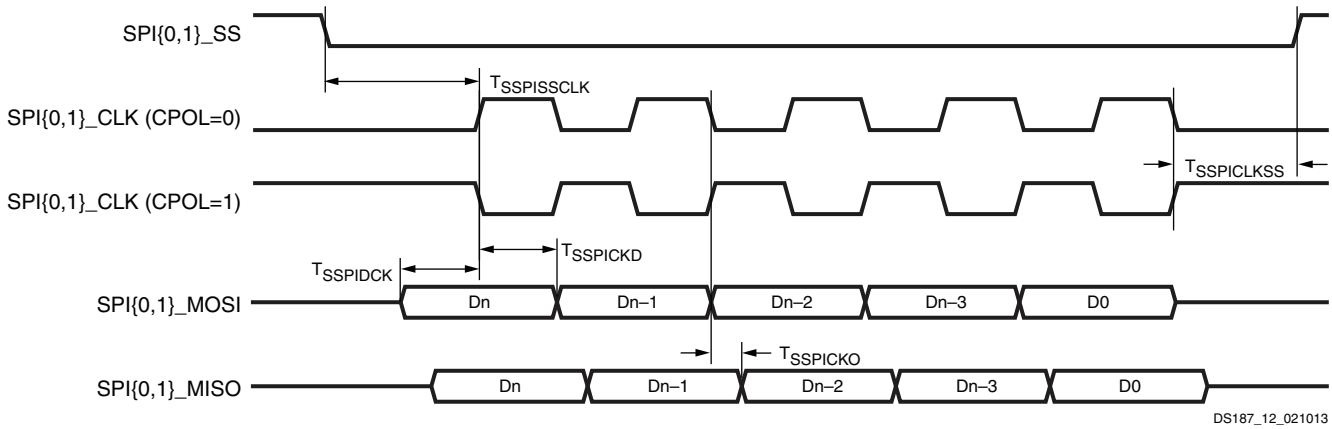

Figure 13: **SPI Slave (CPHA = 0) Interface Timing Diagram**

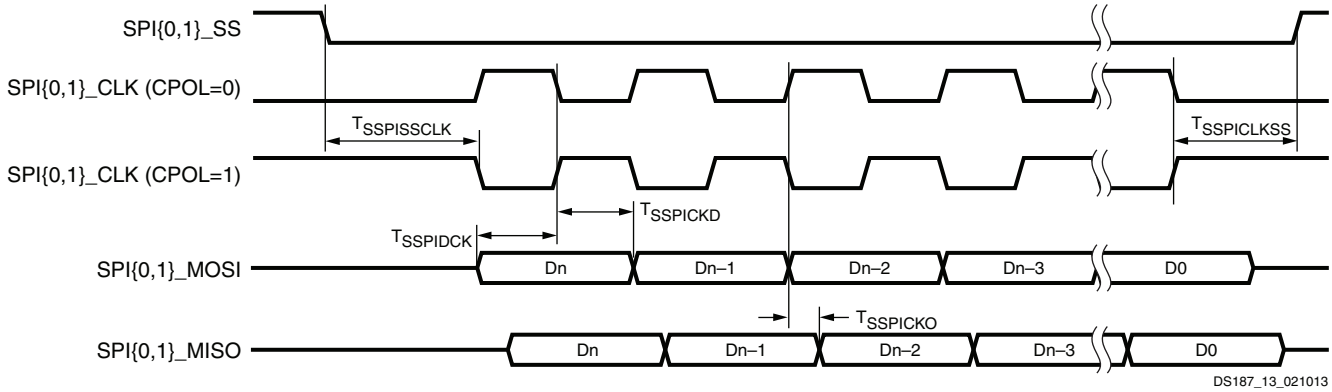

Figure 14: **SPI Slave (CPHA = 1) Interface Timing Diagram**

CAN Interfaces

Table 39: **CAN Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWCANRX}$	Minimum receive pulse width	1	–	µs
$T_{PWCANTX}$	Minimum transmit pulse width	1	–	µs
$F_{CAN\_REF\_CLK}$	Internally sourced CAN reference clock frequency	–	100	MHz
	Externally sourced CAN reference clock frequency	–	40	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

PJTAG Interfaces

Table 40: **PJTAG Interface(1)(2)**

Symbol	Description	Min	Max	Units
$T_{PJTAGDCK}$	PJTAG input setup time	2.4	–	ns
$T_{PJTAGCKD}$	PJTAG input hold time	2.0	–	ns
$T_{PJTAGCKO}$	PJTAG clock to out delay	–	12.5	ns
$T_{PJTAGCLK}$	PJTAG clock frequency	–	20	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

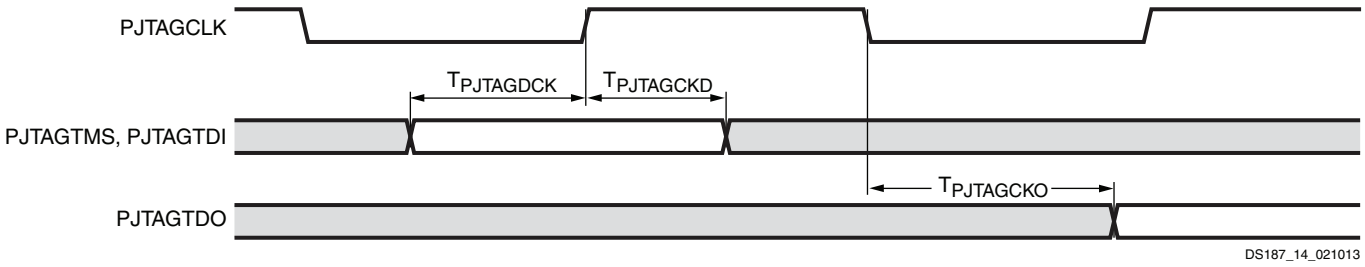

Figure 15: **PJTAG Interface Timing Diagram**

UART Interfaces

Table 41: **UART Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$BAUD_{TXMAX}$	Maximum transmit baud rate	–	1	Mb/s
$BAUD_{RXMAX}$	Maximum receive baud rate	–	1	Mb/s
$F_{UART\_REF\_CLK}$	UART reference clock frequency	–	100	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

GPIO Interfaces

Table 42: **GPIO Banks Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWGPIOH}$	Input high pulse width	10 x 1/cpu1x	–	µs
$T_{PWGPIOL}$	Input low pulse width	10 x 1/cpu1x	–	µs

Notes:

1. Pulse width requirement for interrupt.

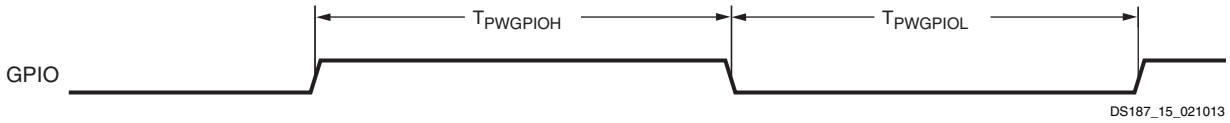

Figure 16: **GPIO Interface Timing Diagram**

Trace Interface

Table 43: **Trace Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
T_{TCECKO}	Trace clock to output delay, all outputs	–1.4	1.5	ns
$T_{DCTCECLK}$	Trace clock duty cycle	40	60	%
F_{TCECLK}	Trace clock frequency	–	80	MHz

Notes:

1. Test conditions: LVCMOS25, fast slew rate, 8 mA drive strength, 15 pF loads.

Triple Timer Counter Interface

Table 44: **Triple Timer Counter interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple time counter output clock pulse width	2 x 1/cpu1x	–	ns
$F_{TTCOCLK}$	Triple time counter output clock frequency	–	cpu1x/4	MHz
$T_{TTCICLKH}$	Triple time counter input clock high pulse width	1.5 x 1/cpu1x	–	ns
$T_{TTCICLKL}$	Triple time counter input clock low pulse width	1.5 x 1/cpu1x	–	ns
$F_{TTCICLK}$	Triple time counter input clock frequency	–	cpu1x/3	MHz

Notes:

1. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

Watchdog Timer

Table 45: **Watchdog Timer Switching Characteristics**

Symbol	Description	Min	Max	Units
F_{WDTCLK}	Watchdog timer input clock frequency	–	10	MHz

PS-PL Interface

Table 46: **PS-PL Interface Performance**

Symbol	Description	Min	Typical	Max	Units
$F_{EMIOGEMCLK}$	EMIO gigabit Ethernet controller maximum frequency	–	–	125	MHz
$F_{EMIOSDCLK}$	EMIO SD controller maximum frequency	–	–	25	MHz
$F_{EMIOSPICLK}$	EMIO SPI controller maximum frequency	–	–	25	MHz
$F_{EMIOJTAGCLK}$	EMIO JTAG controller maximum frequency	–	–	20	MHz
$F_{EMIOTRACECLK}$	EMIO trace controller maximum frequency	–	–	125	MHz
F_{FTMCLK}	Fabric trace monitor maximum frequency	–	–	125	MHz
$F_{EMIODMACLK}$	DMA maximum frequency	–	–	100	MHz

PL Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the PL. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 11.

Table 47: **PL Networking Applications Interface Performances**

Description	Speed Grade			Units
	-3	-2	-1	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	680	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	1250	950	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	680	680	600	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	1250	1250	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 48: **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator(1)(2)**

Memory Standard	Speed Grade			Units
	-3	-2	-1	
4:1 Memory Controllers				
DDR3	1066(3)	800	800	Mb/s
DDR3L	800	800	667	Mb/s
DDR2	800	800	667	Mb/s
LPDDR2	667	667	533	Mb/s
2:1 Memory Controllers				
DDR3	800	700	620	Mb/s
DDR3L	800	700	620	Mb/s
DDR2	800	700	620	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *7 Series FPGAs Memory Interface Solutions User Guide* (UG586).
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. The maximum PHY rate is 800 Mb/s in bank 13 of the XC7Z020 device.

PL Switching Characteristics

IOB Pad Input/Output/3-State

Table 49 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard), and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 49: **3.3V IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2	-1	-3	-2	-1	-3	-2	-1	
LVTTL_S4	1.26	1.34	1.41	3.80	3.93	4.18	4.37	4.59	5.01	ns
LVTTL_S8	1.26	1.34	1.41	3.54	3.66	3.92	4.11	4.32	4.75	ns
LVTTL_S12	1.26	1.34	1.41	3.52	3.65	3.90	4.09	4.31	4.73	ns
LVTTL_S16	1.26	1.34	1.41	3.07	3.19	3.45	3.64	3.85	4.28	ns
LVTTL_S24	1.26	1.34	1.41	3.29	3.41	3.67	3.86	4.07	4.50	ns
LVTTL_F4	1.26	1.34	1.41	3.26	3.38	3.64	3.83	4.04	4.46	ns
LVTTL_F8	1.26	1.34	1.41	2.74	2.87	3.12	3.31	3.52	3.95	ns
LVTTL_F12	1.26	1.34	1.41	2.73	2.85	3.10	3.29	3.51	3.93	ns
LVTTL_F16	1.26	1.34	1.41	2.56	2.68	2.93	3.12	3.34	3.76	ns
LVTTL_F24	1.26	1.34	1.41	2.52	2.65	2.90	3.09	3.31	3.73	ns
LVDS_25	0.73	0.81	0.88	1.29	1.41	1.67	1.86	2.07	2.49	ns
MINI_LVDS_25	0.73	0.81	0.88	1.27	1.40	1.65	1.84	2.06	2.48	ns
BLVDS_25	0.73	0.81	0.88	1.84	1.96	2.21	2.40	2.62	3.04	ns
RSDS_25 (point to point)	0.73	0.81	0.88	1.27	1.40	1.65	1.84	2.06	2.48	ns
PPDS_25	0.73	0.81	0.88	1.29	1.41	1.67	1.86	2.07	2.49	ns
TMDS_33	0.73	0.81	0.88	1.41	1.54	1.79	1.98	2.20	2.62	ns
PCI33_3	1.24	1.32	1.39	3.10	3.22	3.48	3.67	3.88	4.31	ns
HSUL_12	0.67	0.75	0.82	1.81	1.93	2.18	2.37	2.59	3.01	ns
DIFF_HSUL_12	0.68	0.76	0.83	1.81	1.93	2.18	2.37	2.59	3.01	ns
HSTL_I_S	0.67	0.75	0.82	1.62	1.74	1.99	2.19	2.40	2.82	ns
HSTL_II_S	0.65	0.73	0.80	1.41	1.54	1.79	1.98	2.20	2.62	ns
HSTL_I_18_S	0.67	0.75	0.82	1.29	1.41	1.67	1.86	2.07	2.49	ns
HSTL_II_18_S	0.66	0.75	0.81	1.41	1.54	1.79	1.98	2.20	2.62	ns
DIFF_HSTL_I_S	0.68	0.76	0.83	1.59	1.71	1.96	2.15	2.37	2.79	ns
DIFF_HSTL_II_S	0.68	0.76	0.83	1.51	1.63	1.88	2.08	2.29	2.71	ns
DIFF_HSTL_I_18_S	0.71	0.79	0.86	1.38	1.51	1.76	1.95	2.17	2.59	ns
DIFF_HSTL_II_18_S	0.70	0.78	0.85	1.46	1.58	1.84	2.03	2.24	2.67	ns

Table 49: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2	-1	-3	-2	-1	-3	-2	-1	
HSTL_I_F	0.67	0.75	0.82	1.10	1.22	1.48	1.67	1.88	2.31	ns
HSTL_II_F	0.65	0.73	0.80	1.12	1.24	1.49	1.69	1.90	2.32	ns
HSTL_I_18_F	0.67	0.75	0.82	1.13	1.26	1.51	1.70	1.92	2.34	ns
HSTL_II_18_F	0.66	0.75	0.81	1.12	1.24	1.49	1.69	1.90	2.32	ns
DIFF_HSTL_I_F	0.68	0.76	0.83	1.18	1.30	1.56	1.75	1.96	2.39	ns
DIFF_HSTL_II_F	0.68	0.76	0.83	1.21	1.33	1.59	1.78	1.99	2.42	ns
DIFF_HSTL_I_18_F	0.71	0.79	0.86	1.21	1.33	1.59	1.78	1.99	2.42	ns
DIFF_HSTL_II_18_F	0.70	0.78	0.85	1.21	1.33	1.59	1.78	1.99	2.42	ns
LVCMOS33_S4	1.26	1.34	1.41	3.80	3.93	4.18	4.37	4.59	5.01	ns
LVCMOS33_S8	1.26	1.34	1.41	3.52	3.65	3.90	4.09	4.31	4.73	ns
LVCMOS33_S12	1.26	1.34	1.41	3.09	3.21	3.46	3.65	3.87	4.29	ns
LVCMOS33_S16	1.26	1.34	1.41	3.40	3.52	3.77	3.97	4.18	4.60	ns
LVCMOS33_F4	1.26	1.34	1.41	3.26	3.38	3.64	3.83	4.04	4.46	ns
LVCMOS33_F8	1.26	1.34	1.41	2.74	2.87	3.12	3.31	3.52	3.95	ns
LVCMOS33_F12	1.26	1.34	1.41	2.56	2.68	2.93	3.12	3.34	3.76	ns
LVCMOS33_F16	1.26	1.34	1.41	2.56	2.68	2.93	3.12	3.34	3.76	ns
LVCMOS25_S4	1.12	1.20	1.27	3.13	3.26	3.51	3.70	3.91	4.34	ns
LVCMOS25_S8	1.12	1.20	1.27	2.88	3.01	3.26	3.45	3.67	4.09	ns
LVCMOS25_S12	1.12	1.20	1.27	2.48	2.60	2.85	3.05	3.26	3.68	ns
LVCMOS25_S16	1.12	1.20	1.27	2.82	2.94	3.20	3.39	3.60	4.03	ns
LVCMOS25_F4	1.12	1.20	1.27	2.74	2.87	3.12	3.31	3.52	3.95	ns
LVCMOS25_F8	1.12	1.20	1.27	2.18	2.30	2.56	2.75	2.96	3.39	ns
LVCMOS25_F12	1.12	1.20	1.27	2.16	2.29	2.54	2.73	2.95	3.37	ns
LVCMOS25_F16	1.12	1.20	1.27	2.01	2.13	2.39	2.58	2.79	3.21	ns
LVCMOS18_S4	0.74	0.83	0.89	1.62	1.74	1.99	2.19	2.40	2.82	ns
LVCMOS18_S8	0.74	0.83	0.89	2.18	2.30	2.56	2.75	2.96	3.39	ns
LVCMOS18_S12	0.74	0.83	0.89	2.18	2.30	2.56	2.75	2.96	3.39	ns
LVCMOS18_S16	0.74	0.83	0.89	1.52	1.65	1.90	2.09	2.31	2.73	ns
LVCMOS18_S24	0.74	0.83	0.89	1.60	1.72	1.98	2.17	2.38	2.81	ns
LVCMOS18_F4	0.74	0.83	0.89	1.45	1.57	1.82	2.01	2.23	2.65	ns
LVCMOS18_F8	0.74	0.83	0.89	1.68	1.80	2.06	2.25	2.46	2.89	ns
LVCMOS18_F12	0.74	0.83	0.89	1.68	1.80	2.06	2.25	2.46	2.89	ns
LVCMOS18_F16	0.74	0.83	0.89	1.40	1.52	1.77	1.97	2.18	2.60	ns
LVCMOS18_F24	0.74	0.83	0.89	1.34	1.46	1.71	1.90	2.12	2.54	ns
LVCMOS15_S4	0.77	0.86	0.93	2.05	2.18	2.43	2.62	2.84	3.26	ns
LVCMOS15_S8	0.77	0.86	0.93	2.09	2.21	2.46	2.65	2.87	3.29	ns
LVCMOS15_S12	0.77	0.86	0.93	1.59	1.71	1.96	2.15	2.37	2.79	ns
LVCMOS15_S16	0.77	0.86	0.93	1.59	1.71	1.96	2.15	2.37	2.79	ns

Table 49: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2	-1	-3	-2	-1	-3	-2	-1	
LVCMOS15_F4	0.77	0.86	0.93	1.85	1.97	2.23	2.42	2.63	3.06	ns
LVCMOS15_F8	0.77	0.86	0.93	1.60	1.72	1.98	2.17	2.38	2.81	ns
LVCMOS15_F12	0.77	0.86	0.93	1.35	1.47	1.73	1.92	2.13	2.56	ns
LVCMOS15_F16	0.77	0.86	0.93	1.34	1.46	1.71	1.90	2.12	2.54	ns
LVCMOS12_S4	0.87	0.95	1.02	2.57	2.69	2.95	3.14	3.35	3.78	ns
LVCMOS12_S8	0.87	0.95	1.02	2.09	2.21	2.46	2.65	2.87	3.29	ns
LVCMOS12_S12	0.87	0.95	1.02	1.79	1.91	2.17	2.36	2.57	2.99	ns
LVCMOS12_F4	0.87	0.95	1.02	1.98	2.10	2.35	2.54	2.76	3.18	ns
LVCMOS12_F8	0.87	0.95	1.02	1.54	1.66	1.92	2.11	2.32	2.75	ns
LVCMOS12_F12	0.87	0.95	1.02	1.38	1.51	1.76	1.95	2.16	2.59	ns
SSTL135_S	0.67	0.75	0.82	1.35	1.47	1.73	1.92	2.13	2.56	ns
SSTL15_S	0.60	0.68	0.75	1.30	1.43	1.68	1.87	2.09	2.51	ns
SSTL18_I_S	0.67	0.75	0.82	1.67	1.79	2.04	2.23	2.45	2.87	ns
SSTL18_II_S	0.67	0.75	0.82	1.31	1.43	1.68	1.87	2.09	2.51	ns
DIFF_SSTL135_S	0.68	0.76	0.83	1.35	1.47	1.73	1.92	2.13	2.56	ns
DIFF_SSTL15_S	0.68	0.76	0.83	1.30	1.43	1.68	1.87	2.09	2.51	ns
DIFF_SSTL18_I_S	0.71	0.79	0.86	1.68	1.80	2.06	2.25	2.46	2.89	ns
DIFF_SSTL18_II_S	0.71	0.79	0.86	1.38	1.51	1.76	1.95	2.17	2.59	ns
SSTL135_F	0.67	0.75	0.82	1.12	1.24	1.49	1.69	1.90	2.32	ns
SSTL15_F	0.60	0.68	0.75	1.07	1.19	1.45	1.64	1.85	2.28	ns
SSTL18_I_F	0.67	0.75	0.82	1.12	1.24	1.49	1.69	1.90	2.32	ns
SSTL18_II_F	0.67	0.75	0.82	1.12	1.24	1.49	1.69	1.90	2.32	ns
DIFF_SSTL135_F	0.68	0.76	0.83	1.12	1.24	1.49	1.69	1.90	2.32	ns
DIFF_SSTL15_F	0.68	0.76	0.83	1.07	1.19	1.45	1.64	1.85	2.28	ns
DIFF_SSTL18_I_F	0.71	0.79	0.86	1.23	1.35	1.60	1.79	2.01	2.43	ns
DIFF_SSTL18_II_F	0.71	0.79	0.86	1.21	1.33	1.59	1.78	1.99	2.42	ns

Table 50 specifies the values of T_{IOTPHZ} and $T_{IOIBUFDISABLE}$. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Table 50: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
T_{IOTPHZ}	T input to pad high-impedance	2.06	2.19	2.37	ns
$T_{IOIBUFDISABLE}$	IBUF turn-on time from IBUFDISABLE to O output	2.11	2.30	2.60	ns

Input/Output Logic Switching Characteristics

Table 51: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Setup/Hold					
T_{ICE1CK}/T_{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.48/0.02	0.54/0.02	0.76/0.02	ns
T_{ISRCK}/T_{ICKSR}	SR pin setup/hold with respect to CLK	0.60/0.01	0.70/0.01	1.13/0.01	ns
T_{IDOCK}/T_{IOCKD}	D pin setup/hold with respect to CLK without Delay	0.01/0.27	0.01/0.29	0.01/0.33	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin setup/hold with respect to CLK (using IDELAY)	0.02/0.27	0.02/0.29	0.02/0.33	ns
Combinatorial					
T_{IDI}	D pin to O pin propagation delay, no Delay	0.11	0.11	0.13	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IDELAY)	0.11	0.12	0.14	ns
Sequential Delays					
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.41	0.44	0.51	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY)	0.41	0.44	0.51	ns
T_{ICKQ}	CLK to Q outputs	0.53	0.57	0.66	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	0.96	1.08	1.32	ns
T_{GSRQ_ILOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	ns
Set/Reset					
T_{RPW_ILOGIC}	Minimum pulse width, SR inputs	0.61	0.72	0.72	ns, Min

Table 52: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Setup/Hold					
T_{ODCK}/T_{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.67/–0.11	0.71/–0.11	0.84/–0.11	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	ns
T_{OSRCK}/T_{OCKSR}	SR pin setup/hold with respect to CLK	0.37/0.21	0.44/0.21	0.80/0.21	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.69/–0.14	0.73/–0.14	0.89/–0.14	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	ns
Combinatorial					
T_{ODQ}	D1 to OQ out or T1 to TQ out	0.83	0.96	1.16	ns
Sequential Delays					
T_{OCKQ}	CLK to OQ/TQ out	0.47	0.49	0.56	ns
T_{RQ_OLOGIC}	SR pin to OQ/TQ out	0.72	0.80	0.95	ns
T_{GSRQ_OLOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	ns
Set/Reset					
T_{RPW_OLOGIC}	Minimum pulse width, SR inputs	0.64	0.74	0.74	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 53: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Setup/Hold for Control Lines					
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin setup/hold with respect to CLKDIV	0.01/0.14	0.02/0.15	0.02/0.17	ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin setup/hold with respect to CLK (for CE1)	0.45/–0.01	0.50/–0.01	0.72/–0.01	ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin setup/hold with respect to CLKDIV (for CE2)	–0.10/0.33	–0.10/0.36	–0.10/0.40	ns
Setup/Hold for Data Lines					
T_{ISDCK_D} /T_{ISCKD_D}	D pin setup/hold with respect to CLK	–0.02/0.12	–0.02/0.14	–0.02/0.17	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin setup/hold with respect to CLK (using IDELAY)(1)	–0.02/0.12	–0.02/0.14	–0.02/0.17	ns
$T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$	D pin setup/hold with respect to CLK at DDR mode	–0.02/0.12	–0.02/0.14	–0.02/0.17	ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin setup/hold with respect to CLK at DDR mode (using IDELAY)(1)	0.12/0.12	0.14/0.14	0.17/0.17	ns
Sequential Delays					
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.53	0.54	0.66	ns
Propagation Delays					
T_{ISDO_DO}	D input to DO output pin	0.11	0.11	0.13	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in the timing report.

Output Serializer/Deserializer Switching Characteristics

Table 54: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Setup/Hold					
T_{OSDCK_D}/T_{OSCKD_D}	D input setup/hold with respect to CLKDIV	0.42/0.03	0.45/0.03	0.63/0.03	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input setup/hold with respect to CLK	0.69/–0.13	0.73/–0.13	0.88/–0.13	ns
T_{OSDCK_T2}/T_{OSCKD_T2}(1)	T input setup/hold with respect to CLKDIV	0.31/–0.13	0.34/–0.13	0.39/–0.13	ns
T_{OSCCK_OCE}/T_{OSCKC_OCE}	OCE input setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	ns
T_{OSCCK_S}	SR (reset) input setup with respect to CLKDIV	0.47	0.52	0.85	ns
T_{OSCCK_TCE}/T_{OSCKC_TCE}	TCE input setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	ns
Sequential Delays					
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.40	0.42	0.48	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.47	0.49	0.56	ns
Combinatorial					
T_{OSDO_TTQ}	T input to TQ out	0.83	0.92	1.11	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the timing report.

Input Delay Switching Characteristics

Table 55: **Input Delay Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
IDELAYCTRL					
T_{DLYCCO_RDY}	Reset to ready for IDELAYCTRL	3.67	3.67	3.67	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.0(1)	200	200	200	MHz
	Attribute REFCLK frequency = 300.0(1)	300	300	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum reset pulse width	59.28	59.28	59.28	ns
IDELAY					
$T_{IDELAYRESOLUTION}$	IDELAY chain delay resolution	1/(32 x 2 x F_{REF})			ps
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3)	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4)	±9	±9	±9	ps per tap
$T_{IDELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY	680.00	680.00	600.00	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY	0.12/0.11	0.16/0.13	0.21/0.16	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY	0.12/0.16	0.14/0.18	0.16/0.22	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY	0.15/0.09	0.16/0.11	0.18/0.14	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

Table 56: **IO_FIFO Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
IO_FIFO Clock to Out Delays					
T_{OFFCKO_DO}	RDCLK to Q outputs	0.55	0.60	0.68	ns
T_{CKO_FLAGS}	Clock to IO_FIFO flags	0.55	0.61	0.77	ns
Setup/Hold					
T_{CCK_D}/T_{CKC_D}	D inputs to WRCLK	0.47/0.02	0.51/0.02	0.58/0.02	ns
T_{IFFCCK_WREN} /T_{IFFCKC_WREN}	WREN to WRCLK	0.42/–0.01	0.47/–0.01	0.53/–0.01	ns
T_{OFFCCK_RDEN}/T_{OFFCKC_RDEN}	RDEN to RDCLK	0.53/0.02	0.58/0.02	0.66/0.02	ns
Minimum Pulse Width					
$T_{PWH\_IO\_FIFO}$	RESET, RDCLK, WRCLK	1.62	2.15	2.15	ns
$T_{PWL\_IO\_FIFO}$	RESET, RDCLK, WRCLK	1.62	2.15	2.15	ns
Maximum Frequency					
F_{MAX}	RDCLK and WRCLK	266.67	200.00	200.00	MHz

CLB Switching Characteristics

Table 57: **CLB Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Combinatorial Delays					
T_{ILO}	An – Dn LUT address to A	0.10	0.11	0.13	ns, Max
T_{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.27	0.30	0.36	ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A	0.42	0.46	0.55	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.94	1.05	1.27	ns, Max
T_{AXA}	AX inputs to AMUX output	0.62	0.69	0.84	ns, Max
T_{AXB}	AX inputs to BMUX output	0.58	0.66	0.83	ns, Max
T_{AXC}	AX inputs to CMUX output	0.60	0.68	0.82	ns, Max
T_{AXD}	AX inputs to DMUX output	0.68	0.75	0.90	ns, Max
T_{BXB}	BX inputs to BMUX output	0.51	0.57	0.69	ns, Max
T_{BXD}	BX inputs to DMUX output	0.62	0.69	0.82	ns, Max
T_{CXC}	CX inputs to CMUX output	0.42	0.48	0.58	ns, Max
T_{CXD}	CX inputs to DMUX output	0.53	0.59	0.71	ns, Max
T_{DXD}	DX inputs to DMUX output	0.52	0.58	0.70	ns, Max
Sequential Delays					
T_{CKO}	Clock to AQ – DQ outputs	0.40	0.44	0.53	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.47	0.53	0.66	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK					
T_{AS}/T_{AH}	A_N – D_N input to CLK on A – D flip-flops	0.07/0.12	0.09/0.14	0.11/0.18	ns, Min
T_{DICK}/T_{CKDI}	A_X – D_X input to CLK on A – D flip-flops	0.06/0.19	0.07/0.21	0.09/0.26	ns, Min
	A_X – D_X input through MUXs and/or carry logic to CLK on A – D flip-flops	0.59/0.08	0.66/0.09	0.81/0.11	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D flip-flops	0.15/0.00	0.17/0.00	0.21/0.01	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D flip-flops	0.38/0.03	0.43/0.04	0.53/0.05	ns, Min
Set/Reset					
T_{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.53	0.59	0.71	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.52	0.58	0.70	ns, Max
F_{TOG}	Toggle frequency (for export control)	1412	1286	1098	MHz

Notes:

1. These items are of interest for carry-chain applications.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 58: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Sequential Delays					
T_{SHCKO}[1]	Clock to A – B outputs	0.98	1.09	1.32	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.37	1.53	1.86	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{DS_LRAM}/T_{DH_LRAM}	A – D inputs to CLK	0.54/0.28	0.60/0.30	0.72/0.35	ns, Min
T_{AS_LRAM}/T_{AH_LRAM}	Address An inputs to clock	0.27/0.55	0.30/0.60	0.37/0.70	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.69/0.18	0.77/0.21	0.94/0.26	ns, Min
T_{WS_LRAM}/T_{WH_LRAM}	WE input to clock	0.38/0.10	0.43/0.12	0.53/0.17	ns, Min
$T_{CECK\_LRAM}/T_{CKCE\_LRAM}$	CE input to CLK	0.39/0.10	0.44/0.11	0.53/0.17	ns, Min
Clock CLK					
T_{MPW_LRAM}	Minimum pulse width	1.05	1.13	1.25	ns, Min
T_{MCP}	Minimum clock period	2.10	2.26	2.50	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 59: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Sequential Delays					
T_{REG}	Clock to A – D outputs	1.19	1.33	1.61	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.58	1.77	2.15	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	1.12	1.23	1.46	ns, Max
Setup and Hold Times Before/After Clock CLK					
$T_{WS\_SHFREG}/T_{WH\_SHFREG}$	WE input	0.37/0.10	0.41/0.12	0.51/0.17	ns, Min
$T_{CECK\_SHFREG}/T_{CKCE\_SHFREG}$	CE input to CLK	0.37/0.10	0.42/0.11	0.52/0.17	ns, Min
$T_{DS\_SHFREG}/T_{DH\_SHFREG}$	A – D inputs to CLK	0.33/0.34	0.37/0.37	0.44/0.43	ns, Min
Clock CLK					
T_{MPW_SHFREG}	Minimum pulse width	0.77	0.86	0.98	ns, Min

Block RAM and FIFO Switching Characteristics

Table 60: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Block RAM and FIFO Clock to Out Delays					
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$[1]	Clock CLK to DOUT output (without output register)[2][3]	1.85	2.13	2.46	ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.64	0.74	0.89	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)[2][3]	2.77	3.04	3.84	ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.73	0.81	0.94	ns, Max
$T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$	Clock CLK to DOUT output with cascade (without output register)[2]	2.61	2.88	3.30	ns, Max
	Clock CLK to DOUT output with cascade (with output register)[4]	1.16	1.28	1.46	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.76	0.87	1.05	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs[7]	0.94	1.02	1.15	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.78	0.85	0.94	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (without output register)	2.56	2.81	3.55	ns, Max
	Clock CLK to BITERR (with output register)	0.68	0.76	0.89	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.75	0.88	1.07	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.84	0.93	1.08	ns, Max
Setup and Hold Times Before/After Clock CLK					
$T_{RCCK\_ADDRA}/T_{RCKC\_ADDRA}$	ADDR inputs[8]	0.45/0.31	0.49/0.33	0.57/0.36	ns, Min
$T_{RDCK\_DI\_WF\_NC}$/ $T_{RCKD\_DI\_WF\_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode[9]	0.58/0.60	0.65/0.63	0.74/0.67	ns, Min
$T_{RDCK\_DI\_RF}/T_{RCKD\_DI\_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode[9]	0.20/0.29	0.22/0.34	0.25/0.41	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode[9]	0.50/0.43	0.55/0.46	0.63/0.50	ns, Min
	DIN inputs with block RAM ECC encode only[9]	0.93/0.43	1.02/0.46	1.17/0.50	ns, Min
	DIN inputs with FIFO ECC in standard mode[9]	1.04/0.56	1.15/0.59	1.32/0.64	ns, Min
$T_{RCCK\_INJECTBITERR}$/ $T_{RCKC\_INJECTBITERR}$	Inject single/double bit error in ECC mode	0.58/0.35	0.64/0.37	0.74/0.40	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	Block RAM enable (EN) input	0.35/0.20	0.39/0.21	0.45/0.23	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.24/0.15	0.29/0.15	0.36/0.16	ns, Min
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	Synchronous RSTREG input	0.29/0.07	0.32/0.07	0.35/0.07	ns, Min
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.32/0.42	0.34/0.43	0.36/0.46	ns, Min
$T_{RCCK\_WEA}/T_{RCKC\_WEA}$	Write enable (WE) input (block RAM only)	0.44/0.18	0.48/0.19	0.54/0.20	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.46/0.30	0.46/0.35	0.47/0.43	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.42/0.30	0.43/0.35	0.43/0.43	ns, Min

Table 60: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Reset Delays					
T_{RCO_FLAGS}	Reset RST to FIFO flags/pointers(10)	0.90	0.98	1.10	ns, Max
$T_{RREC\_RST}/T_{RREM\_RST}$	FIFO reset recovery and removal timing(11)	1.87/–0.81	2.07/–0.81	2.37/–0.81	ns, Max
Maximum Frequency					
$F_{MAX\_BRAM\_WF\_NC}$	Block RAM (write first and no change modes) When not in SDP RF mode.	509.68	460.83	388.20	MHz
$F_{MAX\_BRAM\_RF\_PERFORMANCE}$	Block RAM (read first, performance mode) When in SDP RF mode but no address overlap between port A and port B.	509.68	460.83	388.20	MHz
$F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$	Block RAM (read first, delayed write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses.	447.63	404.53	339.67	MHz
$F_{MAX\_CAS\_WF\_NC}$	Block RAM cascade (write first, no change mode) When cascade but not in RF mode.	467.07	418.59	345.78	MHz
$F_{MAX\_CAS\_RF\_PERFORMANCE}$	Block RAM cascade (read first, performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled.	467.07	418.59	345.78	MHz
$F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B.	405.35	362.19	297.35	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	509.68	460.83	388.20	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	410.34	365.10	297.53	MHz

Notes:

1. The timing report will report all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, and T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

DSP48E1 Switching Characteristics

Table 61: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Setup and Hold Times of Data/Control Pins to the Input Register Clock					
$T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$	A input to A register CLK	0.26/0.12	0.30/0.13	0.37/0.14	ns
$T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$	B input to B register CLK	0.33/0.15	0.38/0.16	0.45/0.18	ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.17/0.17	0.20/0.19	0.24/0.21	ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.25/0.25	0.32/0.27	0.42/0.27	ns
$T_{DSPDCK\_ACIN\_AREG}$/$T_{DSPCKD\_ACIN\_AREG}$	ACIN input to A register CLK	0.23/0.12	0.27/0.13	0.32/0.14	ns
$T_{DSPDCK\_BCIN\_BREG}$/$T_{DSPCKD\_BCIN\_BREG}$	BCIN input to B register CLK	0.25/0.15	0.29/0.16	0.36/0.18	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock					
$T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_B\_MREG\_MULT}$	{A, B,} input to M register CLK using multiplier	2.40/–0.01	2.76/–0.01	3.29/–0.01	ns
$T_{DSPDCK\_\{A, B\}\_ADREG}$/ $T_{DSPCKD\_ D\_ADREG}$	{A, D} input to AD register CLK	1.29/–0.02	1.48/–0.02	1.76/–0.02	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock					
$T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\} \_PREG\_MULT}$	{A, B} input to P register CLK using multiplier	4.02/–0.28	4.60/–0.28	5.48/–0.28	ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK using multiplier	3.93/–0.73	4.50/–0.73	5.35/–0.73	ns
$T_{DSPDCK\_\{A, B\} \_PREG}$/ $T_{DSPCKD\_\{A, B\} \_PREG}$	A or B input to P register CLK not using multiplier	1.73/–0.28	1.98/–0.28	2.35/–0.28	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK not using multiplier	1.54/–0.26	1.76/–0.26	2.10/–0.26	ns
$T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$	PCIN input to P register CLK	1.32/–0.15	1.51/–0.15	1.80/–0.15	ns
Setup and Hold Times of the CE Pins					
$T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.35/0.06	0.42/0.08	0.52/0.11	ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.28/0.10	0.34/0.11	0.42/0.13	ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.36/–0.03	0.43/–0.03	0.52/–0.03	ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.17/0.18	0.21/0.20	0.27/0.23	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.36/0.01	0.43/0.01	0.53/0.01	ns
Setup and Hold Times of the RST Pins					
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.41/0.11	0.46/0.13	0.55/0.15	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.07/0.10	0.08/0.11	0.09/0.12	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.44/0.07	0.50/0.08	0.59/0.09	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.21/0.22	0.23/0.24	0.27/0.28	ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.27/0.01	0.30/0.01	0.35/0.01	ns

Table 61: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Combinatorial Delays from Input Pins to Output Pins					
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier	3.79	4.35	5.18	ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier	3.72	4.26	5.07	ns
$T_{DSPDO\_B\_P}$	B input to P output not using multiplier	1.53	1.75	2.08	ns
$T_{DSPDO\_C\_P}$	C input to P output	1.33	1.53	1.82	ns
Combinatorial Delays from Input Pins to Cascading Output Pins					
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.55	0.63	0.74	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$	{A, B} input to CARRYCASCOUT output using multiplier	4.06	4.65	5.54	ns
$T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$	D input to CARRYCASCOUT output using multiplier	3.97	4.54	5.40	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.77	2.03	2.41	ns
$T_{DSPDO\_C\_CARRYCASCOUT}$	C input to CARRYCASCOUT output	1.58	1.81	2.15	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins					
$T_{DSPDO\_ACIN\_P\_MULT}$	ACIN input to P output using multiplier	3.65	4.19	5.00	ns
$T_{DSPDO\_ACIN\_P}$	ACIN input to P output not using multiplier	1.37	1.57	1.88	ns
$T_{DSPDO\_ACIN\_ACOUT}$	ACIN input to ACOUT output	0.38	0.44	0.53	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$	ACIN input to CARRYCASCOUT output using multiplier	3.90	4.47	5.33	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT}$	ACIN input to CARRYCASCOUT output not using multiplier	1.61	1.85	2.21	ns
$T_{DSPDO\_PCIN\_P}$	PCIN input to P output	1.11	1.28	1.52	ns
$T_{DSPDO\_PCIN\_CARRYCASCOUT}$	PCIN input to CARRYCASCOUT output	1.36	1.56	1.85	ns
Clock to Outs from Output Register Clock to Output Pins					
$T_{DSPCKO\_P\_PREG}$	CLK PREG to P output	0.33	0.37	0.44	ns
$T_{DSPCKO\_CARRYCASCOUT\_PREG}$	CLK PREG to CARRYCASCOUT output	0.52	0.59	0.69	ns
Clock to Outs from Pipeline Register Clock to Output Pins					
$T_{DSPCKO\_P\_MREG}$	CLK MREG to P output	1.68	1.93	2.31	ns
$T_{DSPCKO\_CARRYCASCOUT\_MREG}$	CLK MREG to CARRYCASCOUT output	1.92	2.21	2.64	ns
$T_{DSPCKO\_P\_ADREG\_MULT}$	CLK ADREG to P output using multiplier	2.72	3.10	3.69	ns
$T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$	CLK ADREG to CARRYCASCOUT output using multiplier	2.96	3.38	4.02	ns
Clock to Outs from Input Register Clock to Output Pins					
$T_{DSPCKO\_P\_AREG\_MULT}$	CLK AREG to P output using multiplier	3.94	4.51	5.37	ns
$T_{DSPCKO\_P\_BREG}$	CLK BREG to P output not using multiplier	1.64	1.87	2.22	ns
$T_{DSPCKO\_P\_CREG}$	CLK CREG to P output not using multiplier	1.69	1.93	2.30	ns
$T_{DSPCKO\_P\_DREG\_MULT}$	CLK DREG to P output using multiplier	3.91	4.48	5.32	ns

Table 61: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Clock to Outs from Input Register Clock to Cascading Output Pins					
$T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.64	0.73	0.87	ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	4.19	4.79	5.70	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$	CLK BREG to CARRYCASCOUT output not using multiplier	1.88	2.15	2.55	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$	CLK DREG to CARRYCASCOUT output using multiplier	4.16	4.76	5.65	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$	CLK CREG to CARRYCASCOUT output	1.94	2.21	2.63	ns
Maximum Frequency					
F_{MAX}	With all registers used	628.93	550.66	464.25	MHz
F_{MAX_PATDET}	With pattern detector	531.63	465.77	392.93	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	349.28	305.62	257.47	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	317.26	277.62	233.92	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	397.30	346.26	290.44	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	397.30	346.26	290.44	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	260.01	227.01	190.69	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	241.72	211.15	177.43	MHz

Clock Buffers and Networks

Table 62: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins setup/hold	0.13/0.39	0.14/0.41	0.18/0.42	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins setup/hold	0.13/0.39	0.14/0.41	0.18/0.42	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.08	0.09	0.11	ns
Maximum Frequency					
F_{MAX_BUFG}	Global clock tree (BUFG)	628.00	628.00	464.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 63: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
T_{BIOCKO_O}	Clock to out delay from I to O	1.16	1.32	1.61	ns
Maximum Frequency					
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	680.00	680.00	600.00	MHz

Table 64: **Regional Clock Buffer Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
T_{BRCKO_O}	Clock to out delay from I to O	0.64	0.80	1.04	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.35	0.41	0.54	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.85	0.89	1.14	ns
Maximum Frequency					
F_{MAX_BUFR}(1)	Regional clock tree (BUFR)	420.00	375.00	315.00	MHz

Notes:

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO F_{MAX} frequency.

Table 65: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
T_{BHCKO_O}	BUFH delay from I to O	0.11	0.11	0.14	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin setup and hold	0.20/0.13	0.23/0.16	0.29/0.21	ns
Maximum Frequency					
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	628.00	628.00	464.00	MHz

Table 66: **Duty-Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
T_{DCD_CLK}	Global clock tree duty-cycle distortion(1)	All	0.20	0.20	0.20	ns
T_{CKSKEW}	Global clock tree skew(2)	XC7Z010	0.27	0.27	0.27	ns
		XC7Z020	0.33	0.38	0.42	ns
T_{DCD_BUFIO}	I/O clock tree duty-cycle distortion	All	0.14	0.14	0.14	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	ns
T_{DCD_BUFR}	Regional clock tree duty-cycle distortion	All	0.18	0.18	0.18	ns

Notes:

1. These parameters represent the worst-case duty-cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty-cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate application specific clock skew.

MMCM Switching Characteristics

Table 67: **MMCM Specification**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
MMCM_F_{INMAX}	Maximum input clock frequency	800.00	800.00	800.00	MHz
MMCM_F_{INMIN}	Minimum input clock frequency	10.00	10.00	10.00	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max			
MMCM_F_{INDUTY}	Allowable input duty cycle: 10—49 MHz	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase-shift clock frequency	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase-shift clock frequency	550.00	500.00	450.00	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency	600.00	600.00	600.00	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency	1600.00	1440.00	1200.00	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical(1)	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical(1)	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs(2)	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter	Note 3			
MMCM_$T_{OUTDUTY}$	MMCM output clock duty-cycle precision(4)	0.20	0.20	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time	100.00	100.00	100.00	µs
MMCM_F_{OUTMAX}	MMCM maximum output frequency	800.00	800.00	800.00	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency(5)(6)	4.69	4.69	4.69	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max			
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector	10.00	10.00	10.00	MHz

Table 67: **MMCM Specification *(Cont'd)***

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle			
MMCM Switching Characteristics Setup and Hold					
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and hold of phase-shift enable	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and hold of phase-shift increment/decrement	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{MMCMCKO\_PSDONE}$	Phase shift clock-to-out of PSDONE	0.59	0.68	0.81	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK					
$T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$	DADDR setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
$T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$	DI setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
$T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$	DEN setup/hold	1.76/0.00	1.97/0.00	2.29/0.00	ns, Min
$T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$	DWE setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY	0.65	0.72	0.99	ns, Max
F_{DCK}	DCLK frequency	200.00	200.00	200.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F_{OUTMIN} is 0.036 MHz.

PLL Switching Characteristics

Table 68: **PLL Specification**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
PLL_F_{INMAX}	Maximum input clock frequency	800.00	800.00	800.00	MHz
PLL_F_{INMIN}	Minimum input clock frequency	19.00	19.00	19.00	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max			
PLL_F_{INDUTY}	Allowable input duty cycle: 19—49 MHz	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency	800.00	800.00	800.00	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency	2133.00	1866.00	1600.00	MHz
PLL_$F_{BANDWIDTH}$	Low PLL bandwidth at typical(1)	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical(1)	4.00	4.00	4.00	MHz
PLL_$T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs(2)	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL output jitter	Note 3			
PLL_$T_{OUTDUTY}$	PLL output clock duty-cycle precision(4)	0.20	0.20	0.20	ns
PLL_$T_{LOCKMAX}$	PLL maximum lock time	100.00	100.00	100.00	µs
PLL_F_{OUTMAX}	PLL maximum output frequency	800.00	800.00	800.00	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency(5)	6.25	6.25	6.25	MHz
PLL_$T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max			
PLL_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector	19.00	19.00	19.00	MHz
PLL_$T_{FBDELAY}$	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle			
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK					
$T_{PLLCCK\_DADDR}/T_{PLLCKC\_DADDR}$	Setup and hold of D address	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
$T_{PLLCCK\_DI}/T_{PLLCKC\_DI}$	Setup and hold of D input	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
$T_{PLLCCK\_DEN}/T_{PLLCKC\_DEN}$	Setup and hold of D enable	1.76/0.00	1.97/0.00	2.29/0.00	ns, Min
$T_{PLLCCK\_DWE}/T_{PLLCKC\_DWE}$	Setup and hold of D write enable	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
T_{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	ns, Max
F_{DCK}	DCLK frequency	200.00	200.00	200.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

Table 69: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *without* MMCM/PLL.						
T_{ICKOF}	Clock-capable clock input and OUTFF without MMCM/PLL (near clock region)	XC7Z010	5.08	5.68	6.65	ns
		XC7Z020	5.42	6.05	7.08	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 70: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *without* MMCM/PLL.						
$T_{ICKOFFAR}$	Clock-capable clock input and OUTFF *without* MMCM/PLL (far clock region)	XC7Z010	5.08	5.68	6.65	ns
		XC7Z020	5.69	6.34	7.40	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 71: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *with* MMCM.						
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM	XC7Z010	1.04	1.03	1.03	ns
		XC7Z020	1.05	1.04	1.05	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 72: **Clock-Capable Clock Input to Output Delay With PLL**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flops, Fast Slew Rate, *with* PLL.						
$T_{ICKOFPLLCC}$	Clock-capable clock input and OUTFF *with* PLL	XC7Z010	0.82	0.82	0.82	ns
		XC7Z020	0.82	0.82	0.82	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 73: **Pin-to-Pin, Clock-to-Out using BUFIO**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.					
$T_{ICKOFCS}$	Clock to out of I/O clock	4.93	5.52	6.20	ns

Device Pin-to-Pin Input Parameter Guidelines

Table 74: **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)						
T_{PSFD}/ T_{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks	XC7Z010	2.00/–0.17	2.13/–0.17	2.44/–0.17	ns
		XC7Z020	2.55/–0.25	2.74/–0.25	3.18/–0.25	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch.

Table 75: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)						
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No delay clock-capable clock input and IFF(2) with MMCM	XC7Z010	2.36/–0.62	2.68/–0.62	3.22/–0.62	ns
		XC7Z020	2.48/–0.62	2.82/–0.62	3.38/–0.62	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 76: **Clock-Capable Clock Input Setup and Hold With PLL**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)						
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No delay clock-capable clock input and IFF(2) with PLL	XC7Z010	2.67/–0.19	3.03/–0.19	3.64/–0.19	ns
		XC7Z020	2.79/–0.20	3.17/–0.20	3.80/–0.20	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 77: **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.					
T_{PSCS}/T_{PHCS}	Setup and hold of I/O clock	–0.36/1.36	–0.36/1.50	–0.36/1.70	ns

Table 78: **Sample Window**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
T_{SAMP}	Sampling error at receiver pins(1)	0.59	0.64	0.70	ns
T_{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO(2)	0.35	0.40	0.46	ns

Notes:

1. This parameter indicates the total sampling error of the PL DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the PL DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for PL clock transmitter and receiver data-valid windows.

Table 79: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package skew(1)	XC7Z010	CLG225	101	ps
			CLG400	155	ps
		XC7Z020	CLG400	166	ps
			CLG484	248	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

XADC Specifications

Table 80: **XADC Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 26 MHz, T_j = –40°C to 100°C, Typical values at T_j=+40°C						
ADC Accuracy(1)						
Resolution			12	–	–	Bits
Integral Nonlinearity(2)	INL		–	–	±2	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Unipolar operation	–	–	±8	LSBs
		Bipolar operation	–	–	±4	LSBs
Gain Error			–	–	±0.5	%
Offset Matching			–	–	4	LSBs
Gain Matching			–	–	0.3	%
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio(2)	SNR	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion(2)	THD	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	70	–	–	dB
ADC Accuracy at Extended Temperatures (-55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity(2)	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs(3)						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T_j = –40°C to 100°C.	–	–	±4	°C
		T_j = –55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –40°C to +100°C	–	–	±1	%
		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –55°C to +125°C	–	–	±2	%
Conversion Rate(4)						
Conversion Time - Continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	Cycles
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz

Table 80: **XADC Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
DCLK Duty Cycle			40	–	60	%
XADC Reference(5)						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V

Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for BitGen option XADCEnhancedLinearity = ON.
3. See the ADC chapter in the *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) for a detailed description.
4. See the Timing chapter in the *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) for a detailed description.
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Configuration Switching Characteristics

Table 81: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Power-up Timing Characteristics					
T_{POR}	Power-on reset	50.00	50.00	50.00	ms, Max
Boundary-Scan Port Timing Specifications					
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup/hold	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	7.00	7.00	7.00	ns, Max
F_{TCK}	TCK frequency	66.00	66.00	66.00	MHz, Max
Internal Configuration Access Port					
F_{ICAPCK}	Internal configuration access port (ICAPE2)	100.00	100.00	100.00	MHz, Max

eFUSE Programming Conditions

Table 82 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470).

Table 82: **eFUSE Programming Conditions**(1)

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
t_j	Temperature range	15	–	125	°C

Notes:

1. The Zynq-7000 device must not be configured during eFUSE programming.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
05/07/2012	1.0	Initial Xilinx release.
06/27/2012	1.1	Updated the descriptions, changed V_{IN}, Note 3, Note 4, and added V_{PREF}, V_{PIN}, and Note 5 in Table 1. In Table 2, updated descriptions and notes. Updated Table 3 and added R_{IN_TERM}. Removed I_{CCMIOQ} from Table 5. Removed I_{CCMIOQ} and updated XC7Z020 in Table 6. Updated LVCMOS12, SSTL135, and SSTL15 in Table 10. Updated Table 17. In PS Performance Characteristics section, added timing diagrams and revised many tables. Updated Table 47 and removed notes 2 and 3. Added Note 2 and Note 3 to Table 48. Changed Table 50 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 57. In Table 80 updated Offset Error and Matching descriptions and Gain Error and Matching descriptions, and added Note 2 to Integral Nonlinearity.
09/12/2012	1.2	Changed Note 3 and added Note 5 in Table 1. Updated T_j in Table 2, also revised Note 4 and Note 8. Updated specifications including R_{IN_TERM} in Table 3. Added Table 4. Updated the XC7Z020 specifications in Table 6. Updated standards in Table 8. Updated specifications in Table 12. Updated the AC Switching Characteristics section for the ISE 14.2 speed specifications throughout the document. In PS Performance Characteristics section introduction, revised tables, updated Figure 4, and added Figure 5. Updated parameters in Figure 5 through Figure 13. Updated values in Table 16. Added Note 2 to Table 23. Added Note 3 to Table 32. Updated descriptions and revised $F_{MSPICLK}$ in Table 37. Updated Note 3 in Table 48. Changed F_{PFDMAX} conditions in Table 67 and Table 68. Updated devices and added values to Table 79.
02/11/2013	1.3	Updated the AC Switching Characteristics based upon ISE 14.4 and Vivado 2012.4, both at v1.05 for the -3, -2, and -1 speed specifications throughout the document. Updated Table 14 and Table 15 to the product status of production for the XC7Z020 devices with -2 and -1 speed specifications. Updated description in Introduction. Revised V_{PIN} in Table 1. Revised V_{PIN} and I_{IN} and added Note 2 to Table 2. Clarified PS specifications, added C_{PIN}, and removed Note 3 on I_{RPD} in Table 3. Added values to Table 5. Updated Power Supply Requirements section. Revised descriptions in Table 7. Revised Note 1, removed LVTTL, notes 2 and 3, and added SSTL135 to Table 8. Added Table 9. Removed HSTL_I_12 and SSTL_12 from Table 10. Removed DIFF_SSTL12 from Table 12. Revise in V_{CCO} min/max in Table 13. Many changes to the PS Switching Characteristics section including adding tables, figures, notes with test conditions where applicable. In Table 16, updated the 6:2:1 clock ratio frequencies. Updated minimum value for $T_{ULPIDCK}$ in Table 31. Added a 2:1 memory controller section to Table 48. Updated Note 1 in Table 64. Updated Note 1 and Note 2 in Table 79.Updated the rows on offset error and matching and gain error and matching and the maximum external channel input ranges in Table 80. Added Internal Configuration Access Port section to Table 81.
02/14/2013	1.4	Corrected $T_{QSPICKD2}$ minimum equation in Table 30. Updated timing parameter names in Figure 3 and Figure 4 to match those in the accompanying table.
02/19/2013	1.4.1	Corrected version history.

Date	Version	Description of Revisions
03/19/2013	1.5	Updated Table 14 and Table 15 to the product status of production for the XC7Z010 devices with -2 and -1 speed specifications. Updated Figure 3 by adding OUT0. Added Note 2 to Table 29. Added Table 34 and Figure 8.
04/24/2013	1.6	All the devices listed in this data sheet are production released. Updated the AC Switching Characteristics based upon ISE 14.5 and Vivado 2013.1, both at v1.06 for the -3, -2, and -1 speed specifications throughout the document. Updated Table 14 and Table 15 for production release of the XC7Z010 and XC7Z020 in the -3 speed designations. Removed the *PS Power-on Reset* section. Updated the PS—PL Power Sequencing section. In Table 1, revised V_{IN} (I/O input voltage) to match values in Table 4, and combined Note 4 with old Note 5 and then added new Note 6. Revised V_{IN} description and added Note 7 in Table 2. Updated first 3 rows in Table 4. Revised PCI33_3 voltage minimum in Table 10 to match values in Table 1 and Table 4. Added Note 1 to Table 13. Clarified the load conditions in Table 30 by adding new data. Clarified title of Table 48. Throughout the data sheet (Table 57, Table 58, Table 59, and Table 74) removed the obvious note “A Zero “0” Hold Time listing indicates no hold time or a negative hold time.”

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