CAP1105 / CAP1106

5 and 6 Channel Capacitive Touch Sensor

PRODUCT FEATURES

Datasheet

General Description

The CAP1106 and CAP1105, which incorporate SMSC's RightTouch® [1] technology, are multiple channel Capacitive Touch sensors. The CAP1106 contains six (6) individual capacitive touch sensor inputs while the CAP1105 contains five (5) sensor inputs. Both devices offer programmable sensitivity for use in touch sensor applications. Each sensor input automatically recalibrates to compensate for gradual environmental changes.

The CAP1105 / CAP1106 includes Multiple Pattern Touch recognition that allows the user to select a specific set of buttons to be touched simultaneously. If this pattern is detected, then a status bit is set and an interrupt generated.

Additionally, the CAP1105 / CAP1106 includes circuitry and support for enhanced sensor proximity detection.

The CAP1105 / CAP1106 offers multiple power states operating at low quiescent currents. In the Standby state of operation, one or more capacitive touch sensor inputs are active.

Deep Sleep is the lowest power state available, drawing 5uA (typical) of current. In this state, no sensor inputs are active. Communications will wake the device.

Applications

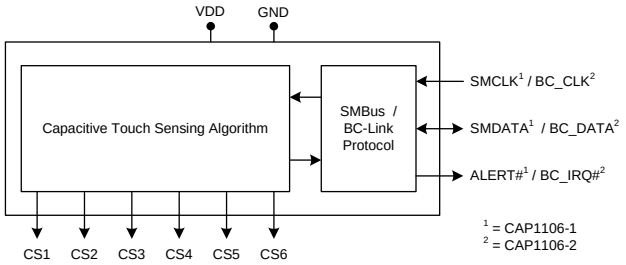
- Desktop and Notebook PCs
- LCD Monitors
- Consumer Electronics
- Appliances

Features

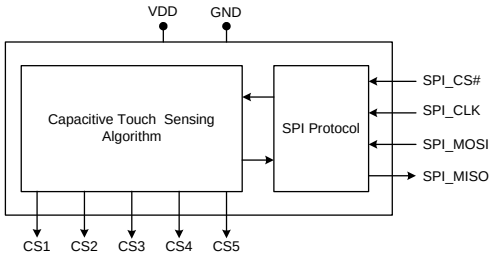
- Six (6) Capacitive Touch Sensor Inputs - CAP1106
- Five (5) Capacitive Touch Sensor Inputs - CAP1105
  - Programmable sensitivity
  - Automatic recalibration
  - Individual thresholds for each button
- Proximity Detection
- Multiple Button Pattern Detection
- Calibrates for Parasitic Capacitance
- Analog Filtering for System Noise Sources
- Press and Hold feature for Volume-like Applications
- Multiple Communication Interfaces
  - SMBus / I^2C compliant interface (CAP1106-1 only)
  - SMSC BC-Link interface (CAP1106-2 only)
  - SPI communications (CAP1105 only)
- Low Power Operation
  - 5uA quiescent current in Deep Sleep
  - 50uA quiescent current in Standby (1 sensor input monitored)
  - Samples one or more channels in Standby
- Available in 10-pin 3mm x 3mm RoHS compliant DFN package

1. SMSC, the SMSC logo and RightTouch are registered trademarks and the RightTouch logo is a trademark of Standard Microsystems Corporation ("SMSC").

CAP1106 BLOCK DIAGRAM



CAP1105 BLOCK DIAGRAM



Ordering Information:

ORDERING NUMBER	PACKAGE	FEATURES
CAP1106-1-AIA-TR	10-pin DFN 3mm x 3mm (Lead-free RoHS compliant)	Six capacitive touch sensor inputs, SMBus interface
CAP1106-2-AIA-TR	10-pin DFN 3mm x 3mm (Lead-free RoHS compliant)	Six capacitive touch sensor inputs, BC-Link interface
CAP1105-1-AIA-TR	10-pin DFN 3mm x 3mm (Lead-free RoHS compliant)	Five capacitive touch sensor inputs, Full Duplex SPI interface

Reel size is 4,000 pieces

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

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Chapter 1 Pin Description

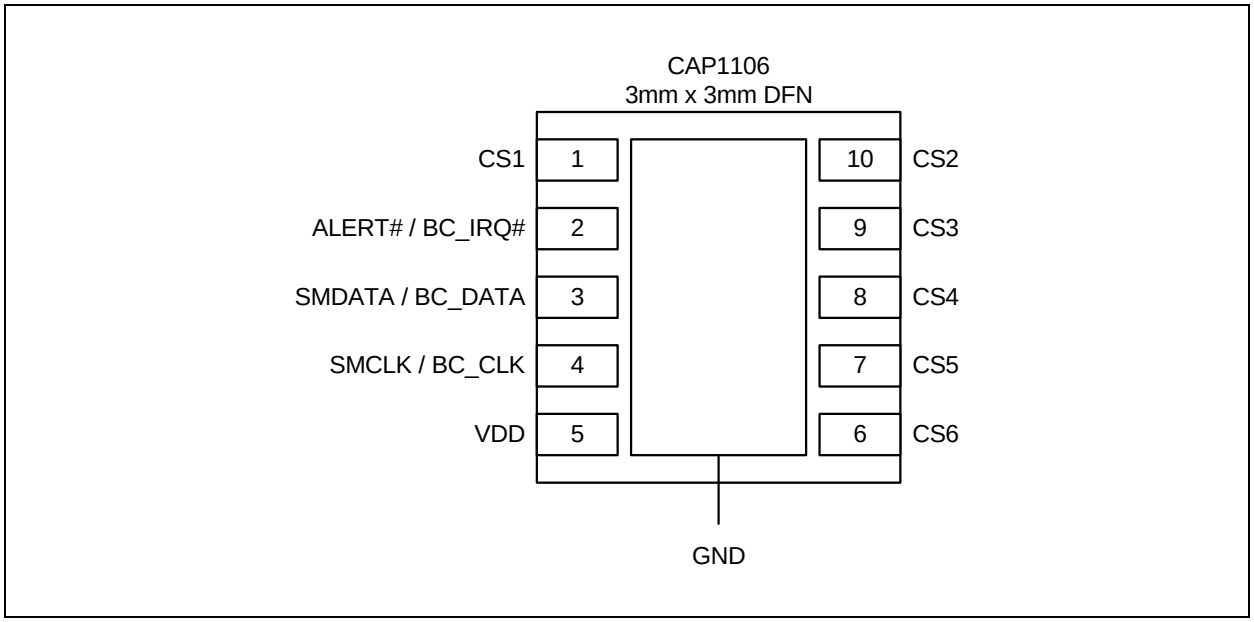


Figure 1.1 CAP1106 Pin Diagram (10-Pin DFN)

Table 1.1 Pin Description for CAP1106

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE	UNUSED CONNECTION
1	CS1	Capacitive Touch Sensor Input 1	AIO	Connect to Ground
2	ALERT# / BC_IRQ#	ALERT# - Active low alert / interrupt output for SMBus alert (CAP1106-1)	OD (5V)	Connect to Ground
		ALERT# - Active high alert / interrupt output for SMBus alert (CAP1106-1)	DO	leave open
		BC_IRQ# - Active low interrupt / optional for BC-Link (CAP1106-2)	OD (5V)	Connect to Ground
		BC_IRQ# - Active high push-pull interrupt / optional for BC-Link (CAP1106-2)	DO	leave open
3	SMDATA / BC_DATA	SMDATA - Bi-directional, open-drain SMBus data - requires pull-up resistor (CAP1106-1)	DIOD (5V)	n/a
		BC_DATA - Bi-directional, open-drain BC-Link data - requires pull-up resistor (CAP1106-2)	DIO	
4	SMCLK / BC_CLK	SMCLK - SMBus clock input - requires pull-up resistor (CAP1106-1)	DI (5V)	n/a
		BC_CLK - BC-Link clock input (CAP1106-2)	DI (5V)	

Table 1.1 Pin Description for CAP1106 (continued)

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE	UNUSED CONNECTION
5	VDD	Positive Power supply	Power	n/a
6	CS6	Capacitive Touch Sensor Input 6	AIO	Connect to Ground
7	CS5	Capacitive Touch Sensor Input 5	AIO	Connect to Ground
8	CS4	Capacitive Touch Sensor Input 4	AIO	Connect to Ground
9	CS3	Capacitive Touch Sensor Input 3	AIO	Connect to Ground
10	CS2	Capacitive Touch Sensor Input 2	AIO	Connect to Ground
Bottom Pad	GND	Ground	Power	n/a

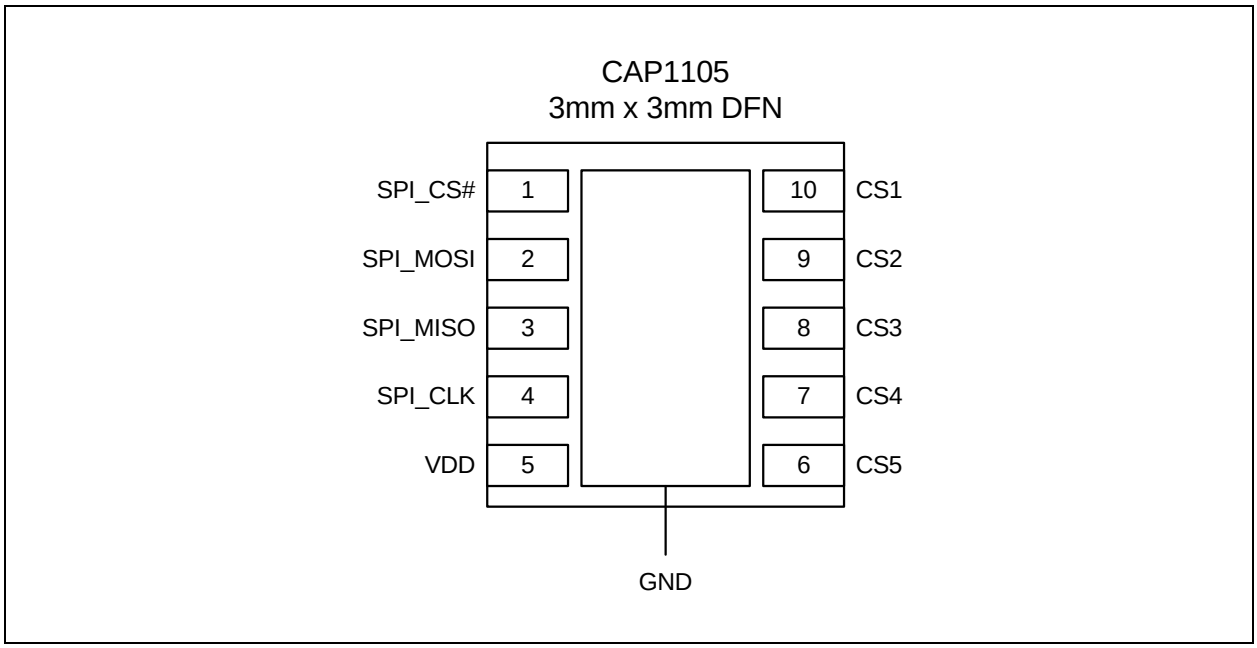


Figure 1.2 CAP1105 Pin Diagram (10-Pin DFN)

Table 1.2 Pin Description for CAP1105

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE	UNUSED CONNECTION
1	SPI_CS#	Active low chip-select for SPI bus	DI (5V)	n/a
2	SPI_MOSI	SPI_MOSI - SPI Master-Out-Slave-In port	DI (5V)	n/a

Table 1.2 Pin Description for CAP1105 (continued)

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE	UNUSED CONNECTION
3	SPI_MISO	SPI Master-In-Slave-Out data port	DO	n/a
4	SPI_CLK	SPI clock input	DI (5V)	n/a
5	VDD	Positive Power supply	Power	n/a
6	CS5	Capacitive Touch Sensor Input 5	AIO	Connect to Ground
7	CS4	Capacitive Touch Sensor Input 4	AIO	Connect to Ground
8	CS3	Capacitive Touch Sensor Input 3	AIO	Connect to Ground
9	CS2	Capacitive Touch Sensor Input 2	AIO	Connect to Ground
10	CS1	Capacitive Touch Sensor Input 1	AIO	Connect to Ground
Bottom Pad	GND	Ground	Power	n/a

APPLICATION NOTE: When the ALERT# pin (CAP1106 only) is configured as an active low output, it will be open drain. When it is configured as an active high output, it will be push-pull.

APPLICATION NOTE: For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the CAP1105 / CAP1106 is unpowered.

The pin types are described in Table 1.3. All pins labeled with (5V) are 5V tolerant.

Table 1.3 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
DI	Digital Input - This pin is used as a digital input. This pin is 5V tolerant.
AIO	Analog Input / Output -This pin is used as an I/O for analog signals.
DIOD	Digital Input / Open Drain Output - This pin is used as a digital I/O. When it is used as an output, it is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output - This pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.
DO	Push-pull Digital Output - This pin is used as a digital output and can sink and source current.
DIO	Push-pull Digital Input / Output - This pin is used as an I/O for digital signals.

Chapter 2 Electrical Specifications

Table 2.1 Absolute Maximum Ratings

Voltage on 5V tolerant pins (V_{5VT_PIN})	-0.3 to 5.5	V
Voltage on 5V tolerant pins ($\|V_{5VT\_PIN} - V_{DD}\|$) Note 2.2	0 to 3.6	V
Voltage on VDD pin	-0.3 to 4	V
Voltage on any other pin to GND	-0.3 to VDD + 0.3	V
Package Power Dissipation up to T_A = 85°C for 10 pin DFN (see Note 2.3)	0.7	W
Junction to Ambient (θ_{JA})	77.7	°C/W
Operating Ambient Temperature Range	-40 to 125	°C
Storage Temperature Range	-55 to 150	°C
ESD Rating, All Pins, HBM	8000	V

Note 2.1 Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note 2.2 For the 5V tolerant pins that have a pull-up resistor, the voltage difference between V_{5VT_PIN} and V_{DD} must never exceed 3.6V.

Note 2.3 The Package Power Dissipation specification assumes a recommended thermal via design consisting of a 2x2 matrix of 0.3mm (12mil) vias at 1.0mm pitch connected to the ground plane with a 1.6 x 2.3mm thermal landing.

Table 2.2 Electrical Specifications

V_{DD} = 3V to 3.6V, T_A = 0°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	

Table 2.2 Electrical Specifications (continued)

V_{DD} = 3V to 3.6V, T_A = 0°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Supply Current	I_{STBY}		120	170	uA	Standby state active 1 sensor input monitored Default conditions (8 avg, 70ms cycle time)
	I_{STBY}		50		uA	Standby state active 1 sensor input monitored 1 avg, 140ms cycle time,
	I_{DSLEEP}		5	15	uA	Deep Sleep state active No communications T_A < 40°C 3.135 < V_{DD} < 3.465V
	I_{DD}		500	600	uA	Capacitive Sensing Active
Capacitive Touch Sensor Inputs						
Maximum Base Capacitance	C_{BASE}		50		pF	Pad untouched
Minimum Detectable Capacitive Shift	ΔC_{TOUCH}	20			fF	Pad touched - default conditions (1 avg, 35ms cycle time, 1x sensitivity)
Recommended Cap Shift	ΔC_{TOUCH}	0.1		2	pF	Pad touched - Not tested
Power Supply Rejection	PSR		±3	±10	counts / V	Untouched Current Counts Base Capacitance 5pF - 50pF Maximum sensitivity Negative Delta Counts disabled All other parameters default
Timing						
Time to communications ready	t_{COMM_DLY}			15	ms	
Time to first conversion ready	t_{CONV_DLY}		170	200	ms	
I/O Pins						
Output Low Voltage	V_{OL}			0.4	V	I_{SINK_IO} = 8mA
Output High Voltage	V_{OH}	V_{DD} - 0.4			V	I_{SOURCE_IO} = 8mA
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Leakage Current	I_{LEAK}			±5	uA	powered or unpowered T_A < 85°C pull-up voltage ≤ 3.6V if unpowered
SMBus Timing (CAP1106-1 only)						

Table 2.2 Electrical Specifications (continued)

V_{DD} = 3V to 3.6V, T_A = 0°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Input Capacitance	C_{IN}		5		pF	
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus Free Time Stop to Start	t_{BUF}	1.3			us	
Start Setup Time	$t_{SU:STA}$	0.6			us	
Start Hold Time	$t_{HD:STA}$	0.6			us	
Stop Setup Time	$t_{SU:STO}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0			us	When transmitting to the master
Data Hold Time	$t_{HD:DAT}$	0.3			us	When receiving from the master
Data Setup Time	$t_{SU:DAT}$	0.6			us	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock / Data Fall Time	t_{FALL}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Clock / Data Rise Time	t_{RISE}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Capacitive Load	C_{LOAD}			400	pF	per bus line
BC-Link Timing (CAP1106-2 only)						
Clock Period	t_{CLK}	250			ns	
Data Hold Time	$t_{HD:DAT}$	0			ns	
Data Setup Time	$t_{SU:DAT}$	30			ns	Data must be valid before clock
Clock Duty Cycle	Duty	40	50	60	%	
SPI Timing (CAP1105 only)						
Clock Period	t_P	250			ns	
Clock Low Period	t_{LOW}	0.4 x t_P		0.6 x t_P	ns	
Clock High Period	t_{HIGH}	0.4 x t_P		0.6 x t_P	ns	
Clock Rise / Fall time	t_{RISE} / t_{FALL}			0.1 x t_P	ns	
Data Output Delay	$t_{D:CLK}$			10	ns	
Data Setup Time	$t_{SU:DAT}$	20			ns	
Data Hold Time	$t_{HD:DAT}$	20			ns	

Table 2.2 Electrical Specifications (continued)

V_{DD} = 3V to 3.6V, T_A = 0°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
SPI_CS# to SPI_CLK setup time	$t_{SU:CS}$	0			ns	
Wake Time	t_{WAKE}	10		20	us	SPI_CS# asserted to CLK assert

Note 2.4 The ALERT pin will not glitch high or low at power up if connected to VDD or another voltage.

Note 2.5 The SMCLK and SMDATA pins will not glitch low at power up if connected to VDD or another voltage.

Chapter 3 Communications

3.1 Communications

The CAP1106-1 communicates using the SMBus or I^2C protocol. The CAP1106-2 communicates using the 2-wire proprietary BC-Link protocol. The CAP1105 communicates using 4-wire SPI bus. Regardless of the communications mechanism, the device functionality remains unchanged.

3.1.1 SMBus (I^2C) Communications

The CAP1106-1 supports the following protocols: Send Byte, Receive Byte, Read Byte, Write Byte, Read Block, and Write Block. In addition, the device supports I^2C formatting for block read and block write protocols.

See Section 3.2 and Section 3.3 for more information on the SMBus bus and protocols respectively.

3.1.2 SPI Communications

The CAP1105 is configured to communicate via SPI bus, using a 4-wire protocol. It does not support the 3-wire protocol.

See Section 3.5 and Section 3.6 for more information on the SPI bus and protocols respectively.

3.1.3 BC-Link Communications

The CAP1106-2 supports the read byte protocol and the write byte protocol.

See Section 3.7 for more information on the BC-Link Bus and protocols respectively.

APPLICATION NOTE: Upon power up, the CAP1106-2 will not respond to any communications for up to 15ms. After this time, full functionality is available.

3.2 System Management Bus

The CAP1106-1 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 3.1. Stretching of the SMCLK signal is supported; however, the CAP1106-1 will not stretch the clock signal.

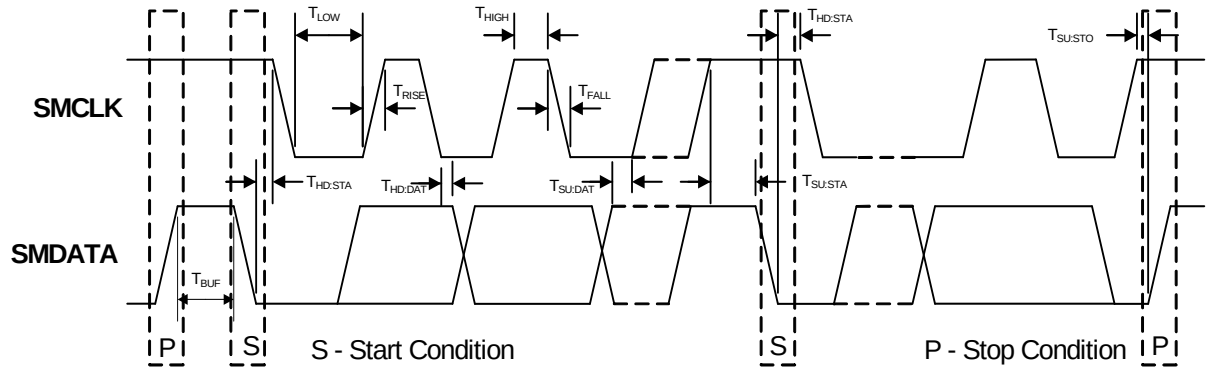


Figure 3.1 SMBus Timing Diagram

3.2.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic ‘1’ state to a logic ‘0’ state while the SMBus Clock line is in a logic ‘1’ state.

3.2.2 SMBus Address and RD / $\overline{WR}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by the RD / $\overline{WR}$ indicator bit. If this RD / $\overline{WR}$ bit is a logic ‘0’, then the SMBus Host is writing data to the client device. If this RD / $\overline{WR}$ bit is a logic ‘1’, then the SMBus Host is reading data from the client device.

The CAP1106-1 responds to SMBus address 0101_000(r/w).

3.2.3 SMBus Data Bytes

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

3.2.4 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives. This is done by the client device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted. This applies to both the Write Byte and Block Write protocols.

The Host will NACK (not acknowledge) the last data byte to be received from the client by holding the SMBus data line high after the 8th data bit has been sent. For the Block Read protocol, the Host will ACK each data byte that it receives except the last data byte.

3.2.5 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic ‘0’ state to a logic ‘1’ state while the SMBus clock line is in a logic ‘1’ state. When the CAP1106-1 detects an SMBus Stop bit and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

3.2.6 SMBus Timeout

The CAP1106-1 includes an SMBus timeout feature. Following a 30ms period of inactivity on the SMBus where the SMCLK pin is held low, the device will timeout and reset the SMBus interface.

The timeout function defaults to disabled. It can be enabled by setting the TIMEOUT bit in the Configuration register (see Section 5.6, "Configuration Registers").

3.2.7 SMBus and I²C Compatibility

The major differences between SMBus and I²C devices are highlighted here. For more information, refer to the SMBus 2.0 and I²C specifications. For information on using the CAP1106-1 in an I²C system, refer to SMSC AN 14.0 SMSC Dedicated Slave Devices in I²C Systems.

1. CAP1106-1 supports I²C fast mode at 400kHz. This covers the SMBus max time of 100kHz.
2. Minimum frequency for SMBus communications is 10kHz.
3. The SMBus client protocol will reset if the clock is held at a logic '0' for longer than 30ms. This timeout functionality is disabled by default in the CAP1106-1 and can be enabled by writing to the TIMEOUT bit. I²C does not have a timeout.
4. The SMBus client protocol will reset if both the clock and data lines are held at a logic '1' for longer than 200µs (idle condition). This function is disabled by default in the CAP1106-1 and can be enabled by writing to the TIMEOUT bit. I²C does not have an idle condition.
5. I²C devices do not support the Alert Response Address functionality (which is optional for SMBus).
6. I²C devices support block read and write differently. I²C protocol allows for unlimited number of bytes to be sent in either direction. The SMBus protocol requires that an additional data byte indicating number of bytes to read / write is transmitted. The CAP1106-1 supports I²C formatting only.

3.3 SMBus Protocols

The CAP1106-1 is SMBus 2.0 compatible and supports Write Byte, Read Byte, Send Byte, and Receive Byte as valid protocols as shown below.

All of the below protocols use the convention in Table 3.1.

Table 3.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
Data sent	Data sent

3.3.1 SMBus Write Byte

The Write Byte is used to write one byte of data to a specific register as shown in Table 3.2.

Table 3.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1 ->0	0101_000	0	0	XXh	0	XXh	0	0 -> 1

3.3.2 SMBus Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 3.3.

Table 3.3 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	CLIENT ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1->0	0101_000	0	0	XXh	0	1 ->0	0101_000	1	0	XXh	1	0 -> 1

3.3.3 SMBus Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 3.4.

APPLICATION NOTE: The Send Byte protocol is not functional in Deep Sleep (i.e., DSLEEP bit is set).

Table 3.4 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1 -> 0	0101_000	0	0	XXh	0	0 -> 1

3.3.4 SMBus Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g., set via Send Byte). This is used for consecutive reads of the same register as shown in Table 3.5.

APPLICATION NOTE: The Receive Byte protocol is not functional in Deep Sleep (i.e., DSLEEP bit is set).

Table 3.5 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	0101_000	1	0	XXh	1	0 -> 1

3.4 I^2C Protocols

The CAP1106-1 supports I^2C Block Write and Block Read.

The protocols listed below use the convention in Table 3.1.

3.4.1 Block Write

The Block Write is used to write multiple data bytes to a group of contiguous registers as shown in Table 3.6.

APPLICATION NOTE: When using the Block Write protocol, the internal address pointer will be automatically incremented after every data byte is received. It will wrap from FFh to 00h.

Table 3.6 Block Write Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK
1 ->0	0101_000	0	0	XXh	0	XXh	0
REGISTER DATA	**ACK**	**REGISTER DATA**	**ACK**	**. . .**	**REGISTER DATA**	**ACK**	**STOP**
XXh	0	XXh	0	. . .	XXh	0	0 -> 1

3.4.2 Block Read

The Block Read is used to read multiple data bytes from a group of contiguous registers as shown in Table 3.7.

APPLICATION NOTE: When using the Block Read protocol, the internal address pointer will be automatically incremented after every data byte is received. It will wrap from FFh to 00h.

Table 3.7 Block Read Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA
1->0	0101_000	0	0	XXh	0	1 ->0	0101_000	1	0	XXh
ACK	**REGISTER DATA**	**ACK**	**REGISTER DATA**	**ACK**	**REGISTER DATA**	**ACK**	**. . .**	**REGISTER DATA**	**NACK**	**STOP**
0	XXh	0	XXh	0	XXh	0	. . .	XXh	1	0 -> 1

3.5 SPI Interface (CAP1105 only)

The SMBus has a predefined packet structure, the SPI does not. The SPI Bus can operate in two modes of operation, normal 4-wire mode and bi-directional 3-wire mode. The CAP1105 only supports normal 4-wire mode. All SPI commands consist of 8-bit packets sent to a specific slave device (identified by the CS pin).

The SPI bus will latch data on the rising edge of the clock and the clock and data both idle high.

All commands are supported via both operating modes. The supported commands are: Reset Serial interface, set address pointer, write command and read command. Note that all other codes received during the command phase are ignored and have no effect on the operation of the device.

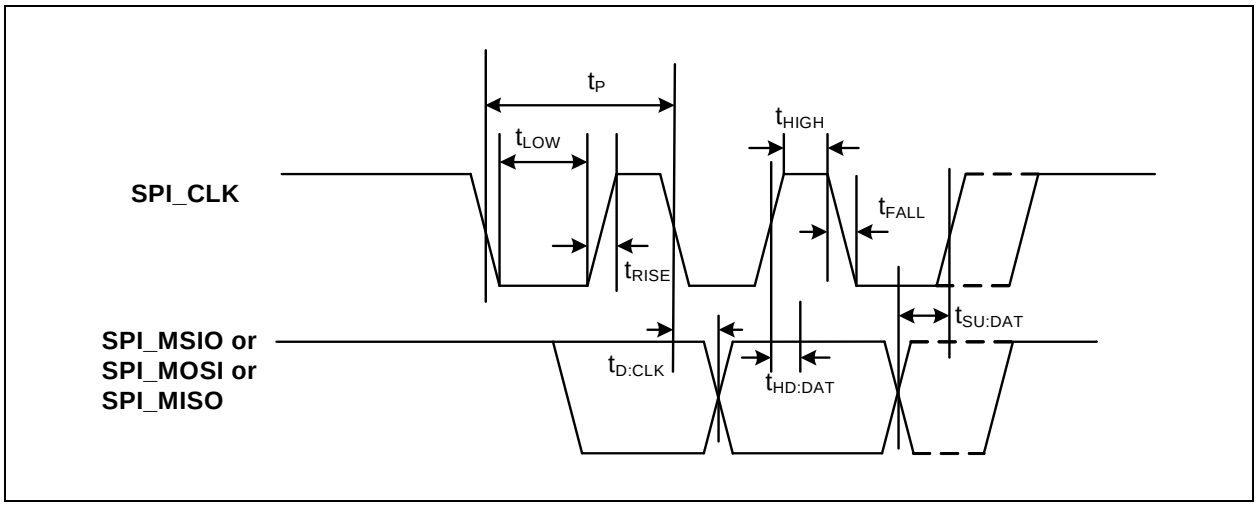


Figure 3.2 SPI Timing

3.5.1 SPI Normal Mode

In the normal mode of operation, there are dedicated input and output data lines. The host communicates by sending a command along the CAP1105 SPI_MOSI data line and reading data on the SPI_MISO data line. Both communications occur simultaneously which allows for larger throughput of data transactions.

All basic transfers consist of two 8 bit transactions from the Master device while the slave device is simultaneously sending data at the current address pointer value.

Data writes consist of two or more 8-bit transactions. The host sends a specific write command followed by the data to write the address pointer. Data reads consist of one or more 8-bit transactions. The host sends the specific read data command and continues clocking for as many data bytes as it wishes to receive.

3.5.2 SPI_CS# Pin

The SPI Bus is a single master, multiple slave serial bus. Each slave has a dedicated CS pin (chip select) that the master asserts low to identify that the slave is being addressed. There are no formal addressing options.

3.5.3 Address Pointer

All data writes and reads are accessed from the current address pointer. In both Bi-directional mode and Full Duplex mode, the Address pointer is automatically incremented following every read command or every write command.

The address pointer will return to 00h after reaching FFh.

3.5.4 SPI Timeout

The CAP1105 does not detect any timeout conditions on the SPI bus.

3.6 Normal SPI Protocols

When operating in normal mode, the SPI bus internal address pointer is incremented depending upon which command has been transmitted. Multiple commands may be transmitted sequentually so long as the SPI_CS# pin is asserted low. Figure 3.3 shows an example of this operation.

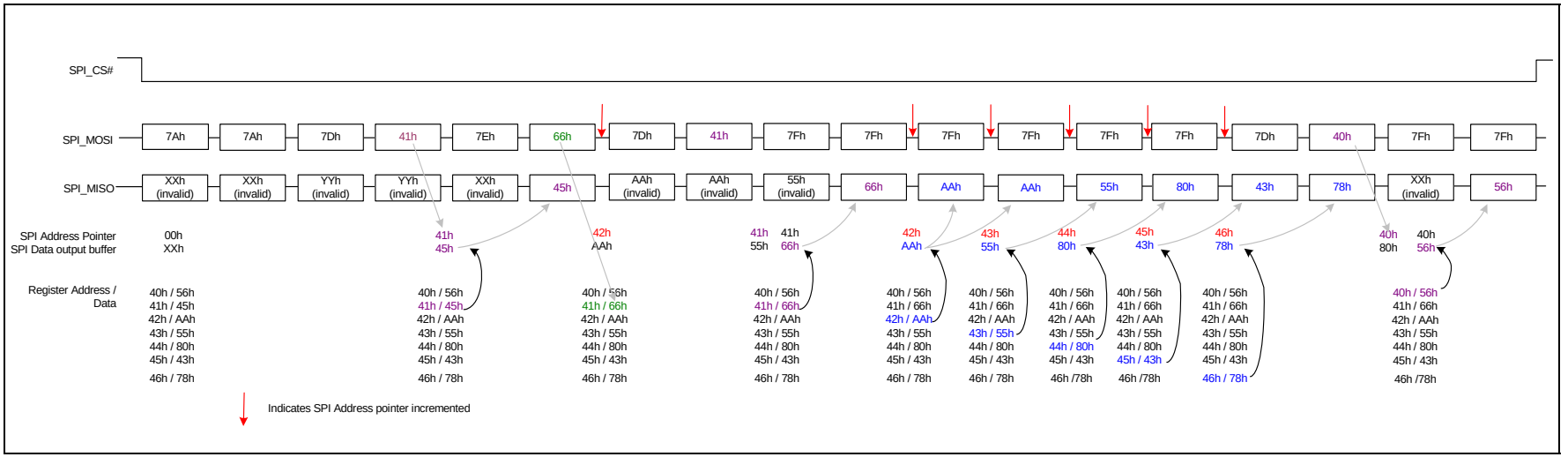


Figure 3.3 Example SPI Bus Communication - Normal Mode

3.6.1 Reset Interface

Resets the Serial interface whenever two successive 7Ah codes are received. Regardless of the current phase of the transaction - command or data, the receipt of the successive reset commands resets the Serial communication interface only. All other functions are not affected by the reset operation.

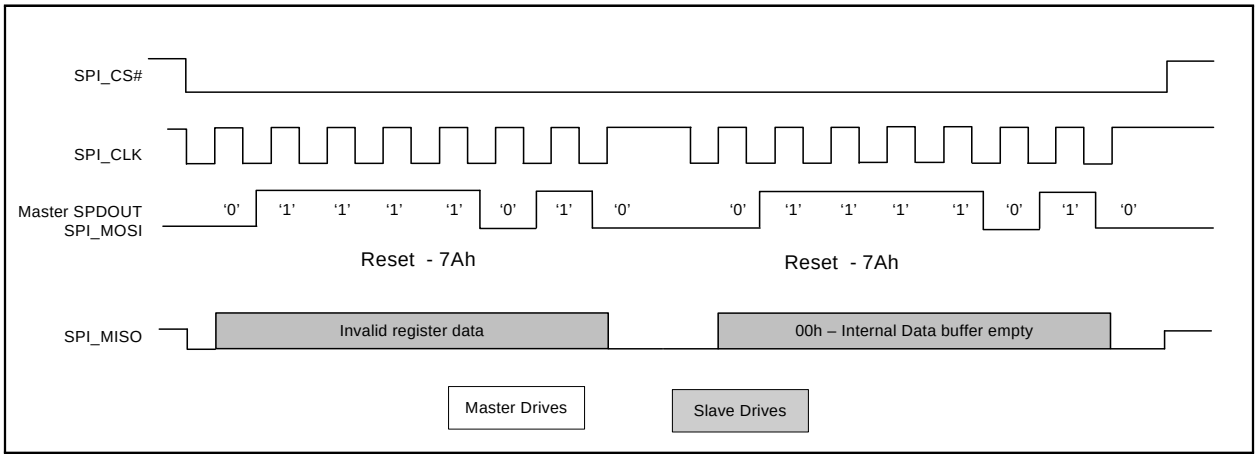


Figure 3.4 SPI Reset Interface Command - Normal Mode

3.6.2 Set Address Pointer

The Set Address Pointer command sets the Address pointer for subsequent reads and writes of data. The pointer is set on the rising edge of the final data bit. At the same time, the data that is to be read is fetched and loaded into the internal output buffer but is not transmitted.

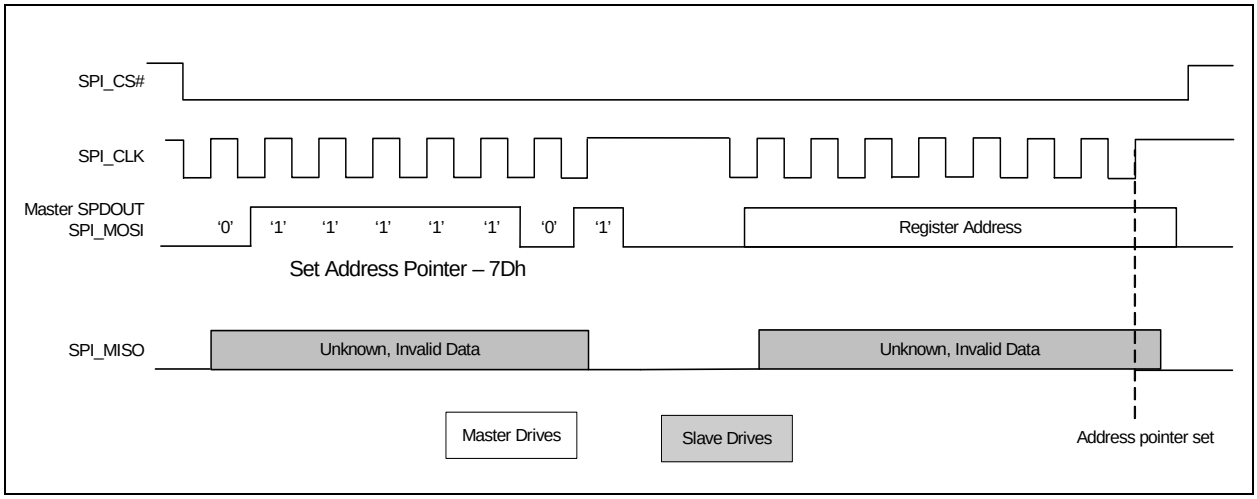


Figure 3.5 SPI Set Address Pointer Command - Normal Mode

3.6.3 Write Data

The Write Data protocol updates the contents of the register referenced by the address pointer. As the command is processed, the data to be read is fetched and loaded into the internal output buffer but not transmitted. Then, the register is updated with the data to be written. Finally, the address pointer is incremented.

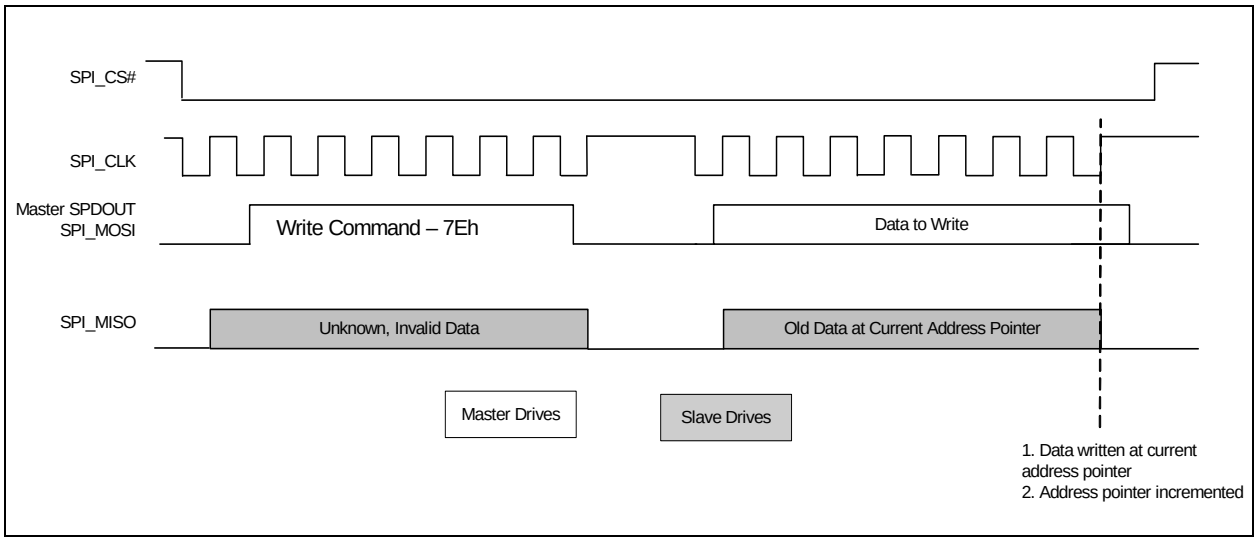
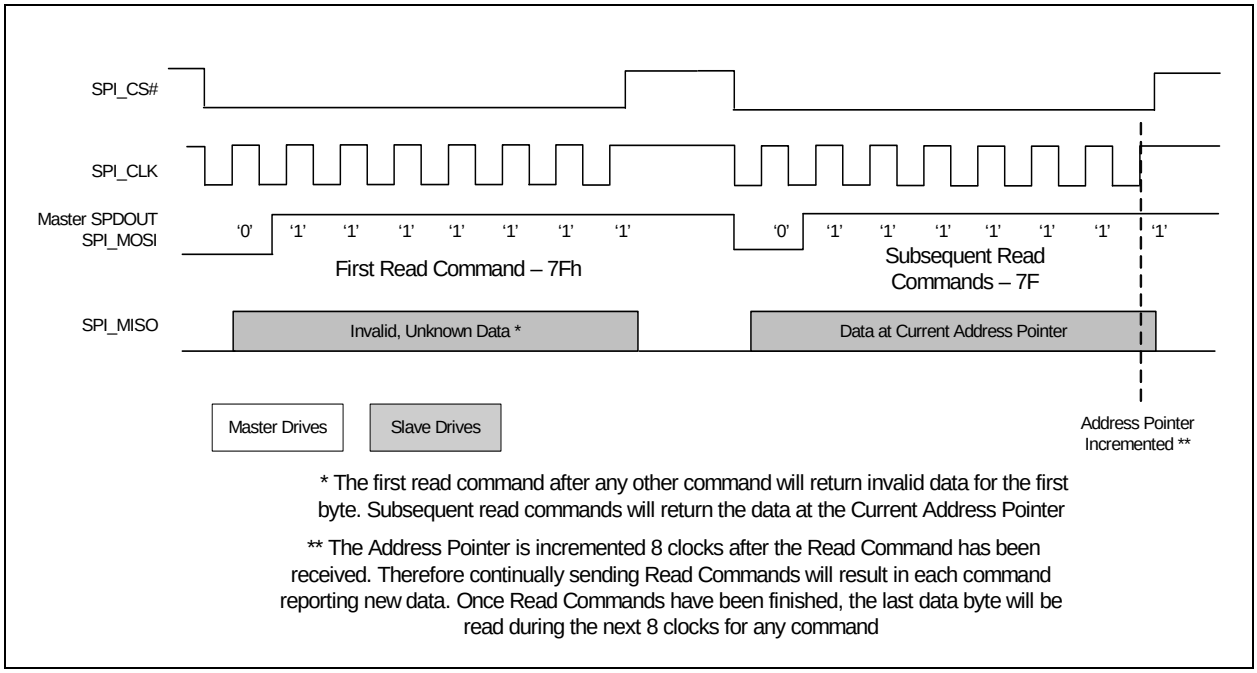


Figure 3.6 SPI Write Command - Normal Mode

3.6.4 Read Data

The Read Data protocol is used to read data from the device. During the normal mode of operation, while the device is receiving data, the CAP1105 is simultaneously transmitting data to the host. For the Set Address commands and the Write Data commands, this data may be invalid and it is recommended that the Read Data command is used.



* The first read command after any other command will return invalid data for the first byte. Subsequent read commands will return the data at the Current Address Pointer

** The Address Pointer is incremented 8 clocks after the Read Command has been received. Therefore continually sending Read Commands will result in each command reporting new data. Once Read Commands have been finished, the last data byte will be read during the next 8 clocks for any command

Figure 3.7 SPI Read Command - Normal Mode

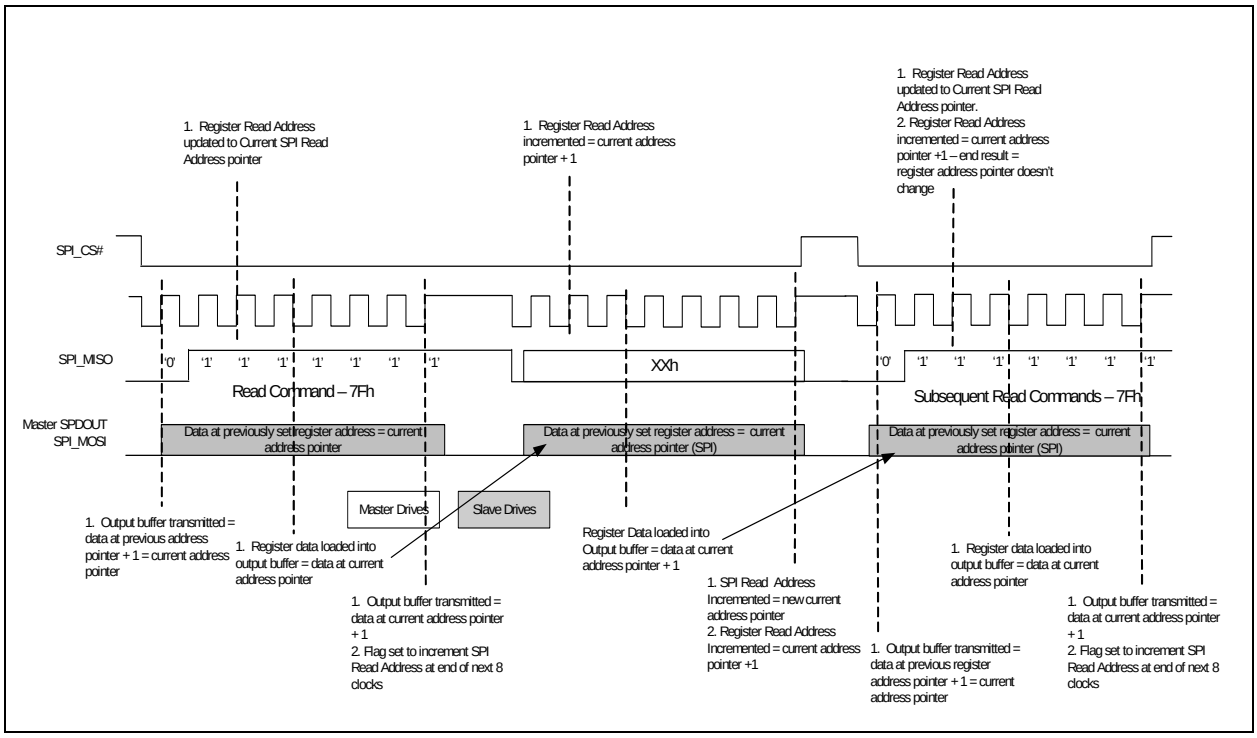


Figure 3.8 SPI Read Command - Normal Mode - Full

3.7 BC-Link Interface (CAP1106-2 only)

The BC-Link is a proprietary bus developed to allow communication between a host controller device to a companion device. This device uses this serial bus to read and write registers and for interrupt processing. The interface uses a data port concept, where the base interface has an address register, data register and a control register, defined in the SMSC's 8051's SFR space.

Refer to documentation for the BC-Link compatible host controller for details on how to access the CAP1106-2 via the BC-Link Interface.

Chapter 4 General Description

The CAP1106 / 1105 are multiple channel Capacitive Touch sensors. The CAP1106 contains six (6) individual capacitive touch sensor inputs while the CAP1105 contains five (5) sensor inputs. Both devices offer programmable sensitivity for use in touch sensor applications. Each sensor input automatically recalibrates to compensate for gradual environmental changes.

The CAP1105 / CAP1106 offers multiple power states. It operates at the lowest quiescent current during its Deep Sleep state. In the low power Standby state, it can monitor one or more channels and respond to communications normally.

The device communicates with a host controller using the SPI bus (CAP1105 only), SMSC BC-Link bus (CAP1106-2 only), or via SMBus / I^2C (CAP1106-1 only). The host controller may poll the device for updated information at any time or it may configure the device to flag an interrupt whenever a touch is detected on any sensor pad.

A typical system diagram for the CAP1106 is shown in Figure 4.1 and a system diagram for the CAP1105 is shown in Figure 4.2.

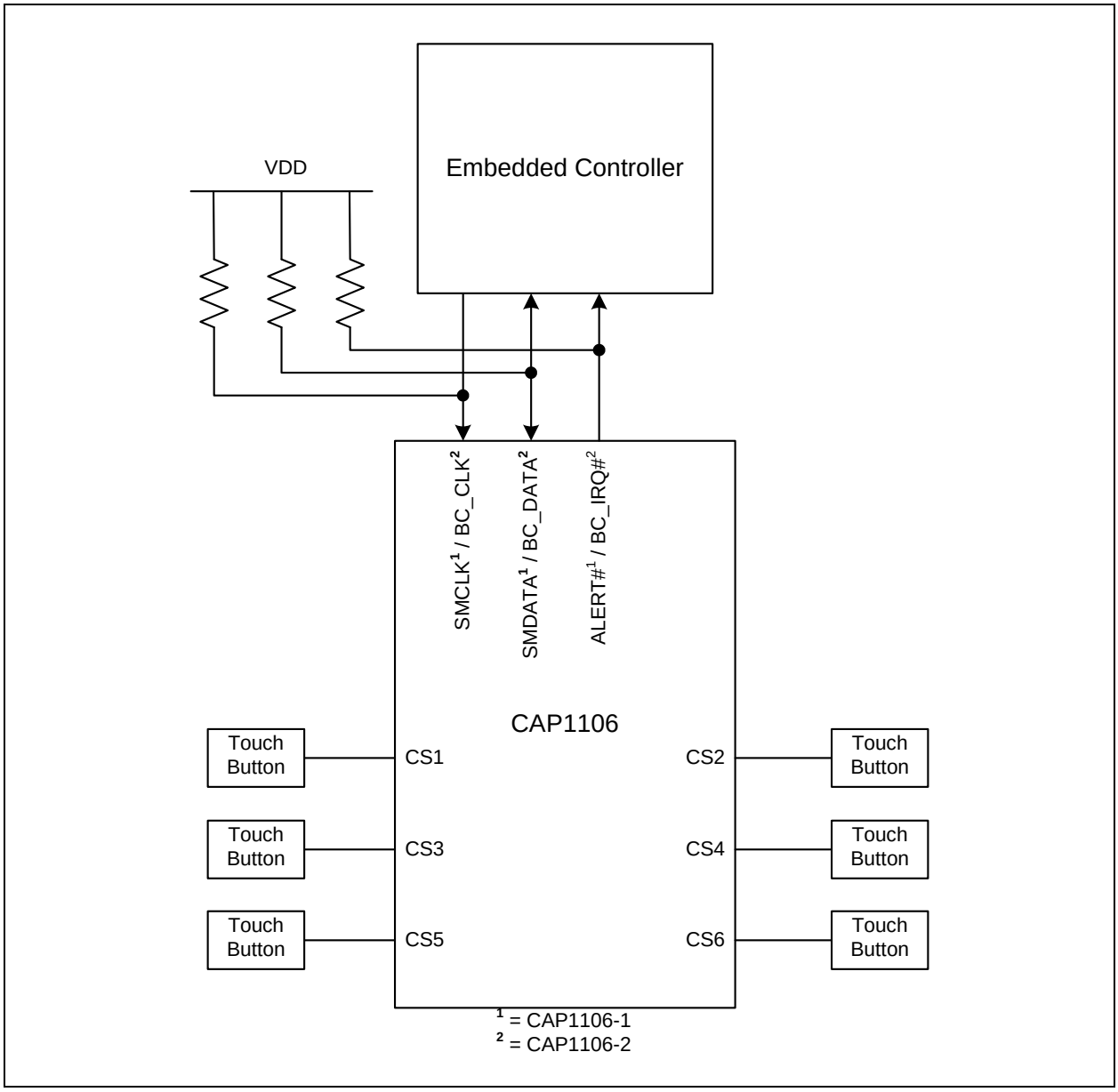


Figure 4.1 System Diagram for CAP1106

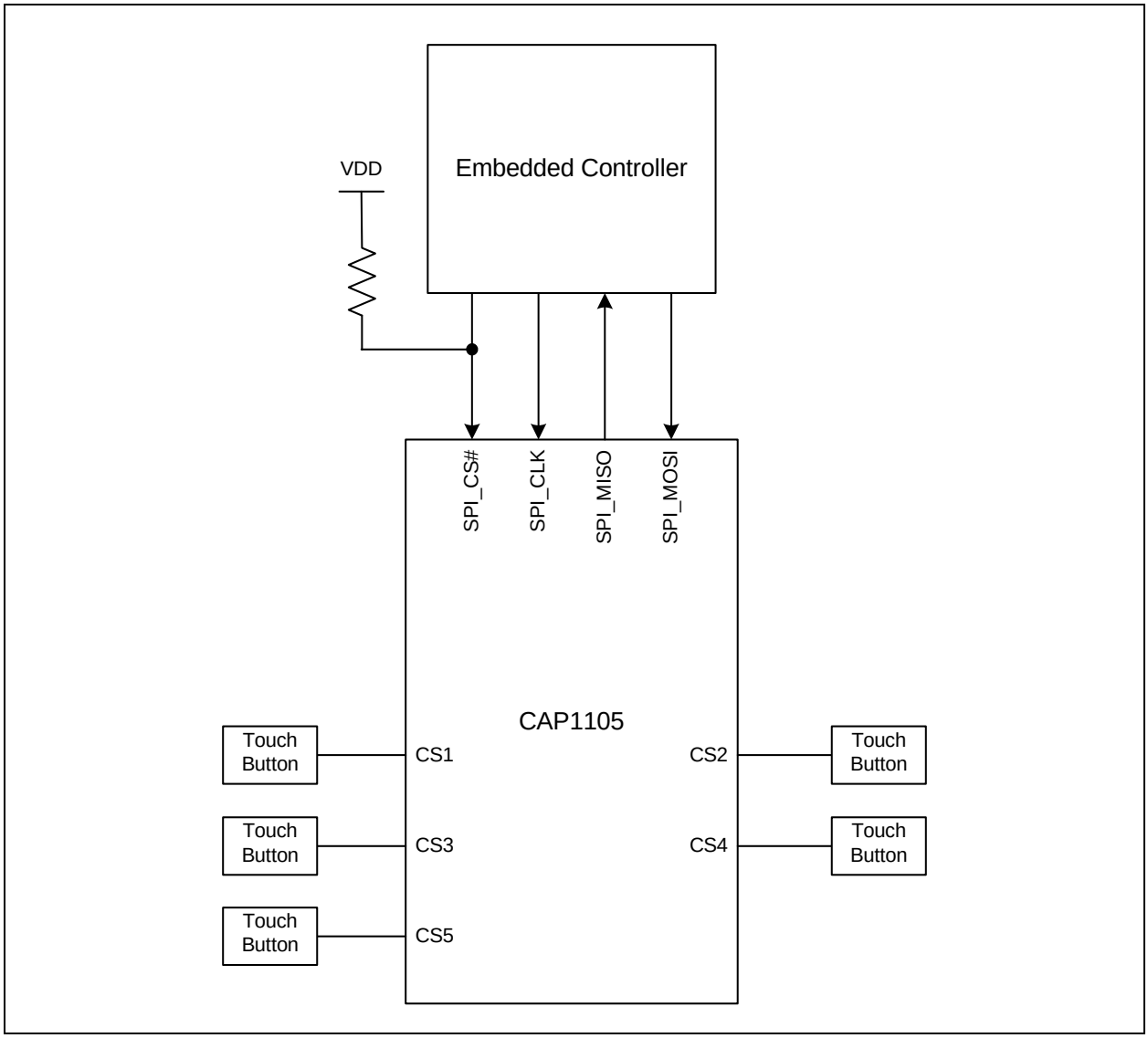


Figure 4.2 System Diagram for CAP1105

4.1 Power States

The CAP1105 / CAP1106 has three operating states depending on the status of the STBY and DSLEEP bits. When the device transitions between power states, previously detected touches (for inactive channels) are cleared and the status bits reset.

1. Fully Active - The device is fully active. It is monitoring all active capacitive sensor inputs.
2. Standby - The device is in a lower power state. It will measure a programmable number of channels using the Standby Configuration controls (see Section 5.20 through Section 5.22). Interrupts will still be generated based on the active channels. The device will still respond to communications normally and can be returned to the Fully Active state of operation by clearing the STBY bit.
3. Deep Sleep - The device is in its lowest power state. It is not monitoring any capacitive sensor inputs. While in Deep Sleep, the device can be awakened by SMBus or SPI communications targeting the device. This will not cause the DSLEEP to be cleared so the device will return to Deep Sleep once all communications have stopped.

APPLICATION NOTE: The CAP1106-2, which communicates using the BC-Link protocol, does not support Deep Sleep.

4.2 Capacitive Touch Sensing

The CAP1105 / CAP1106 contains six (6) (CAP1106) or five (5) (CAP1105) independent capacitive touch sensor inputs. Each sensor input has dynamic range to detect a change of capacitance due to a touch. Additionally, each sensor input can be configured to be automatically and routinely re-calibrated.

4.2.1 Sensing Cycle

Each capacitive touch sensor input has controls to be activated and included in the sensing cycle. When the device is active, it automatically initiates a sensing cycle and repeats the cycle every time it finishes. The cycle polls through each active sensor input starting with CS1 and extending through CS6. As each capacitive touch sensor input is polled, its measurement is compared against a baseline “Not Touched” measurement. If the delta measurement is large enough, a touch is detected and an interrupt is generated.

The sensing cycle time is programmable (see Section 5.10, "Averaging and Sampling Configuration Register").

4.2.2 Recalibrating Sensor Inputs

There are various options for recalibrating the capacitive touch sensor inputs. Recalibration re-sets the Base Count Registers (Section 5.24, "Sensor Input Base Count Registers") which contain the “not touched” values used for touch detection comparisons.

APPLICATION NOTE: The device will recalibrate all sensor inputs that were disabled when it transitions from Standby. Likewise, the device will recalibrate all sensor inputs when waking out of Deep Sleep.

4.2.2.1 Manual Recalibration

The Calibration Activate Registers (Section 5.11, "Calibration Activate Register") force recalibration of selected sensor inputs. When a bit is set, the corresponding capacitive touch sensor input will be recalibrated (both analog and digital). The bit is automatically cleared once the recalibration routine has finished.

Note: During this recalibration routine, the sensor inputs will not detect a press for up to 200ms and the Sensor Base Count Register values will be invalid. In addition, any press on the corresponding sensor pads will invalidate the recalibration.

4.2.2.2 Automatic Recalibration

Each sensor input is regularly recalibrated at a programmable rate (see Section 5.17, "Recalibration Configuration Register"). By default, the recalibration routine stores the average 64 previous measurements and periodically updates the base “not touched” setting for the capacitive touch sensor input.

Note: Automatic recalibration only works when the delta count is below the active sensor input threshold. It is disabled when a touch is detected.

4.2.2.3 Negative Delta Count Recalibration

It is possible that the device loses sensitivity to a touch. This may happen as a result of a noisy environment, an accidental recalibration during a touch, or other environmental changes. When this occurs, the base untouched sensor input may generate negative delta count values. The

NEG_DELTA_CNT bits (see Section 5.17, "Recalibration Configuration Register") can be set to force a recalibration after a specified number of consecutive negative delta readings.

Note: During this recalibration, the device will not respond to touches.

4.2.2.4 Delayed Recalibration

It is possible that a “stuck button” occurs when something is placed on a button which causes a touch to be detected for a long period. By setting the MAX_DUR_EN bit (see Section 5.6, "Configuration Registers"), a recalibration can be forced when a touch is held on a button for longer than the duration specified in the MAX_DUR bits (see Section 5.8, "Sensor Input Configuration Register").

Note: Delayed recalibration only works when the delta count is above the active sensor input threshold. If enabled, it is invoked when a sensor pad touch is held longer than the MAX_DUR bit setting.

4.2.3 Proximity Detection

Each sensor input can be configured to detect changes in capacitance due to proximity of a touch. This circuitry detects the change of capacitance that is generated as an object approaches, but does not physically touch, the enabled sensor pad(s). When a sensor input is selected to perform proximity detection, it will be sampled from 1x to 128x per sampling cycle. The larger the number of samples that are taken, the greater the range of proximity detection is available at the cost of an increased overall sampling time.

4.2.4 Multiple Touch Pattern Detection

The multiple touch pattern (MTP) detection circuitry can be used to detect lid closure or other similar events. An event can be flagged based on either a minimum number of sensor inputs or on specific sensor inputs simultaneously exceeding an MTP threshold or having their Noise Flag Status Register bits set. An interrupt can also be generated. During an MTP event, all touches are blocked (see Section 5.15, "Multiple Touch Pattern Configuration Register").

4.2.5 Low Frequency Noise Detection

Each sensor input has an EMI noise detector that will sense if low frequency noise is injected onto the input with sufficient power to corrupt the readings. If this occurs, the device will reject the corrupted sample and set the corresponding bit in the Noise Status register to a logic ‘1’.

4.2.6 RF Noise Detection

Each sensor input contains an integrated RF noise detector. This block will detect injected RF noise on the CS pin. The detector threshold is dependent upon the noise frequency. If RF noise is detected on a CS line, that sample is removed and not compared against the threshold.

4.3 ALERT# Pin

The ALERT# pin is an active low (or active high when configured) output that is driven when an interrupt event is detected.

Whenever an interrupt is generated, the INT bit (see Section 5.1, "Main Control Register") is set. The ALERT# pin is cleared when the INT bit is cleared by the user. Additionally, when the INT bit is cleared by the user, status bits are only cleared if no touch is detected.

4.3.1 Sensor Interrupt Behavior

The sensor interrupts are generated in one of two ways:

1. An interrupt is generated when a touch is detected and, as a user selectable option, when a release is detected (by default - see Section 5.6). See Figure 4.4.
2. If the repeat rate is enabled then, so long as the touch is held, another interrupt will be generated based on the programmed repeat rate (see Figure 4.3).

When the repeat rate is enabled, the device uses an additional control called MPRESS that determines whether a touch is flagged as a simple “touch” or a “press and hold”. The MPRESS[3:0] bits set a minimum press timer. When the button is touched, the timer begins. If the sensor pad is released before the minimum press timer expires, it is flagged as a touch and an interrupt is generated upon release. If the sensor input detects a touch for longer than this timer value, it is flagged as a “press and hold” event. So long as the touch is held, interrupts will be generated at the programmed repeat rate and upon release (if enabled).

APPLICATION NOTE: Figure 4.3 and Figure 4.4 show default operation which is to generate an interrupt upon sensor pad release and an active-low ALERT# pin.

APPLICATION NOTE: The host may need to poll the device twice to determine that a release has been detected.

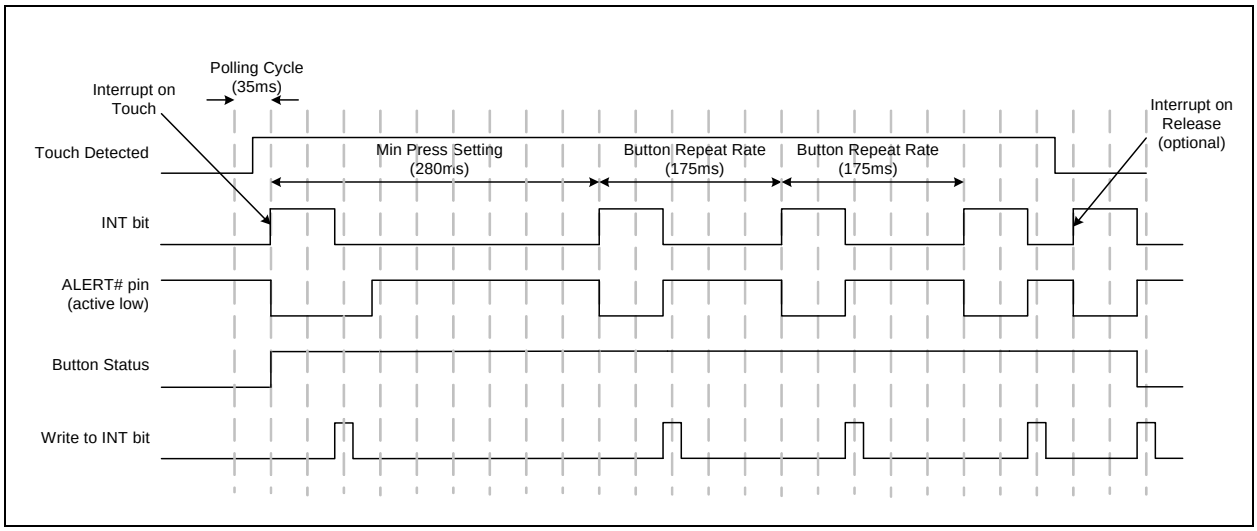


Figure 4.3 Sensor Interrupt Behavior - Repeat Rate Enabled

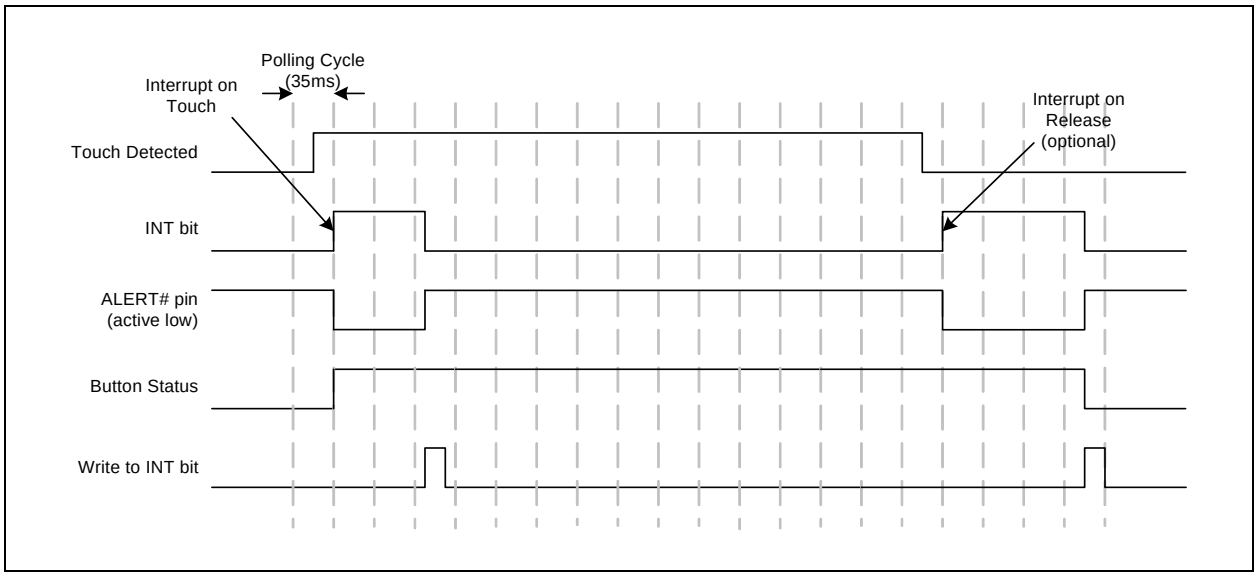


Figure 4.4 Sensor Interrupt Behavior - No Repeat Rate Enabled

Chapter 5 Register Description

The registers shown in Table 5.1 are accessible through the communications protocol. An entry of '-' indicates that the bit is not used and will always read '0'.

Table 5.1 Register Set in Hexadecimal Order

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
00h	R/W	Main Control	Controls general power states and power dissipation	00h	Page 36
02h	R	General Status	Stores general status bits	00h	Page 37
03h	R	Sensor Input Status	Returns the state of the sampled capacitive touch sensor inputs	00h	Page 37
0Ah	R	Noise Flag Status	Stores the noise flags for sensor inputs	00h	Page 38
10h	R	Sensor Input 1 Delta Count	Stores the delta count for CS1	00h	Page 38
11h	R	Sensor Input 2 Delta Count	Stores the delta count for CS2	00h	Page 38
12h	R	Sensor Input 3 Delta Count	Stores the delta count for CS3	00h	Page 38
13h	R	Sensor Input 4 Delta Count	Stores the delta count for CS4	00h	Page 38
14h	R	Sensor Input 5 Delta Count	Stores the delta count for CS5	00h	Page 38
15h	R	Sensor Input 6 Delta Count	Stores the delta count for CS6	00h	Page 38
1Fh	R/W	Sensitivity Control	Controls the sensitivity of the threshold and delta counts and data scaling of the base counts	2Fh	Page 39
20h	R/W	Configuration	Controls general functionality	20h	Page 40
21h	R/W	Sensor Input Enable	Controls whether the capacitive touch sensor inputs are sampled	3Fh	Page 42
22h	R/W	Sensor Input Configuration	Controls max duration and auto-repeat delay for sensor inputs operating in the full power state	A4h	Page 42
23h	R/W	Sensor Input Configuration 2	Controls the MPRESS controls for all sensor inputs	07h	Page 44
24h	R/W	Averaging and Sampling Config	Controls averaging and sampling window	39h	Page 45
26h	R/W	Calibration Activate	Forces re-calibration for capacitive touch sensor inputs	00h	Page 47

Table 5.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
27h	R/W	Interrupt Enable	Enables Interrupts associated with capacitive touch sensor inputs	3Fh	Page 47
28h	R/W	Repeat Rate Enable	Enables repeat rate for all sensor inputs	3Fh	Page 48
2Ah	R/W	Multiple Touch Configuration	Determines the number of simultaneous touches to flag a multiple touch condition	80h	Page 48
2Bh	R/W	Multiple Touch Pattern Configuration	Determines the multiple touch pattern (MTP) configuration	00h	Page 49
2Dh	R/W	Multiple Touch Pattern	Determines the pattern or number of sensor inputs used by the MTP circuitry	3Fh	Page 50
2Fh	R/W	Recalibration Configuration	Determines re-calibration timing and sampling window	8Ah	Page 51
30h	R/W	Sensor Input 1 Threshold	Stores the delta count threshold to determine a touch for Capacitive Touch Sensor Input 1	40h	Page 53
31h	R/W	Sensor Input 2 Threshold	Stores the delta count threshold to determine a touch for Capacitive Touch Sensor Input 2	40h	Page 53
32h	R/W	Sensor Input 3 Threshold	Stores the delta count threshold to determine a touch for Capacitive Touch Sensor Input 3	40h	Page 53
33h	R/W	Sensor Input 4 Threshold	Stores the delta count threshold to determine a touch for Capacitive Touch Sensor Input 4	40h	Page 53
34h	R/W	Sensor Input 5 Threshold	Stores the delta count threshold to determine a touch for Capacitive Touch Sensor Input 5	40h	Page 53
35h	R/W	Sensor Input 6 Threshold	Stores the delta count threshold to determine a touch for Capacitive Touch Sensor Input 6	40h	Page 53
38h	R/W	Sensor Input Noise Threshold	Stores controls for selecting the noise threshold for all sensor inputs	01h	Page 53
Standby Configuration Registers					
40h	R/W	Standby Channel	Controls which sensor inputs are enabled while in standby	00h	Page 54
41h	R/W	Standby Configuration	Controls averaging and cycle time while in standby	39h	Page 54
42h	R/W	Standby Sensitivity	Controls sensitivity settings used while in standby	02h	Page 56
43h	R/W	Standby Threshold	Stores the touch detection threshold for active sensor inputs in standby	40h	Page 57

Table 5.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
44h	R/W	Configuration 2	Stores additional configuration controls for the device	40h	Page 40
Base Count Registers					
50h	R	Sensor Input 1 Base Count	Stores the reference count value for sensor input 1	C8h	Page 57
51h	R	Sensor Input 2 Base Count	Stores the reference count value for sensor input 2	C8h	Page 57
52h	R	Sensor Input 3 Base Count	Stores the reference count value for sensor input 3	C8h	Page 57
53h	R	Sensor Input 4 Base Count	Stores the reference count value for sensor input 4	C8h	Page 57
54h	R	Sensor Input 5 Base Count	Stores the reference count value for sensor input 5	C8h	Page 57
55h	R	Sensor Input 6 Base Count	Stores the reference count value for sensor input 6	C8h	Page 57
B1h	R	Sensor Input 1 Calibration	Stores the upper 8-bit calibration value for sensor input 1	00h	Page 58
B2h	R	Sensor Input 2 Calibration	Stores the upper 8-bit calibration value for sensor input 2	00h	Page 58
B3h	R	Sensor Input 3 Calibration	Stores the upper 8-bit calibration value for sensor input 3	00h	Page 58
B4h	R	Sensor Input 4 Calibration	Stores the upper 8-bit calibration value for sensor input 4	00h	Page 58
B5h	R	Sensor Input 5 Calibration	Stores the upper 8-bit calibration value for sensor input 5	00h	Page 58
B6h	R	Sensor Input 6 Calibration	Stores the upper 8-bit calibration value for sensor input 6	00h	Page 58
B9h	R	Sensor Input Calibration LSB 1	Stores the 2 LSBs of the calibration value for sensor inputs 1 - 4	00h	Page 58
BAh	R	Sensor Input Calibration LSB 2	Stores the 2 LSBs of the calibration value for sensor inputs 5- 6	00h	Page 58
FDh	R	Product ID CAP1106	Stores a fixed value that identifies each product	55h	Page 59
		Product ID CAP1105	Stores a fixed value that identifies each product	56h	
FEh	R	Manufacturer ID	Stores a fixed value that identifies SMSC	5Dh	Page 59
FFh	R	Revision	Stores a fixed value that represents the revision number	83h	Page 59

During Power-On-Reset (POR), the default values are stored in the registers. A POR is initiated when power is first applied to the part and the voltage on the VDD supply surpasses the POR level as

specified in the electrical characteristics. Any reads to undefined registers will return 00h. Writes to undefined registers will not have an effect.

When a bit is “set”, this means that the user writes a logic ‘1’ to it. When a bit is “cleared”, this means that the user writes a logic ‘0’ to it.

5.1 Main Control Register

Table 5.2 Main Control Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
00h	R/W	Main Control	GAIN[1:0]		STBY	DSLEEP	-	-	-	INT	00h

The Main Control register controls the primary power state of the device.

Bits 7 - 6 - GAIN[1:0] - Controls the gain used by the capacitive touch sensing circuitry. As the gain is increased, the effective sensitivity is likewise increased as a smaller delta capacitance is required to generate the same delta count values. The sensitivity settings may need to be adjusted along with the gain settings such that data overflow does not occur.

APPLICATION NOTE: The gain settings apply to both Standby and Active states.

Table 5.3 GAIN Bit Decode

GAIN[1:0]		CAPACITIVE TOUCH SENSOR GAIN
1	0	
0	0	1
0	1	2
1	0	4
1	1	8

Bit 5 - STBY - Enables Standby.

- ‘0’ (default) - Sensor input scanning is active.
- ‘1’ - Capacitive touch sensor input scanning is limited to the sensor inputs set in the Standby Channel register (see Section 5.20). The status registers will not be cleared until read. Sensor inputs that are no longer sampled will flag a release and then remain in a non-touched state.

Bit 4 - DSLEEP - Enables Deep Sleep by deactivating all functions. For the CAP1106-2, which uses the BC-Link protocol, this bit is ignored.

- ‘0’ (default) - Sensor input scanning is active.
- ‘1’ - All sensor input scanning is disabled.. The status registers are automatically cleared and the INT bit is cleared.

Bit 0 - INT - Indicates that there is an interrupt. When this bit is set, it asserts the ALERT# pin. If a channel detects a touch and its associated interrupt enable bit is not set to a logic ‘1’, no action is taken.

This bit is cleared by writing a logic ‘0’ to it. When this bit is cleared, the ALERT# pin will be deasserted and all status registers will be cleared if the condition has been removed.

- ‘0’ - No interrupt pending.
- ‘1’ - A touch has been detected on one or more channels and the interrupt has been asserted.

5.2 Status Registers

Table 5.4 Status Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
02h	R	General Status	-	-	-	-	-	MULT	MTP	TOUCH	00h
03h	R	Sensor Input Status	-	-	CS6	CS5	CS4	CS3	CS2	CS1	00h

All status bits are cleared when the device enters the Deep Sleep (DSLEEP = ‘1’ - see Section 5.1).

5.2.1 General Status - 02h

Bit 2 - MULT - Indicates that the device is blocking detected touches due to the Multiple Touch detection circuitry (see Section 5.14). This bit will not cause the INT bit to be set and hence will not cause an interrupt.

Bit 1 - MTP - Indicates that the device has detected a number of sensor inputs that exceed the MTP threshold either via the pattern recognition or via the number of sensor inputs (see Section 5.15). This bit will cause the INT bit to be set if the MTP_ALERT bit is also set. This bit will not be cleared until the condition that caused it to be set has been removed.

Bit 0 - TOUCH - Indicates that a touch was detected. This bit is set if any bit in the Sensor Input Status register is set.

5.2.2 Sensor Input Status - 03h

The Sensor Input Status Register stores status bits that indicate a touch has been detected. A value of ‘0’ in any bit indicates that no touch has been detected. A value of ‘1’ in any bit indicates that a touch has been detected.

All bits are cleared when the INT bit is cleared and if a touch on the respective capacitive touch sensor input is no longer present. If a touch is still detected, the bits will not be cleared (but this will not cause the interrupt to be asserted - see Section 5.6).

Bit 5 - CS6 - Indicates that a touch was detected on Sensor Input 6.

Bit 4 - CS5 - Indicates that a touch was detected on Sensor Input 5.

Bit 3 - CS4 - Indicates that a touch was detected on Sensor Input 4.

Bit 2 - CS3 - Indicates that a touch was detected on Sensor Input 3.

Bit 1 - CS2 - Indicates that a touch was detected on Sensor Input 2.

Bit 0 - CS1 - Indicates that a touch was detected on Sensor Input 1.

5.3 Noise Flag Status Registers

Table 5.5 Noise Flag Status Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0Ah	R	Noise Flag Status	-	-	CS6_ NOISE	CS5_ NOISE	CS4_ NOISE	CS3_ NOISE	CS2_ NOISE	CS1_ NOISE	00h

The Noise Flag Status registers store status bits that are generated from the analog block if the detected noise is above the operating region of the analog detector or the RF noise detector. These bits indicate that the most recently received data from the sensor input is invalid and should not be used for touch detection. So long as the bit is set for a particular channel, the delta count value is reset to 00h and thus no touch is detected.

These bits are not sticky and will be cleared automatically if the analog block does not report a noise error.

APPLICATION NOTE: If the MTP detection circuitry is enabled, these bits count as sensor inputs above the MTP threshold (see Section 4.2.4, "Multiple Touch Pattern Detection") even if the corresponding delta count is not. If the corresponding delta count also exceeds the MTP threshold, it is not counted twice.

APPLICATION NOTE: Regardless of the state of the Noise Status bits, if low frequency noise is detected on a sensor input, that sample will be discarded unless the DIS_ANA_NOISE bit is set. As well, if RF noise is detected on a sensor input, that sample will be discarded unless the DIS_RF_NOISE bit is set.

5.4 Sensor Input Delta Count Registers

Table 5.6 Sensor Input Delta Count Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
10h	R	Sensor Input 1 Delta Count	Sign	64	32	16	8	4	2	1	00h
11h	R	Sensor Input 2 Delta Count	Sign	64	32	16	8	4	2	1	00h
12h	R	Sensor Input 3 Delta Count	Sign	64	32	16	8	4	2	1	00h
13h	R	Sensor Input 4 Delta Count	Sign	64	32	16	8	4	2	1	00h
14h	R	Sensor Input 5 Delta Count	Sign	64	32	16	8	4	2	1	00h
15h	R	Sensor Input 6 Delta Count	Sign	64	32	16	8	4	2	1	00h

The Sensor Input Delta Count registers store the delta count that is compared against the threshold used to determine if a touch has been detected. The count value represents a change in input due to the capacitance associated with a touch on one of the sensor inputs and is referenced to a calibrated

base “Not Touched” count value. The delta is an instantaneous change and is updated once per sensor input per sensing cycle (see Section 4.2.1, "Sensing Cycle").

The value presented is a standard 2’s complement number. In addition, the value is capped at a value of 7Fh. A reading of 7Fh indicates that the sensitivity settings are too high and should be adjusted accordingly (see Section 5.5).

The value is also capped at a negative value of 80h for negative delta counts which may result upon a release.

5.5 Sensitivity Control Register

Table 5.7 Sensitivity Control Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Fh	R/W	Sensitivity Control	-	DELTA_SENSE[2:0]			BASE_SHIFT[3:0]				2Fh

The Sensitivity Control register controls the sensitivity of a touch detection.

Bits 6-4 DELTA_SENSE[2:0] - Controls the sensitivity of a touch detection. The sensitivity settings act to scale the relative delta count value higher or lower based on the system parameters. A setting of 000b is the most sensitive while a setting of 111b is the least sensitive. At the more sensitive settings, touches are detected for a smaller delta capacitance corresponding to a “lighter” touch. These settings are more sensitive to noise, however, and a noisy environment may flag more false touches with higher sensitivity levels.

APPLICATION NOTE: A value of 128x is the most sensitive setting available. At the most sensitivity settings, the MSB of the Delta Count register represents 64 out of ~25,000 which corresponds to a touch of approximately 0.25% of the base capacitance (or a ΔC of 25fF from a 10pF base capacitance). Conversely, a value of 1x is the least sensitive setting available. At these settings, the MSB of the Delta Count register corresponds to a delta count of 8192 counts out of ~25,000 which corresponds to a touch of approximately 33% of the base capacitance (or a ΔC of 3.33pF from a 10pF base capacitance).

Table 5.8 DELTA_SENSE Bit Decode

DELTA_SENSE[2:0]			SENSITIVITY MULTIPLIER
2	1	0	
0	0	0	128x (most sensitive)
0	0	1	64x
0	1	0	32x (default)
0	1	1	16x
1	0	0	8x
1	0	1	4x
1	1	0	2x
1	1	1	1x - (least sensitive)

Bits 3 - 0 - BASE_SHIFT[3:0] - Controls the scaling and data presentation of the Base Count registers. The higher the value of these bits, the larger the range and the lower the resolution of the data presented. The scale factor represents the multiplier to the bit-weighting presented in these register descriptions.

APPLICATION NOTE: The BASE_SHIFT[3:0] bits normally do not need to be updated. These settings will not affect touch detection or sensitivity. These bits are sometimes helpful in analyzing the Cap Sensing board performance and stability.

Table 5.9 BASE_SHIFT Bit Decode

BASE_SHIFT[3:0]				DATA SCALING FACTOR
3	**2**	**1**	**0**	
0	0	0	0	1x
0	0	0	1	2x
0	0	1	0	4x
0	0	1	1	8x
0	1	0	0	16x
0	1	0	1	32x
0	1	1	0	64x
0	1	1	1	128x
1	0	0	0	256x
All others				256x (default = 1111b)

5.6 Configuration Registers

Table 5.10 Configuration Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
20h	R/W	Configuration	TIMEOUT	-	DIS_ DIG_ NOISE	DIS_ ANA_ NOISE	MAX_ DUR_EN	-	-	-	A0h (rev B) 20h (rev C)
44h	R/W	Configuration 2	-	ALT_ POL	BLK_PWR_ CTRL	-	SHOW_ RF_ NOISE	DIS_ RF_ NOISE	-	INT_ REL_n	40h

The Configuration registers control general global functionality that affects the entire device.

5.6.1 Configuration - 20h

Bit 7 - TIMEOUT - Enables the timeout and idle functionality of the SMBus protocol (CAP1106-1 only).

- ‘0’ (default for Functional Revision C) - The SMBus timeout and idle functionality are disabled. The SMBus interface will not time out if the clock line is held low. Likewise, it will not reset if both the data and clock lines are held high for longer than 200us. This is used for I^2C compliance.
- ‘1’ (default for Functional Revision B) - The SMBus timeout and idle functionality are enabled. The SMBus interface will time out if the clock line is held low for longer than 30ms. Likewise, it will reset if both the data and clock lines are held high for longer than 200us.

Bit 5 - DIS_DIG_NOISE - Determines whether the digital noise threshold (see Section 5.19, "Sensor Input Noise Threshold Register") is used by the device. Setting this bit disables the feature.

- ‘0’ - The digital noise threshold is used. If a delta count value exceeds the noise threshold but does not exceed the touch threshold, the sample is discarded and not used for the automatic re-calibration routine.
- ‘1’ (default) - The noise threshold is disabled. Any delta count that is less than the touch threshold is used for the automatic re-calibration routine.

Bit 4 - DIS_ANA_NOISE - Determines whether the analog noise filter is enabled. Setting this bit disables the feature.

- ‘0’ (default) - If low frequency noise is detected by the analog block, the delta count on the corresponding channel is set to 0. Note that this does not require that Noise Status bits be set.
- ‘1’ - A touch is not blocked even if low frequency noise is detected.

Bit 3 - MAX_DUR_EN - Determines whether the maximum duration recalibration is enabled.

- ‘0’ (default) - The maximum duration recalibration functionality is disabled. A touch may be held indefinitely and no re-calibration will be performed on any sensor input.
- ‘1’ - The maximum duration recalibration functionality is enabled. If a touch is held for longer than the MAX_DUR bit settings, then the re-calibration routine will be restarted (see Section 5.8).

5.6.2 Configuration 2 - 44h

Bit 6 - ALT_POL - Determines the ALERT# pin polarity and behavior.

- ‘0’ - The ALERT# pin is active high and push-pull.
- ‘1’ (default) - The ALERT# pin is active low and open drain.

Bit 5 - BLK_PWR_CTRL - Determines whether the device will reduce power consumption while waiting between conversion time completion and the end of the polling cycle.

- ‘0’ (default) - The device will always power down as much as possible during the time between the end of the last conversion and the end of the polling cycle.
- ‘1’ - The device will not power down the Cap Sensor during the time between the end of the last conversion and the end of the polling cycle.

Bit 3 - SHOW_RF_NOISE - Determines whether the Noise Status bits will show RF Noise as the only input source.

- ‘0’ (default) - The Noise Status registers will show both RF noise and low frequency EMI noise if either is detected on a capacitive touch sensor input.
- ‘1’ - The Noise Status registers will only show RF noise if it is detected on a capacitive touch sensor input. EMI noise will still be detected and touches will be blocked normally; however, the status bits will not be updated.

Bit 2 - DIS_RF_NOISE - Determines whether the RF noise filter is enabled. Setting this bit disables the feature.

- ‘0’ (default) - If RF noise is detected by the analog block, the delta count on the corresponding channel is set to 0. Note that this does not require that Noise Status bits be set.
- ‘1’ - A touch is not blocked even if RF noise is detected.

Bit 0 - INT_REL_n - Controls the interrupt behavior when a release is detected on a button.

- '0' (default) - An interrupt is generated when a press is detected and again when a release is detected and at the repeat rate (if enabled - see Section 5.13).
- '1' - An interrupt is generated when a press is detected and at the repeat rate but not when a release is detected.

5.7 Sensor Input Enable Registers

Table 5.11 Sensor Input Enable Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
21h	R/W	Sensor Input Enable	-	-	CS6_EN	CS5_EN	CS4_EN	CS3_EN	CS2_EN	CS1_EN	3Fh

The Sensor Input Enable registers determine whether a capacitive touch sensor input is included in the sampling cycle. The length of the sampling cycle is not affected by the number of sensor inputs measured.

Bit 5 - CS6_EN - Enables the CS6 input to be included during the sampling cycle.

- '0' - The CS6 input is not included in the sampling cycle.
- '1' (default) - The CS6 input is included in the sampling cycle.

Bit 4 - CS5_EN - Enables the CS5 input to be included during the sampling cycle.

Bit 3 - CS4_EN - Enables the CS4 input to be included during the sampling cycle.

Bit 2 - CS3_EN - Enables the CS3 input to be included during the sampling cycle.

Bit 1 - CS2_EN - Enables the CS2 input to be included during the sampling cycle.

Bit 0 - CS1_EN - Enables the CS1 input to be included during the sampling cycle.

5.8 Sensor Input Configuration Register

Table 5.12 Sensor Input Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
22h	R/W	Sensor Input Configuration	MAX_DUR[3:0]				RPT_RATE[3:0]				A4h

The Sensor Input Configuration Register controls timings associated with the Capacitive sensor inputs 1 - 6.

Bits 7 - 4 - MAX_DUR[3:0] - (default 1010b) - Determines the maximum time that a sensor pad is allowed to be touched until the capacitive touch sensor input is recalibrated, as shown in Table 5.13.

Table 5.13 MAX_DUR Bit Decode

MAX_DUR[3:0]				TIME BEFORE RECALIBRATION
3	**2**	**1**	**0**	
0	0	0	0	560ms
0	0	0	1	840ms
0	0	1	0	1120ms
0	0	1	1	1400ms
0	1	0	0	1680ms
0	1	0	1	2240ms
0	1	1	0	2800ms
	1	1	1	3360ms
1	0	0	0	3920ms
1	0	0	1	4480ms
1	0	1	0	5600ms (default)
1	0	1	1	6720ms
1	1	0	0	7840ms
1	1	0	1	8906ms
1	1	1	0	10080ms
1	1	1	1	11200ms

Bits 3 - 0 - RPT_RATE[3:0] - (default 0100b) Determines the time duration between interrupt assertions when auto repeat is enabled. The resolution is 35ms the range is from 35ms to 560ms as shown in Table 5.14.

Table 5.14 RPT_RATE Bit Decode

RPT_RATE[3:0]				INTERRUPT REPEAT RATE
3	**2**	**1**	**0**	
0	0	0	0	35ms
0	0	0	1	70ms
0	0	1	0	105ms
0	0	1	1	140ms
0	1	0	0	175ms (default)
0	1	0	1	210ms
0	1	1	0	245ms

Table 5.14 RPT_RATE Bit Decode (continued)

RPT_RATE[3:0]				INTERRUPT REPEAT RATE
3	**2**	**1**	**0**	
0	1	1	1	280ms
1	0	0	0	315ms
1	0	0	1	350ms
1	0	1	0	385ms
1	0	1	1	420ms
1	1	0	0	455ms
1	1	0	1	490ms
1	1	1	0	525ms
1	1	1	1	560ms

5.9 Sensor Input Configuration 2 Register

Table 5.15 Sensor Input Configuration 2 Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
23h	R/W	Sensor Input Configuration 2	-	-	-	-	M_PRESS[3:0]				07h

Bits 3 - 0 - M_PRESS[3:0] - (default 0111b) - Determines the minimum amount of time that sensor inputs configured to use auto repeat must detect a sensor pad touch to detect a “press and hold” event. If the sensor input detects a touch for longer than the M_PRESS[3:0] settings, a “press and hold” event is detected. If a sensor input detects a touch for less than or equal to the M_PRESS[3:0] settings, a touch event is detected.

The resolution is 35ms the range is from 35ms to 560ms as shown in Table 5.16.

Table 5.16 M_PRESS Bit Decode

M_PRESS[3:0]				M_PRESS SETTINGS
3	**2**	**1**	**0**	
0	0	0	0	35ms
0	0	0	1	70ms
0	0	1	0	105ms
0	0	1	1	140ms
0	1	0	0	175ms
0	1	0	1	210ms

Table 5.16 M_PRESS Bit Decode (continued)

M_PRESS[3:0]				M_PRESS SETTINGS
3	**2**	**1**	**0**	
0	1	1	0	245ms
0	1	1	1	280ms (default)
1	0	0	0	315ms
1	0	0	1	350ms
1	0	1	0	385ms
1	0	1	1	420ms
1	1	0	0	455ms
1	1	0	1	490ms
1	1	1	0	525ms
1	1	1	1	560ms

5.10 Averaging and Sampling Configuration Register

Table 5.17 Averaging and Sampling Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
24h	R/W	Averaging and Sampling Config		AVG[2:0]			SAMP_TIME[1:0]		CYCLE_TIME [1:0]		39h

The Averaging and Sampling Configuration register controls the number of samples taken and the total sensor input cycle time for all active sensor inputs while the device is functioning in Active state.

Bits 6 - 4 - AVG[2:0] - Determines the number of samples that are taken for all active channels during the sensor cycle as shown in Table 5.18. All samples are taken consecutively on the same channel before the next channel is sampled and the result is averaged over the number of samples measured before updating the measured results.

For example, if CS1, CS2, and CS3 are sampled during the sensor cycle, and the AVG[2:0] bits are set to take 4 samples per channel, then the full sensor cycle will be: CS1, CS1, CS1, CS1, CS2, CS2, CS2, CS2, CS3, CS3, CS3, CS3.

Table 5.18 AVG Bit Decode

AVG[2:0]			NUMBER OF SAMPLES TAKEN PER MEASUREMENT
2	**1**	**0**	
0	0	0	1
0	0	1	2

Table 5.18 AVG Bit Decode (continued)

AVG[2:0]			NUMBER OF SAMPLES TAKEN PER MEASUREMENT
2	**1**	**0**	
0	1	0	4
0	1	1	8 (default)
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Bits 3 - 2 - SAMP_TIME[1:0] - Determines the time to take a single sample as shown in Table 5.19.

Table 5.19 SAMP_TIME Bit Decode

SAMP_TIME[1:0]		SAMPLE TIME
1	**0**	
0	0	320us
0	1	640us
1	0	1.28ms (default)
1	1	2.56ms

Bits 1 - 0 - CYCLE_TIME[1:0] - Determines the overall cycle time for all measured channels during normal operation as shown in Table 5.20. All measured channels are sampled at the beginning of the cycle time. If additional time is remaining, then the device is placed into a lower power state for the remaining duration of the cycle.

Table 5.20 CYCLE_TIME Bit Decode

CYCLE_TIME[1:0]		OVERALL CYCLE TIME
1	**0**	
0	0	35ms
0	1	70ms (default)
1	0	105ms
1	1	140ms

APPLICATION NOTE: The programmed cycle time is only maintained if the total averaging time for all samples is less than the programmed cycle. The AVG[2:0] bits will take priority so that if more samples are required than would normally be allowed during the cycle time, the cycle time will be extended as necessary to accommodate the number of samples to be measured.

5.11 Calibration Activate Register

Table 5.21 Calibration Activate Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
26h	R/W	Calibration Activate	-	-	CS6_ CAL	CS5_ CAL	CS4_ CAL	CS3_ CAL	CS2_ CAL	CS1_ CAL	00h

The Calibration Activate register forces the respective sensor inputs to be re-calibrated affecting both the analog and digital blocks. During the re-calibration routine, the sensor inputs will not detect a press for up to 600ms and the Sensor Input Base Count register values will be invalid. During this time, any press on the corresponding sensor pads will invalidate the re-calibration. When finished, the CALX[9:0] bits will be updated (see Section 5.25).

When the corresponding bit is set, the device will perform the calibration and the bit will be automatically cleared once the re-calibration routine has finished.

Bit 5 - CS6_CAL - When set, the CS6 input is re-calibrated. This bit is automatically cleared once the sensor input has been re-calibrated successfully.

Bit 4 - CS5_CAL - When set, the CS5 input is re-calibrated. This bit is automatically cleared once the sensor input has been re-calibrated successfully.

Bit 3 - CS4_CAL - When set, the CS4 input is re-calibrated. This bit is automatically cleared once the sensor input has been re-calibrated successfully.

Bit 2 - CS3_CAL - When set, the CS3 input is re-calibrated. This bit is automatically cleared once the sensor input has been re-calibrated successfully.

Bit 1 - CS2_CAL - When set, the CS2 input is re-calibrated. This bit is automatically cleared once the sensor input has been re-calibrated successfully.

Bit 0 - CS1_CAL - When set, the CS1 input is re-calibrated. This bit is automatically cleared once the sensor input has been re-calibrated successfully.

5.12 Interrupt Enable Register

Table 5.22 Interrupt Enable Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
27h	R/W	Interrupt Enable	-	-	CS6_ INT_EN	CS5_ INT_EN	CS4_ INT_EN	CS3_ INT_EN	CS2_ INT_EN	CS1_ INT_EN	3Fh

The Interrupt Enable register determines whether a sensor pad touch or release (if enabled) causes the interrupt pin to be asserted.

Bit 5 - CS6_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS6 (associated with the CS6 status bit).

- '0' - The interrupt pin will not be asserted if a touch is detected on CS6 (associated with the CS6 status bit).
- '1' (default) - The interrupt pin will be asserted if a touch is detected on CS6 (associated with the CS6 status bit).

Bit 4 - CS5_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS5 (associated with the CS5 status bit).

Bit 3 - CS4_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS4 (associated with the CS4 status bit).

Bit 2 - CS3_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS3 (associated with the CS3 status bit).

Bit 1 - CS2_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS2 (associated with the CS2 status bit).

Bit 0 - CS1_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS1 (associated with the CS1 status bit).

5.13 Repeat Rate Enable Register

Table 5.23 Repeat Rate Enable Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
28h	R/W	Repeat Rate Enable	-	-	CS6_ RPT_EN	CS5_ RPT_EN	CS4_ RPT_EN	CS3_ RPT_EN	CS2_ RPT_EN	CS1_ RPT_EN	3Fh

The Repeat Rate Enable register enables the repeat rate of the sensor inputs as described in Section 4.3.1.

Bit 5 - CS6_RPT_EN - Enables the repeat rate for capacitive touch sensor input 6.

- '0' - The repeat rate for CS6 is disabled. It will only generate an interrupt when a touch is detected and when a release is detected no matter how long the touch is held for.
- '1' (default) - The repeat rate for CS6 is enabled. In the case of a "touch" event, it will generate an interrupt when a touch is detected and a release is detected (as determined by the INT_REL_n bit - see Section 5.6). In the case of a "press and hold" event, it will generate an interrupt when a touch is detected and at the repeat rate so long as the touch is held.

Bit 4 - CS5_RPT_EN - Enables the repeat rate for capacitive touch sensor input 5.

Bit 3 - CS4_RPT_EN - Enables the repeat rate for capacitive touch sensor input 4.

Bit 2 - CS3_RPT_EN - Enables the repeat rate for capacitive touch sensor input 3.

Bit 1 - CS2_RPT_EN - Enables the repeat rate for capacitive touch sensor input 2.

Bit 0 - CS1_RPT_EN - Enables the repeat rate for capacitive touch sensor input 1.

5.14 Multiple Touch Configuration Register

Table 5.24 Multiple Touch Configuration

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
2Ah	R/W	Multiple Touch Config	MULT_ BLK_ EN	-	-	-	B_MULT_T[1:0]		-	-	80h

The Multiple Touch Configuration register controls the settings for the multiple touch detection circuitry. These settings determine the number of simultaneous buttons that may be pressed before additional buttons are blocked and the MULT status bit is set.

Bit 7 - MULT_BLK_EN - Enables the multiple button blocking circuitry.

- '0' - The multiple touch circuitry is disabled. The device will not block multiple touches.
- '1' (default) - The multiple touch circuitry is enabled. The device will flag the number of touches equal to programmed multiple touch threshold and block all others. It will remember which sensor inputs are valid and block all others until that sensor pad has been released. Once a sensor pad has been released, the N detected touches (determined via the cycle order of CS1 - CS6) will be flagged and all others blocked.

Bits 3 - 2 - B_MULT_T[1:0] - Determines the number of simultaneous touches on all sensor pads before a Multiple Touch Event is detected and sensor inputs are blocked. The bit decode is given by Table 5.25.

Table 5.25 B_MULT_T Bit Decode

B_MULT_T[1:0]		NUMBER OF SIMULTANEOUS TOUCHES
1	**0**	
0	0	1 (default)
0	1	2
1	0	3
1	1	4

5.15 Multiple Touch Pattern Configuration Register

Table 5.26 Multiple Touch Pattern Configuration

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
2Bh	R/W	Multiple Touch Pattern Config	MTP_ EN	-	-		MTP_TH[1:0]		COMP_ PTRN	MTP_ ALERT	00h

The Multiple Touch Pattern Configuration register controls the settings for the multiple touch pattern detection circuitry. This circuitry works like the multiple touch detection circuitry with the following differences:

1. The detection threshold is a percentage of the touch detection threshold as defined by the MTP_TH[1:0] bits whereas the multiple touch circuitry uses the touch detection threshold.
2. The MTP detection circuitry either will detect a specific pattern of sensor inputs as determined by the Multiple Touch Pattern register settings or it will use the Multiple Touch Pattern register settings to determine a minimum number of sensor inputs that will cause the MTP circuitry to flag an event. When using pattern recognition mode, if all of the sensor inputs set by the Multiple Touch Pattern register have a delta count greater than the MTP threshold or have their corresponding Noise Flag Status bits set, the MTP bit will be set. When using the absolute number mode, if the number of sensor inputs with thresholds above the MTP threshold or with Noise Flag Status bits set is equal to or greater than this number, the MTP bit will be set.
3. When an MTP event occurs, all touches are blocked and an interrupt is generated.

4. All sensor inputs will remain blocked so long as the requisite number of sensor inputs are above the MTP threshold or have Noise Flag Status bits set. Once this condition is removed, touch detection will be restored. Note that the MTP status bit is only cleared by writing a '0' to the INT bit once the condition has been removed.

Bit 7 - MTP_EN - Enables the multiple touch pattern detection circuitry.

- '0' (default) - The MTP detection circuitry is disabled.
- '1' - The MTP detection circuitry is enabled.

Bits 3-2 - MTP_TH[1:0] - Determine the MTP threshold, as shown in Table 5.27. This threshold is a percentage of sensor input threshold (see Section 5.18, "Sensor Input Threshold Registers") when the device is in the Fully Active state or of the standby threshold (see Section 5.23, "Standby Threshold Register") when the device is in the Standby state.

Table 5.27 MTP_TH Bit Decode

MTP_TH[1:0]		THRESHOLD DIVIDE SETTING
1	**0**	
0	0	12.5% (default)
0	1	25%
1	0	37.5%
1	1	100%

Bit 1 - COMP_PTRN - Determines whether the MTP detection circuitry will use the Multiple Touch Pattern register as a specific pattern of sensor inputs or as an absolute number of sensor inputs.

- '0' (default) - The MTP detection circuitry will use the Multiple Touch Pattern register bit settings as an absolute minimum number of sensor inputs that must be above the threshold or have Noise Flag Status bits set. The number will be equal to the number of bits set in the register.
- '1' - The MTP detection circuitry will use pattern recognition. Each bit set in the Multiple Touch Pattern register indicates a specific sensor input that must have a delta count greater than the MTP threshold or have a Noise Flag Status bit set. If the criteria are met, the MTP status bit will be set.

Bit 0 - MTP_ALERT - Enables an interrupt if an MTP event occurs. In either condition, the MTP status bit will be set.

- '0' (default) - If an MTP event occurs, the ALERT# pin is not asserted.
- '1' - If an MTP event occurs, the ALERT# pin will be asserted.

5.16 Multiple Touch Pattern Register

Table 5.28 Multiple Touch Pattern Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
2Dh	R/W	Multiple Touch Pattern	-	-	CS6_ PTRN	CS5_ PTRN	CS4_ PTRN	CS3_ PTRN	CS2_ PTRN	CS1_ PTRN	3Fh

The Multiple Touch Pattern register acts as a pattern to identify an expected sensor input profile for diagnostics or other significant events. There are two methods for how the Multiple Touch Pattern

register is used: as specific sensor inputs or number of sensor input that must exceed the MTP threshold or have Noise Flag Status bits set. Which method is used is based on the COMP_PTRN bit (see Section 5.15). The methods are described below.

1. Specific Sensor Inputs: If, during a single polling cycle, the specific sensor inputs above the MTP threshold or with Noise Flag Status bits set match those bits set in the Multiple Touch Pattern register, an MTP event is flagged.
2. Number of Sensor Inputs: If, during a single polling cycle, the number of sensor inputs with a delta count above the MTP threshold or with Noise Flag Status bits set is equal to or greater than the number of pattern bits set, an MTP event is flagged.

Bit 5 - CS6_PTRN - Determines whether CS6 is considered as part of the Multiple Touch Pattern.

- '0' - CS6 is not considered a part of the pattern.
- '1' - CS6 is considered a part of the pattern or the absolute number of sensor inputs that must have a delta count greater than the MTP threshold or have the Noise Flag Status bit set is increased by 1.

Bit 4 - CS5_PTRN - Determines whether CS5 is considered as part of the Multiple Touch Pattern.

Bit 3 - CS4_PTRN - Determines whether CS4 is considered as part of the Multiple Touch Pattern.

Bit 2 - CS3_PTRN - Determines whether CS3 is considered as part of the Multiple Touch Pattern.

Bit 1 - CS2_PTRN - Determines whether CS2 is considered as part of the Multiple Touch Pattern.

Bit 0 - CS1_PTRN - Determines whether CS1 is considered as part of the Multiple Touch Pattern.

5.17 Recalibration Configuration Register

Table 5.29 Recalibration Configuration Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
2Fh	R/W	Recalibration Configuration	BUT_ LD_TH	NO_ CLR_ INTD	NO_ CLR_ NEG	NEG_DELTA_ CNT[1:0]		CAL_CFG[2:0]			8Ah

The Recalibration Configuration register controls the automatic re-calibration routine settings as well as advanced controls to program the Sensor Input Threshold register settings.

Bit 7 - BUT_LD_TH - Enables setting all Sensor Input Threshold registers by writing to the Sensor Input 1 Threshold register.

- '0' - Each Sensor Input X Threshold register is updated individually.
- '1' (default) - Writing the Sensor Input 1 Threshold register will automatically overwrite the Sensor Input Threshold registers for all sensor inputs (Sensor Input Threshold 1 through Sensor Input Threshold 6). The individual Sensor Input X Threshold registers (Sensor Input 2 Threshold through Sensor Input 6 Threshold) can be individually updated at any time.

Bit 6 - NO_CLR_INTD - Controls whether the accumulation of intermediate data is cleared if the noise status bit is set.

- '0' (default) - The accumulation of intermediate data is cleared if the noise status bit is set.
- '1' - The accumulation of intermediate data is not cleared if the noise status bit is set.

APPLICATION NOTE: Bits 5 and 6 should both be set to the same value. Either both should be set to '0' or both should be set to '1'.

Bit 5 - NO_CLR_NEG - Controls whether the consecutive negative delta counts counter is cleared if the noise status bit is set.

- '0' (default) - The consecutive negative delta counts counter is cleared if the noise status bit is set.
- '1' - The consecutive negative delta counts counter is not cleared if the noise status bit is set.

Bits 4 - 3 - NEG_DELTA_CNT[1:0] - Determines the number of negative delta counts necessary to trigger a digital re-calibration as shown in Table 5.30.

Table 5.30 NEG_DELTA_CNT Bit Decode

NEG_DELTA_CNT[1:0]		NUMBER OF CONSECUTIVE NEGATIVE DELTA COUNT VALUES
1	**0**	
0	0	8
0	1	16 (default)
1	0	32
1	1	None (disabled)

Bits 2 - 0 - CAL_CFG[2:0] - Determines the update time and number of samples of the automatic re-calibration routine. The settings apply to all sensor inputs universally (though individual sensor inputs can be configured to support re-calibration - see Section 5.11).

Table 5.31 CAL_CFG Bit Decode

CAL_CFG[2:0]			RECALIBRATION SAMPLES (SEE Note 5.1)	UPDATE TIME (SEE Note 5.2)
2	**1**	**0**		
0	0	0	16	16
0	0	1	32	32
0	1	0	64	64 (default)
0	1	1	128	128
1	0	0	256	256
1	0	1	256	1024
1	1	0	256	2048
1	1	1	256	4096

Note 5.1 Recalibration Samples refers to the number of samples that are measured and averaged before the Base Count is updated however does not control the base count update period.

Note 5.2 Update Time refers to the amount of time (in polling cycle periods) that elapses before the Base Count is updated. The time will depend upon the number of channels active, the averaging setting, and the programmed cycle time.

5.18 Sensor Input Threshold Registers

Table 5.32 Sensor Input Threshold Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
30h	R/W	Sensor Input 1 Threshold	-	64	32	16	8	4	2	1	40h
31h	R/W	Sensor Input 2 Threshold	-	64	32	16	8	4	2	1	40h
32h	R/W	Sensor Input 3 Threshold	-	64	32	16	8	4	2	1	40h
33h	R/W	Sensor Input 4 Threshold	-	64	32	16	8	4	2	1	40h
34h	R/W	Sensor Input 5 Threshold	-	64	32	16	8	4	2	1	40h
35h	R/W	Sensor Input 6 Threshold	-	64	32	16	8	4	2	1	40h

The Sensor Input Threshold registers store the delta threshold that is used to determine if a touch has been detected. When a touch occurs, the input signal of the corresponding sensor pad changes due to the capacitance associated with a touch. If the sensor input change exceeds the threshold settings, a touch is detected.

When the BUT_LD_TH bit is set (see Section 5.17 - bit 7), writing data to the Sensor Input 1 Threshold register will update all of the sensor input threshold registers (31h - 35h inclusive).

5.19 Sensor Input Noise Threshold Register

Table 5.33 Sensor Input Noise Threshold Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
38h	R/W	Sensor Input Noise Threshold							CS_BN_TH [1:0]		01h

The Sensor Input Noise Threshold register controls the value of a secondary internal threshold to detect noise and improve the automatic recalibration routine. If a capacitive touch sensor input exceeds the Sensor Input Noise Threshold but does not exceed the sensor input threshold, it is determined to be caused by a noise spike. That sample is not used by the automatic re-calibration routine. This feature can be disabled by setting the DIS_DIG_NOISE bit.

Bits 1-0 - CS1_BN_TH[1:0] - Controls the noise threshold for all capacitive touch sensor inputs, as shown in Table 5.34. The threshold is proportional to the threshold setting.

Table 5.34 CSx_BN_TH Bit Decode

CS_BN_TH[1:0]		PERCENT THRESHOLD SETTING
1	**0**	
0	0	25%
0	1	37.5% (default)
1	0	50%
1	1	62.5%

5.20 Standby Channel Register

Table 5.35 Standby Channel Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
40h	R/W	Standby Channel	-	-	CS6_ STBY	CS5_ STBY	CS4_ STBY	CS3_ STBY	CS2_ STBY	CS1_ STBY	00h

The Standby Channel register controls which (if any) capacitive touch sensor inputs are active during Standby.

Bit 5 - CS6_STBY - Controls whether the CS6 channel is active in Standby.

- '0' (default) - The CS6 channel not be sampled during Standby mode.
- '1' - The CS6 channel will be sampled during Standby Mode. It will use the Standby threshold setting, and the standby averaging and sensitivity settings.

Bit 4 - CS5_STBY - Controls whether the CS5 channel is active in Standby.

Bit 3 - CS4_STBY - Controls whether the CS4 channel is active in Standby.

Bit 2 - CS3_STBY - Controls whether the CS3 channel is active in Standby.

Bit 1 - CS2_STBY - Controls whether the CS2 channel is active in Standby.

Bit 0 - CS1_STBY - Controls whether the CS1 channel is active in Standby.

5.21 Standby Configuration Register

Table 5.36 Standby Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
41h	R/W	Standby Configuration	AVG_ SUM	STBY_AVG[2:0]			STBY_SAMP_ TIME[1:0]		STBY_CY_TIME [1:0]		39h

The Standby Configuration register controls averaging and cycle time for those sensor inputs that are active in Standby. This register is useful for detecting proximity on a small number of sensor inputs as

it allows the user to change averaging and sample times on a limited number of sensor inputs and still maintain normal functionality in the fully active state.

Bit 7 - AVG_SUM - Determines whether the active sensor inputs will average the programmed number of samples or whether they will accumulate for the programmed number of samples.

- '0' - (default) - The active sensor input delta count values will be based on the average of the programmed number of samples when compared against the threshold.
- '1' - The active sensor input delta count values will be based on the summation of the programmed number of samples when compared against the threshold. This bit should only be set when performing proximity detection as a physical touch will overflow the delta count registers and may result in false readings.

Bits 6 - 4 - STBY_AVG[2:0] - Determines the number of samples that are taken for all active channels during the sensor cycle as shown in Table 5.37. All samples are taken consecutively on the same channel before the next channel is sampled and the result is averaged over the number of samples measured before updating the measured results.

Table 5.37 STBY_AVG Bit Decode

STBY_AVG[2:0]			NUMBER OF SAMPLES TAKEN PER MEASUREMENT
2	**1**	**0**	
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8 (default)
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Bit 3-2 - STBY SAMP_TIME[1:0] - Determines the time to take a single sample when the device is in Standby as shown in Table 5.38.

Table 5.38 STBY_SAMP_TIME Bit Decode

STBY_SAMP_TIME[1:0]		SAMPLING TIME
1	**0**	
0	0	320us
0	1	640us
1	0	1.28ms (default)
1	1	2.56ms

Bits 1 - 0 - STBY_CY_TIME[2:0] - Determines the overall cycle time for all measured channels during standby operation as shown in Table 5.39. All measured channels are sampled at the beginning of the

cycle time. If additional time is remaining, the device is placed into a lower power state for the remaining duration of the cycle.

Table 5.39 STBY_CY_TIME Bit Decode

STBY_CY_TIME[1:0]		OVERALL CYCLE TIME
1	**0**	
0	0	35ms
0	1	70ms (default)
1	0	105ms
1	1	140ms

APPLICATION NOTE: The programmed cycle time is only maintained if the total averaging time for all samples is less than the programmed cycle. The STBY_AVG[2:0] bits will take priority so that if more samples are required than would normally be allowed during the cycle time, the cycle time will be extended as necessary to accommodate the number of samples to be measured.

5.22 Standby Sensitivity Register

Table 5.40 Standby Sensitivity Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
42h	R/W	Standby Sensitivity	-	-	-	-	-	STBY_SENSE[2:0]			02h

The Standby Sensitivity register controls the sensitivity for sensor inputs that are active in Standby.

Bits 2 - 0 - STBY_SENSE[2:0] - Controls the sensitivity for sensor inputs that are active in Standby. The sensitivity settings act to scale the relative delta count value higher or lower based on the system parameters. A setting of 000b is the most sensitive while a setting of 111b is the least sensitive. At the more sensitive settings, touches are detected for a smaller delta C corresponding to a “lighter” touch. These settings are more sensitive to noise however and a noisy environment may flag more false touches than higher sensitivity levels.

APPLICATION NOTE: A value of 128x is the most sensitive setting available. At the most sensitivity settings, the MSB of the Delta Count register represents 64 out of ~25,000 which corresponds to a touch of approximately 0.25% of the base capacitance (or a ΔC of 25fF from a 10pF base capacitance). Conversely a value of 1x is the least sensitive setting available. At these settings, the MSB of the Delta Count register corresponds to a delta count of 8192 counts out of ~25,000 which corresponds to a touch of approximately 33% of the base capacitance (or a ΔC of 3.33pF from a 10pF base capacitance).

Table 5.41 STBY_SENSE Bit Decode

STBY_SENSE[2:0]			
2	**1**	**0**	**SENSITIVITY MULTIPLIER**
0	0	0	128x (most sensitive)
0	0	1	64x
0	1	0	32x (default)
0	1	1	16x
1	0	0	8x
1	0	1	4x
1	1	0	2x
1	1	1	1x - (least sensitive)

5.23 Standby Threshold Register

Table 5.42 Standby Threshold Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
43h	R/W	Standby Threshold	-	64	32	16	8	4	2	1	40h

The Standby Threshold register stores the delta threshold that is used to determine if a touch has been detected. When a touch occurs, the input signal of the corresponding sensor pad changes due to the capacitance associated with a touch. If the sensor input change exceeds the threshold settings, a touch is detected.

5.24 Sensor Input Base Count Registers

Table 5.43 Sensor Input Base Count Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
50h	R	Sensor Input 1 Base Count	128	64	32	16	8	4	2	1	C8h
51h	R	Sensor Input 2 Base Count	128	64	32	16	8	4	2	1	C8h
52h	R	Sensor Input 3 Base Count	128	64	32	16	8	4	2	1	C8h
53h	R	Sensor Input 4 Base Count	128	64	32	16	8	4	2	1	C8h

Table 5.43 Sensor Input Base Count Registers (continued)

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
54h	R	Sensor Input 5 Base Count	128	64	32	16	8	4	2	1	C8h
55h	R	Sensor Input 6 Base Count	128	64	32	16	8	4	2	1	C8h

The Sensor Input Base Count registers store the calibrated “Not Touched” input value from the capacitive touch sensor inputs. These registers are periodically updated by the re-calibration routine.

The routine uses an internal adder to add the current count value for each reading to the sum of the previous readings until sample size has been reached. At this point, the upper 16 bits are taken and used as the Sensor Input Base Count. The internal adder is then reset and the re-calibration routine continues.

The data presented is determined by the BASE_SHIFT[3:0] bits (see Section 5.5).

5.25 Sensor Input Calibration Registers

Table 5.44 Sensor Input Calibration Registers

ADDR	REGISTER	R/W	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
B1h	Sensor Input 1 Calibration	R	CAL1_9	CAL1_8	CAL1_7	CAL1_6	CAL1_5	CAL1_4	CAL1_3	CAL1_2	00h
B2h	Sensor Input 2 Calibration	R	CAL2_9	CAL2_8	CAL2_7	CAL2_6	CAL2_5	CAL2_4	CAL2_3	CAL2_2	00h
B3h	Sensor Input 3 Calibration	R	CAL3_9	CAL3_8	CAL3_7	CAL3_6	CAL3_5	CAL3_4	CAL3_3	CAL3_2	00h
B4h	Sensor Input 4 Calibration	R	CAL4_9	CAL4_8	CAL4_7	CAL4_6	CAL4_5	CAL4_4	CAL4_3	CAL4_2	00h
B5h	Sensor Input 5 Calibration	R	CAL5_9	CAL5_8	CAL5_7	CAL5_6	CAL5_5	CAL5_4	CAL5_3	CAL5_2	00h
B6h	Sensor Input 6 Calibration	R	CAL6_9	CAL6_8	CAL6_7	CAL6_6	CAL6_5	CAL6_4	CAL6_3	CAL6_2	00h
B9h	Sensor Input Calibration LSB 1	R	CAL4_1	CAL4_0	CAL3_1	CAL3_0	CAL2_1	CAL2_0	CAL1_1	CAL1_0	00h
BAh	Sensor Input Calibration LSB 2	R	-	-	-	-	CAL6_1	CAL6_0	CAL5_1	CAL5_0	00h

The Sensor Input Calibration registers hold the 10-bit value that represents the last calibration value.

5.26 Product ID Register

Table 5.45 Product ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FDh	R	Product ID CAP1106	0	1	0	1	0	1	0	1	55h
		Product ID CAP1105	0	1	0	1	0	1	1	0	56h

The Product ID register stores a unique 8-bit value that identifies the device.

5.27 Manufacturer ID Register

Table 5.46 Vendor ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FEh	R	Manufacturer ID	0	1	0	1	1	1	0	1	5Dh

The Vendor ID register stores an 8-bit value that represents SMSC.

5.28 Revision Register

Table 5.47 Revision Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FFh	R	Revision	1	0	0	0	0	0	1	1	83h

The Revision register stores an 8-bit value that represents the part revision.

Chapter 6 Package Information

6.1 CAP1106 and CAP1105 Package Drawings

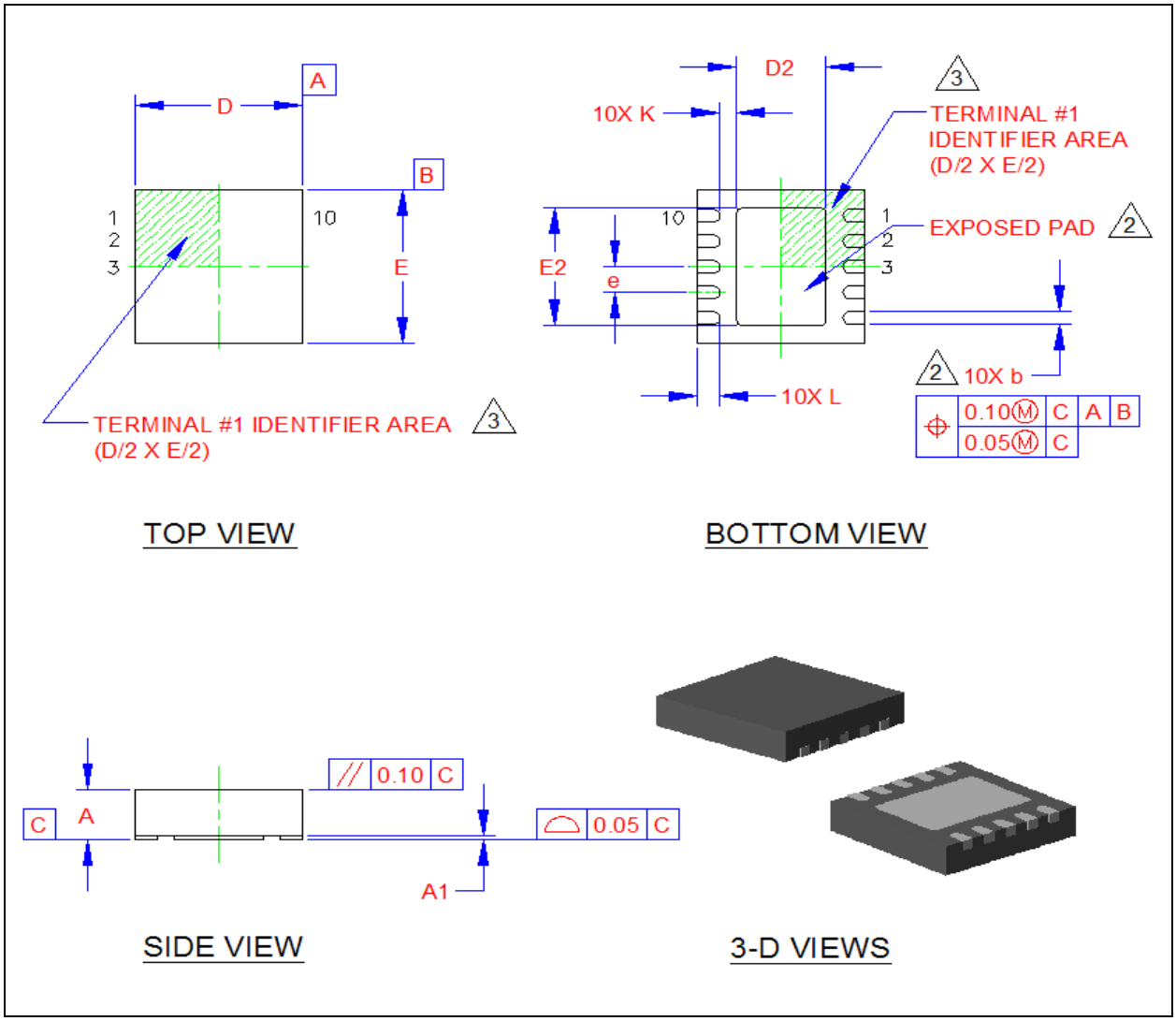


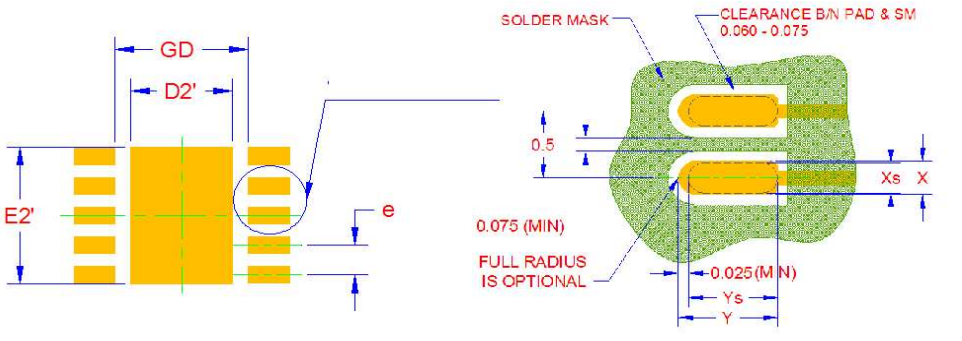
Figure 6.1 10-Pin DFN 3mm x 3mm Package Drawings

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
D/E	2.90	3.00	3.10	-	X/Y BODY SIZE
D2	1.50	1.60	1.70	2	X EXPOSED PAD SIZE
E2	2.20	2.30	2.40	2	Y EXPOSED PAD SIZE
L	0.35	0.40	0.45	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
K	0.25	0.30	-	-	TERMINAL TO PAD DISTANCE
e	0.50 BSC			-	TERMINAL PITCH

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD, AS WELL AS THE TERMINALS. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

Figure 6.2 10-Pin DFN 3mm x 3mm Package Dimensions



PCB LAND PATTERN

LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD	2.10	-	2.20
D2'	-	1.60	1.60
E2'	-	2.30	-
Pad: X	-	0.28	0.28
Pad: Y	-	0.69	0.69
e		0.50	

Figure 6.3 10-Pin DFN 3mm x 3mm PCB Footprint

6.2 Package Marking

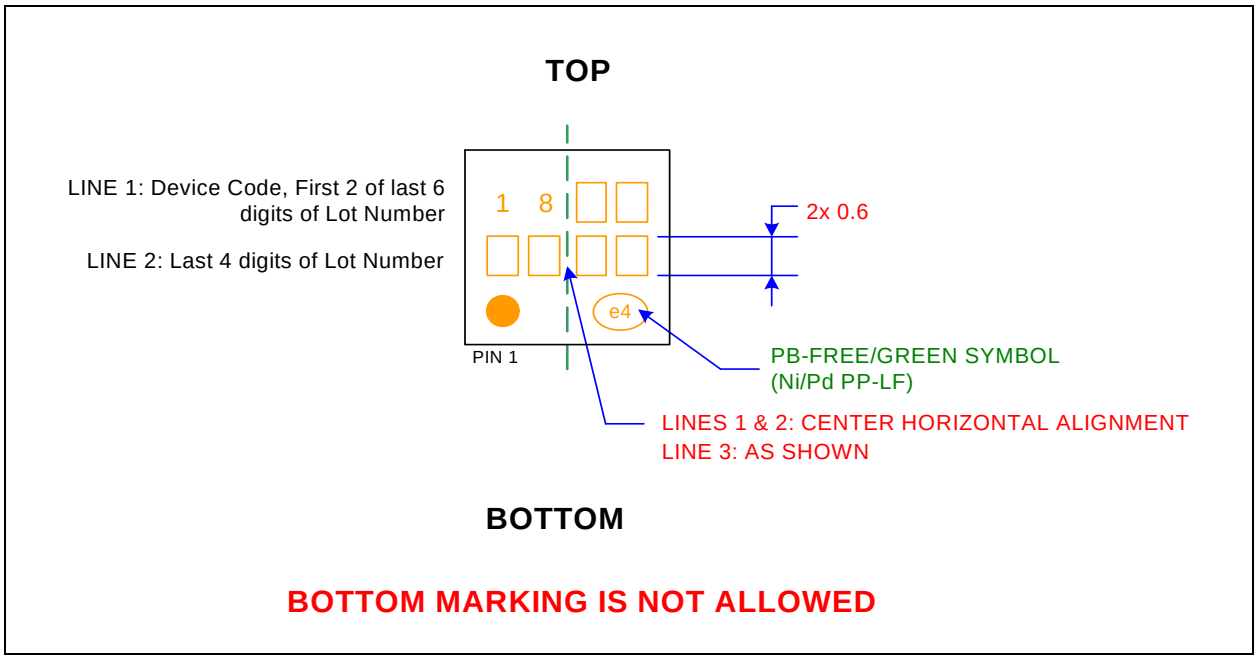


Figure 6.4 CAP1106-1 Package Markings

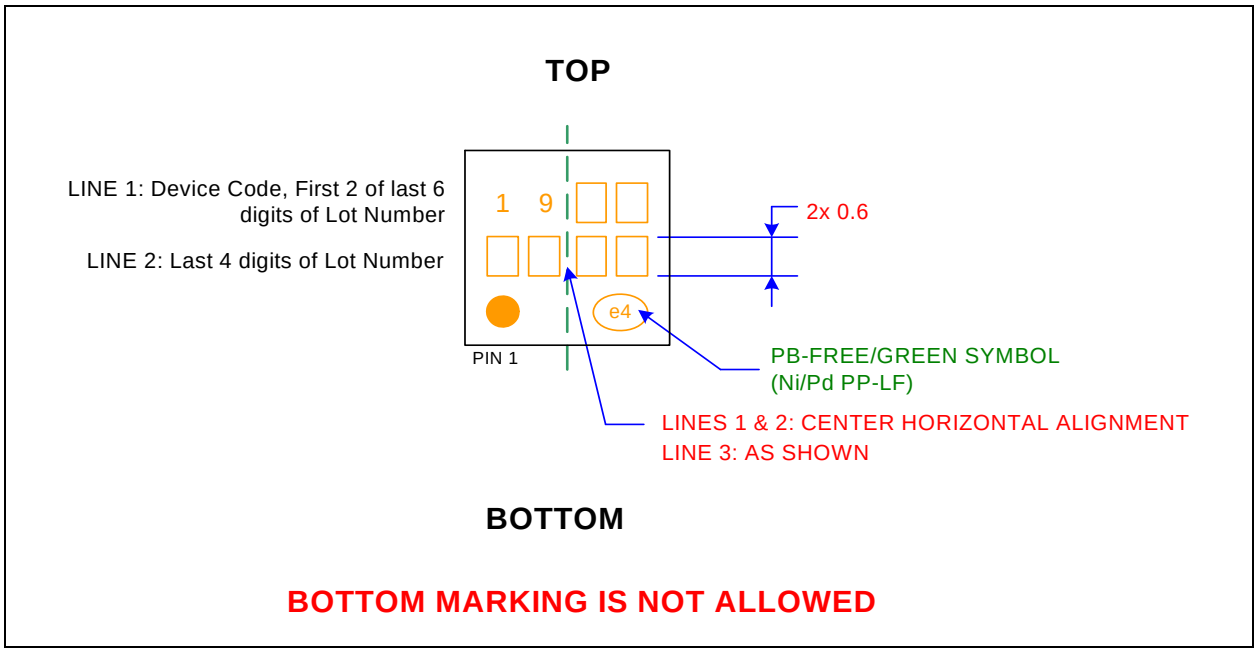


Figure 6.5 CAP1106-2 Package Markings

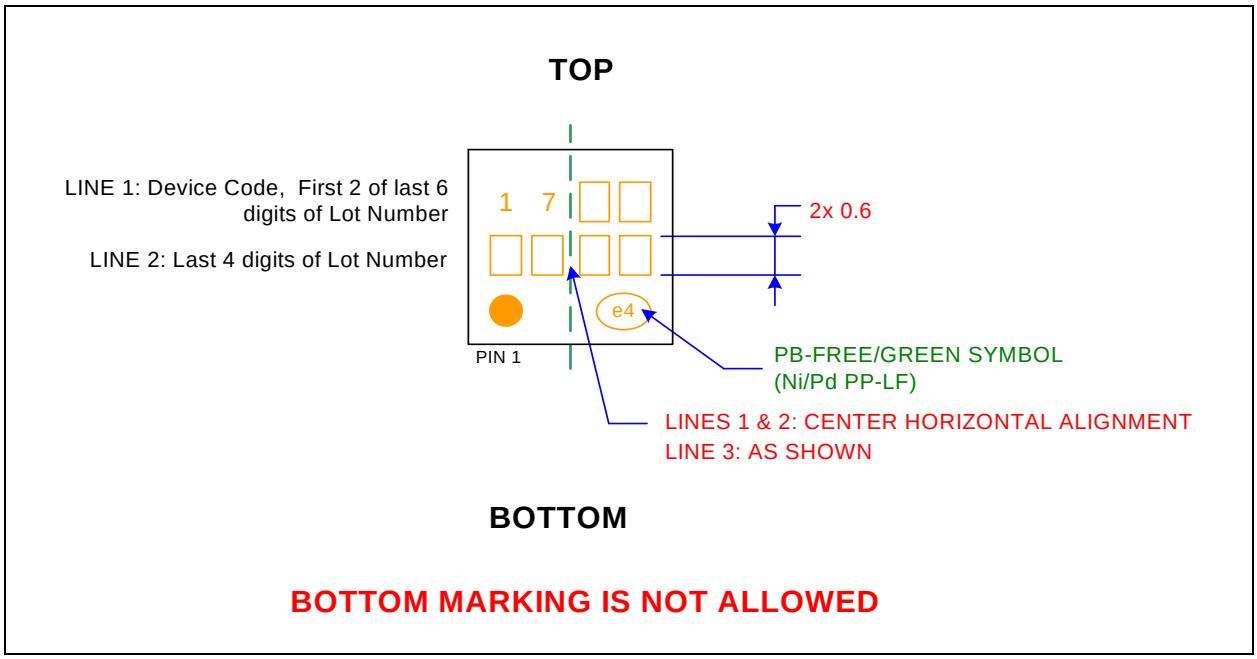


Figure 6.6 CAP1105 Package Markings

Appendix A Device Delta

A.1 Delta from CAP1006 to CAP1106 and CAP1005 to CAP1105

1. Updated circuitry to improve power supply rejection.
2. Added Multiple Touch Pattern detection circuitry. See Section 5.15, "Multiple Touch Pattern Configuration Register".
3. Added General Status register to flag Multiple touches, Multiple Touch Pattern issues and general touch detections. See Section 5.2, "Status Registers".
4. Added bits 6 and 5 to the Recalibration Configuration register (2Dh - see Section 5.17, "Recalibration Configuration Register"). These bits control whether the accumulation of intermediate data and the consecutive negative delta counts counter are cleared when the noise status bit is set.
5. Added Configuration 2 register for noise detection controls and control to interrupt on press but not on release. Added control to change alert pin polarity. See Section 5.6, "Configuration Registers".
6. Updated Deep Sleep behavior so that device does not clear DSLEEP bit on received communications but will wake to communicate.
7. Register delta:

Table A.1 Register Delta From CAP1006/1005 to CAP1106/1105

ADDRESS	REGISTER DELTA	DELTA	DEFAULT
00h Page 36	Changed - Main Status / Control	added bits 7-6 to control gain	00h
02h Page 37	New - General Status	new register to store MTP, MULT, and general TOUCH bits	00h
44h Page 40	New - Configuration 2	new register to control alert polarity, and noise detection, and interrupt on release	00h
24h Page 45	Changed - Averaging Control	updated register bits - moved SAMP_AVG[2:0] bits and added SAMP_TIME bit 1. Default changed	39h
2Bh Page 49	New - Multiple Touch Pattern Configuration	new register for Multiple Touch Pattern configuration - enable and threshold settings	80h
2Dh Page 50	New - Multiple Touch Pattern Register	new register for Multiple Touch Pattern detection circuitry - pattern or number of sensor inputs	3Fh
2Fh Page 51	Changed - Recalibration Configuration	updated register - updated CAL_CFG bit decode to add a 128 averages setting and removed highest time setting. Default changed. Added bit 6 NO_CLR_INTD and bit 5 NO_CLR_NEG.	8Ah
38h Page 53	Changed - Sensor Input Noise Threshold	updated register bits - removed bits 7 - 3 and consolidated all controls into bits 1 - 0. These bits will set the noise threshold for all channels. Default changed	01h

Table A.1 Register Delta From CAP1006/1005 to CAP1106/1105 (continued)

ADDRESS	REGISTER DELTA	DELTA	DEFAULT
39h	Removed - Noise Threshold Register 2	removed register	n/a
41h Page 54	Changed - Standby Configuration	updated register bits - moved STBY_AVG[2:0] bits and added STBY_TIME bit 1. Default changed	39h
FDh Page 59	Changed - Product ID	Changed bit decode for CAP1106	55h
		Changed bit decode for CAP1105	56h

Chapter 7 Datasheet Revision History

Table 7.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.32 (01-05-12)	Table 2.2, "Electrical Specifications"	Added conditions for $t_{HD:DAT}$.
	Section 3.2.7, "SMBus and I2C Compatibility"	Renamed from “SMBus and I2C Compliance.” First paragraph, added last sentence: “For information on using the CAP1106-1 in an I^2C system, refer to SMSC AN 14.0 SMSC Dedicated Slave Devices in I^2C Systems.” Added: CAP1106-1 supports I^2C fast mode at 400kHz. This covers the SMBus max time of 100kHz.
	Section 5.4, "Sensor Input Delta Count Registers"	Changed negative value cap from FFh to 80h.
Rev. 1.31 (08-18-11)	Section 3.3.3, "SMBus Send Byte"	Added an application note: The Send Byte protocol is not functional in Deep Sleep (i.e., DSLEEP bit is set).
	Section 3.3.4, "SMBus Receive Byte"	Added an application note: The Receive Byte protocol is not functional in Deep Sleep (i.e., DSLEEP bit is set).
	Section 5.2, "Status Registers"	Removed RESET as bit 3 in register 02h.
Rev. 1.3 (05-18-11)	Section 5.28, "Revision Register"	Updated revision ID from 82h to 83h.
	Section 5.2, "Status Registers"	Added RESET as bit 3 in register 02h.
Rev. 1.2 (02-10-11)	Section A.8, "Delta from Rev B (Mask B0) to Rev C (Mask B1)"	Added.
	Table 2.2, "Electrical Specifications"	PSR improvements made in functional revision B. Changed PSR spec from ±100 typ and ±200 max counts / V to ±3 and ±10 counts / V. Conditions updated.
	Section 4.2.2, "Recalibrating Sensor Inputs"	Added more detail with subheadings for each type of recalibration.
	Section 5.6, "Configuration Registers"	Added bit 5 BLK_PWR_CTRL to the Configuration 2 Register 44h. The TIMEOUT bit is set to ‘1’ by default for functional revision B and is set to ‘0’ by default for functional revision C (this only affects CAP1106-1).
	Section 5.28, "Revision Register"	Updated revision ID in register FFh from 81h to 82h.
Rev. 1.1 (11-17-10)	Document	Updated for functional revision B. See Section A.7, "Delta from Rev A (Mask A0) to Rev B (Mask B0)".

Table 7.1 Customer Revision History (continued)

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
	Cover	Added to General Description: “includes circuitry and support for enhanced sensor proximity detection.” Added the following Features: ▪ Calibrates for Parasitic Capacitance ▪ Analog Filtering for System Noise Sources ▪ Press and Hold feature for Volume-like Applications
	Table 2.2, "Electrical Specifications"	Conditions for Power Supply Rejection modified adding the following: Sampling time = 2.56ms Averaging = 1 Negative Delta Counts = Disabled All other parameters default
	Section 5.11, "Calibration Activate Register"	Updated register description to indicate which re-calibration routine is used.
	Section 5.14, "Multiple Touch Configuration Register"	Updated register description to indicate what will happen.
	Table 5.34, "CSx_BN_TH Bit Decode"	Table heading changed from “Threshold Divide Setting” to “Percent Threshold Setting”.
Rev. 1.0 (06-14-10)	Initial release	