PERICOM Semiconductor Corporation

Product Brief

Product: PCI Express-to-PCI Reversible Bridge
Part Number: PI7C9X110

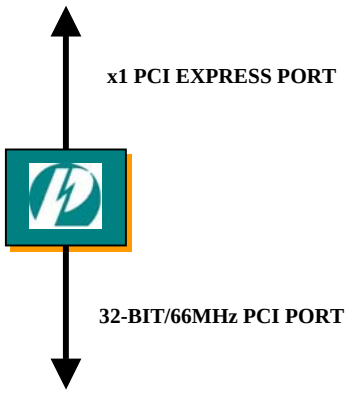
Product Description

As one of the leading PCI Express Solution Providers, Pericom is committed to introducing a line of performance tuned PCI Express Bridge Products. The PI7C9X110 is composed of one x1 PCI Express port and one standard 32-bit / 66MHz PCI port. The versatile PI7C9X110 is capable of both "forward" and "reverse" bridging. In "forward" mode, the PI7C9X110 is configured with the PCI Express port on the primary and the PCI port on the downstream side. The typical usage in this configuration is to "bridge" legacy PCI product to PCI Express systems. In "reverse" mode, the PI7C9X110 is configured with the PCI port on the primary and the PCI Express port on the downstream side. The "reverse" configuration will be mainly used to "bridge" new PCI Express products to legacy PCI systems.

Industry Specifications Compliance

- *PCI Express Base Specification*, Revision 1.0a
- *PCI Express CEM Specification*, Revision 1.0a
- *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0
- PCI-to-PCI Bridge Architecture Specification, Revision 1.2
- PCI Local Bus Specification, Revision 3.0
- PCI Hot-Plug Specification, Revision 1.1
- PCI SHPC and Subsystem Specification, Revision 1.0
- PCI Mobile Design Guide, Version 1.1
- System Management (SM) Bus, Version 2.0
- PCI Bus PM Interface Specification, Revision 1.2
- Advanced Configuration and Power Interface Specification, Revision 2.0

PI7C9X110 Topology



Special Features

- ***Fully Reversible***
  - *Forward – PCIe primary, PCI secondary*
  - *Reverse – PCI primary, PCIe secondary*
- ***Maximum Payload Size – Up to 512 bytes***
- ***Transparent and Non-transparent mode***
- ***GPIO Support***
  - *4 dedicated bi-directional*
  - *When external arbiter is used:*
    - *4 additional outputs*
    - *4 additional inputs*
- ***Masquerade* support**
  - *User defined vendor, device, revision, subsystem device, and subsystem vendor ID*
- ***Large 10KB Buffer***
  - *6KB for reads & 4KB for writes*
- ***Tiny 12 x 12mm, 160-pin LFBGA Package***
- ***Industrial Temp (-40°C ~ +85°C)***

PCI Express Features

- Virtual Isochronous Support
  - Upstream TC 1 – 7 generation
  - Downstream TC 1 – 7 mapping
- 16-bit CRC, LCRC (32-bit)
- ECRC and Advanced Error Reporting
- Error Forwarding (Data Poisoning)
- Loop back (serial and parallel)
- Lane Reversal (Polarity Toggle)
- VDDAUX Support (1.8V)
- Hot Plug Support

PCI Features

- Two Level Internal Arbitration
  - Support for up to 8 bus masters
- 3.3V Signaling with 5V I/O Tolerance
- PME# Support
- 16-bit Address Decode for VGA
- CLKRUN# Support
- VAUX Support (3.3V)
- Hot Plug Support
- Subsystem Device and Subsystem Vendor ID
- MSI and INT Support
- SM Bus
  - PHY, data link, network layer, PEC, ARP, etc.
- I2C Serial EEPROM Support

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