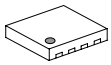
Single-phase DC Brushless Motor Driver IC

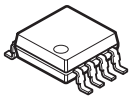
■ GENERAL DESCRIPTION

The NJU7325 is a dual power amplifier designed for small actuator applications. It incorporates MOS-FET transistor in the output stage which can offer a low saturation output voltage in high current operation. The NJU7325 is available in small and thin surface mount packages MSOP8 (VSP8), MSOP8 (TVSP8) and ESON8-V1, which provides downsizing and thinning in motor applications.

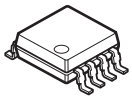
■ PACKAGE OUTLINE



NJU7325KV1
(DFN8-V1(ESON8-V1))



NJU7325R
(MSOP8(VSP8))



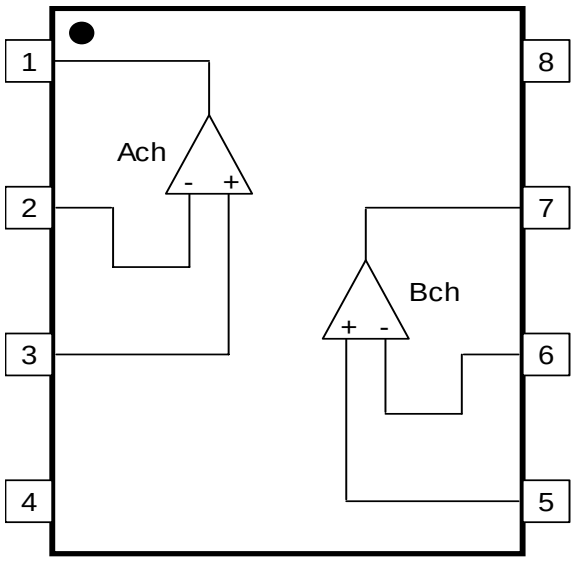
NJU7325RB1
(MSOP8(TVSP8))

■ FEATURES

- Single Supply
- Operating Voltage V_{DD}=2.4 to 5.5V
- Low Operating Current
- Low Saturation Output Voltage Vsat=±0.35V @Io=±250mA
- CMOS Technology
- Package Outline MSOP8 (VSP8)*, MSOP8 (TVSP8)**, DFN8-V1(ESON8-V1)

*MEET JEDEC MO-187-DA, **MEET JEDEC MO-187-DA / THIN TYPE

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	NOTE
Supply Voltage	V_{DD}	+7	V	-
Input Voltage	Vid	-0.3 to V_{DD}+0.3	V	-
Operating Temperature	Topr	-40 to +85	°C	-
Storage Temperature	Tstg	-50 to +150	°C	-
Power Dissipation (MSOP8(VSP8/TVSP8))	P_D	400	mW	Device itself
Power Dissipation (DFN8-V1(ESON8-V1))	P_D	520	mW	(*1)Mounted on 2-Layers Board
		1100	mW	(*2)Mounted on 4-Layers Board

(*1): Mounted on glass epoxy board based on EIA/JEDEC. (101.5×114.5×1.6mm: 2-Layers)

(*2): Mounted on glass epoxy board based on EIA/JEDEC.
(101.5×114.5×1.6mm: 4-Layers Internal foil area: 99.5×99.5mm)

■ ELECTRICAL CHARACTERISTICS

(V_{DD}=5V, V_{SS}=0V, f=1kHz, Ta=25°C)

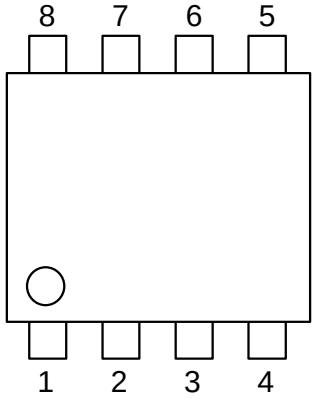
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage Range	V_{DD}		2.4	5.0	5.5	V
Quiescent Current	I_{DD}	No Load Condition, Voltage Follower, Vo=2.5V, per 1ch	-	3.0	4.0	mA
Input Offset Voltage	V_{IO}		-15	-	+15	mV
Input Offset Current	I_{IO}		-	10	-	pA
Input Bias Current	I_{IB}		-	10	-	pA
Input Impedance	R_{IN}		-	10^{12}	-	Ω
Input Common Mode Voltage Range	V_{ICM}		0.4 to 4.0	-	-	V
Maximum Output Voltage Range	V_{OM}	Io= +250mA	4.55	4.65	-	V
		Io= -250mA	-	0.35	0.45	V
Large Signal Voltage Gain	AV		55	-	-	dB
Common Mode Rejection Ratio	CMRR	V_{ICM}=0.4 to 4.0V	53	-	-	dB
Supply Voltage Rejection Ratio	PSRR	V_{DD}=4.5 to 5.5V	55	-	-	dB
Unity Gain Bandwidth	F_T	C_L=10pF, Open Loop	-	1.5	-	MHz
Slew Rate	SR	Voltage Follower, R_L=16.5Ω	-	1	-	V/us

(*3): Oscillation margin of NJU7325 will be narrow if the application features light load current and low gain.
(ex. Voltage Follower).
Maintain the value of stray capacitance at the output terminal with less than 100pF to prevent the oscillation.

(*4): Place decoupling-capacitor near Vss and V_{DD} pins.

■ **PIN CONFIGURATION**

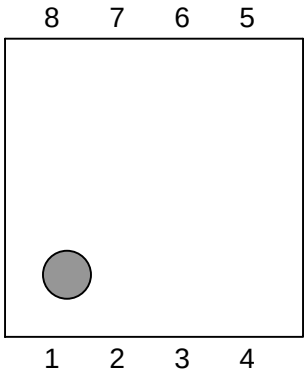
• MSOP8 (VSP8/TVSP8)



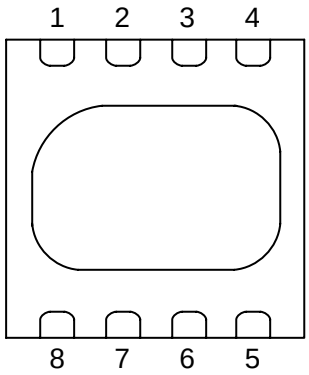
Surface

1: A OUTPUT
2: A - INPUT
3: A+ INPUT
4: V_{SS}
5: B+ INPUT
6: B - INPUT
7: B OUTPUT
8: V_{DD}

• DFN8-V1(ESON8-V1)



Surface



Backside

1: A OUTPUT
2: A - INPUT
3: A+ INPUT
4: V_{SS}
5: B+ INPUT
6: B - INPUT
7: B OUTPUT
8: V_{DD}

(*5): The PAD in the center part on the back is connected with the internal V_{DD}, therefore it is open or connects to V_{DD}.

■ APPLICATION CIRCUIT