8-BIT SERIAL TO PARALLEL CONVERTER

■ GENERAL DESCRIPTION

The **NJU3712** is an 8-bit serial to parallel converter especially applying to MPU outport expander.

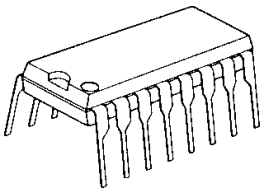
The effective outport assignment of MPU is available as the connection between **NJU3712** and MPU is required only 4 lines.

The serial data synchronizing with 5MHz or more clock can be input to the serial data input terminal and the data are output from parallel output buffer through serial in parallel out shift register and parallel data latches.

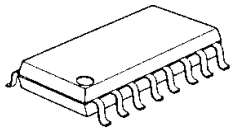
Furthermore, the **NJU3712** outputs the serial data from SO terminal through the shift register. Therefore, it connects with other SIPO ICs like as NJU3711 in cascade for expanding the parallel conversion outputs.

The hysteresis input circuit realizes wide noise margin and the high drive-ability output buffer (25mA) can drive LED directly.

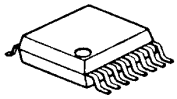
■ PACKAGE OUTLINE



NJU3712D



NJU3712M

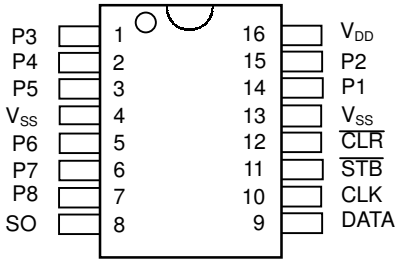


NJU3712V

■ FEATURES

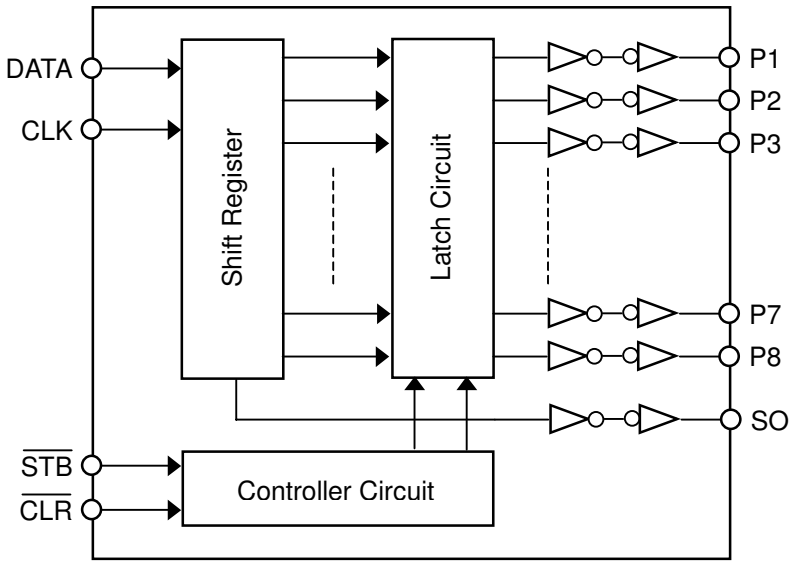
- 8-Bit Serial In Parallel Out
- Hysteresis Input 0.5V typ
- Operating Voltage 5V±10%
- Maximum Operating Frequency 5MHz and more
- Output Current 25mA
- C-MOS Technology
- Package Outline DIP16/DMP16/SSOP16

■ PIN CONFIGURATION



NJU3712D/M/V

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	FUNCTION
1	P3	O	Parallel Conversion Data Output Terminals
2	P4	O	
3	P5	O	
4	V_{SS}	-	GND
5	P6	O	Parallel Conversion Data Output Terminals
6	P7	O	
7	P8	O	
8	SO	O	Serial Data Output Terminal
9	DATA	I	Serial Data Input Terminal
10	CLK	I	Clock Signal Input Terminal
11	$\overline{STB}$	I	Strobe Signal Input Terminal
12	$\overline{CLR}$	I	Clear Signal Input Terminal
13	V_{SS}	-	GND
14	P1	O	Parallel Conversion Data Output Terminals
15	P2	O	
16	V_{DD}	-	Power Supply Terminal (4.5 to 5.5V)

■ FUNCTIONAL DESCRIPTION

(1) Reset

When the "L" level is input to the $\overline{CLR}$ terminal, all latches are reset and all of parallel conversion output are "L" level.

Normally, the $\overline{CLR}$ terminal should be "H" level.

(2) Data Transmission

In the $\overline{STB}$ terminal is "H" level and the clock signals are inputted to the CLK terminal, the serial data into the DATA terminal are shifted in the shift register synchronizing at a rising edge of the clock signal.

When the $\overline{STB}$ terminal is changed to "L" level, the data in the shift register are transferred to the latches.

Even if the $\overline{STB}$ terminal is "L" level, the input clock signal shifts the data in the shift register, therefore, the clock signal should be controlled for data order.

(3) Cascade Connection

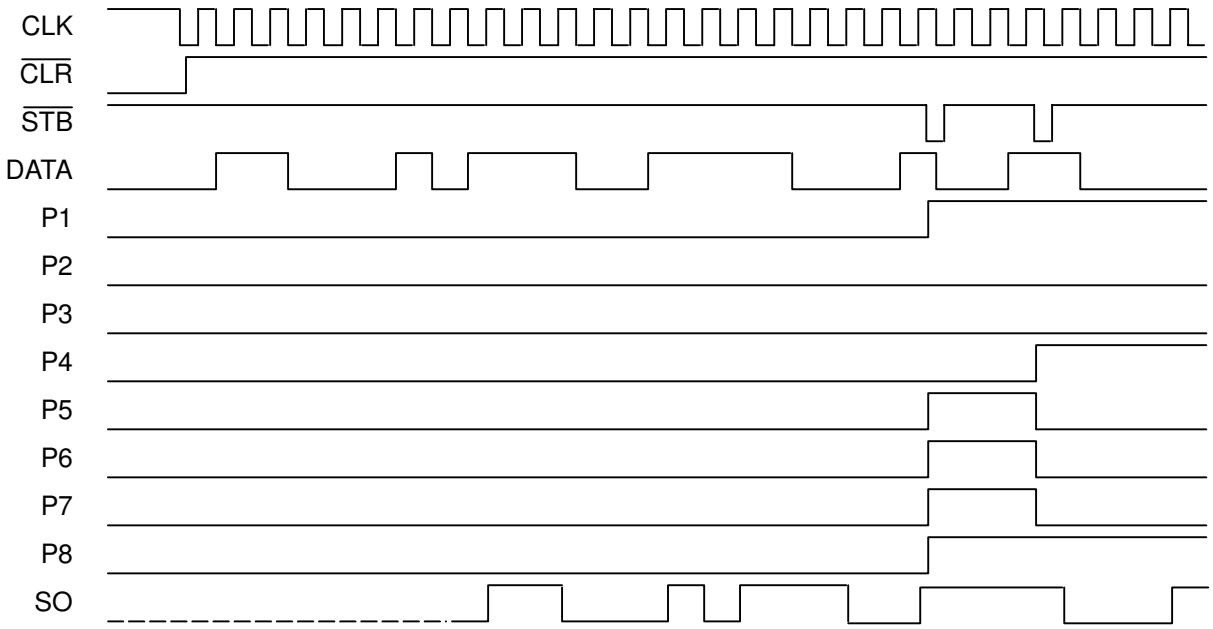
The serial data input from DATA terminal is output from the SO terminal through internal shift register unrelated with the $\overline{CLR}$ and $\overline{STB}$ status.

Furthermore, the 4 input circuits provide a hysteresis characteristics using the schmitt trigger structure to protect the noise.

CLK	$\overline{STB}$	$\overline{CLR}$	OPERATION
X	X	L	All of latches are reset (the data in the shift register is no change). All of parallel conversion outputs are "L".
↑	H	H	The serial data into the DATA terminal are inputted to the shift register. In this stage, the data in the latch is not changed.
L	L	H	The data in the shift register is transferred to the latch. And the data in the latch is output from the parallel conversion output terminals.
H			
↑			When the clock signal is inputted into the CLK terminal in state of the $\overline{STB}$="L" and $\overline{CLR}$="H", the data is shifted in the shift register and latched data is also changed in accordance with the shift register.

Note 1) X: Don't care

■ TIMING CHART



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS		UNIT
Supply Voltage Range	V_{DD}	-0.5 ~ +7.0		V
Input Voltage Range	V_I	V_{SS}-0.5 ~ V_{DD}+0.5		V
Output Voltage Range	V_O	V_{SS}-0.5 ~ V_{DD}+0.5		V
Output Current	I_O	±25		mA
Output Short Current (SO Terminal) (Note 5)	I_{OS}	V_O=7V, V_I=0V	10 (max)	mA
		V_O=0V, V_I=7V	-10 (max)	
Output Short Current (P1~P8 Terminals) (Note 5)	I_{OSD}	V_O=7V, V_I=0V	20 (max)	mA
		V_O=0V, V_I=7V	-20 (max)	
Power Dissipation	P_D	700 (DIP) 300 (DMP) 300 (SSOP)		mW
Operating Temperature Range	Topr	-25 ~ +85		°C
Storage Temperature Range	Tstg	-65 ~+150		°C

Note 2) All voltage are relative to V_{SS}=0V reference.

Note 3) Do not exceed the absolute maximum ratings, otherwise the stress may cause a permanent damage to the IC. It is also recommended that the IC be used in the range specified in the DC electrical characteristics, or the electrical stress may cause malfunctions and impact on the reliability.

Note 4) To stabilize the IC operation, place decoupling capacitor between V_{DD} and V_{SS}.

Note 5) V_{DD}=7V, V_{SS}=0V, less than 1 second per pin.

■ DC ELECTRICAL CHARACTERISTICS

(V_{DD}=4.5~5.5V, V_{SS}=0V, Ta=25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}			4.5	-	5.5	V
Operating Current	I_{DDS}	V_{IH}=V_{DD}, V_{IL}=V_{SS}		-	-	0.1	mA
High-level Output Voltage	V_{OH}	I_{OH}=-0.4mA	SO Terminal	4.0	-	V_{DD}	V
Low-level Output Voltage	V_{OL}	I_{OL}=+3.2mA		V_{SS}	-	0.4	V
High-level Input Voltage	V_{IH}			0.7V_{DD}	-	V_{DD}	V
Low-level Input Voltage	V_{IL}			V_{SS}	-	0.3V_{DD}	V
Input Leakage Current	I_{LI}	V_I=0~V_{DD}		-10	-	10	µA
High-level Output Voltage (Note 6)	V_{OHD}	I_{OH}=-25mA	P1~P8 Terminals	V_{DD}-1.5	-	V_{DD}	V
		I_{OH}=-15mA		V_{DD}-1.0	-	V_{DD}	
		I_{OH}=-10mA		V_{DD}-0.5	-	V_{DD}	
Low-level Output Voltage (Note 6)	V_{OLD}	I_{OL}=+25mA	P1~P8 Terminals	V_{SS}	-	1.5	V
		I_{OL}=+15mA		V_{SS}	-	0.8	
		I_{OL}=+10mA		V_{SS}	-	0.4	

Note 6) Specified value represent output current per pin. When use, total current consideration and less than power dissipation in rating operation should be required.

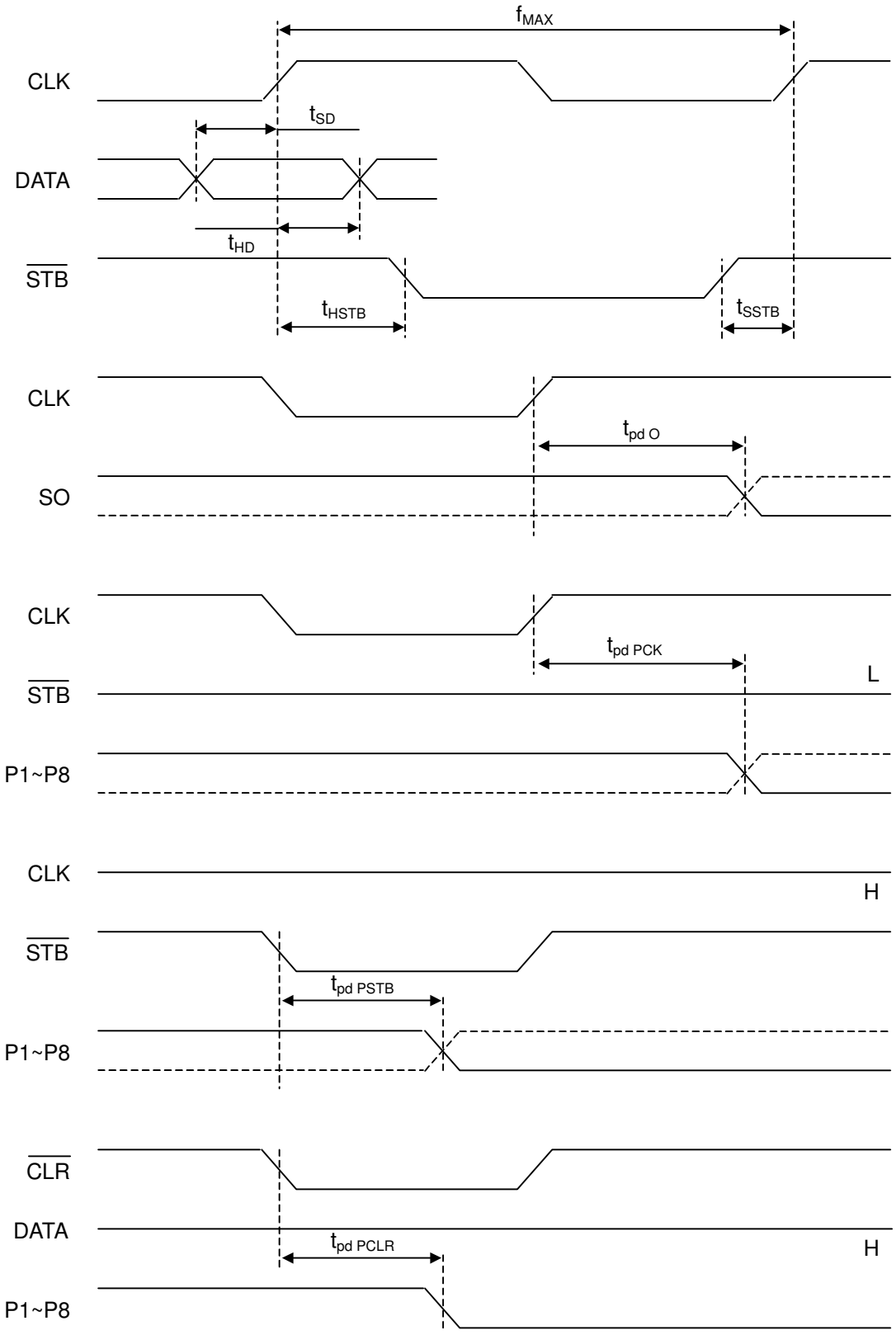
■ SWITCHING CHARACTERISTICS

(V_{DD}=4.5~5.5V, V_{SS}=0V, Ta=25°C, unless otherwise noted)

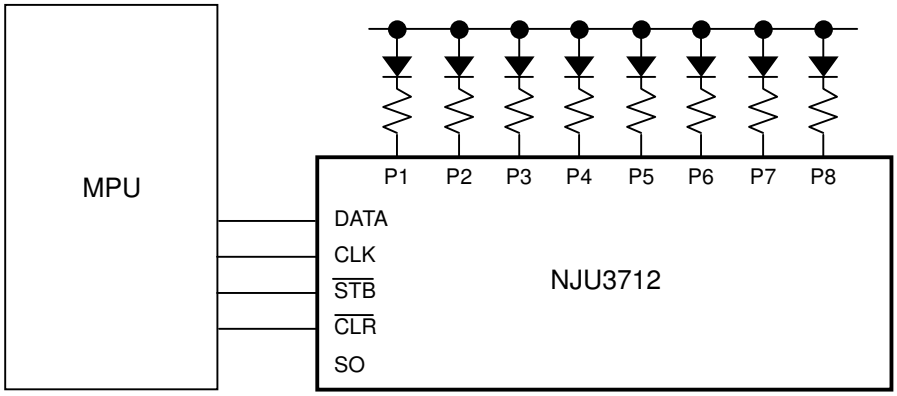
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Set-Up Time	t_{SD}	DATA-CLK	20	-	-	ns
Hold Time	t_{HD}	CLK-DATA	20	-	-	ns
Set-Up Time	t_{SSTB}	$\overline{STB}$-CLK	30	-	-	ns
Hold Time	t_{HSTB}	CLK-$\overline{STB}$	30	-	-	ns
Output Delay Time	$t_{pd\ O}$	CLK-SO	-	-	70	ns
	$t_{pd\ PCK}$	CLK-P1~P8	-	-	100	ns
	$t_{pd\ PSTB}$	$\overline{STB}$-P1~P8	-	-	80	ns
	$t_{pd\ PCLR}$	$\overline{CLR}$-P1~P8	-	-	80	ns
Maximum Operating Frequency	f_{MAX}		5	-	-	MHz

Note 7) C_{OUT}=50pF

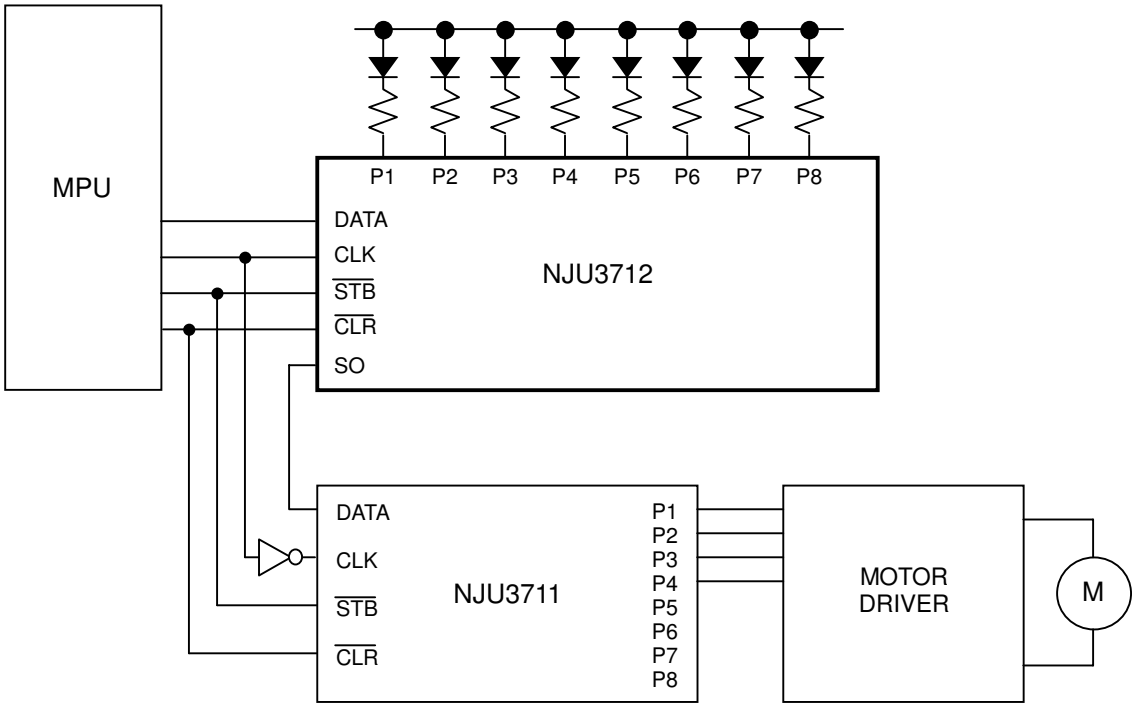
■ SWITCHING CHARACTERISTICS TEST WAVEFORM



■ APPLICATION CIRCUIT (1)



■ APPLICATION CIRCUIT (2) (Combined with NJU3711)



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