

ASSP
BIPOLAR

SWITCHING REGULATOR CONTROLLER

MB3775

■ LOW VOLTAGE DUAL PWM SWITCHING REGULATOR CONTROLLER

The MB3775 is a dual pulse-width-modulation control circuit. It contains the basic circuits required for two PWM control circuits. Complete synchronization is obtained by using the same oscillator output waveform. This IC can provide following types of output voltage: step down, step up, and inverter. Power consumption is low, thus the MB3775 is ideal for use in high-efficiency portable equipment.

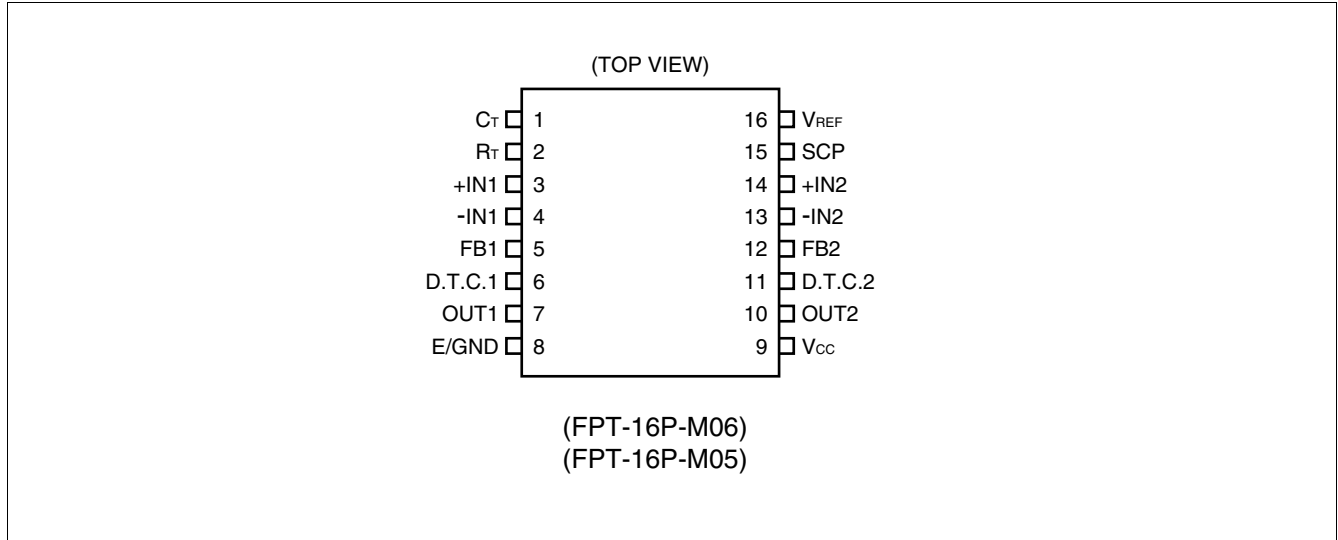
■ FEATURES

- Wide supply voltage range: 3.6 V to 18 V
- Low current consumption: 1.3 mA typical
- Wide oscillation frequency range: 1 kHz to 500 kHz
- On-chip timer latch short protection circuit
- On-chip under voltage lockout protection
- On-chip reference voltage: 1.28 V
- Variable dead time provides control over total operating range.
- Two types of packages (SOP-16pin : 1 type, SSOP-16pin : 1 type)

■ APPLICATIONS

- LCD monitor/panel
- Surveillance camera etc.

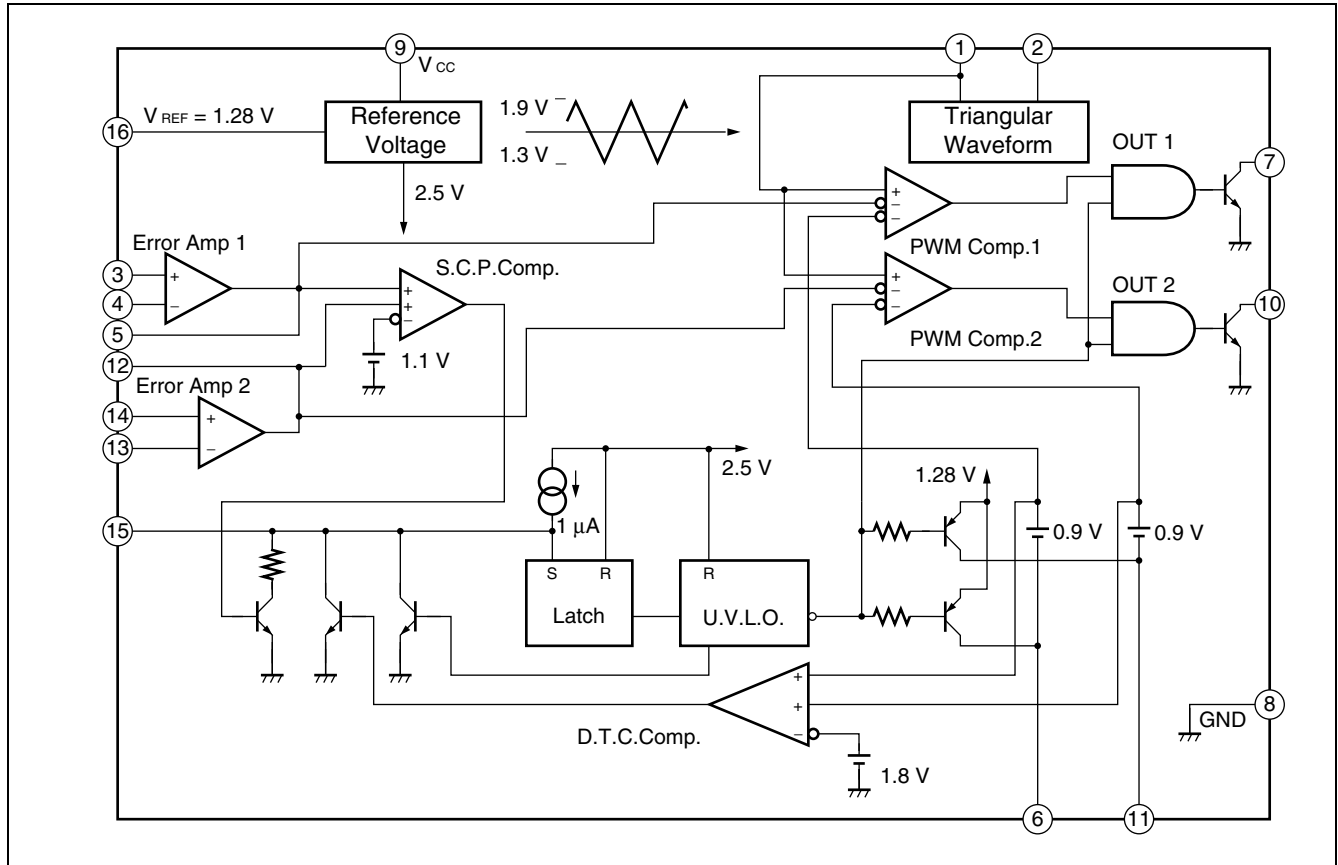
■ PIN ASSIGNMENT



■ PIN DESCRIPTION

No.	Pin	Function
1	C _T	Oscillator timing capacitor pin (150 pF to 15,000 pF) .
2	R _T	Oscillator timing resistor pin (5.1 kΩ to 100 kΩ) .
3	+IN1	Error amplifier 1 non-inverted input pin.
4	-IN1	Error amplifier 1 inverted input pin.
5	FB1	Error amplifier 1 output pin. A resistor and a capacitor are connected between this pin and the -IN1 pin to adjust gain and frequency.
6	DTC1	OUT1 dead-time control pin. Dead-time control is adjusted by an external resistive divider connected to the V _{REF} pin. A capacitor connected between this pin and GND enables soft-start operation.
7	OUT1	Open collector output pin. Output transistor has common ground independent of signal ground. This output can source or sink up to 50 mA.
8	E/GND	Ground pin.
9	V _{CC}	Power supply pin (3.6 V to 18 V)
10	OUT2	Open collector output pin. Output transistor has common ground independent of signal ground. This output can source or sink up to 50 mA.
11	DTC2	Sets the dead-time of OUT2. The use of this pin is the same as that of DTC1.
12	FB2	Error amplifier 2 output pin. A resistor and a capacitor are connected between this pin and the -IN2 pin to adjust gain and frequency.
13	-IN2	Error amplifier 2 inverted input pin.
14	+ IN2	Error amplifier 2 non-inverted input pin.
15	SCP	The time constant setting capacitor connection pin of the timer latch short-circuit protection circuit. Connects a capacitor between this pin and GND. For details, see “■ HOW TO SET TIME CONSTANT FOR TIMER LATCH SHORT-CIRCUIT PROTECTION CIRCUIT”.
16	V _{REF}	1.28 V reference voltage output pin which can be obtained up to 1 mA. This pin is used to set the reference input and idle period of the error amplifiers.

■ BLOCK DIAGRAM



■ OPERATION DESCRIPTION

1. Reference voltage

The reference voltage circuit generates a stable, temperature-compensated 2.5 V reference from V_{CC} pin (pin 9) for use by internal circuits.

A reference voltage of temperature compensated 1/2 V_{REF} can be obtained to external circuit by V_{REF} pin (pin 16).

2. Oscillator

A triangular waveform of any frequency is obtained by connecting an external capacitor and resistor to the C_T pin (pin 1) and R_T pin (pin 2).

The amplitude of this waveform is from 1.3 V to 1.9 V. The oscillator is internally connected to the non-inverting inputs of the PWM comparators. The oscillator waveform is available at the C_T pin (pin 1).

3. Error amplifiers

The error amplifier detects the output voltage of the switching regulator.

The common-mode input voltage range is -0.2 V to 1.45 V, so the input reference voltage can be set the V_{REF} pin (pin 16) and GND pin levels. Error amplifiers can be used as either inverting and non-inverting amplifiers.

The voltage gain is fixed. Phase compensation is possible by connecting a capacitor to the FB pins (pins 5 and 12) of the error amplifiers.

The error amplifier output are internally connected to the inverting inputs of the PWM comparators and also to the short protection circuit.

4. Timer latch short protection circuit

The timer latch short protection circuit detects the output levels of the error amplifiers. If one or both error amplifier outputs are 1.1 V or lower, the timer circuit begins charging the externally connected protection enable capacitor. If the output level of the error amplifier does not drop below the normal voltage range before the capacitor voltage reaches the transistor base-emitter voltage V_{BE} (\approx 0.65 V), the latch circuit turns the output drive transistor off and sets the dead time to 100 %.

5. Under voltage lockout protection circuit

An ambiguous transition state at power-on or a momentary fluctuation in the supply line may result in loss of control and may adversely affect or even destroy the system. The under voltage lockout protection circuit compares the internal reference voltage level with the supply voltage level. If the supply voltage level falls below the reference level the latch circuit is reset the output drive transistor is turned off and the dead time is set to 100%. The protection enable pin (pin 15) is pulled "Low".

6. PWM comparator

Each PWM comparator has two inverting inputs and one non-inverting input. This voltage-to-pulse-width converter controls the output pulse width according to the input voltage.

The PWM comparator turns the output drive transistor on when the oscillator triangular waveform is higher than the error amplifier output and the dead time control pin voltage.

7. Output drive transistor

The open-collector output-drive transistors provide common-emitter output of 18 V dielectric capability. The output drive transistors can source up to 50 mA of drive current to the switching power transistor.

■ ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power Supply Voltage	V _{CC}	—	—	20	V
Error Amp Input Voltage	V _I	—	-0.3	+10	V
Collector Output Voltage	V _O	—	—	20	V
Collector Output Current	I _O	—	—	75	mA
Power Dissipation	P _D	T _a ≤ +25 °C(SOP)	—	*620	mW
		T _a ≤ +25 °C(SSOP)	—	*430	mW
Operating Ambient Temperature	T _a	—	-30	+85	°C
Storage temperature	T _{stg}	—	-55	+125	°C

*: The packages are mounted on the epoxy board (4 cm x 4 cm x 1.5 mm).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V _{CC}	3.6	6.0	18	V
Error Amp Input Voltage	V _I	-0.2	—	+1.45	V
Collector Output Voltage	V _O	—	—	18	V
Collector Output Current	I _O	0.3	—	50	mA
Phase Compensation Capacitor	C _P	—	0.1	—	μF
Timing Capacitor	C _T	150	—	15000	pF
Timing Resistor	R _T	5.1	—	100	kΩ
Oscillator Frequency	f _{OSC}	1	—	500	kHz
Reference Voltage Output Current	I _{REF}	-3	-1	—	mA
Operating Ambient Temperature	T _a	-30	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Ta = +25 °C, VCC = 6 V)

Parameter	Condition	Symbol	Value			Unit	
			Min	Typ	Max		
Reference Section	Output Voltage	I _{OR} = -1 mA	V _{REF}	1.26	1.28	1.30	V
	Output Temp. Stability	Ta = -30 °C to +85 °C	V _{RTC}	-2	±0.2	+2	%
	Input Stability	VCC = 3.6 V to 18 V	Line	—	2	10	mV
	Load Stability	I _{OR} = -0.1 mA to -1 mA	Load	—	1	7.5	mV
	Short Circuit Output Current	V _{REF} = 0 V	I _{OS}	—	-30	-10	mA
Under Voltage Lockout Protection Section	Threshold Voltage	I _{OR} = -0.1 mA	V _{tH}	—	2.72	—	V
		I _{OR} = -0.1 mA	V _{tL}	—	2.60	—	V
	Hysteresis Width	I _{OR} = -0.1 mA	V _{HYS}	80	120	—	mV
	Reset Voltage (V _{CC})	—	V _R	1.5	1.9	—	V
Protection Circuit Section	Input Threshold Voltage	—	V _{tPC}	0.60	0.65	0.7	V
	Input Stand by Voltage	No pull up	V _{STB}	—	50	100	mV
	Input Latch Voltage	No pull up	V _I	—	50	100	mV
	Input Source Current	—	I _{bpc}	-1.4	-1.0	-0.6	μA
	Comparator Threshold Voltage	Pin 5, Pin 12	V _{tC}	—	1.1	—	V
Triangular Waveform Oscillator Section	Oscillator Frequency	C _T = 330 pF, R _T = 15 kΩ	f _{osc}	—	200	—	kHz
	Frequency Deviation	C _T = 330 pF, R _T = 15 kΩ	f _{dev}	—	10	—	%
	Frequency Stability (V _{CC})	VCC = 3.6 V to 18 V	f _{dV}	—	1	—	%
	Frequency Stability (Ta)	Ta = -30 °C to +85 °C	f _{dT}	-4	—	+4	%
Dead-Time Control Section	Input Threshold Voltage (f _{osc} = 10 kHz)	Duty Cycle = 0 %	V _{t0}	—	1.0	V _{REF} - 0.15	V
		Duty Cycle = 100 %	V _{t100}	0.2	0.4	—	V
	Input Bias Current	—	I _{bdt}	—	-0.2	-1	μA
	Latch Mode Source Current	V _{dt} = 0.7 V	I _{dt}	—	-150	-80	μA
	Latch Input Voltage	I _{dt} = -40 μA	V _{dt}	V _{REF} - 0.1	—	—	V

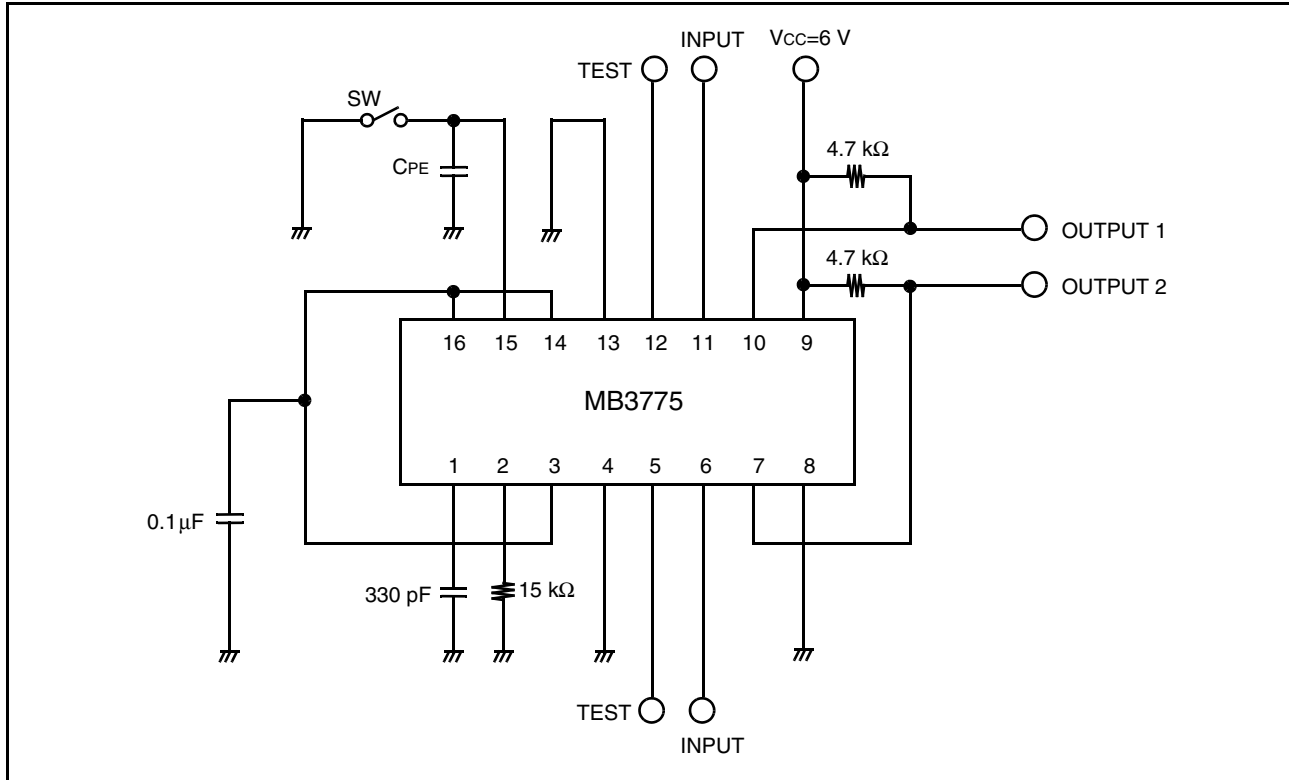
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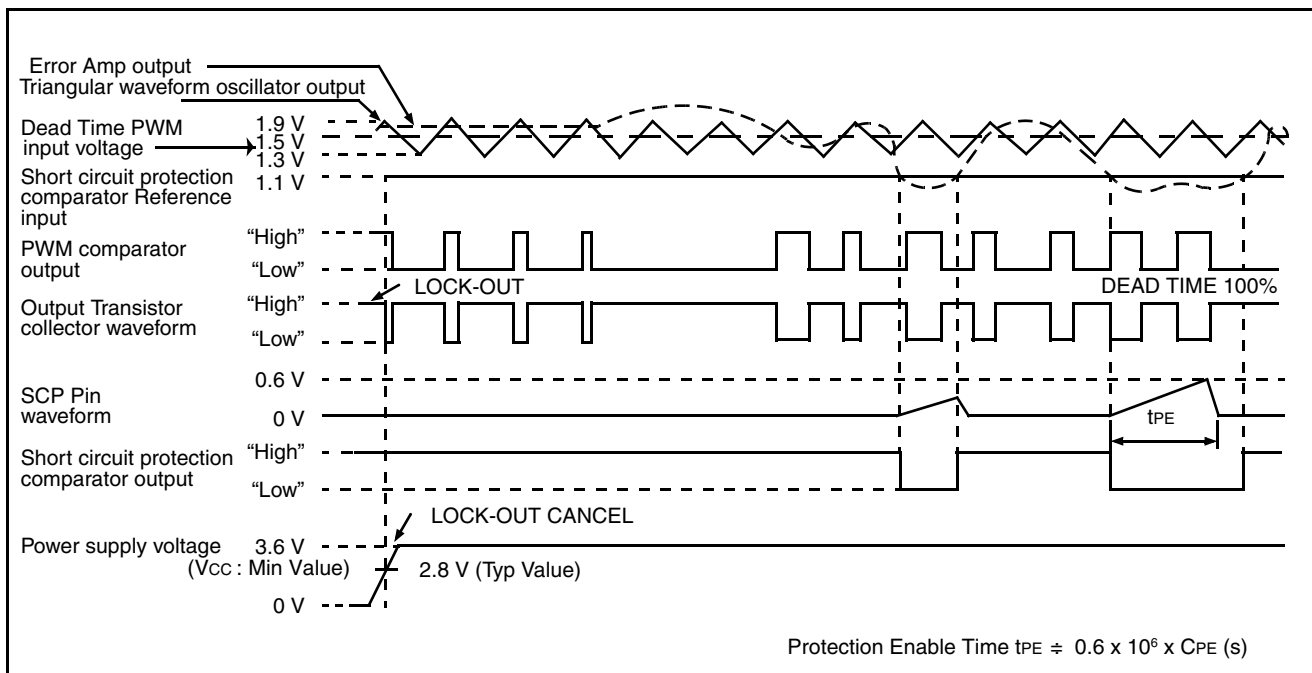
(Ta = +25 °C, VCC = 6 V)

Parameter	Condition	Symbol	Value			Unit	
			Min	Typ	Max		
Error Amp Section	Input Offset Voltage	Vo = 1.6 V	V _{IO}	-10	—	+10	mV
	Input Offset Current	Vo = 1.6 V	I _{IO}	-100	—	+100	nA
	Input Bias Current	Vo = 1.6 V	I _B	-500	-100	—	nA
	Common Mode Input Voltage Range	VCC = 3.6 V to 18 V	V _{ICR}	-0.2	—	+1.45	V
	Voltage Gain		A _v	84	120	—	V/V
	Frequency Band Width	A _v = -3 dB	BW	—	3	—	MHz
	Common Mode Rejection Ratio		CMRR	60	80	—	dB
	Max Output Voltage Width		V _{OM+}	2.2	2.4	—	V
			V _{OM-}	-	0.7	0.9	V
	Output Sink Current	Vo = 1.6 V	I _{OM+}	24	50	—	μA
Output Source Current	Vo = 1.6 V	I _{OM-}	—	-1.2	-0.7	mA	
PWM Com-parator Section	Input Threshold Voltage (fosc=10 kHz)	Duty Cycle = 0 %	V _{t0}	—	1.9	2.1	V
		Duty Cycle = 100 %	V _{t100}	1.05	1.3	—	V
	Input Sink Current	Pin 5, Pin 12 = 1.6 V	I _{IN+}	24	50	—	μA
	Input Source Current	Pin 5, Pin 12 = 1.6 V	I _{IN-}	—	-1.2	-0.7	mA
Output Section	Output Leak Current	Vo = 18 V	Leak	—	—	10	μA
	Output Saturation Voltage	I _o = 50 mA	V _{SAT}	—	1.1	1.4	V
Stand by Current	Output "OFF"	I _{CCS}	—	1.3	1.8	mA	
Average Supply Current	R _T = 15 kΩ	I _{CCa}	—	1.7	2.4	mA	

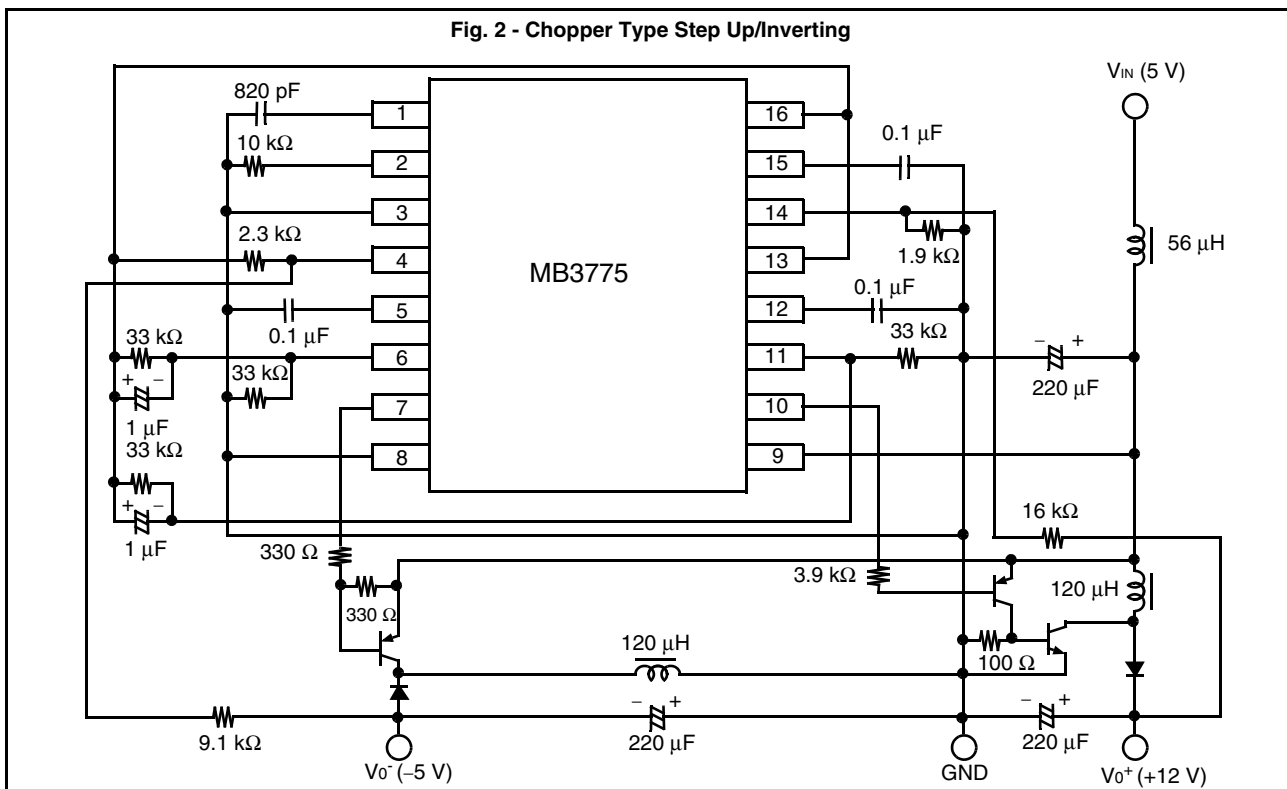
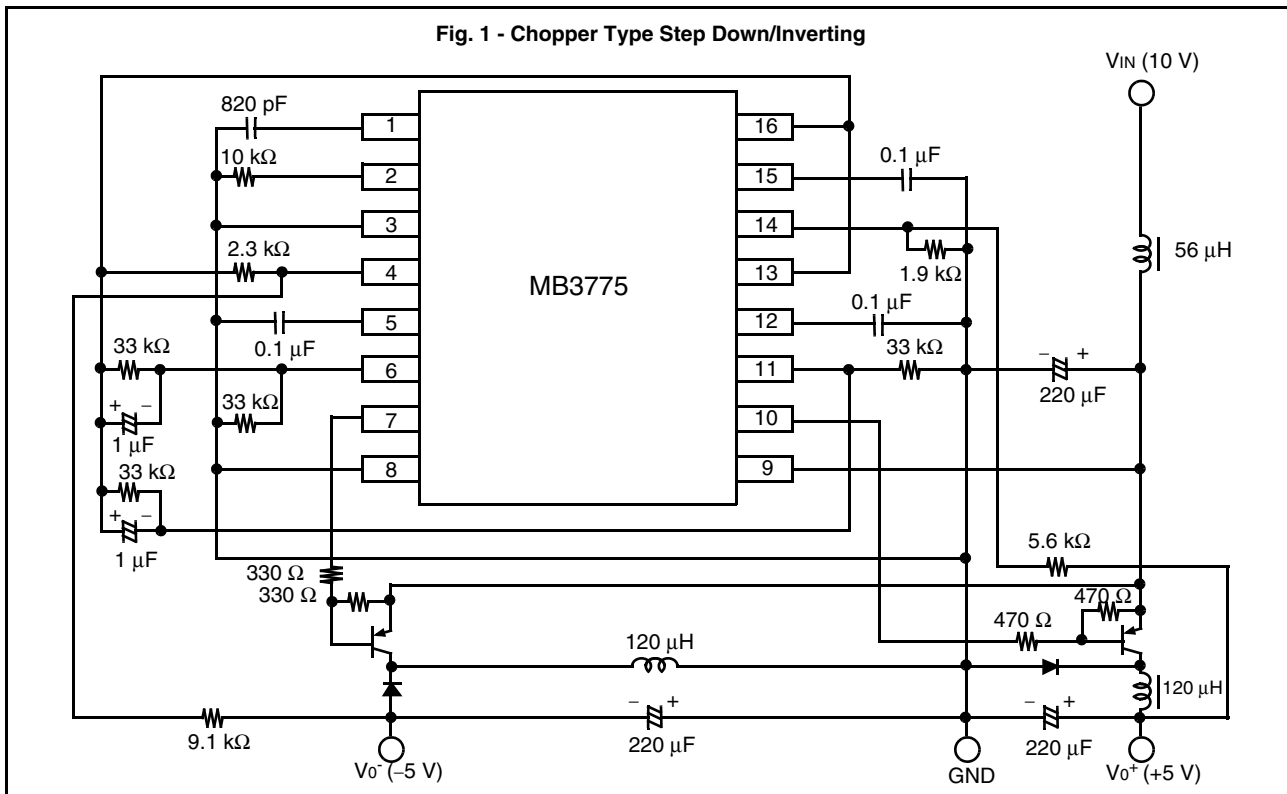
TEST CIRCUIT



TIMING CHART (Internal Waveform)

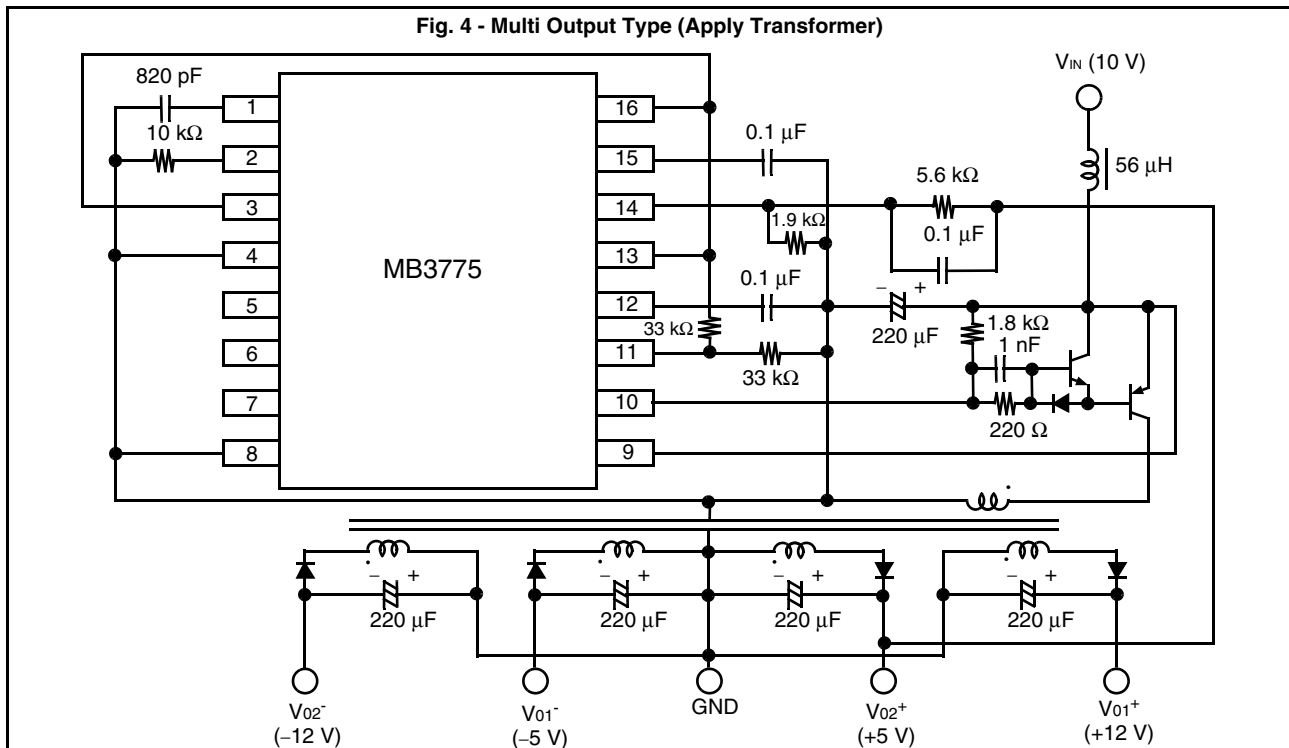
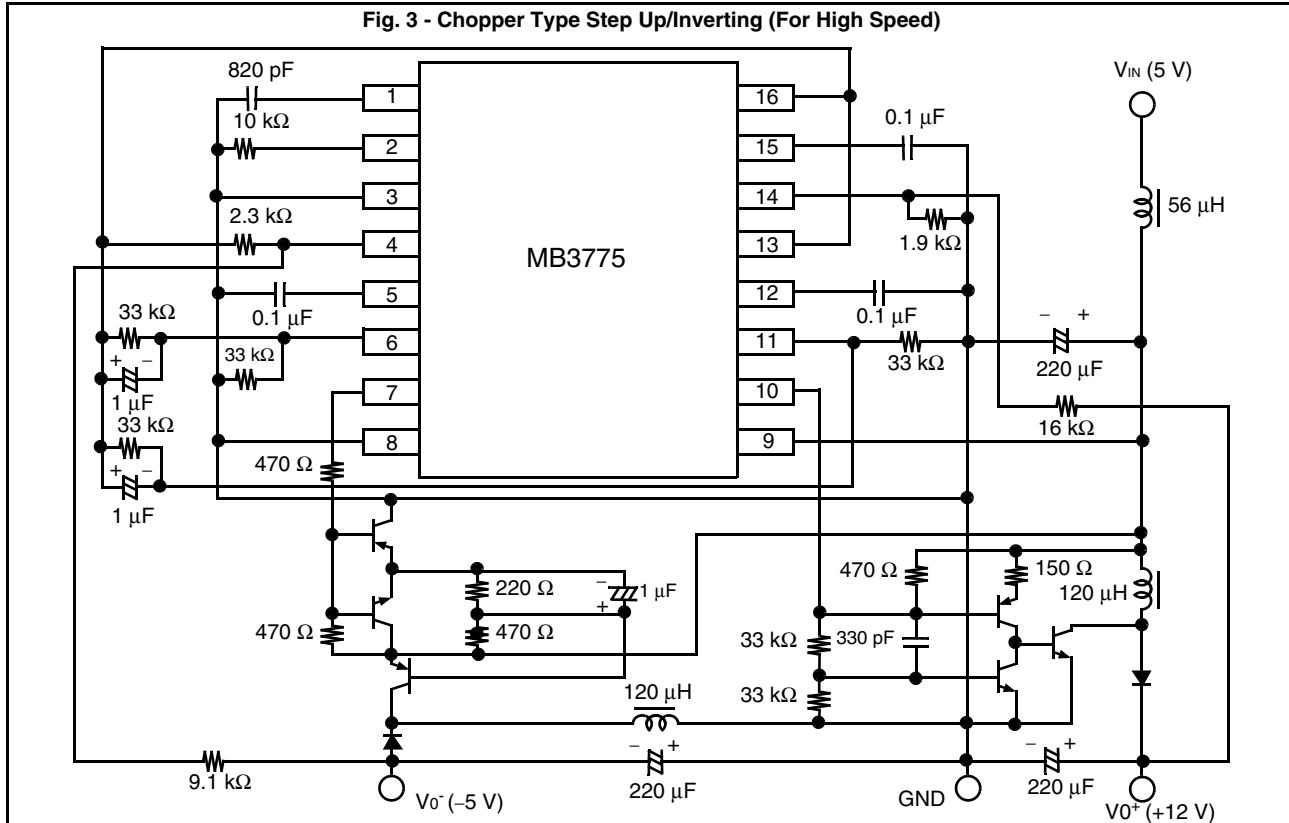


APPLICATION CIRCUIT



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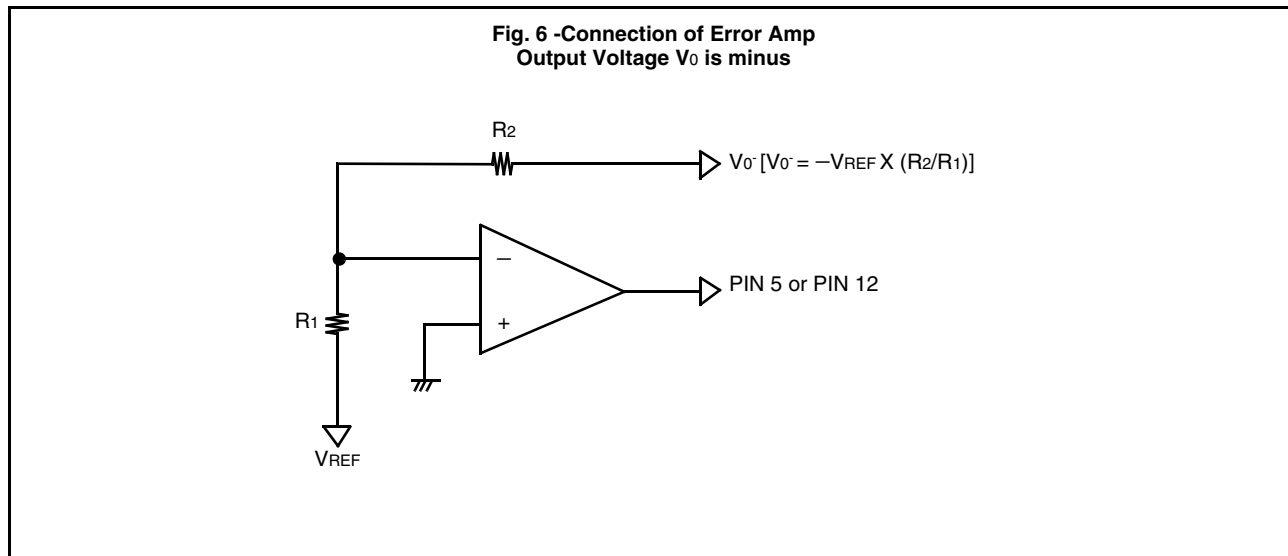
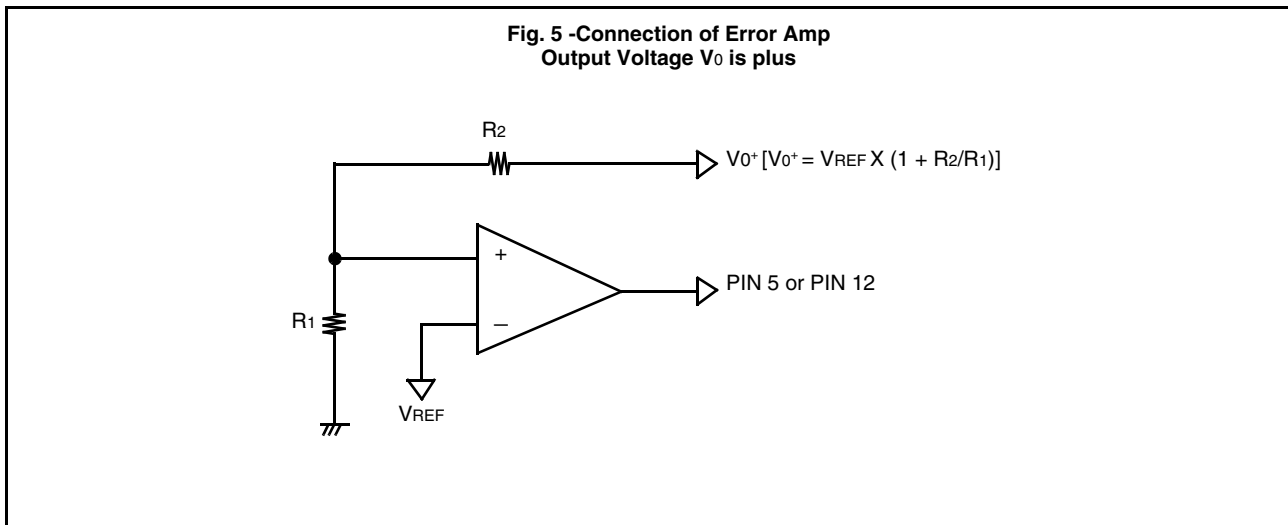


■ HOW TO SET OUTPUT VOLTAGE

The output voltage is set using the connection shown in Fig. 5 and 6.

The error amplifiers are supplied to the internal reference voltage circuit as are the other internal circuits. The common-mode input voltage range is from -0.2 V to $+1.45\text{ V}$.

When the amplifiers are operated non-inverting, tie the inverting pin to V_{REF} ($\approx 1.28\text{ V}$). When the amplifiers are operated inverting, tie the non-inverting pin to ground.



■ HOW TO SET TIME CONSTANT FOR TIMER LATCH SHORT PROTECTION CIRCUIT

TIMING CHART shows the configuration of the protection latch circuit.

Error amplifier outputs, are internally connected to the non-inverting inputs of the short-circuit protection comparator and are compared with the reference voltage (1.1 V) connected to the inverting input.

When the load condition of the switching regulator is stable, the error amplifier has no output fluctuation. Thus, short-circuit protection control is also kept in balance, and the protection enable pin (pin 15) voltage is kept at about 50 mV.

If the load condition drastically changes due to a load short-circuit and if low-level signals (1.1 V or lower) are input to the non-inverting inputs of the short-circuit protection comparator from the error amplifiers, the short-circuit protection comparator outputs a “Low” level to turn transistor Q₁ off. The protection enable pin voltage is discharged, and then the short-circuit protection comparator charges the externally connected protection enable capacitor C_{PE} according to the following formula:

$$V_{PE} = 50 \text{ mV} + t_{PE} \times 10^{-6} / C_{PE}$$

$$0.65 = 50 \text{ mV} + t_{PE} \times 10^{-6} / C_{PE}$$

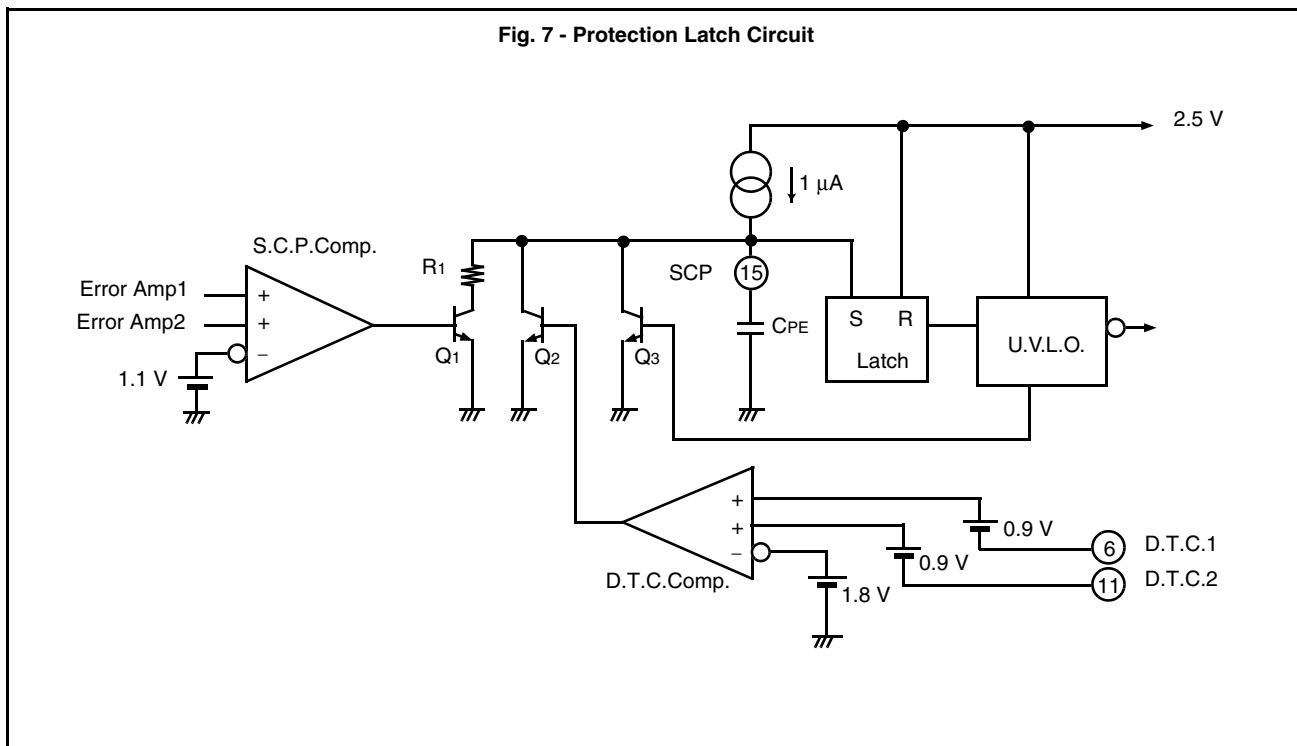
$$C_{PE} = t_{PE} / 0.6 \text{ (}\mu\text{F)}$$

When the protection enable capacitor charges to about 0.65 V, the protection latch is set to enable the under voltage lockout protection circuit and to turn the output drive transistor off. The dead time is set to 100 %.

Once the under voltage lockout protection circuit is enabled, the protection enable is released; however, the protection latch is not reset if the power is not turned off.

The non-inverting inputs of the D.T.C. comparator are connected to the D.T.C. pins (pins 6 and 11) through the power supply (about 0.9 V) and are compared with a reference voltage (about 1.8 V) connected to the inverting input.

To prevent malfunction of the short protection circuit in soft-start mode (using D.T.C. pins), the D.T.C. comparator outputs a “High” level to turn Q₂ on until the D.T.C. pins (pins 6 and 11) voltage drops to about 0.9 V.



■ SETTING THE IDLE PERIOD

When voltage step-up, fly-back step-up or inverted output are set, the voltage at the FB pin may go lower than the triangular wave voltage due to load fluctuation, etc. In this case the output transistor will be in full-on state (ON duty 100%). This can be prevented by setting the maximum duty for the output transistor. This is done by setting the DTC1 pin (pin 6) voltage using resistance division of the V_{REF} voltage as illustrated below.

When the DTC1 pin voltage is lower than the triangular waveform voltage, the output transistor is turned on. If the triangular waveform amplitude ≈ 0.6 V, the lower limit voltage of the triangular waveform ≈ 1.3 V and the offset voltage is 0.9 V, the formula for the maximum duty would be as follows (Other channels are this conditions) :

$$\text{Duty (ON) Max (\%)} \approx \frac{1.9 \text{ V} - (V_{dt} + 0.9 \text{ V})}{0.6 \text{ V}} \times 100 \approx \frac{1.0 \text{ V} - V_{dt}}{0.6 \text{ V}} \times 100, \quad V_{dt} (\text{V}) = \frac{R_b}{(R_a + R_b)} \times V_{REF}$$

Also, if no output duty setting is required, the voltage should be set greater than the lower limit voltage of the triangular waveform, which is 1.3 V ($V_{dt} = 0.4$ V).

- Setting the idle time at DTC1 (DTC2 is similar)

