FUJITSU MICROELECTRONICS
DATA SHEET

DS07-13751-2E

16-bit Microcontroller

CMOS

F²MC-16LX MB90820B Series

MB90822B/823B/F822B/F823B/F828B/V820B

■ DESCRIPTION

The MB90820B series is a line of general-purpose, Fujitsu 16-bit microcontrollers designed for process control applications which require high-speed real-time processing, such as consumer products.
While inheriting the AT architecture of the F²MC family, the instruction set for the F²MC-16LX CPU core of the MB90820B series incorporates additional instructions for high-level languages, supports extended addressing modes, and contains enhanced multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions. In addition, the MB90820B series has an on-chip 32-bit accumulator which enables processing of long-word data.
The peripheral resources integrated in the MB90820B series include : an 8/10-bit A/D converter, 8-bit D/A converters, UARTs (SCI) 0, 1, multi-functional timer (16-bit free-run timer, input capture units (ICUs) 0 to 3, output compare units (OCUs) 0 to 5, 16-bit PPG timer 0, waveform generator), 16-bit PPG timer 1, 2, PWC 0, 1, 16-bit reload timer 0, 1 and DTP/external interrupt.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- Minimum execution time of instruction : 42 ns / 4 MHz oscillation (uses PLL clock multiplication) maximum multiplier = 6
- Maximum memory space 16 M bytes, Linear/bank access
- Instruction set optimized for controller applications
  Supported data types : bit, byte, word, and long-word types
  Standard addressing modes : 23 types
  32-bit accumulator enhancing high-precision operations
  Signed multiplication/division instructions and enhanced RETI instructions

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For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

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- Enhanced high level language (C) and multi-tasking support instructions
  Use of a system stack pointer
  Symmetrical instruction set and barrel shift instructions
- Program patch function (for two address pointers)
- Increased execution speed : 4-byte instruction queue
- Powerful interrupt function
  Up to eight priority levels programmable
  External interrupt inputs : 8 channels
- Automatic data transmission function independent of CPU operation
  Up to 16 channels for the extended intelligent I/O service
  DTP request inputs : 8 channels
- Internal ROM
  Flash memory : 64 K/128 K bytes with flash security
  MASK ROM : 64 K/128 K bytes
- Internal RAM
  Evaluation product : 16 K bytes
  Flash memory : 4 K/8 K bytes
  MASK ROM : 4 K bytes
- General-purpose ports
  Up to 66 channels (ports where pull-up resistor can be configured : 32 channels)
- A/D Converter (RC) : 16 channels
  8/10-bit resolution selectable
  Conversion time : Min 3 µs (24 MHz operation, including sampling time)
- 8-bit D/A Converter : 2 channels
- UART : 2 channels
- 16-bit PPG timer : 3 channels
  Mode switching function provided (PWM mode or one-shot mode)
  ch.0 can be worked with multi-functional timer or independently
- 16-bit reload timer : 2 channels
- 16-bit PWC timer : 2 channels
- Clock supervisor
- Multi-functional timer
  Input capture : 4 channels
  Output compare with selectable buffer : 6 channels
  Free-run timer with up or up-down mode selection and selectable buffer: 1 channel
  16-bit PPG timer : 1 channel
  Waveform generator : (16-bit timer : 3 channels, 3-phase waveform or dead time)
- Time-base timer/watchdog timer : 18-bit
- Low-power consumption mode :
  Sleep mode
  Stop mode
  CPU intermittent operation mode
- Package :
  LQFP-80 (FPT-80P-M21 : 0.50 mm pitch)
  LQFP-80 (FPT-80P-M22 : 0.65 mm pitch)
  QFP-80 (FPT-80P-M06 : 0.80 mm pitch)
- CMOS technology

■ PRODUCT LINEUP

Item \ Part number	MB90V820B	MB90F822B	MB90F823B	MB90F828B	MB90822B	MB90823B
Classification	Evaluation product	Flash memory product with flash security			MASK ROM product	
ROM size	—	64 K bytes	128 K bytes	128 K bytes	64 K bytes	128 K bytes
RAM size	16 K bytes	4 K bytes		8 K bytes	4 K bytes	
CPU function	Number of instruction : 351 Minimum execution time : 42 ns / 4 MHz (PLL × 6) Addressing mode : 23 Data bit length : 1, 8, 16 bits Maximum memory space: 16 M bytes					
I/O port	I/O port (CMOS) : 66					
PWC	Pulse width counter timer : 2 channels Timer function (select the counter timer from three internal clocks) Various pulse width measuring function (“H” pulse width, “L” pulse width, rising edge to falling edge period, falling edge to rising edge period, rising edge to rising edge period and falling edge to falling edge period)					
UART	UART : 2 channels With full-duplex double buffer (8-bit length) Clock asynchronized or clock synchronized transmission (with start and stop bits) can be selected and used. Transmission can be one-to-one (bidirectional communication) or one-to-n (master-slave communication).					
16-bit reload timer	Reload timer : 2 channels Reload mode, single-shot mode or event count mode selectable					
16-bit PPG timer	PPG timer : 3 channels PWM mode or single-shot mode selectable Ch.0 can be worked with multi-functional timer or independently.					
Multi-functional timer (for AC/DC motor control)	16-bit free-run timer with up or up-down mode selection and buffer : 1 channel 16-bit output compare : 6 channels 16-bit input capture : 4 channels 16-bit PPG timer : 1 channel Waveform generator (16-bit timer : 3 channels, 3-phase waveform or dead time)					
8/10-bit A/D converter	8/10-bit resolution (16 channels) Conversion time : Min 3 µs (24 MHz internal clock, including sampling time)					
8-bit D/A converter	8-bit resolution (2 channels)					
DTP/External interrupt	8 independent channels Interrupt trigger : Rising edge, falling edge, “L” level or “H” level					
Clock supervisor	No			Yes	No	
Low-power consumption	Stop mode / Sleep mode / CPU intermittent operation mode					

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Item \ Part number	MB90V820B	MB90F822B	MB90F823B	MB90F828B	MB90822B	MB90823B
Package	PGA-299	LQFP-80 (FPT-80P-M21 : 0.50 mm pitch) LQFP-80 (FPT-80P-M22 : 0.65 mm pitch) QFP-80 (FPT-80P-M06 : 0.80 mm pitch)				
Power supply voltage for operation	4.5 V to 5.5 V*1	3.5 V to 5.5 V : Normal operation when A/D converter and D/A converter are not used 4.0 V to 5.5 V : Normal operation when D/A converter is not used 4.5 V to 5.5 V : Normal operation when A/D converter and D/A converter are used				
Process	CMOS					
Emulator power supply*2	Included	—				

*1 : MB90V820B is operating guaranteed temperature 0 °C to + 25 °C.

*2 : Configured by a jumper switch (TOOL VCC) when emulator (MB2147-01) is used.
Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply switching) about details.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB90V820B	MB90F822B	MB90F823B	MB90F828B	MB90822B	MB90823B
PGA-299	○	X	X	X	X	X
FPT-80P-M21	X	○	○	○	○	○
FPT-80P-M22	X	○	○	○	○	○
FPT-80P-M06	X	○	○	○	○	○

○ : Available
X : Not available

Note: For more information about each package, refer to “■ PACKAGE DIMENSIONS”.

■ DIFFERENCES AMONG PRODUCTS

Memory Size

In evaluation with an evaluation product, note the difference between the evaluation product and the product actually used. The following items must be taken into consideration.

- The MB90V820B does not have an internal ROM, however, operations equivalent to chips with an internal ROM can be evaluated by using a dedicated development tool, enabling selection of ROM size by settings of the development tool.
- In the MB90V820B, images from $FF8000_H$ to $FFFFFF_H$ are mapped to bank 00, and $FE0000_H$ to $FF7FFF_H$ are mapped to bank FE and bank FF only. (This setting can be changed by configuring the development tool.)
- In the MB90822B/F822B/F828B, images from $FF8000_H$ to $FFFFFF_H$ are mapped to bank 00, and $FF0000_H$ to $FF7FFF_H$ are mapped to bank FF only. In the MB90823B/F823B/F828B, images from $FF8000_H$ to $FFFFFF_H$ are mapped to bank 00, and $FE0000_H$ to $FF7FFF_H$ are mapped to bank FE and bank FF only.

Clock Supervisor Function

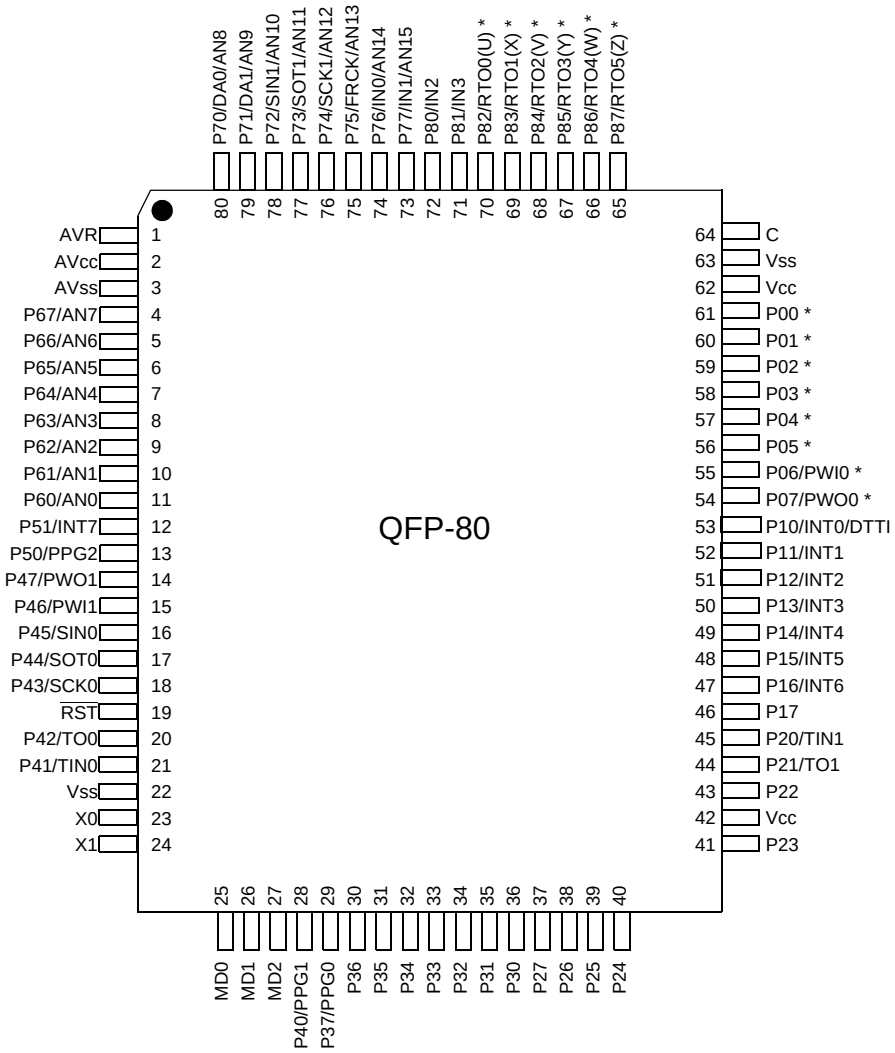
The clock supervisor is built-in in MB90F828B only. Note that the evaluation products and products actually used are different when evaluating evaluation products. Please contact the sales representatives for more information on evaluation of this function.

Modify ROM data

The registers include this function between $001FF0_H$ and $001FF5_H$ which overlap the RAM area of MB90F828B. Do not access to the RAM when using this function in MB90F282B.

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-80P-M06)

* : High current pin.

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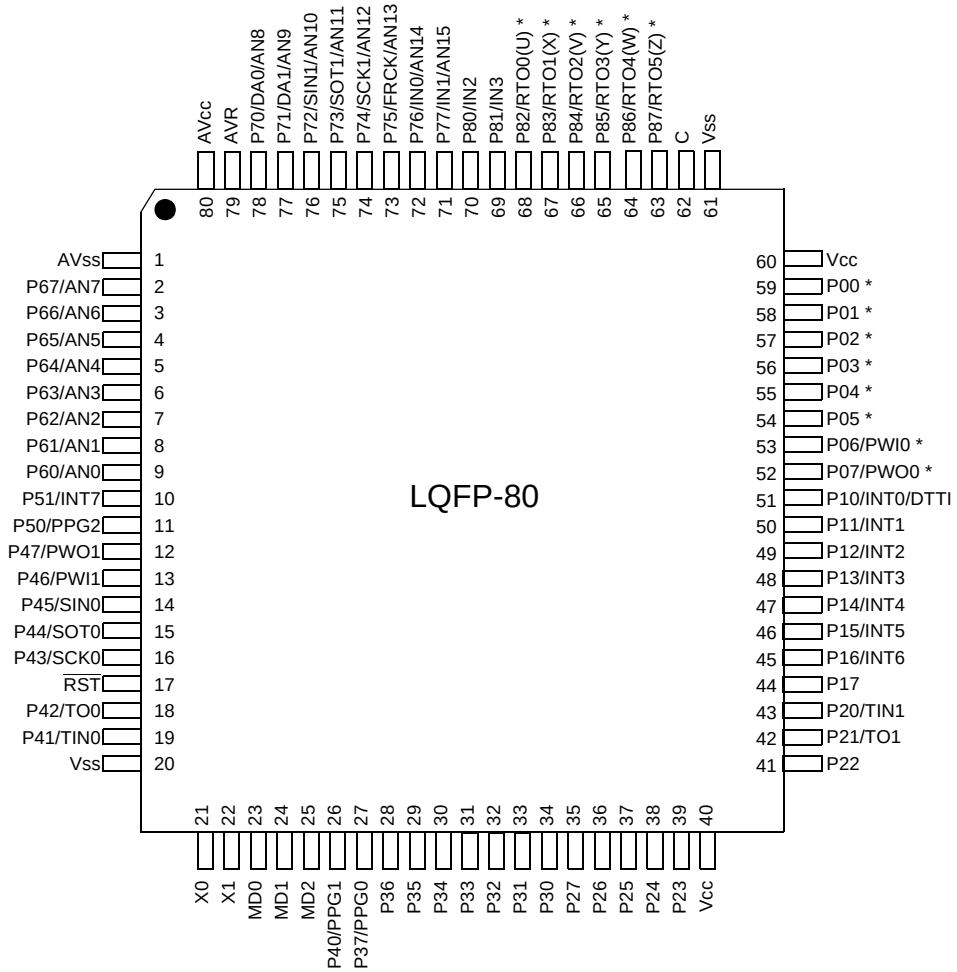
(TOP VIEW)



(FPT-80P-M22)
(FPT-80P-M21)

* : High current pin.

■ PIN DESCRIPTION

Pin no.		Pin name	I/O circuit *3	Pin status during reset	Function
LQFP *1	QFP *2				
21, 22	23, 24	X0,X1	A	Oscillating	Oscillation pins.
17	19	$\overline{RST}$	B	Reset input	External reset input pin.
59 to 54	61 to 56	P00 to P05	C	Port input	General-purpose I/O ports.
53	55	P06	C		General-purpose I/O port.
		PWI0			PWC ch.0 signal input pin.
52	54	P07	C		General-purpose I/O port.
		PWO0			PWC ch.0 signal output pin.
51	53	P10	D		General-purpose I/O port.
		INT0			External interrupt request input ch.0 pin.
		DTTI			RTO0 to RTO5 pins for fixed-level input. This function is enabled when the waveform generator specifies its input bits.
50 to 45	52 to 47	P11 to P16	D		General-purpose I/O ports.
		INT1 to INT6			External interrupt request input ch.1 to ch.6 pins.
44	46	P17	D		General-purpose I/O port.
43	45	P20	D		General-purpose I/O port.
		TIN1			External clock input pin for reload timer ch.1.
42	44	P21	D		General-purpose I/O port.
		TO1			Event output pin for reload timer ch.1.
41, 39 to 35	43, 41 to 37	P22 to P27	D		General-purpose I/O ports.
34 to 28	36 to 30	P30 to P36	E		General-purpose I/O ports.
27	29	P37	E		General-purpose I/O port.
		PPG0			Output pin for PPG timer ch.0.
26	28	P40	F		General-purpose I/O port.
		PPG1			Output pin for PPG timer ch.1.
19	21	P41	F		General-purpose I/O port.
		TIN0			External clock input pin for reload timer ch.0.
18	20	P42	F		General-purpose I/O port.
		TO0			Event output pin for reload timer ch.0.

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Pin no.		Pin name	I/O circuit *3	Pin status during reset	Function
LQFP *1	QFP *2				
16	18	P43	F	Port Input	General-purpose I/O port.
		SCK0			Serial clock I/O pin for UART ch.0.
15	17	P44	F		General-purpose I/O port.
		SOT0			Serial data output pin for UART ch.0.
14	16	P45	G		General-purpose I/O port.
		SIN0			Serial data input pin for UART ch.0.
13	15	P46	F		General-purpose I/O port.
		PWI1			PWC ch.1 signal input pin.
12	14	P47	F		General-purpose I/O port.
		PWO1			PWC ch.1 signal output pin.
11	13	P50	F		General-purpose I/O port.
		PPG2			Output pin for PPG timer ch.2.
10	12	P51	F		General-purpose I/O port.
		INT7			External interrupt request input ch.7 pin.
9 to 2	11 to 4	P60 to P67	H	Analog input	General-purpose I/O ports.
		AN0 to AN7			A/D converter analog input pins.
78, 77	80, 79	P70, P71	I		General-purpose I/O ports.
		DA0, DA1			D/A converter analog output pins.
		AN8, AN9			A/D converter analog input pins.
76	78	P72	J		General-purpose I/O port.
		SIN1			Serial data input pin for UART ch.1.
		AN10			A/D converter analog input pin.
75	77	P73	K		General-purpose I/O port.
		SOT1			Serial data output pin for UART ch.1.
		AN11			A/D converter analog input pin.
74	76	P74	K		General-purpose I/O port.
		SCK1			Serial clock I/O pin for UART ch.1.
		AN12			A/D converter analog input pin.
73	75	P75	K		General-purpose I/O port.
		FRCK			External clock input pin for free-run timer.
		AN13			A/D converter analog input pin.

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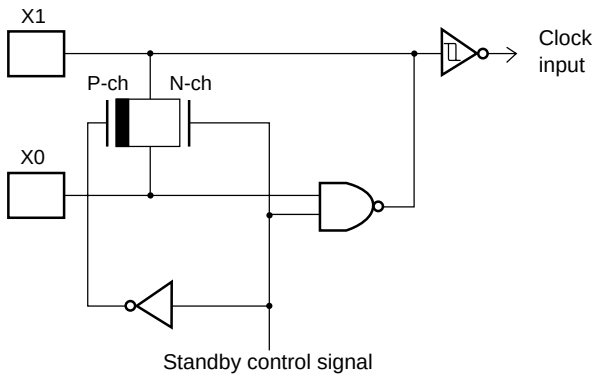
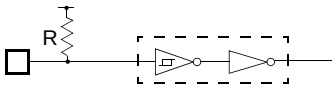
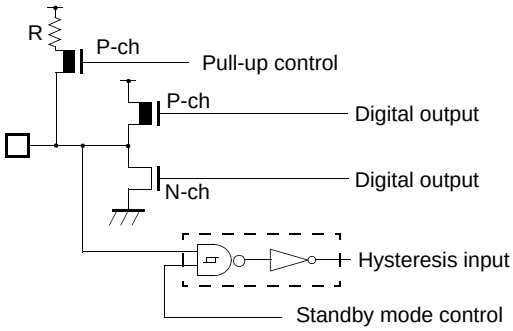
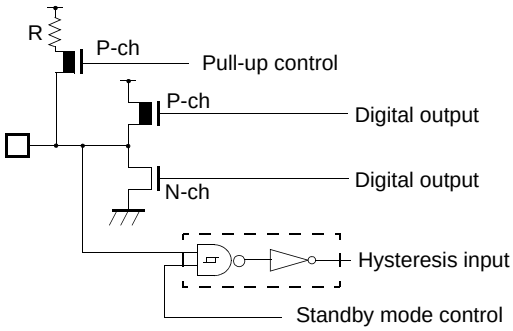
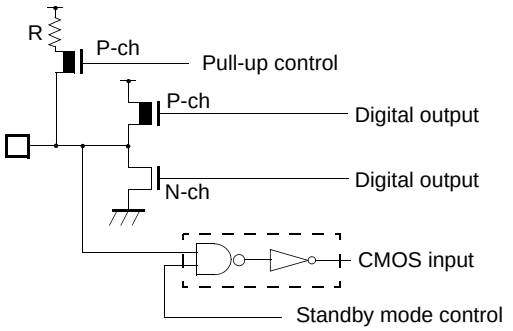
Pin no.		Pin name	I/O circuit *3	Pin status during reset	Function
LQFP *1	QFP *2				
72, 71	74, 73	P76, P77	K	Analog input	General-purpose I/O ports.
		IN0, IN1			Trigger input pins for input capture ch.0, ch.1.
		AN14, AN15			A/D converter analog input pins.
70, 69	72, 71	P80, P81	F	Port input	General-purpose I/O ports.
		IN2, IN3			Trigger input pins for input capture ch.2, ch.3.
68 to 63	70 to 65	P82 to P87	L		General-purpose I/O ports.
		RTO0 (U) to RTO5 (Z)			Waveform generator output pins. (U) to (Z) represent the coils for controlling a 3-phase motor.
25	27	MD2	M	Mode input	Input pin for operation mode specification.
24, 23	26, 25	MD1, MD0	N		Input pins for operation mode specification.
80	2	AV_{CC}	—	—	Analog power supply pin.
79	1	AVR	—		Vref + pin for the A/D converter. Vref - is fixed to AVss internally.
1	3	AV_{SS}	—		Analog power supply (Ground) pin.
20, 61	22, 63	Vss	—		Power (Ground) pins.
40, 60	42, 62	Vcc	—		Power pins.
62	64	C	—		Connect pin for smoothing capacitor to stabilize internal power supply.

*1 : FPT-80P-M21,
FPT-80P-M22

*2 : FPT-80P-M06

*3 : Refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types.

■ I/O CIRCUIT TYPE

Classification	Type	Remarks
A		Oscillation feedback resistor : approx. 1 MΩ
B		• Hysteresis input • Pull-up resistor : approx. 50 kΩ
C		• CMOS output • Hysteresis input • Selectable pull-up resistor : approx. 50 kΩ • I_{OL} = 12 mA
D		• CMOS output • Hysteresis input • Selectable pull-up resistor : approx. 50 kΩ • I_{OL} = 4 mA
E		• CMOS output • CMOS input • With pull-up control • I_{OL} = 4 mA

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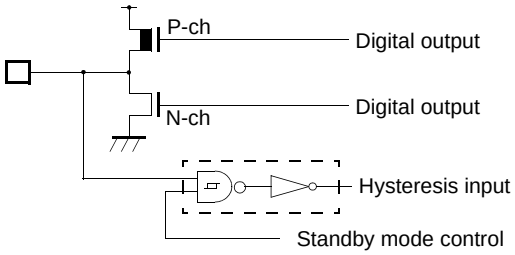
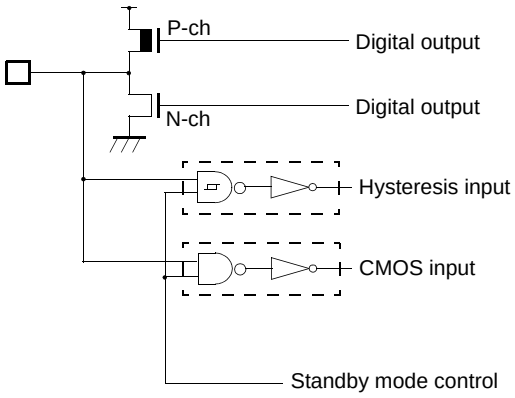
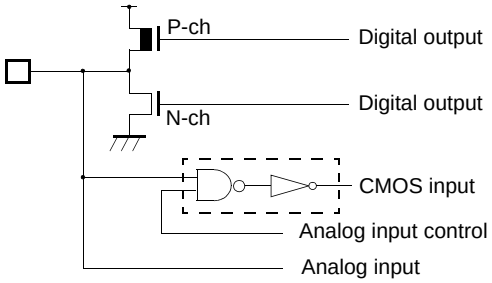
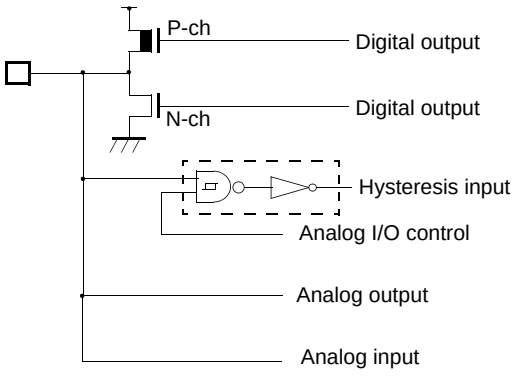
Classification	Type	Remarks
F		• CMOS output • Hysteresis input • I_{OL} = 4 mA
G		• CMOS output • Hysteresis input • CMOS input (selectable for UART ch.0 data input pin) • I_{OL} = 4 mA
H		• CMOS output • CMOS input • Analog input • I_{OL} = 4 mA
I		• CMOS output • Hysteresis input • Analog output • Analog input • I_{OL} = 4 mA

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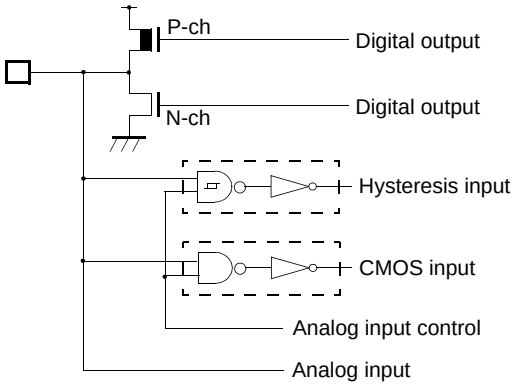
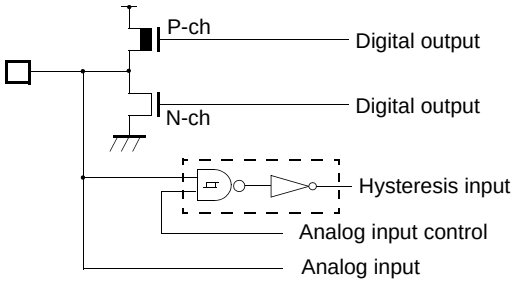
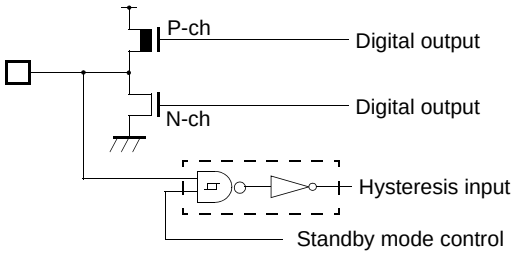
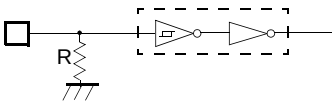
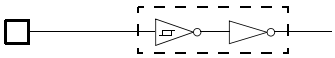
Classification	Type	Remarks
J		• CMOS output • Hysteresis input • CMOS input (selectable for UART ch.1 data input pin) • I_{OL} = 4 mA
K		• CMOS output • Hysteresis input • Analog input • I_{OL} = 4 mA
L		• CMOS output • Hysteresis input • I_{OL} = 12 mA
M		MASK ROM / evaluation product • Hysteresis input • Pull-down resistor : approx. 50 kΩ Flash memory product • CMOS input • No pull-down resistor
N		MASK ROM / evaluation product • Hysteresis input Flash memory product • CMOS input

■ HANDLING DEVICES

Special care is required for the following when handling the device :

- Preventing latch-up
- Stabilization of supply voltage
- Treatment of unused pins
- Using external clock
- Power supply pins (V_{CC} /V_{SS})
- Pull-up/pull-down resistors
- Crystal Oscillator Circuit
- Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
- Connection of Unused Pins of A/D Converter
- Notes on turning the power on
- Notes on During Operation of PLL Clock Mode

1. Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

In using the devices, take sufficient care to avoid exceeding maximum ratings.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVR) exceed the digital power-supply voltage.

2. Stabilization of supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the specified V_{CC} supply voltage operation range. Therefore, the V_{CC} supply voltage should be stabilized.

For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak values) at commercial frequencies (50 Hz/60 Hz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

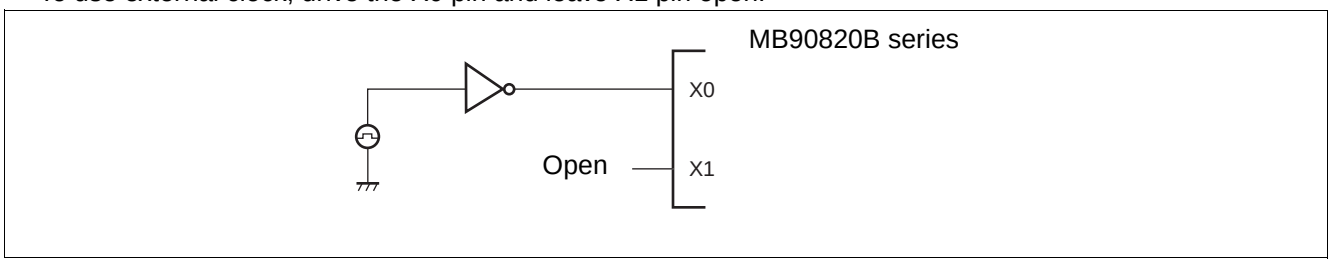
3. Treatment of unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

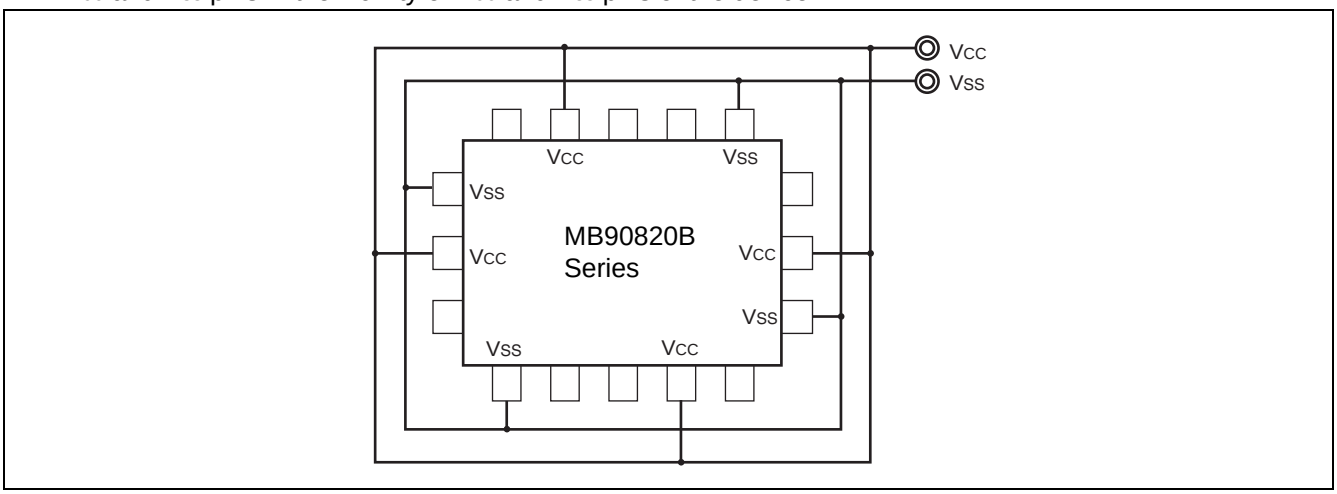
4. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.



5. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up.
  To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
- Connect V_{CC} and V_{SS} pins to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about 0.1 µF as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device.



6. Pull-up/pull-down resistors

The MB90820B series does not support internal pull-up/pull-down resistors option (Port 0 to Port 3 : built-in pull-up resistors) . Use external components where needed.

7. Crystal oscillator circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit do not cross the lines of other circuits while you design a printed circuit board.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.

8. Turning-on sequence of power supply to A/D converter and D/A converter, and analog inputs

Make sure to turn on the A/D converter power supply, D/A converter power supply (AV_{CC}, AVRH, AVR) and analog inputs (AN0 to AN15) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter power supply, D/A converter power supply, and analog inputs. In this case, make sure that the voltage not exceed AVR or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

9. Pin connections when A/D converter and D/A converter are unused

When the A/D converter and D/A converter are not used, connect AV_{CC} = V_{CC}, AV_{SS} = AVRH = AVRL = V_{SS}.

10. Notes on turning the power on

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during power on at 50 µs or more (0.2 V to 2.7 V) .

11. Notes on During Operation of PLL Clock Mode

If the PLL clock mode is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit within the PLL even if the external oscillator is disconnected or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

12. Internal CR Oscillation Circuit

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Oscillation frequency	f_{RC}	50	100	200	kHz
Oscillation stabilization waiting time	tstab	—	—	100	µs

■ SECTOR CONFIGURATION OF FLASH MEMORY

The flash memory has the sector configuration illustrated below. The addresses in the illustration are the upper and lower addresses of each sector.

When 512K bits flash memory is accessed from the CPU, SA0 to SA3 are allocated in the FF bank.

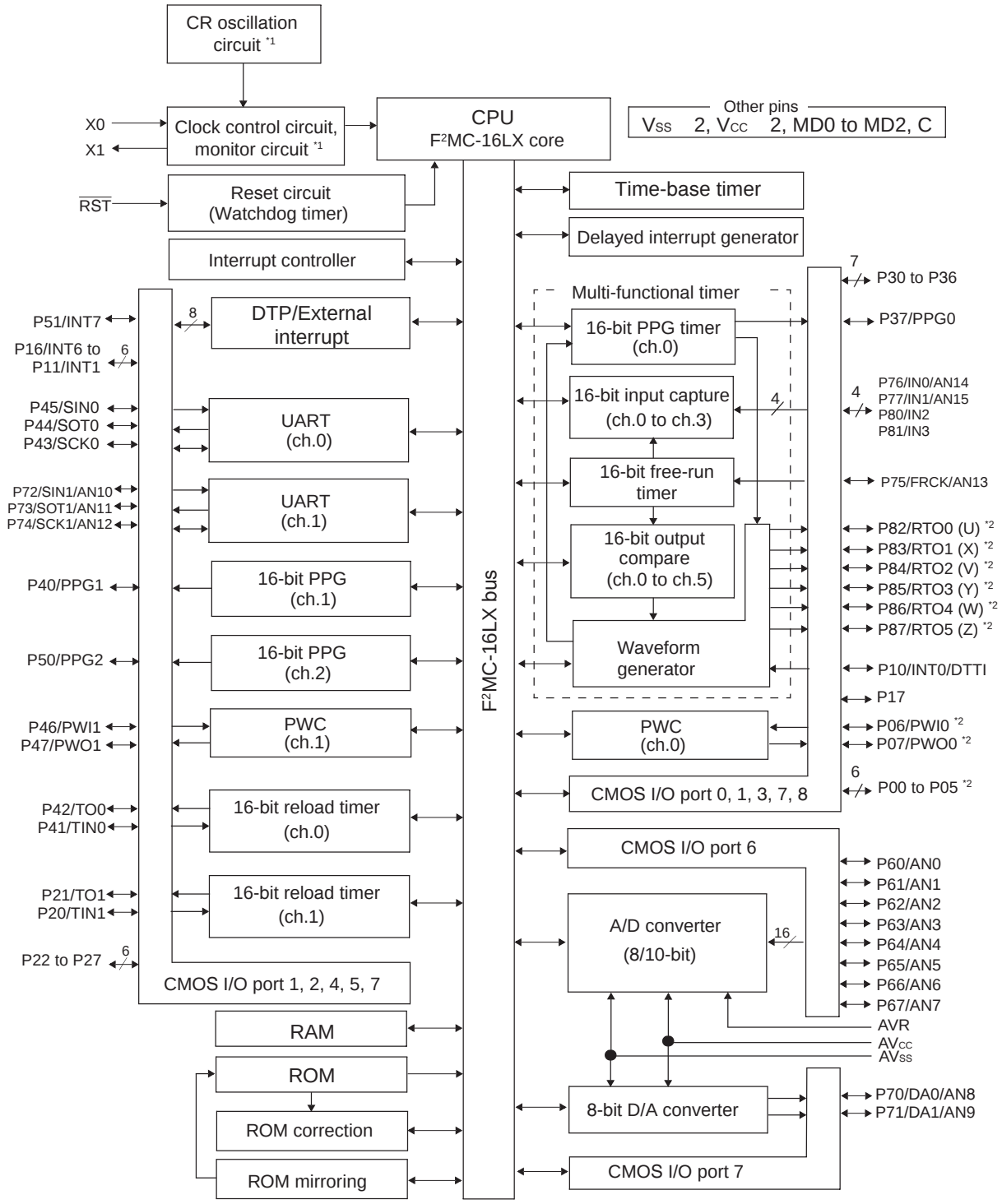
Flash memory	CPU address	*Writer address
SA3 (16K bytes)	$FFFFFF_H$	$7FFFF_H$
	$FFC000_H$	$7C000_H$
SA2 (8K bytes)	$FFBFFF_H$	$7BFFF_H$
	$FFA000_H$	$7A000_H$
SA1 (8K bytes)	$FF9FFF_H$	$79FFF_H$
	$FF8000_H$	78000_H
SA0 (32K bytes)	$FF7FFF_H$	$77FFF_H$
	$FF0000_H$	70000_H

When 1024K bits flash memory is accessed from the CPU, SA0 to SA4 are allocated in the FE and FF bank.

Flash memory	CPU address	*Writer address
SA4 (16K bytes)	$FFFFFF_H$	$7FFFF_H$
	$FFC000_H$	$7C000_H$
SA3 (8K bytes)	$FFBFFF_H$	$7BFFF_H$
	$FFA000_H$	$7A000_H$
SA2 (8K bytes)	$FF9FFF_H$	$79FFF_H$
	$FF8000_H$	78000_H
SA1 (32K bytes)	$FF7FFF_H$	$77FFF_H$
	$FF0000_H$	70000_H
SA0 (64K bytes)	$FEFFFF_H$	$6FFFF_H$
	$FE0000_H$	60000_H

* : The writer address is the address corresponding to the CPU address when writing data from a parallel flash memory writer. Use the writer address when programming or erasing using a general-purpose parallel writer.

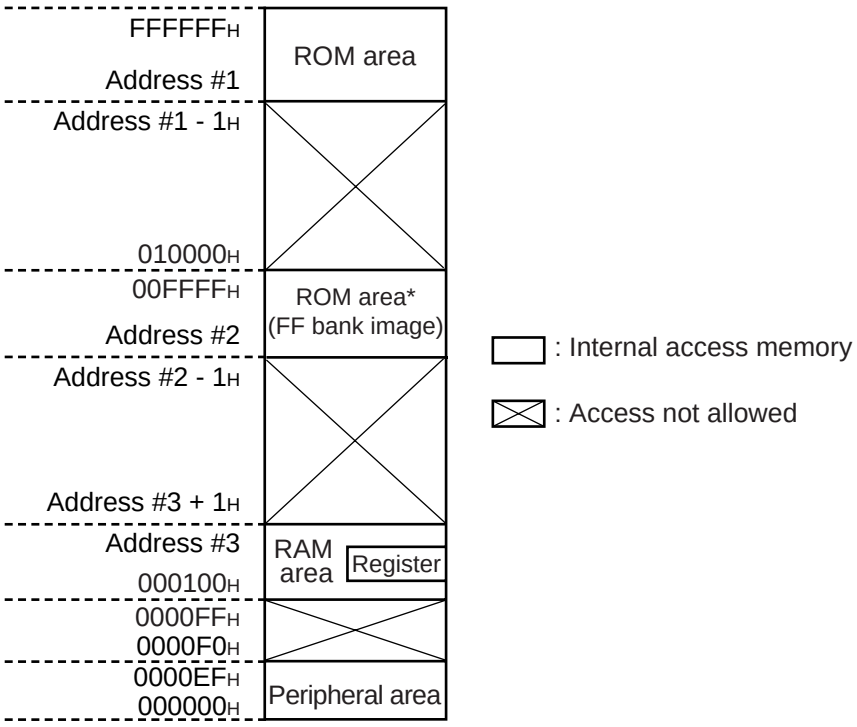
■ BLOCK DIAGRAM



Note : P00 to P07, P10 to P17, P20 to P27 and P30 to P37: With build-in resistors that can be used as input pull-up resistors.

*1 : MB90F828B
*2 : High current drive pin.

■ MEMORY MAP



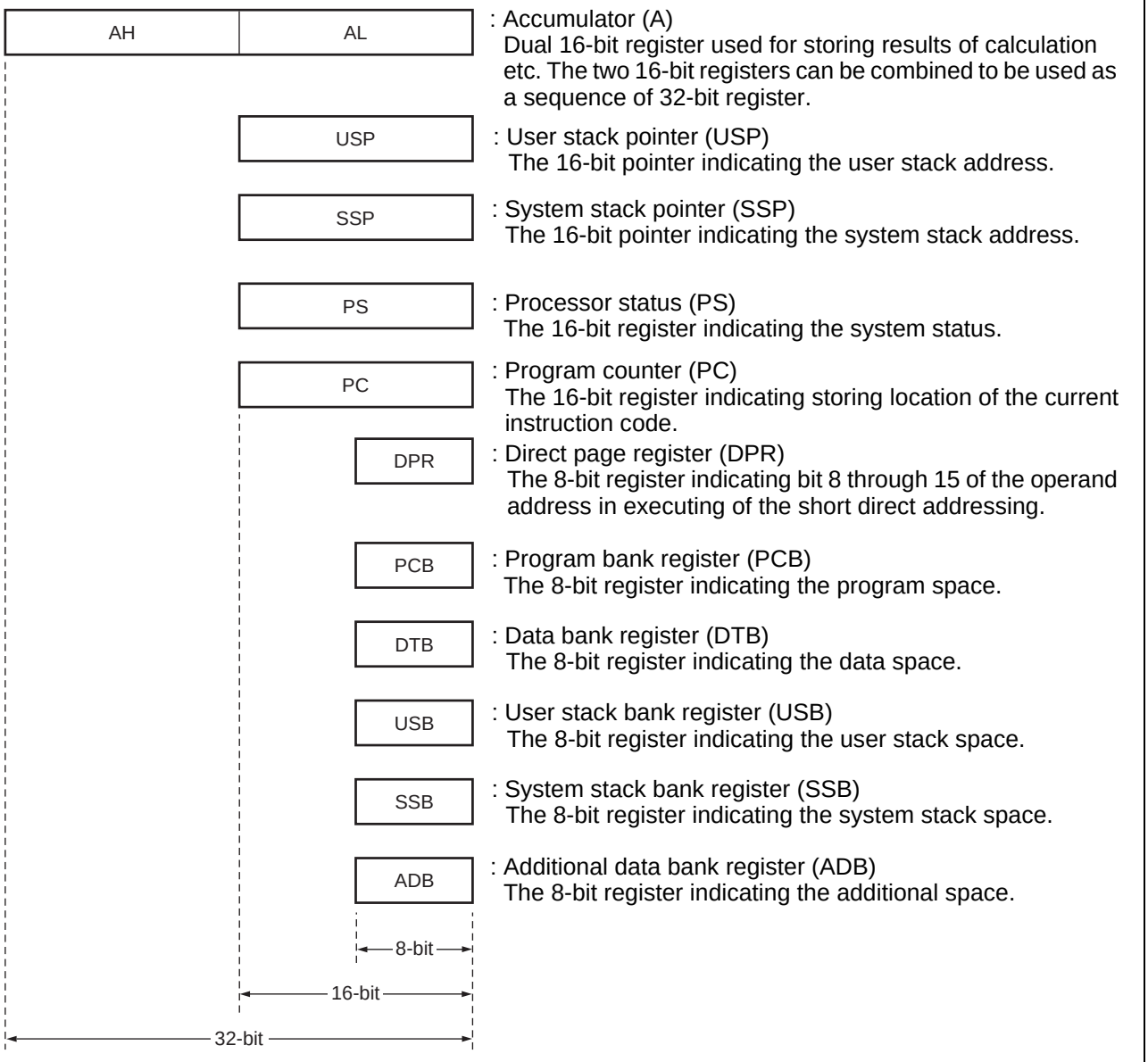
* : In Single chip mode, the mirror function is supported.

Parts no.	Address#1	Address#2	Address#3
MB90822B	FF0000H	008000H	0010FFH
MB90823B	FE0000H	008000H	0010FFH
MB90F822B	FF0000H	008000H	0010FFH
MB90F823B	FE0000H	008000H	0010FFH
MB90F828B	FE0000H	008000H	0020FFH
MB90V820B	(FE0000H)	008000H	0040FFH

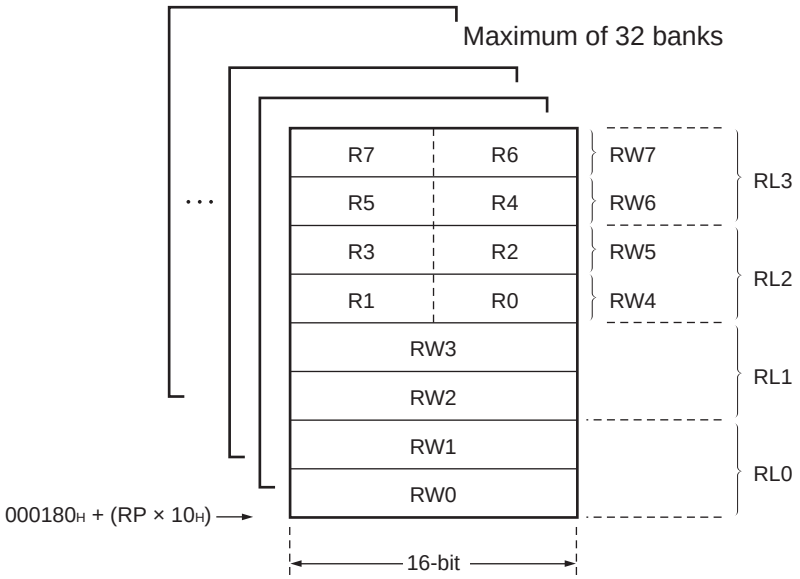
Note: The ROM data of bank FF is reflected to the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit is assigned to the same address, enabling reference of the table on the ROM without stating “far”. For example, if an attempt has been made to access 00C000H, the contents of the ROM at FFC000H are accessed actually. Since the ROM area of the FF bank exceeds 32 K bytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF8000H to FFFFFFH looks, therefore, as if it were the image for 008000H to 00FFFFH. Thus, it is recommended that the ROM data table be stored in the area of FF8000H to FFFFFFH.

■ F²MC-16LX CPU PROGRAMMING MODEL

- Dedicated registers



- General-purpose registers



- Processor status (PS)

	ILM			RP					CCR							
	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PS	ILM2	ILM1	ILM0	B4	B3	B2	B1	B0	—	I	S	T	N	Z	V	C
Initial value	0	0	0	0	0	0	0	0	—	0	1	X	X	X	X	X

— : Unused
X : Undefined

■ I/O MAP

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000000H	PDR0	Port 0 data register	R/W	R/W	Port 0	XXXXXXXXB
000001H	PDR1	Port 1 data register	R/W	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 data register	R/W	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 data register	R/W	R/W	Port 5	XXXXXXXXB
000006H	PDR6	Port 6 data register	R/W	R/W	Port 6	XXXXXXXXB
000007H	PDR7	Port 7 data register	R/W	R/W	Port 7	XXXXXXXXB
000008H	PDR8	Port 8 data register	R/W	R/W	Port 8	XXXXXXXXB
000009H to 00000FH	Prohibited area					
000010H	DDR0	Port 0 data direction register	R/W	R/W	Port 0	00000000B
000011H	DDR1	Port 1 data direction register	R/W	R/W	Port 1	00000000B
000012H	DDR2	Port 2 data direction register	R/W	R/W	Port 2	00000000B
000013H	DDR3	Port 3 data direction register	R/W	R/W	Port 3	00000000B
000014H	DDR4	Port 4 data direction register	R/W	R/W	Port 4	00000000B
000015H	DDR5	Port 5 data direction register	R/W	R/W	Port 5	XXXXXX00B
000016H	DDR6	Port 6 data direction register	R/W	R/W	Port 6	00000000B
000017H	DDR7	Port 7 data direction register	R/W	R/W	Port 7	00000000B
000018H	DDR8	Port 8 data direction register	R/W	R/W	Port 8	00000000B
000019H to 00001FH	Prohibited area					
000020H	SMR0	Serial mode register ch.0	R/W	R/W	UART ch.0	00000000B
000021H	SCR0	Serial control register ch.0	W, R/W	W, R/W		00000100B
000022H	SIDR0 / SODR0	Serial input data register ch.0 / Serial output data register ch.0	R/W	R/W		XXXXXXXXB
000023H	SSR0	Serial status register ch.0	R, R/W	R, R/W		00001000B
000024H	SMR1	Serial mode register ch.1	R/W	R/W	UART ch.1	00000000B
000025H	SCR1	Serial control register ch.1	W, R/W	W, R/W		00000100B
000026H	SIDR1 / SODR1	Serial input data register ch.1 / Serial output data register ch.1	R/W	R/W		XXXXXXXXB
000027H	SSR1	Serial status register ch.1	R, R/W	R, R/W		00001000B

(Continued)

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000028H	PWCSL1	PWC control status register ch.1	R/W	R/W	PWC timer ch.1	00000000B
000029H	PWCSH1		R, R/W	R, R/W		00000000B
00002AH	PWC1	PWC data buffer register ch.1	—	R/W		XXXXXXXXB
00002BH						XXXXXXXXB
00002CH	DIV1	Divide ratio control register ch.1	R/W	R/W		XXXXXX00B
00002DH, 00002EH	Prohibited area					
00002FH	PCKCR	PLL clock control register	W	W	PLL	XXXX0000B
000030H	ENIR	DTP / Interrupt enable register	R/W	R/W	DTP/ external interrupt ch.0 to ch.7	00000000B
000031H	EIRR	DTP / Interrupt cause register	R/W	R/W		XXXXXXXXB
000032H	ELVRL	Request level setting register (lower byte)	R/W	R/W		00000000B
000033H	ELVRH	Request level setting register (higher byte)	R/W	R/W		00000000B
000034H	Prohibited area					
000035H	CDCR0	Clock division ratio control register ch.0	R/W	R/W	Communication prescaler ch.0	00XXX000B
000036H	Prohibited area					
000037H	CDCR1	Clock division ratio control register ch.1	R/W	R/W	Communication prescaler ch.1	00XXX000B
000038H	PDCR0	PPG down counter register ch.0	—	R	16-bit PPG timer ch.0	11111111B
000039H						11111111B
00003AH	PCSR0	PPG cycle setting register ch.0	—	W		XXXXXXXXB
00003BH						XXXXXXXXB
00003CH	PDUT0	PPG duty setting register ch.0	—	W		XXXXXXXXB
00003DH						XXXXXXXXB
00003EH	PCNTL0	PPG control status register ch.0	R/W	R/W		XX000000B
00003FH	PCNTH0		R/W	R/W		00000000B
000040H	PDCR1	PPG down counter register ch.1	—	R	16-bit PPG timer ch.1	11111111B
000041H						11111111B
000042H	PCSR1	PPG cycle setting register ch.1	—	W		XXXXXXXXB
000043H						XXXXXXXXB
000044H	PDUT1	PPG duty setting register ch.1	—	W		XXXXXXXXB
000045H						XXXXXXXXB
000046H	PCNTL1	PPG control status register ch.1	R/W	R/W		XX000000B
000047H	PCNTH1		R/W	R/W		00000000B

(Continued)

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000048H	PDCR2	PPG down counter register ch.2	—	R	16-bit PPG timer ch.2	11111111B
000049H						11111111B
00004AH	PCSR2	PPG cycle setting register ch.2	—	W		XXXXXXXXB
00004BH						XXXXXXXXB
00004CH	PDUT2	PPG duty setting register ch.2	—	W		XXXXXXXXB
00004DH						XXXXXXXXB
00004EH	PCNTL2	PPG control status register ch.2	R/W	R/W		XX000000B
00004FH	PCNTH2		R/W	R/W		00000000B
000050H	TMRR0	16-bit timer register ch.0	—	R/W	Waveform generator	XXXXXXXXB
000051H						XXXXXXXXB
000052H	TMRR1	16-bit timer register ch.1	—	R/W		XXXXXXXXB
000053H						XXXXXXXXB
000054H	TMRR2	16-bit timer register ch.2	—	R/W		XXXXXXXXB
000055H						XXXXXXXXB
000056H	DTCR0	16-bit timer control register ch.0	R/W	R/W		00000000B
000057H	DTCR1	16-bit timer control register ch.1	R/W	R/W		00000000B
000058H	DTCR2	16-bit timer control register ch.2	R/W	R/W		00000000B
000059H	SIGCR	Waveform control register	R/W	R/W		00000000B
00005AH	CPCLRB / CPCLR	Compare clear buffer register/ Compare clear register	—	R/W	16-bit free-run timer	11111111B
00005BH						11111111B
00005CH	TCDT	Timer data register	—	R/W		00000000B
00005DH						00000000B
00005EH	TCCSL	Timer control status register (lower)	R/W	R/W		X0100000B
00005FH	TCCSH	Timer control status register (upper)	R/W	R/W		00000000B
000060H	IPCP0	Input capture data register ch.0	—	R	16-bit input capture (ch.0 to ch.3)	XXXXXXXXB
000061H						XXXXXXXXB
000062H	IPCP1	Input capture data register ch.1	—	R		XXXXXXXXB
000063H						XXXXXXXXB
000064H	IPCP2	Input capture data register ch.2	—	R		XXXXXXXXB
000065H						XXXXXXXXB
000066H	IPCP3	Input capture data register ch.3	—	R		XXXXXXXXB
000067H						XXXXXXXXB

(Continued)

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000068H	PICSL01	Input capture control status register ch.0,ch.1 (lower)	R/W	R/W	16-bit input capture (ch.0 to ch.3)	00000000B
000069H	PICSH01	PPG output control / Input capture control status register ch.0,ch.1 (upper)	R, R/W	R, R/W		00000000B
00006AH	ICSL23	Input capture control status register ch.2,ch.3 (lower)	R/W	R/W		00000000B
00006BH	ICSH23	Input capture control status register ch.2,ch.3 (upper)	R	R		XXXXXX00B
00006CH to 00006EH	Prohibited area					
00006FH	ROMM	ROM mirroring function selection register	W	W	ROM mirroring function	XXXXXXX1B
000070H	OCCPB0 / OCCP0	Output compare buffer register / Output compare register ch.0	—	R/W	Output compare (ch.0 to ch.5)	XXXXXXXXB
000071H						XXXXXXXXB
000072H	OCCPB1 / OCCP1	Output compare buffer register / Output compare register ch.1	—	R/W		XXXXXXXXB
000073H						XXXXXXXXB
000074H	OCCPB2 / OCCP2	Output compare buffer register / Output compare register ch.2	—	R/W		XXXXXXXXB
000075H						XXXXXXXXB
000076H	OCCPB3 / OCCP3	Output compare buffer register / Output compare register ch.3	—	R/W		XXXXXXXXB
000077H						XXXXXXXXB
000078H	OCCPB4 / OCCP4	Output compare buffer register / Output compare register ch.4	—	R/W		XXXXXXXXB
000079H						XXXXXXXXB
00007AH	OCCPB5 / OCCP5	Output compare buffer register / Output compare register ch.5	—	R/W		XXXXXXXXB
00007BH						XXXXXXXXB
00007CH	OCS0	Compare control register ch.0	R/W	R/W		00001100B
00007DH	OCS1	Compare control register ch.1	R/W	R/W		X1100000B
00007EH	OCS2	Compare control register ch.2	R/W	R/W		00001100B
00007FH	OCS3	Compare control register ch.3	R/W	R/W		X1100000B
000080H	OCS4	Compare control register ch.4	R/W	R/W		00001100B
000081H	OCS5	Compare control register ch.5	R/W	R/W		X1100000B
000082H	TMCSRL0	Timer control status register ch.0 (lower)	R/W	R/W	16-bit reload timer (ch.0)	00000000B
000083H	TMCSRH0	Timer control status register ch.0 (upper)	R/W	R/W		XXX10000B
000084H	TMR0 / TMRD0	16 bit timer register ch.0 / 16-bit reload register ch.0	—	R/W		XXXXXXXXB
000085H						XXXXXXXXB
000086H	TMCSRL1	Timer control status register ch.1 (lower)	R/W	R/W	16-bit reload timer (ch.1)	00000000B

(Continued)

Address	Abbrevia-tion	Register	Byte access	Word access	Resource name	Initial value
000087H	TMCSRH1	Timer control status register ch.1 (upper)	R/W	R/W	16-bit reload timer (ch.1)	XXX10000B
000088H	TMR1 / TMRD1	16 bit timer register ch.1 / 16-bit reload register ch.1	—	R/W		XXXXXXXXB
000089H						XXXXXXXXB
00008AH	CSVCR	Clock supervisor control register*	R, R/W	—	Clock supervisor	00011100B
00008BH	Prohibited area					
00008CH	RDR0	Port 0 pull-up resistor setting register	R/W	R/W	Port 0	00000000B
00008DH	RDR1	Port 1 pull-up resistor setting register	R/W	R/W	Port 1	00000000B
00008EH	RDR2	Port 2 pull-up resistor setting register	R/W	R/W	Port 2	00000000B
00008FH	RDR3	Port 3 pull-up resistor setting register	R/W	R/W	Port 3	00000000B
000090H to 00009DH	Prohibited area					
00009EH	PACSR	Program address detection control status register	R/W	R/W	Address match detection	XXXX0000B
00009FH	DIRR	Delayed interrupt cause / clear register	R/W	R/W	Delayed interrupt	XXXXXXX0B
0000A0H	LPMCR	Low-power consumption mode control register	W, R/W	W, R/W	Low-power consumption control register	00011000B
0000A1H	CKSCR	Clock selection register	R, R/W	R, R/W		11111100B
0000A2H to 0000A7H	Prohibited area					
0000A8H	WDTC	Watchdog timer control register	R, W	R, W	Watchdog timer	XXXXX111B
0000A9H	TBTC	Time-base timer control register	W, R/W	W, R/W	Time-base timer	1XX00100B
0000AAH to 0000ADH	Prohibited area					
0000AEH	FMCS	Flash memory control status register	R, R/W	R, R/W	Flash memory interface circuit	000X0000B
0000AFH	Prohibited area					

(Continued)

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
0000B0H	ICR00	Interrupt control register 00	R/W	R/W	Interrupt controller	00000111B
0000B1H	ICR01	Interrupt control register 01	R/W	R/W		00000111B
0000B2H	ICR02	Interrupt control register 02	R/W	R/W		00000111B
0000B3H	ICR03	Interrupt control register 03	R/W	R/W		00000111B
0000B4H	ICR04	Interrupt control register 04	R/W	R/W		00000111B
0000B5H	ICR05	Interrupt control register 05	R/W	R/W		00000111B
0000B6H	ICR06	Interrupt control register 06	R/W	R/W	Interrupt controller	00000111B
0000B7H	ICR07	Interrupt control register 07	R/W	R/W		00000111B
0000B8H	ICR08	Interrupt control register 08	R/W	R/W		00000111B
0000B9H	ICR09	Interrupt control register 09	R/W	R/W		00000111B
0000BAH	ICR10	Interrupt control register 10	R/W	R/W		00000111B
0000BBH	ICR11	Interrupt control register 11	R/W	R/W		00000111B
0000BCH	ICR12	Interrupt control register 12	R/W	R/W		00000111B
0000BDH	ICR13	Interrupt control register 13	R/W	R/W		00000111B
0000BEH	ICR14	Interrupt control register 14	R/W	R/W		00000111B
0000BFH	ICR15	Interrupt control register 15	R/W	R/W		00000111B
0000C0H	PWCSL0	PWC control status register ch.0	R/W	R/W	PWC timer (ch.0)	00000000B
0000C1H	PWCSH0		R, R/W	R, R/W		00000000B
0000C2H	PWC0	PWC data buffer register ch.0	—	R/W		XXXXXXXXB
0000C3H						XXXXXXXXB
0000C4H	DIV0	Divide ratio control register ch.0	R/W	R/W		XXXXXX00B
0000C5H	ADER0	A/D input enable register 0	R/W	R/W	Port 6, A/D	11111111B
0000C6H	ADCS0	A/D control status register 0	R/W	R/W	8/10-bit A/D converter	000XXXX0B
0000C7H	ADCS1	A/D control status register 1	W, R/W	W, R/W		0000000XB
0000C8H	ADCR0	A/D data register 0	R	R		XXXXXXXXB
0000C9H	ADCR1	A/D data register 1	R	R		XXXXXXXXB
0000CAH	ADSR0	A/D setting register 0	R/W	R/W		00000000B
0000CBH	ADSR1	A/D setting register 1	R/W	R/W		00000000B
0000CCH	DAT0	D/A data register 0	R/W	R/W	8-bit D/A converter	XXXXXXXXB
0000CDH	DAT1	D/A data register 1	R/W	R/W		XXXXXXXXB
0000CEH	DACR0	D/A control register 0	R/W	R/W		XXXXXXX0B
0000CFH	DACR1	D/A control register 1	R/W	R/W		XXXXXXX0B
0000D0H	ADER1	A/D input enable register 1	R/W	R/W	Port 7, A/D	11111111B
0000D1H to 0000EFH	Prohibited area					

(Continued)

(Continued)

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
0000F0H to 0000FFH	External area					
001FF0H	PADRL0	Program address detection register 0 (lower)	R/W	R/W	Address match detection	XXXXXXXXB
001FF1H	PADRM0	Program address detection register 0 (middle)	R/W	R/W		XXXXXXXXB
001FF2H	PADRH0	Program address detection register 0 (higher)	R/W	R/W	Address match detection	XXXXXXXXB
001FF3H	PADRL1	Program address detection register 1 (lower)	R/W	R/W		XXXXXXXXB
001FF4H	PADRM1	Program address detection register 1 (middle)	R/W	R/W		XXXXXXXXB
001FF5H	PADRH1	Program address detection register 1 (higher)	R/W	R/W		XXXXXXXXB

* : For MB90F828B only. Prohibited for the other products.

- Meaning of abbreviations used for reading and writing
  R/W: Read and write enabled
  R : Read-only
  W : Write-only
- Explanation of initial values
  0 : The bit is initialized to “0”.
  1 : The bit is initialized to “1”.
  X : The initial value of the bit is undefined.

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI²OS support	Interrupt vector			Interrupt control register		Priority
		Number		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	—	—	High
INT9 instruction	×	#09	09H	FFFFD8H	—	—	
Exception processing	×	#10	0AH	FFFFD4H	—	—	
A/D converter conversion complete	○	#11	0BH	FFFFD0H	ICR00	0000B0H	
Output compare ch.0 match	○	#12	0CH	FFFFCCH			
End of measurement by PWC timer ch.0 / PWC timer ch.0 overflow	○	#13	0DH	FFFFC8H	ICR01	0000B1H	
16-bit PPG timer ch.0	○	#14	0EH	FFFFC4H			
Output compare ch.1 match	○	#15	0FH	FFFFC0H	ICR02	0000B2H	
16-bit PPG timer ch.1	○	#16	10H	FFFFBCH			
Output compare ch.2 match	○	#17	11H	FFFFB8H	ICR03	0000B3H	
16-bit reload timer ch.1 underflow	○	#18	12H	FFFFB4H			
Output compare ch.3 match	○	#19	13H	FFFFB0H	ICR04	0000B4H	
DTP/ext. interrupt ch.0/ch.1 detection	○	#20	14H	FFFFACH			
DTTI	△						
Output compare ch.4 match	○	#21	15H	FFFFA8H	ICR05	0000B5H	
DTP/ext. interrupt ch.2/ch.3 detection	○	#22	16H	FFFFA4H			
Output compare ch.5 match	○	#23	17H	FFFFA0H	ICR06	0000B6H	
End of measurement by PWC timer ch.1 / PWC timer ch.1 overflow	○	#24	18H	FFFF9CH			
DTP/ext. interrupt ch.4 detection	○	#25	19H	FFFF98H	ICR07	0000B7H	
DTP/ext. interrupt ch.5 detection	○	#26	1AH	FFFF94H			
DTP/ext. interrupt ch.6 detection	○	#27	1BH	FFFF90H	ICR08	0000B8H	
DTP/ext. interrupt ch.7 detection	○	#28	1CH	FFFF8CH			
Waveform generator 16-bit timers ch.0/ ch.1/ch.2 underflow	△	#29	1DH	FFFF88H	ICR09	0000B9H	
16-bit reload timer ch.0 underflow	○	#30	1EH	FFFF84H			
16-bit free-run timer zero detect	△	#31	1FH	FFFF80H	ICR10	0000BAH	
16-bit PPG timer ch.2	○	#32	20H	FFFF7CH			
Input capture ch.0/ch.1	○	#33	21H	FFFF78H	ICR11	0000BBH	
16-bit free-run timer compare clear	△	#34	22H	FFFF74H			
Input capture ch.2/ch.3	○	#35	23H	FFFF70H	ICR12	0000BCH	
Time-base timer	△	#36	24H	FFFF6CH			
UART ch.1 receive	◎	#37	25H	FFFF68H	ICR13	0000BDH	
UART ch.1 send	△	#38	26H	FFFF64H			
UART ch.0 receive	◎	#39	27H	FFFF60H	ICR14	0000BEH	
UART ch.0 send	△	#40	28H	FFFF5CH			
Flash memory status	△	#41	29H	FFFF58H	ICR15	0000BFH	Low
Delayed interrupt generator module	△	#42	2AH	FFFF54H			

◎ : Can be used and support the EI²OS stop request.
○ : Can be used and interrupt request flag is cleared by EI²OS interrupt clear signal.
× : Cannot be used.
△ : Usable when an interrupt cause that shares the ICR is not used.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$ *2
	AVR	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVR$, $AVR \geq AV_{SS}$
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*5
Total maximum clamp current	$\Sigma \mid I_{CLAMP} \mid$	—	20	mA	*5
“L” level maximum output current	I_{OL}	—	15	mA	*4
“L” level average output current	I_{OLAV1}	—	4	mA	Except for P00 to P07, P82 to P87
	I_{OLAV2}	—	12	mA	P00 to P07, P82 to P87
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	
“H” level maximum output current	I_{OH}	—	–15	mA	*4
“H” level average output current	I_{OHAV}	—	–4	mA	
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–50	mA	
Power consumption	P_D	—	430	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1 : This parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

*2 : AV_{CC} must never exceed V_{CC} when the power is turned on.

*3 : V_I and V_O must never exceed V_{CC} + 0.3 V. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

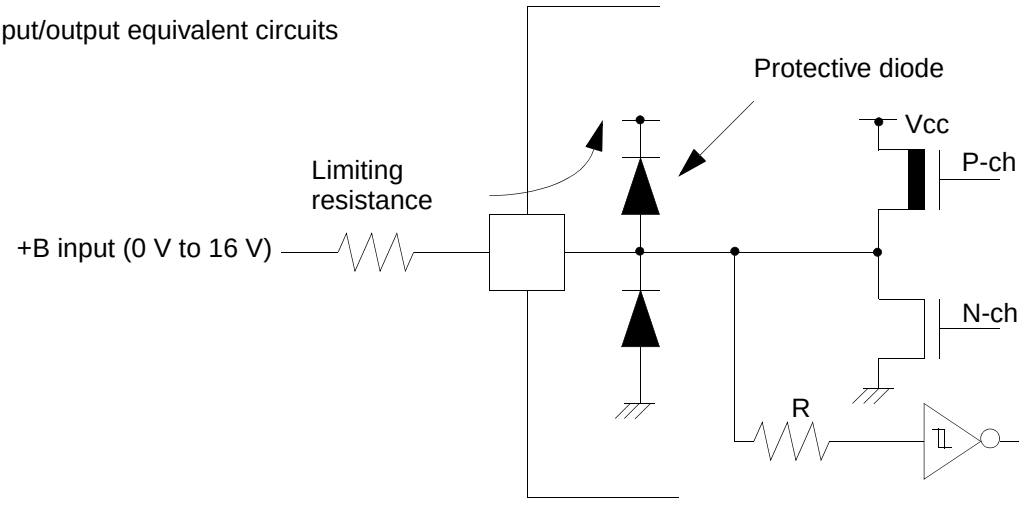
*4 : The maximum output current is a peak value for a corresponding pin.

(Continued)

(Continued)

*5 :
- Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50, P51, P80 to P87.
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal is an input signal exceeding V_{CC} voltage. The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the Vcc pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins (LCD drive pins and comparator input pins, etc.) other than the A/D input pins cannot accept +B input.
- Sample recommended circuits:

Input/output equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply voltage	V_{CC} AV_{CC}	—	—	4.5	5.5	V	At normal operation T_A = –40 °C to +85 °C
		—	—	4.0	5.5	V	Normal operation when D/A converter is not used T_A = –40 °C to +85 °C
		—	—	3.5	5.5	V	Normal operation when A/D converter and D/A converter are not used T_A = –40 °C to +85 °C
		—	—	3.0	5.5	V	Maintains state in stop mode
"H" level input voltage	V_{IH}	P30 to P37, P60 to P67	V_{CC} = 5 V ± 10%	0.7 V_{CC}	V_{CC} + 0.3	V	CMOS input
	V_{IHS}	P00 to P07, P10 to P17, P20 to P27, P40 to P44, P45*1, P46, P47, P50, P51, P70, P71, P72*1, P73 to P77, P80 to P87, $\overline{RST}$		0.8 V_{CC}	V_{CC} + 0.3	V	CMOS hysteresis input
	V_{IHM}	MD0, MD1, MD2		V_{CC} – 0.3	V_{CC} + 0.3	V	MD input
"L" level input voltage	V_{IL}	P30 to P37, P60 to P67		V_{SS} – 0.3	0.3 V_{CC}	V	CMOS input
	V_{ILS}	P00 to P07, P10 to P17, P20 to P27, P40 to P44, P45*1, P46, P47, P50, P51, P70, P71, P72*1, P73 to P77, P80 to P87, $\overline{RST}$		V_{SS} – 0.3	0.2 V_{CC}	V	CMOS hysteresis input
	V_{ILM}	MD0, MD1, MD2		V_{SS} – 0.3	V_{SS} + 0.3	V	MD input
Smoothing capacitor	C_S	—	—	0.1	1.0	µF	*2
Reference input voltage of A/D converter	AVR	—	—	2.7	AV_{CC}	V	
Operating temperature	T_A	—	—	–40	+85	°C	

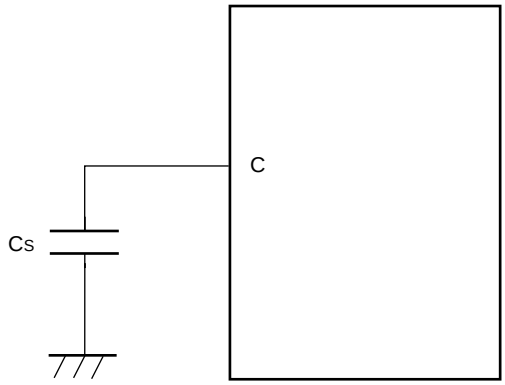
*1 : UART ch.0/ch.1 data input pins P45/SIN0, P72/SIN1/AN10 can be used as CMOS input by the communication prescaler control register (CDRR).

*2 : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. On the V_{CC} pin, connect a bypass capacitor that has a larger capacity than that of C_S. Refer to the following figure for connection of smoothing capacitor C_S.

(Continued)

(Continued)

• C pin connection circuit



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH}	All output pins	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL1}	All pins except P00 to P07 P82 to P87	V_{CC} = 4.5 V, I_{OL1} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P00 to P07 P82 to P87	V_{CC} = 4.5 V, I_{OL2} = 12.0 mA	—	—	0.4	V	
Input leakage current	I_{IL}	All input pins	V_{CC} = 5.5 V, $V_{SS} < V_I < V_{CC}$	–5	—	+ 5	µA	At pull-up disabled
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, $\overline{RST}$	—	25	50	100	kΩ	MASK ROM product
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	MASK ROM product

(Continued)

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal frequency: 24 MHz, At normal operation	—	35	50	mA	MASK ROM product
				—	45	60	mA	Flash memory product
			V_{CC} = 5.0 V, Internal frequency: 24 MHz, At writing in flash memory	—	60	75	mA	Flash memory product
			V_{CC} = 5.0 V, Internal frequency: 24 MHz, At erasing memory	—	65	80	mA	Flash memory product
	I_{CCS}		V_{CC} = 5.0 V, Internal frequency: 24 MHz, At sleep mode	—	15	25	mA	MASK ROM product
				—			mA	Flash memory product
	I_{CTS}		V_{CC} = 5.0 V, Internal frequency: 2 MHz, At main timer mode	—	0.3	0.8	mA	MASK ROM product
				—			mA	Flash memory product
	I_{CCT}		V_{CC} = 5.0 V, Internal frequency: 8 MHz, At timer mode, T_A = +25 °C	—	3	7	mA	MASK ROM product
				—			mA	Flash memory product
	I_{CCH}		In stop mode, T_A = +25 °C	—	5	20	µA	MASK ROM product
				—			mA	Flash memory product
Input capacitance	C_{IN}	Except AV_{CC}, AV_{SS}, AVR, C, V_{CC} and V_{SS}	—	—	5	15	pF	

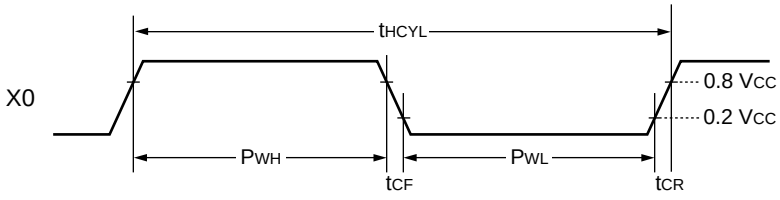
* : The power supply current is regulated with an external clock.

4. AC Characteristics

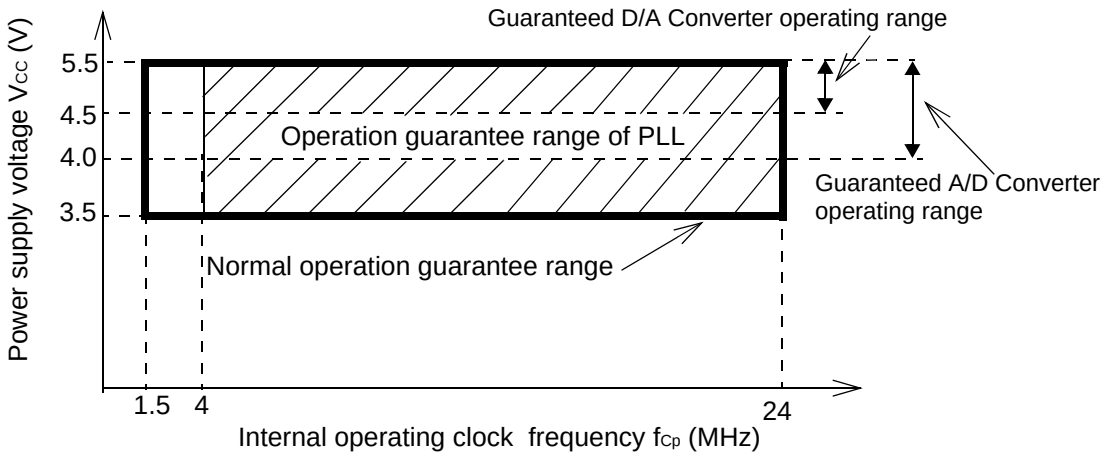
(1) Clock Timings

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

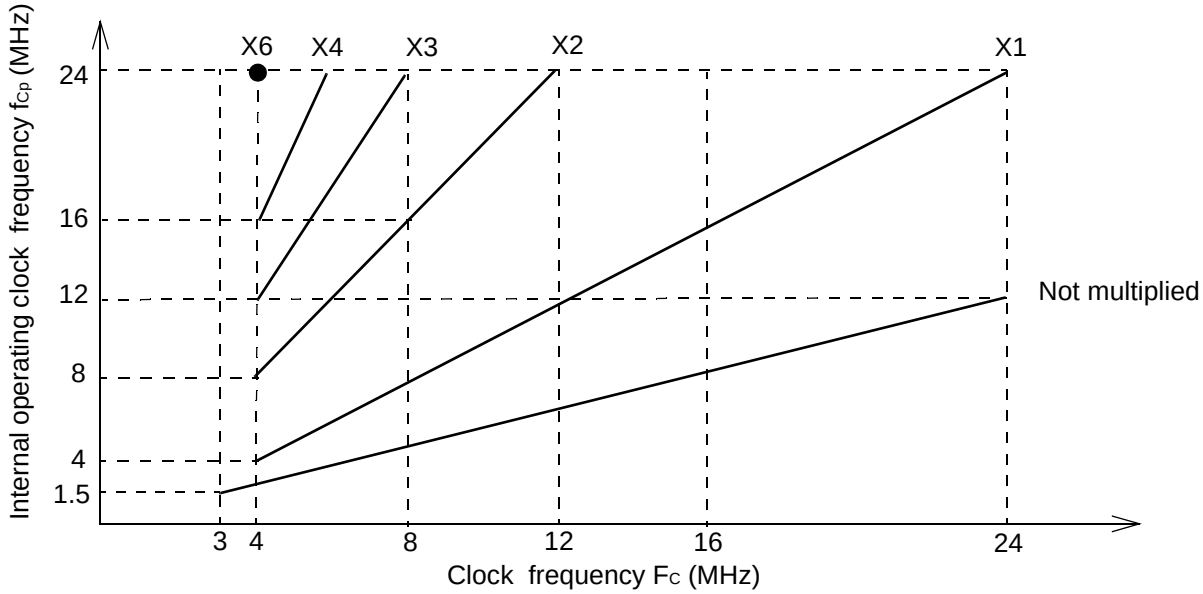
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_C	X0, X1	3	—	16	MHz	When using oscillation circuit
			3	—	24		When using external clock
			4	—	24		1 multiplied PLL
			4	—	12		2 multiplied PLL
			4	—	8		3 multiplied PLL
			4	—	6		4 multiplied PLL
			4	—	4		6 multiplied PLL
Clock cycle time	t_{HCYL}	X0, X1	62.5	—	333	ns	When using oscillation circuit
			41.67	—	333	ns	When using external clock
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	When using external clock, duty ratio is about 30% to 70%.
Input clock rise/fall time	t_{CR} t_{CF}	X0	—	—	5	ns	When using external clock
Internal operating clock frequency	f_{CP}	—	1.5	—	24	MHz	
Internal operating clock cycle time	t_{CP}	—	41.67	—	666	ns	



Relationship between internal operating clock frequency and power supply voltage



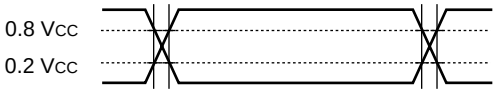
Relationship between clock frequency and internal operating clock frequency



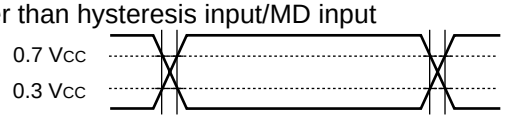
The AC ratings are measured for the following measurement reference voltages

• Input signal waveform

Hysteresis input pin

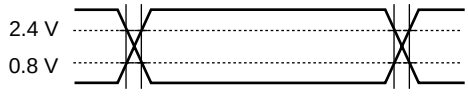


Pins other than hysteresis input/MD input



• Output signal waveform

Output pin



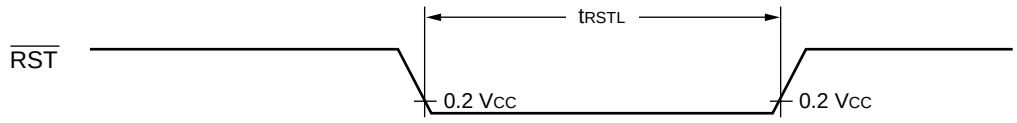
(2) External Reset

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

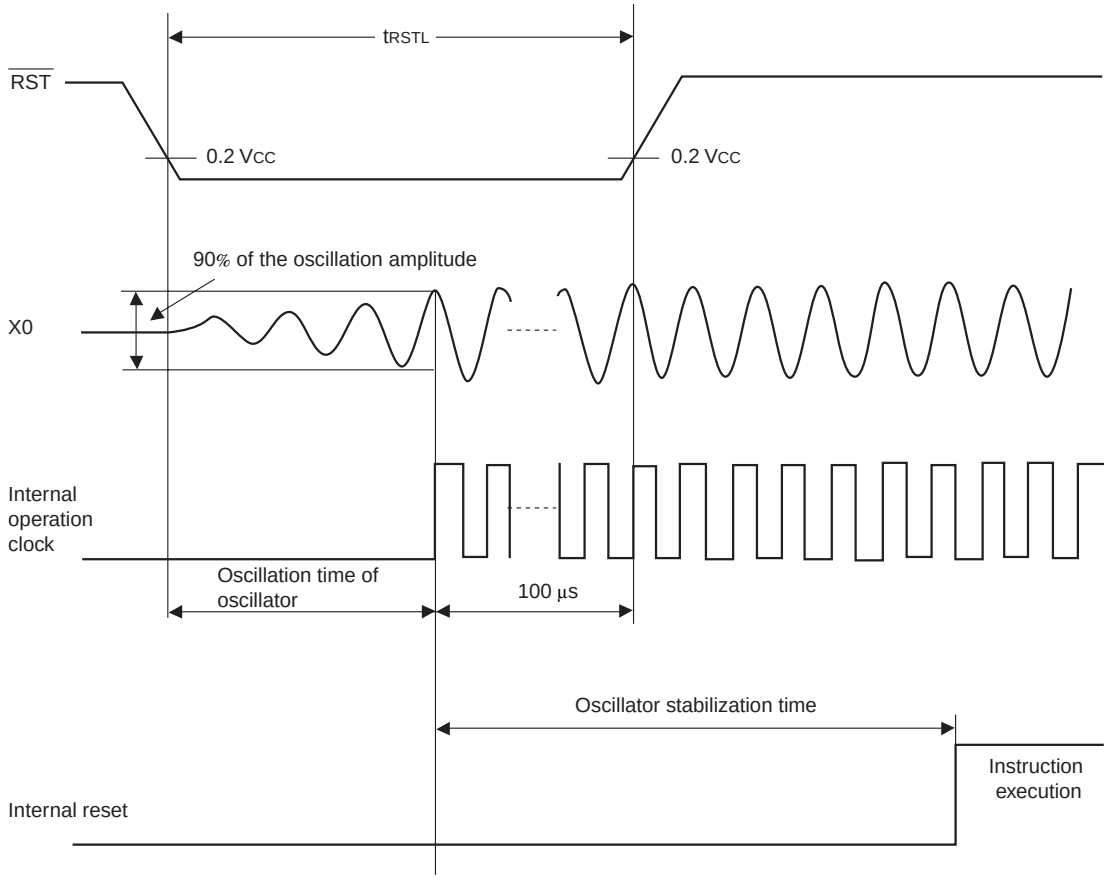
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	—	ns	In normal operation
			Oscillation time of oscillator* + 100	—	µs	In stop mode
			100	—	µs	In time-base timer mode

* : Oscillation time of oscillator is the time to reach to 90% of the oscillation amplitude from stand still. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of µs to several ms. In the external clock, the oscillation time is 0 ms.

- In normal operation mode



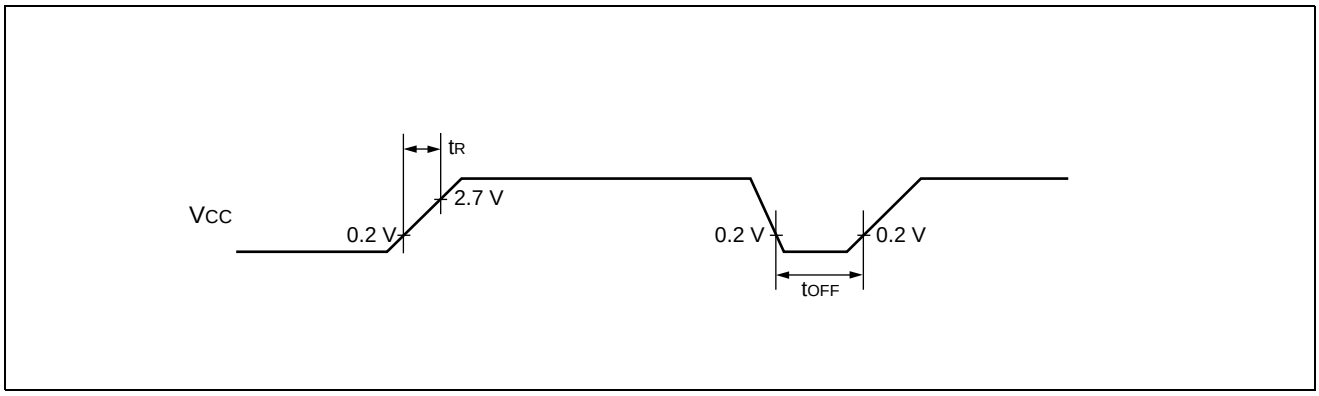
- In stop mode, at power on



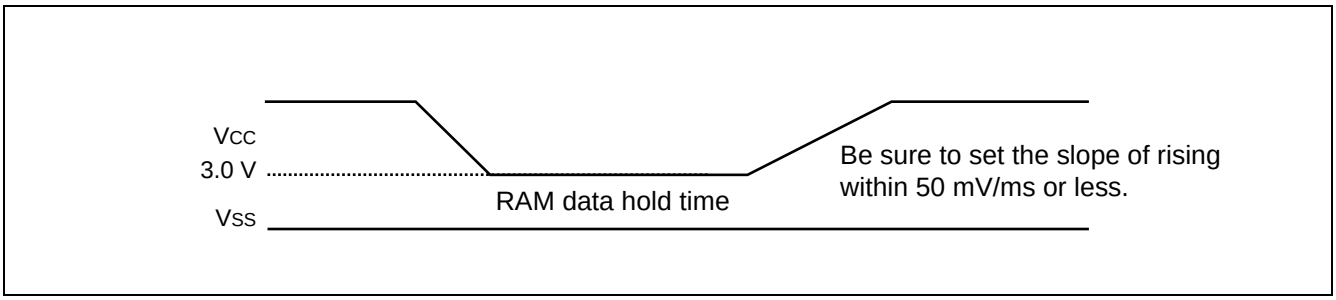
(3) Power-on Reset

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rising time	t_R	V_{CC}	—	0.05	30	ms	
Power supply cut-off time	t_{OFF}	V_{CC}		1	—	ms	Waiting time for power supply on



Note : Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, be sure to set the slope of rising within 50 mV/ms or less as shown below.



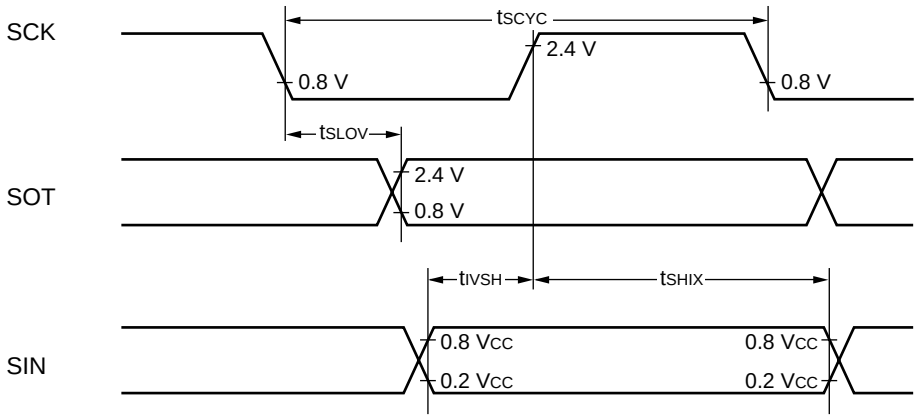
(4) UART

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

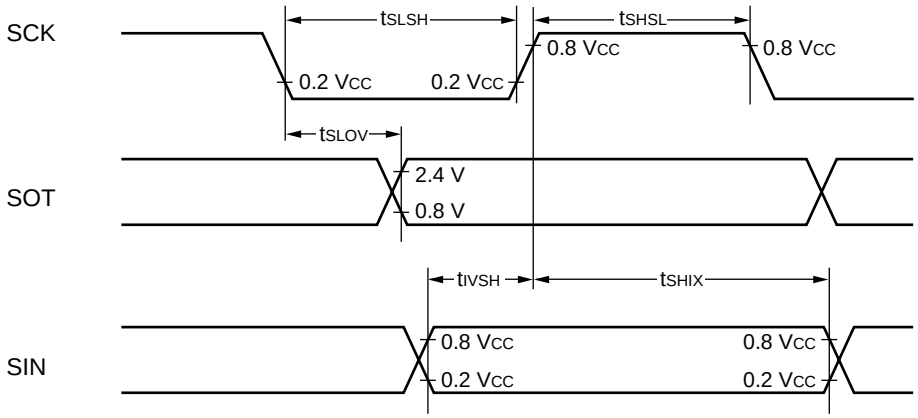
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK1	C_L = 80 pF + 1 TTL for an output pin of internal shift clock mode	8 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK1 SOT0 to SOT1		–80	+ 80	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK1 SIN0 to SIN1		100	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK1 SIN0 to SIN1		60	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK1	C_L = 80 pF + 1 TTL for an output pin of external shift clock mode	4 t_{CP}	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK1		4 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK1 SOT0 to SOT1		—	150	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK1 SIN0 to SIN1		60	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK1 SIN0 to SIN1		60	—	ns

Notes : • These are AC ratings in the CLK synchronous mode.
• CL is the load capacitance value connected to pins while testing.
• t_{CP} is machine cycle time (unit : ns).

• Internal shift clock mode



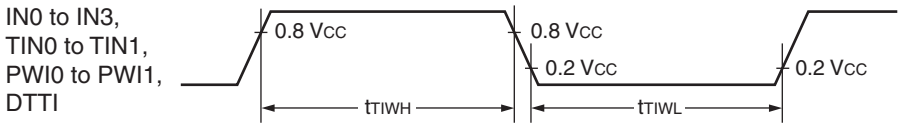
• External shift clock mode



(5) Resources Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

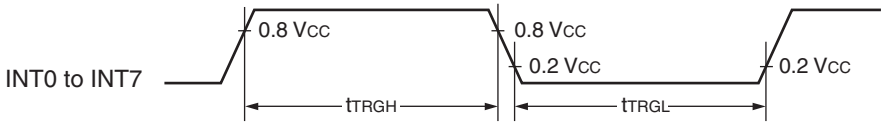
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	IN0 to IN3, TIN0 to TIN1, PWI0 to PWI1, DTTI	—	4 t_{CP}	—	ns



(6) Trigger Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT7	—	5 t_{CP}	—	ns



5. A/D Converter Electrical Characteristics

(3.0 V ≤ AVR – AV_{SS}, V_{CC} = AV_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

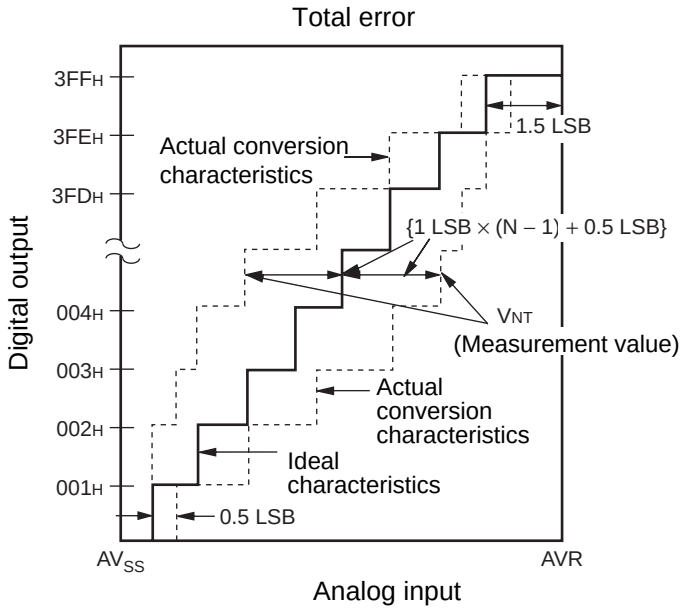
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	10	—	bit	
Total error	—	—		—	—	±3.0	LSB	
Non-linearity error	—	—		—	—	±2.5	LSB	
Differential linearity error	—	—		—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN15		AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	AN0 to AN15		AVR – 3.5 LSB	AVR – 1.5 LSB	AVR + 0.5 LSB	V	
Compare time	—	—		1.0	—	—	µs	4.5 V ≤ AVcc ≤ 5.5 V
				2.0	—	—	µs	4.0 V ≤ AVcc < 4.5 V
Sampling time	—	—		0.5	—	—	µs	4.5 V ≤ AVcc ≤ 5.5 V
				1.2	—	—	µs	4.0 V ≤ AVcc < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN15		– 0.3	—	+ 0.3	µA	
Analog input voltage	V_{AIN}	AN0 to AN15		AV_{SS}	—	AVR	V	
Reference voltage	—	AVR		AV_{SS} + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}		—	2.4	4.7	mA	
	I_{AH}			—	—	5	µA	*
Reference voltage supply current	I_R	AVR		—	600	900	µA	
	I_{RH}			—	—	5	µA	*
Offset between channels	—	AN0 to AN15		—	—	4	LSB	

* : The current when the A/D converter is not operating or the CPU is in stop mode (for V_{CC} = AV_{CC} = AVR = 5.0 V)

Note : The error increases proportionally as |AVR - AV_{SS}| decreases.

6. A/D Converter Glossary

Resolution	:	Analog variation that is recognized by an A/D converter.
Non linearity error	:	Deviation between a line across zero-transition line (“00 0000 0000”↔“00 0000 0001”) and full-scale transition line (“11 1111 1110”↔“11 1111 1111”) and actual conversion characteristics.
Differential linearity error	:	Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value
Total error	:	Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{AVR - AVss}{1024}\ [\text{V}]$$

N : A/D converter digital output value

V_{OT}(Ideal value) = AVss + 0.5 LSB [V]

V_{FST}(Ideal value) = AVR – 1.5 LSB [V]

V_{NT} : Voltage at which of digital output transitions from $(N - 1)_H$ to N_H.

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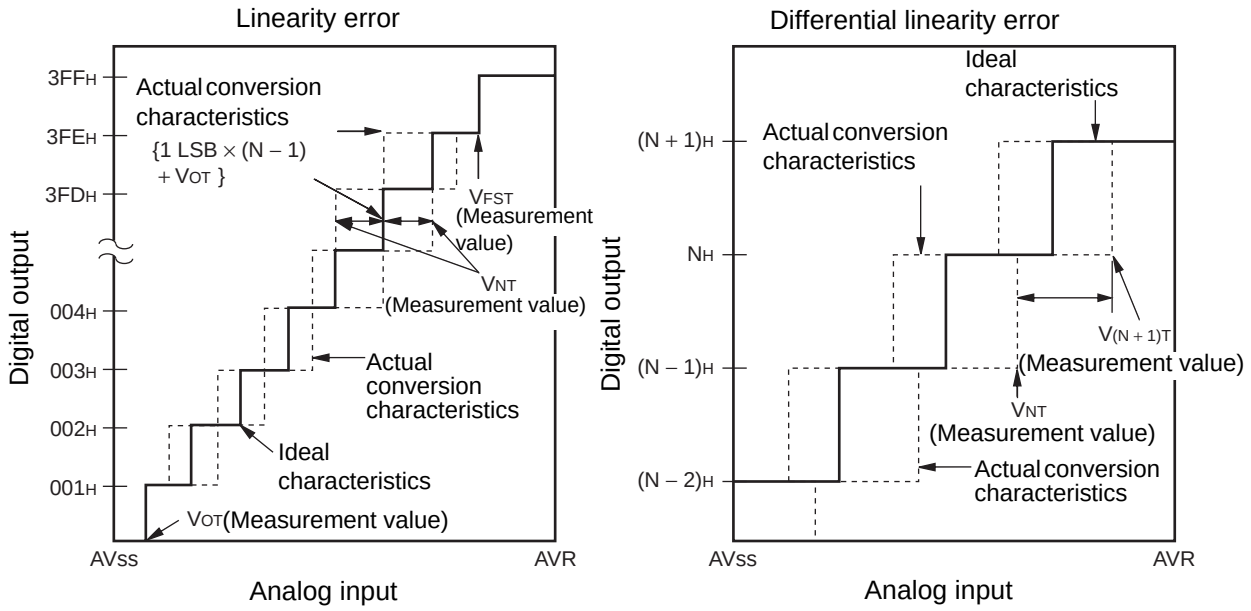


$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

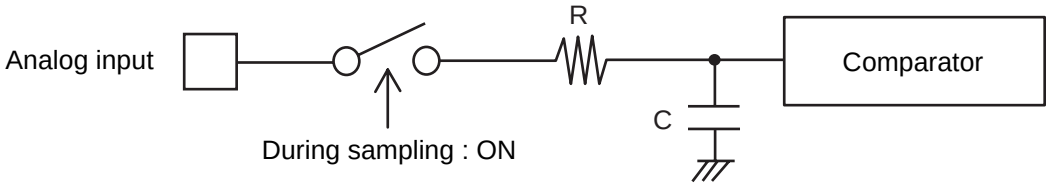
N : A/D converter digital output value

V_{OT} : Voltage at which of digital output transmissions from “000_H” to “001_H”.
V_{FST} : Voltage at which of digital output transmissions from “$3FE_H$” to “$3FF_H$”.

7. Notes on Using A/D Converter

- **About the external impedance of the analog input and its sampling time**
  - A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. And if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

• Analog input circuit model

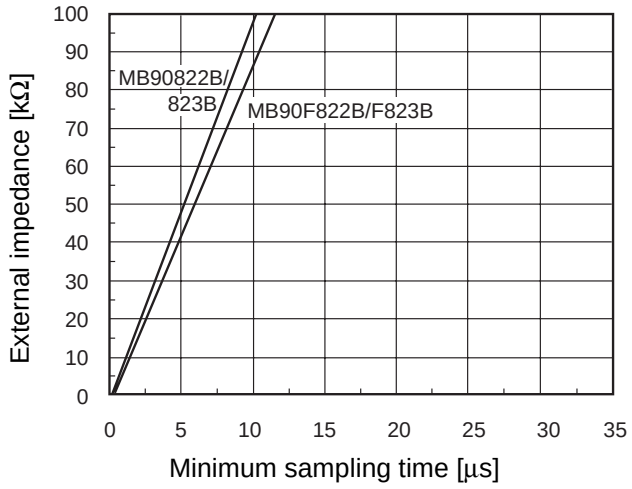


	R	C
MB90822B/823B	2.0 kΩ (Max)	14.4 pF (Max)
MB90F822B/F823B	2.0 kΩ (Max)	16.0 pF (Max)

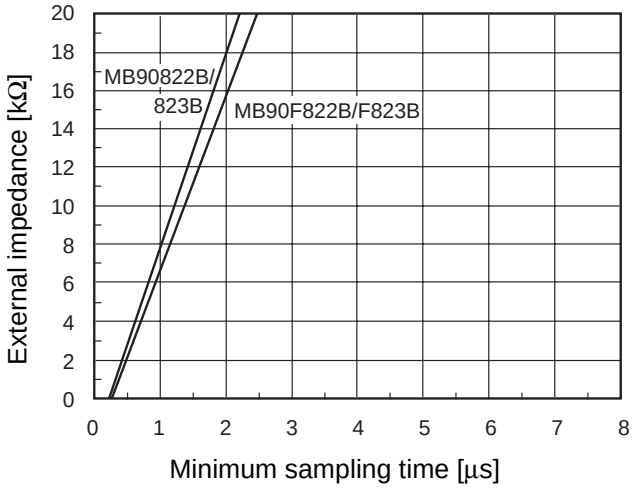
Note : The values are reference values.

• The relationship between the external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



- About the error
  The accuracy gets worse as $|AVR - AV_{SS}|$ becomes smaller.

8. Electrical Characteristics of D/A convertor

(V_{CC} = AV_{CC} = 4.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	8	—	bit	
Differential linearity error	—	—		—	—	±0.5	LSB	
Conversion time	—	—		—	0.45	—	µs	*
Analog output impedance	—	—		—	2.9	3.8	kΩ	
Power supply current	I_{DVR}	AV_{CC}		—	160	920	µA	
	I_{DVRS}			—	0.1	—	µA	D/A stops

* : With load capacitance 20 pF.

9. Flash Memory Program/Erase Characteristics

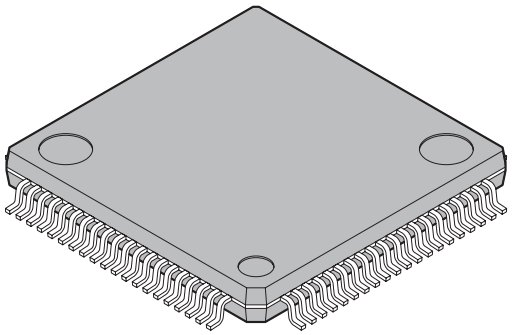
Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = +25 °C V_{CC} = 5.0 V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16 bit width) programing time		—	16	3,600	µs	Except for the overhead time of the system
Program/Erase cycle	—	10,000	—	—	cycle	
Flash data retention time	Average T_A = +85 °C	20	—	—	year	*

* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

■ ORDERING INFORMATION

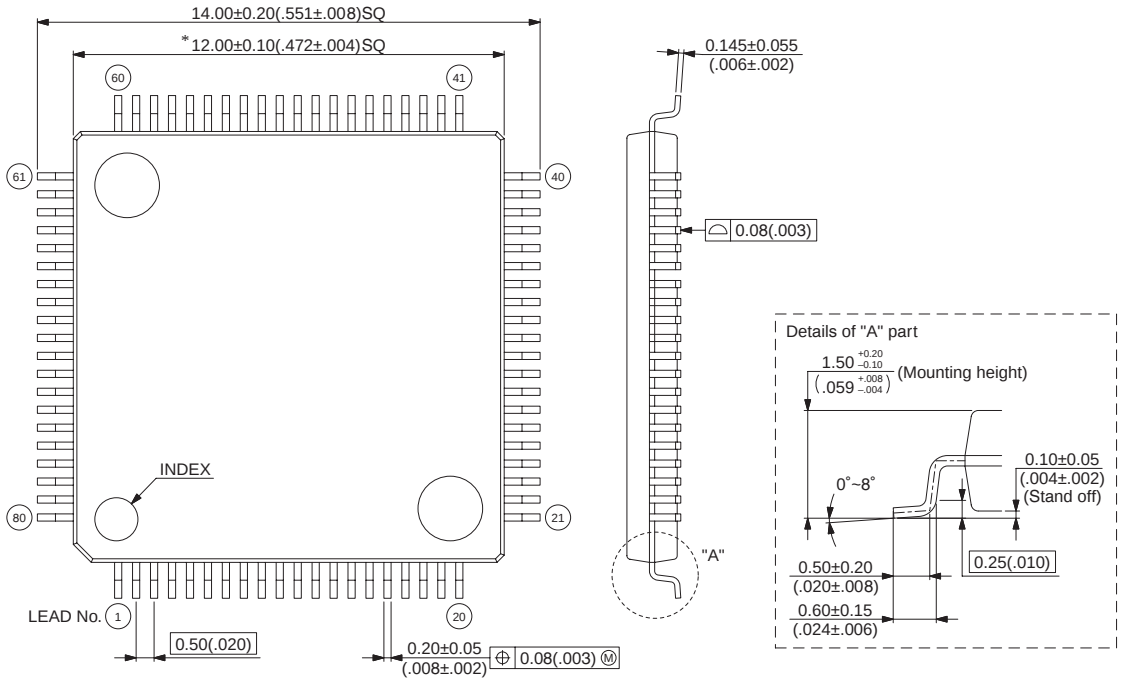
Part number	Package
MB90F823BPMC MB90F822BPMC MB90822BPMC MB90823BPMC MB90F828BPMC	80-pin plastic LQFP (FPT-80P-M21)
MB90F823BPMC1 MB90F822BPMC1 MB90822BPMC1 MB90823BPMC1 MB90F828BPMC1	80-pin plastic LQFP (FPT-80P-M22)
MB90F823BPF MB90F822BPF MB90822BPF MB90823BPF MB90F828BPF	80-pin plastic QFP (FPT-80P-M06)

■ PACKAGE DIMENSIONS

80-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width package length	12 mm 12 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.47 g
(FPT-80P-M21)	Code (Reference)	P-LFQFP80-12 12-0.50

80-pin plastic LQFP
(FPT-80P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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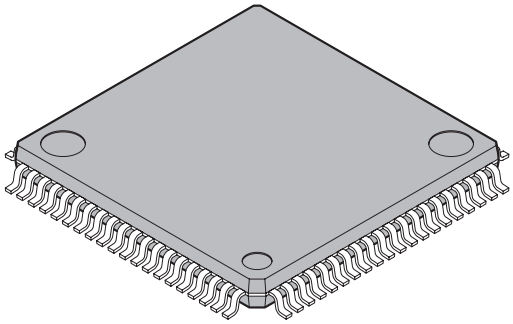
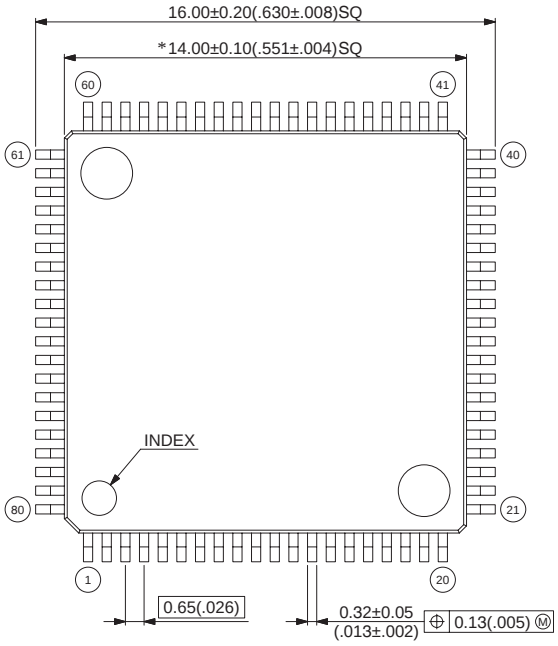
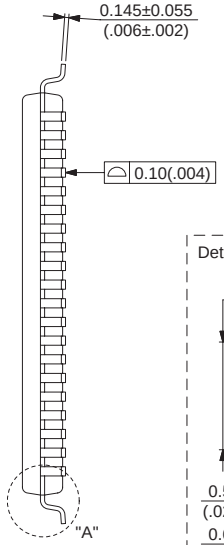
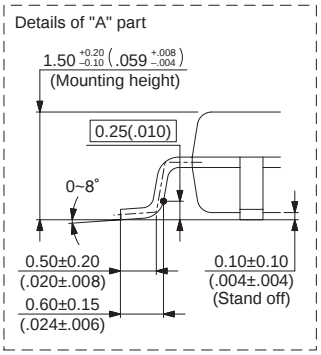
80-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width package length	14.00 mm 14.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.62 g
(FPT-80P-M22)	Code (Reference)	P-LFQFP80-14 14-0.65

80-pin plastic LQFP
(FPT-80P-M22)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.







Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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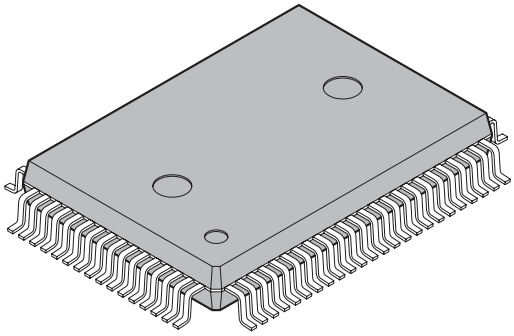
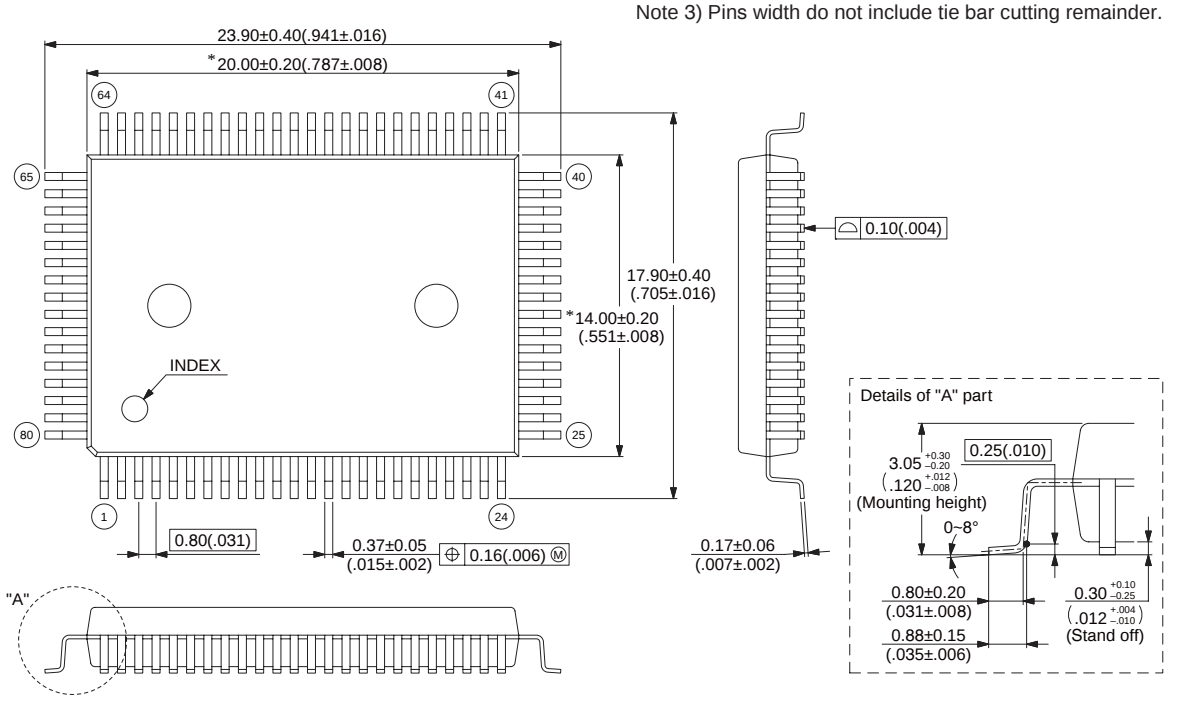
80-pin plastic QFP		
 (FPT-80P-M06)	Lead pitch	0.80 mm
	Package width package length	14.00 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP80-14 20-0.80

80-pin plastic QFP
(FPT-80P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
4	■ PACKAGE AND CORRESPONDING PRODUCTS	Changed the MB90822B (FPT-80P-M21). X : Not available → ○ : Available
43	■ ELECTRICAL CHARACTERISTICS 5. A/D Converter Electrical Characteristics	Changed the unit of zero transition voltage and full-scale transition voltage. mV → V
48	■ ORDERING INFORMATION	Added the part number. MB90822BPMC MB90823BPMC

The vertical lines marked in the left side of the page show the changes.

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FUJITSU MICROELECTRONICS LIMITED

Shinjuku Dai-Ichi Seimei Bldg. 7-1, Nishishinjuku 2-chome, Shinjuku-ku,
Tokyo 163-0722, Japan Tel: +81-3-5322-3347 Fax: +81-3-5322-3387
http://jp.fujitsu.com/fml/en/

For further information please contact:

North and South America
FUJITSU MICROELECTRONICS AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://www.fma.fujitsu.com/

Europe
FUJITSU MICROELECTRONICS EUROPE GmbH
Pittlerstrasse 47, 63225 Langen,
Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/microelectronics/

Korea
FUJITSU MICROELECTRONICS KOREA LTD.
206 KOSMO TOWER, 1002 Daechi-Dong,
Kangnam-Gu,Seoul 135-280
Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://www.fmk.fujitsu.com/

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE LTD.
151 Lorong Chuan, #05-08 New Tech Park,
Singapore 556741
Tel: +65-6281-0770 Fax: +65-6281-0220
http://www.fujitsu.com/sg/services/micro/semiconductor/

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.
Rm.3102, Bund Center, No.222 Yan An Road(E),
Shanghai 200002, China
Tel: +86-21-6335-1560 Fax: +86-21-6335-1605
http://cn.fujitsu.com/fmc/

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road
Tsimshatsui, Kowloon
Hong Kong
Tel: +852-2377-0226 Fax: +852-2376-3269
http://cn.fujitsu.com/fmc/tw

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