FUJITSU SEMICONDUCTOR
DATA SHEET

DS411-00003-1v0-E

ASSP

ISO/IEC 18000-6 Type-C Compliant FRAM Embedded UHF Band RFID LSI FerVID family™

MB97R803A/B, MB97R804A/B

■ OVERVIEW

This specification defines the LSI specification for the passive RFID Tag LSI “MB97R803A/B, MB97R804A/B” based on international standard “EPCglobal Class 1 Generation 2 (Ver.1.2.0).

In this document, the term “interrogator” used in the EPCglobal standard is changed to R/W (reader/writer) in accordance with customary practice. The term “Tag” is used as it is.

■ FEATURE

- Compliant with EPCglobal Class 1 Generation 2 (C1G2) Ver.1.2.0
  - Compliant with all UHF bands all over the world (carrier frequency: 860 MHz to 960 MHz)
  - High-speed data transmission (compliant with EPCglobal C1G2)
    R/W → Tag: 26.7 kbps to 128 kbps (when the counts of data 0 and 1are equal)
    Tag → R/W: 40 kbps to 640 kbps
  - DSB-ASK, SSB-ASK, PR-ASK modulation (compliant with EPCglobal C1G2)
  - Anti-collision function
  - Frequency Hopping
  - BlockPermalock: User memory area can be locked from writing in unit of 1 block (16 bits).
  - ReadLock (custom command): User memory area can be locked from reading in unit of 1 Area (256 bits)
- Serial Interface (SPI)
  - Accessible area: User memory area can be read/written through SPI.
  - Access control with RF interface is prioritized
  - Power supply: 2.3 V to 3.6 V (power is required for the memory access via SPI.)
  - Low power consumption : Operating current=70μA(Typ@2MHz), Standby current=10μA(Typ)
  - Power down mode : Power down current =10nA(Typ)
  - Package: 16-pin TSSOP (FPT-16P-M08)
- FRAM 4 Kbytes (4,096 bytes): High speed read/write Non-volatile memory
  - User Memory Area: 3,424 bytes
  - System Memory Area (including Reserved, EPC, and TID): 672 bytes
  - Read/Write Endurance: 10^{10} times
  - Memory Data Retention: 10years (+ 55 °C)

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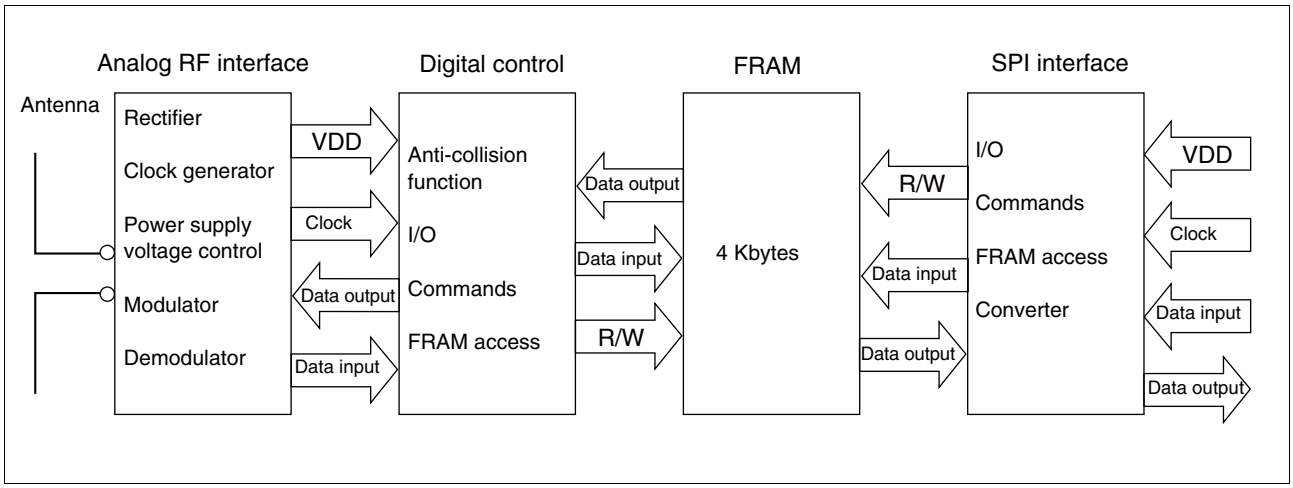
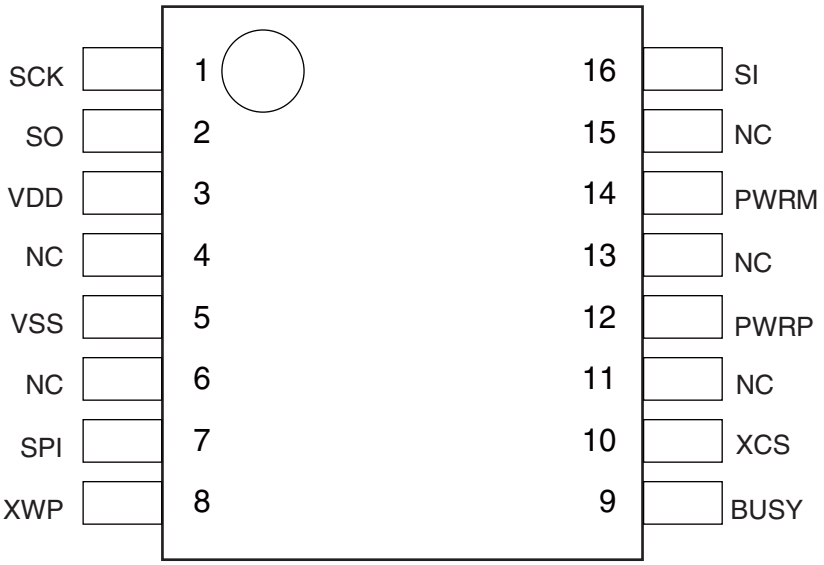
■ BLOCK DIAGRAM



■ PIN ASSIGNMENT



Pin Number	Pin Name	Interface	Function Description
12	PWRP	RF	Antenna pin
14	PWRM	RF	Antenna pin
9	BUSY	Serial	RF Interface Status pin
7	SPI	Serial	SPI Mode Switch pin
10	XCS	Serial	Chip Select pin
8	XWP	Serial	Write Protect pin
1	SCK	Serial	Serial Clock pin
16	SI	Serial	Serial Data Input pin
2	SO	Serial	Serial Data Output pin
3	VDD	Serial	Supply Voltage pin
5	VSS	Serial	Ground pin
4,6,11,13,15	NC	-	No Connection pin (There is no internal connection.)

■ RF INTERFACE

RF signal interface is compliant with EPCglobal C1G2 Ver.1.2.0 (as described in 6.3.1).

■ SERIAL INTERFACE

This LSI has SPI (Serial Peripheral Interface) interface. It is able to access FRAM User memory through the SPI interface. In this case, the external power supply is required.

1. Pin Function Description

The Serial Pin and its function descriptions are shown in the table below.

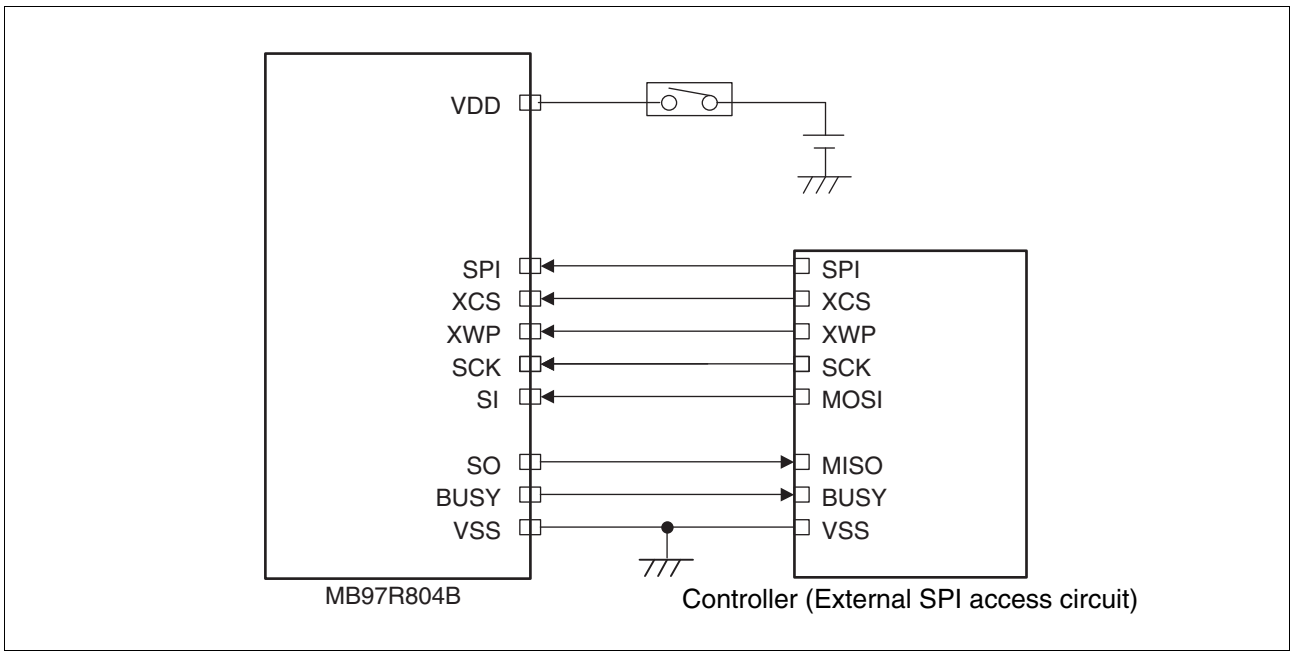
- Pin function

Pin Number	Pin Name	Function Description
9	BUSY	RF interface status pin When the VDD pin is set to ON during RF communication, BUSY will output “H”. In this status, Serial communication will be ignored even if RF and Serial communications are both being performed at the same time, because the chip can only perform RF communication when BUSY outputs “H”. Switching to the serial communication can be performed only when BUSY is “L”.
7	SPI	SPI Mode Switch pin This is an input pin to control to switch to Serial communication mode. When SPI is “H”, the LSI can be transfer to Serial communication mode.
10	XCS	Chip Select pin This is an input pin to select chip. When XCS is “H”, device is deselect (standby status) as long as the LSI is not write status internally. And SO becomes High-Z. In this case, inputs from all pins other than the antenna pin are ignored. When XCS is "L", the chip will be in selected state (active). XCS must fall before inputting op-code.
8	XWP	Write Protect pin This is an input pin to protect FRAM from writing.When WXP is “L”, FRAM memory is protected.
1	SCK	Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge. SO is output synchronously to a falling edge.
16	SI	Serial Data Input pin This is an input pin of serial data. It inputs op-code, address, and writing data.
2	SO	Serial Data Output pin This is an output pin of serial data. Reading data of FRAM memory are output. Its High-Z during standby.
3	VDD	Supply Voltage pin: 2.3 V to 3.6 V
5	VSS	Ground pin

2. Connection to SPI Interface

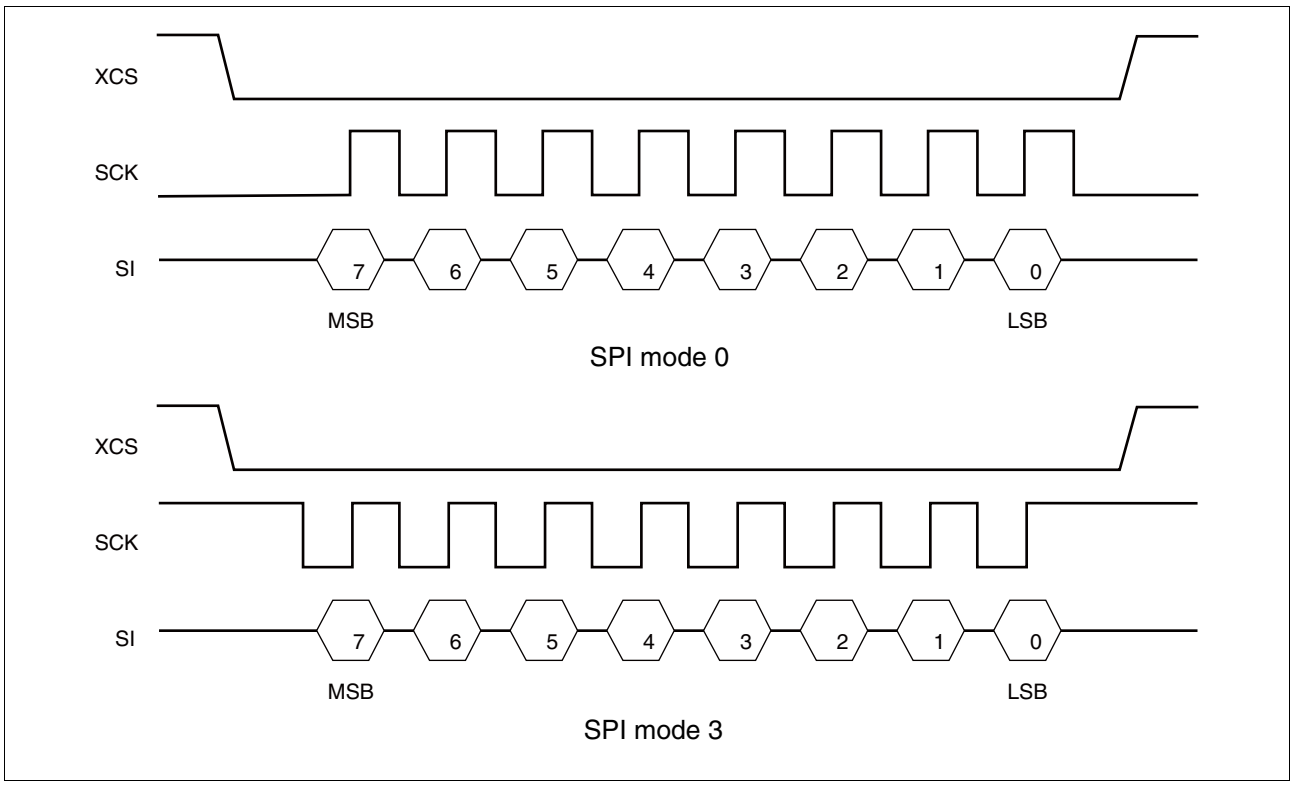
This LSI works as a slave of SPI. It can be connected to the microcontroller equipped with SPI port as shown in the figure below.

The external SPI controller shall monitor the BUSY signal. When BUSY signal is “H”, the external power must be disconnected and the other signal must be “L”.



3. SPI Mode

MB97R8030 is corresponding to the SPI mode 0 (CPOL = 0, CPHA = 0), and SPI mode 3.

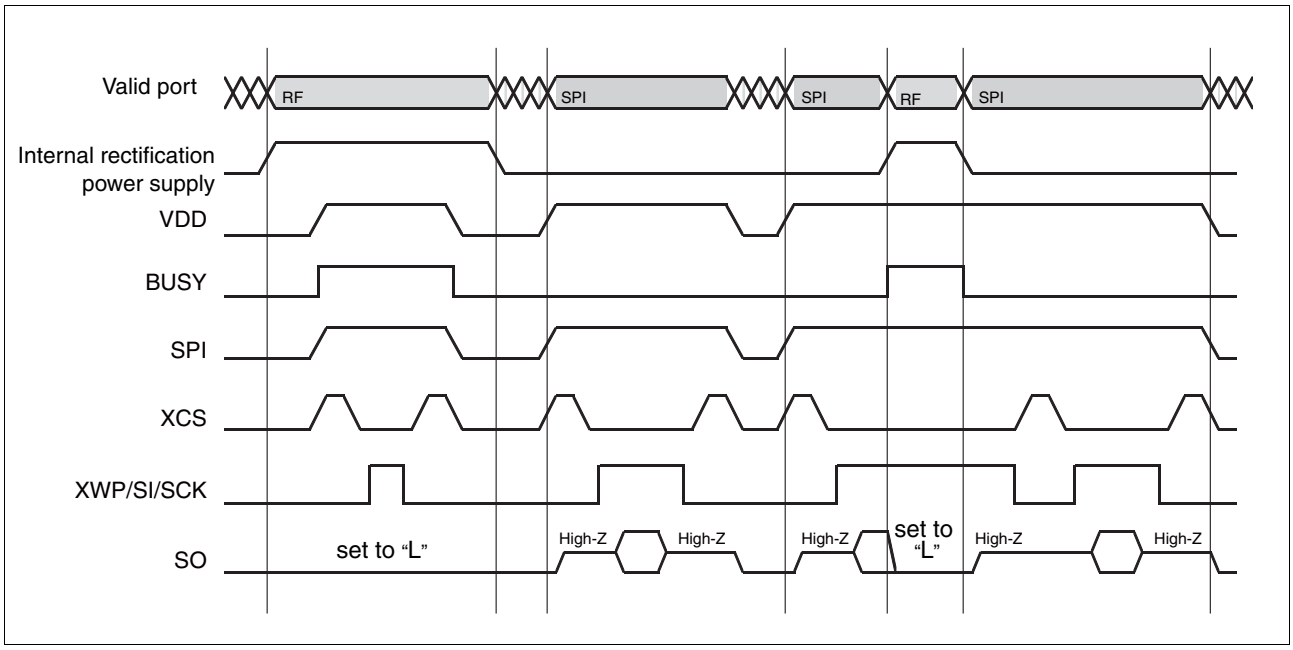


4. Arbitration between RF and SPI communication

This LSI has access arbitration feature when there is access from both RF I/F and SPI I/F simultaneously. In this case, RF communication has priority.
BUSY signal indicates that there is access from RF I/F, and it is validated when VDD is connected.

The controller needs to confirm the BUSY signal before changing to the SPI communication mode. When the BUSY signal is in “H”, the SPI communication is ignored if the SPI communication is performed at the same time because the LSI is executing RF communication.
The BUSY pin outputs “H” if the VDD pin is turned on during RF communication as the figure shown below.

- Arbitration between RF and SPI communication

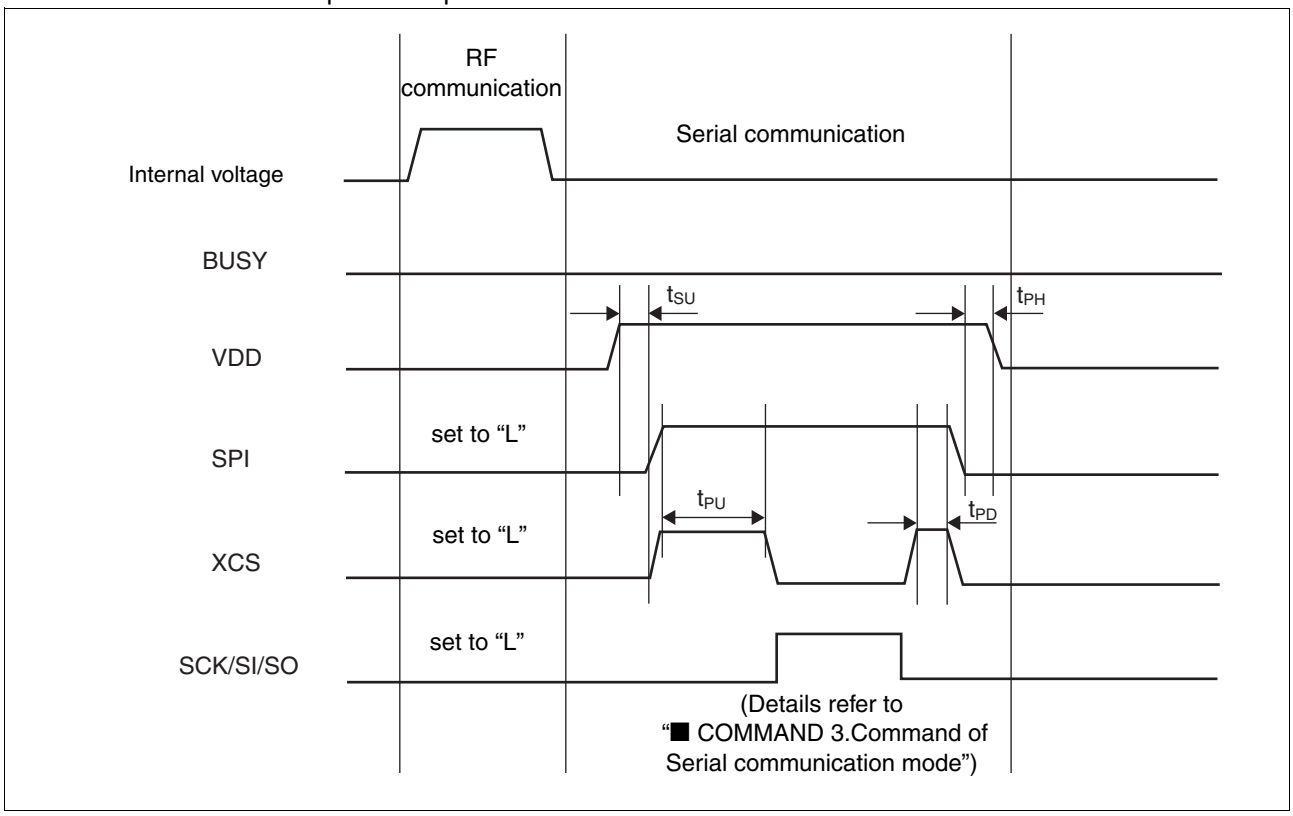


5. Power Sequence in Serial Communication Mode

The power sequence in Serial communication mode is shown in the figure below.

After asserting VDD, check that BUSY is “L” and then assert SPI and XCS at the same time. Wait for 1 ms or more after asserting XCS and then release XCS and begin Serial communication. The timing specifications for the power sequence are shown in the following table. Refer to “■ COMMAND 3. Command of Serial communication mode” for details on the Serial communication timing specifications.

- Serial communication power sequence



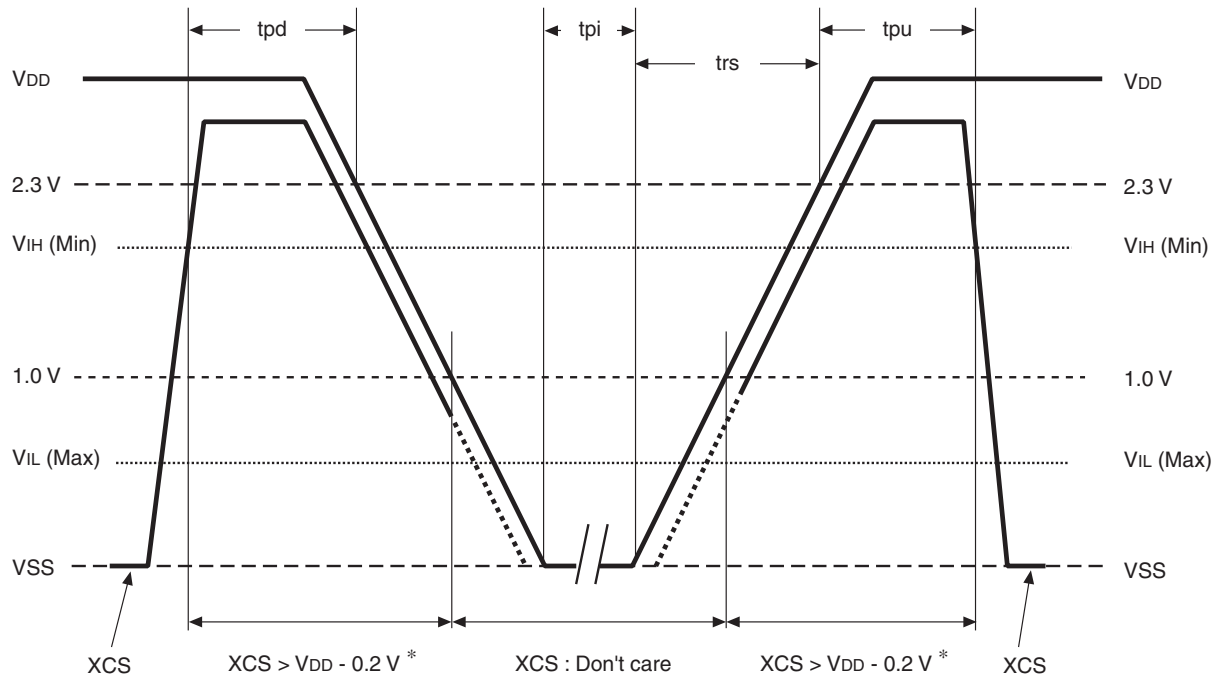
- Timing specifications during Serial communication

Parameter	Symbol	Value (Min)	Unit
SPI rising start time	t_{SU}	0	µs
Power supply hold time	t_{PH}	0	µs
XCS level hold time at power ON	t_{PU}	1000	µs
XCS level hold time at power OFF	t_{PD}	0.06	µs

6. XCS Level Hold Time at Power ON/OFF

Power ON/OFF sequence while switching to the serial communication is shown in the figure below and XCS level hold time at power ON/OFF is shown in the table below.

- Power ON/OFF sequence in serial communication



*: XCS (Max)< V_{DD} + 0.5 V

Note • Since power ON from middle-level may cause malfunction, VDD should rise from 0 V at power ON.
• If any operation other than the specified read cycle, write cycle or power ON/OFF sequence is performed, the stored data cannot be guaranteed.

Parameter	Symbol	Value		Unit
		Min	Max	
XCS level hold time at power OFF	tpd	0.06	—	us
XCS level hold time at power ON	tpu	1000	—	us
Power supply falling time	tpi	10		ms
Power supply rising time	trs	0.05	200	ms

■ MEMORY

1. Memory addressing

(1) Memory addressing in RF communication mode

Memory addressing in RF communication mode use Extensible bit vectors (EBV) format, which is compliant with EPCglobal C1G2 Ver1.2.0 (Annex A).

(2) Memory addressing in Serial communication mode

The logical address is used for memory addressing in Serial communication mode.

2. Memory Map

(1) Memory area

The memory is divided into the following five areas.

- Five memory areas

Name	Memory size	BANK	Address range	Access command	
				RF communication	SPI communication
User	1712w × 16b = 27,392bit	11	000H to 06AFH	R/W/S/BLW/BLE	R/W
TID	16w × 16b = 256bit	10	000H to 00FH	R/S	R
EPC	35w × 16b = 560bit	01	000H to 022H	R/W/S/BLW/BLE	R
Reserved	4w × 16b = 64bit	00	000H to 003H	R/W	—
System	14w × 16b = 224bit	—	—	L/BPL	*

* : Only lock and SPI error information can be read

Note : Command abbreviation:
R:READ, W: WRITE, S: SELECT, L: Lock, BPL: BlockPermalock, BLW: BlockWrite, BLE: BlockErase

The User, TID, EPC, and Reserved memory areas contain the data that is defined by the EPCglobal C1G2 specification (Chapter 6.3.2.1). The memory areas are also called as “Memory bank or “Bank” in EPC standard (In this specification, the User memory area is also called as “User memory ”).

In each memory bank, the logical address starts from zero (00H).

Logical addressing in EBV-8 format is used.

The system area stores user memory lock information and AreaGroup passwords.

The memory map is shown in shown in the table on next page. (The system area is not disclosed). The User memory consists of 7 Area Group and 107 Areas. The Area is defined as “16 × 16 bits word” (256 bits)” of data and each AreaGroup contains several areas. The first 6 AreaGroup contain 16 areas, the last AreaGroup contains 11 areas.

In addition, the idea of “Bank” “Area” and “AreaGroup” shall be ignored when using the Serial communication mode.

- Memory map

Bank	Logical Address (RF communication)			Logical Address (SPI)	Data Description		Size (word)	Total (word)	Total (bit)
	bank	(bit)	(word)						
USER	11	00000H - 000FFH	0000H - 000FH	0000H - 000FH	AreaGroup00	Area00	16	1,712	27,392
		00100H - 001FFH	0010H - 001FH	0010H - 001FH		Area01	16		
		00200H - 00EFFH	0020H - 00EFH	0020H - 00EFH		Area02 - 14	208		
		00F00H - 00FFFH	00F0H - 00FFH	00F0H - 00FFH		Area15	16		
		01000H - 01FFFH	0100H - 01FFH	0100H - 01FFH	AreaGroup01	Area00 - 15	256		
		02000H - 02FFFH	0200H - 02FFH	0200H - 02FFH	AreaGroup02	Area00 - 15	256		
		03000H - 03FFFH	0300H - 03FFH	0300H - 03FFH	AreaGroup03	Area00 - 15	256		
		04000H - 04FFFH	0400H - 04FFH	0400H - 04FFH	AreaGroup04	Area00 - 15	256		
		05000H - 05FFFH	0500H - 05FFH	0500H - 05FFH	AreaGroup05	Area00 - 15	256		
		06000H - 06AFFH	0600H - 06AFH	0600H - 06AFH	AreaGroup06	Area00 - 10	176		
EPC	1	00000H - 0000FH	0000H - 0000H	06C0H - 06C0H	StoredCRC16 (PC, EPC)		1	35	560
		00010H - 0001FH	0001H - 0001H	06C1H - 06C1H	StoredPC (Protocol Control)		1		
		00020H - 0020FH	0002H - 0020H	06C2H - 06E0H	EPC		31		
		00210H - 0021FH	0021H - 0021H	06E1H - 06E1H	XPC_W1		1		
		00220H - 0022FH	0022H - 0022H	06E2H - 06E2H	XPC_W2		1		
TID	10	00000H - 000FFH	0000H - 000FH	06F0H - 06FFH	TID		16	16	256
Re-served	00	00000H - 0000FH	0000H - 0000H	076CH - 076CH	KILL - Password[31:16]		1	4	64
		00010H - 0001FH	0001H - 0001H	076DH - 076DH	KILL - Password[15:0]		1		
		00020H - 0002FH	0002H - 0002H	076EH - 076EH	ACCESS - Password[31:16]		1		
		00030H - 0003FH	0003H - 0003H	076FH - 076FH	ACCESS - Password[15:0]		1		
Lock	—			06E5H - 06E5H	{LOCK[9:0], 5'h0, BPLI}		1	1	16
Read Lock	—			0778H - 0778H	AreaGroup00	Area00 - 15	1	7	112
				0779H - 0779H	AreaGroup01	Area00 - 15	1		
				077AH - 077AH	AreaGroup02	Area00 - 15	1		
				077BH - 077BH	AreaGroup03	Area00 - 15	1		
				077CH - 077CH	AreaGroup04	Area00 - 15	1		
				077DH - 077DH	AreaGroup05	Area00 - 15	1		
				077EH - 077EH	AreaGroup06	Area00 - 10	1		
BPL	——			0780H - 0780H	AreaGroup00	Area00	1	107	1,712
				0781H - 0781H		Area01	1		
				0782H - 078EH		Area02 - 14	13		
				078FH - 078FH		Area15	1		
				0790H - 079FH	AreaGroup01	Area00- 15	16		
				07A0H - 07AFH	AreaGroup02	Area00 - 15	16		
				07B0H - 07BFH	AreaGroup03	Area00 - 15	16		
				07C0H - 07CFH	AreaGroup04	Area00 - 15	16		
				07D0H - 07DFH	AreaGroup05	Area00 - 15	16		
				07E0H - 07EAH	AreaGroup06	Area00 - 10	11		

• **TID**

This LSI has a 96 bits TID that complies with EPC C1G2 standard. The TID consist of the 4 items shown in the following.

- An 8 bits data of EPC whose value is always “E2$_H$”(bit89 to bit96)
- “A 12 bits IC manufacture code whose values is always “010$_H$” (bit77 to bit88)
- Unique 60 bits serial number assigned by Fujitsu Semiconductor (bit17 to bit76)
- RFU 16 bits (bit1 to bit16)

Among the unique 60 bits serial number assigned by Fujitsu Semiconductor, the 8 bits from bit69 to bit76 define MB97R8030 code whose value is “03$_H$”. And 52 bits from bit17 to bit68 define chip information.

- TID configuration

MSB LSB

96 89	88 77	76 69	68 17	16 1
EPC standard	IC manufacture	“06$_H$”	Chip information	RFU*
“E2$_H$”	“010$_H$”	unique serial number assigned by FUJITSU SEMICONDUCTOR		

* : Reserved for Future Use

- Notes on TID

TID has been written in FRAM during shipment test by the Fujitsu Semiconductor. However, FUJITSU SEMICONDUCTOR do not guarantee that the data written in FRAM before IR reflow is still retained after IR reflow. If this may cause problems, TID should be written by the customer after IR reflow.

■ FLAGS AND RANDOM NUMBER GENERATOR

The inventoried flag, selected flag, and random number generator are compliant with EPCglobal C1G2 Ver. 1.2.0. (Chapter 6.3.2.2, 6.3.2.3, 6.3.2.5)

■ TAG STATES AND SLOT COUNTER

The Tag states and slot counter are compliant with EPCglobal C1G2 Ver. 1.2.0. (Chapter 6.3.2.4)

■ COLLISION ARBITRATION ALGORITHM

The collision arbitration algorithm is compliant with EPCglobal C1G2 Ver. 1.2.0. (Chapter 6.3.2.6, 6.3.2.7, 6.3.2.8, 6.3.2.9)

■ COMMAND

1. Command of RF communication mode.

This LSI supports all mandatory commands and optional commands that defined by EPCglobal C1G2 Ver. 1.2.0. (Chapter 6.3.2.11). In addition, the ChgAreaGroupPwd and ReadLock is supported as custom command. The commands list and codes is shown in the table below.
For BlockWrite and BlockErase command (Optional command), parts of the specifications are different form the EPC C1G2 standard as described in “(1)BlockWrite (Optional command)” and “(2)BlockErase (Optional command)”. ChgAreaGroupPwd and ReadLock command (Custom command) are described in “(4)ChgAreaGroupPwd (Custom command)” and “(5)ReadLock (Custom command)”. Initialize command(Proprietary command) is described in "(6)Initialize(Proprietary command)".

- Command of RF communication mode

Items	Command	Code
Mandatory	QueryRep	00
	ACK	01
	Query	1000
	QueryAdjust	1001
	Slect	1010
	NAK	11000000
	Req_RN	11000001
	Read	11000010
	Write	11000011
	Kill	11000100
	Lock	11000101
Optional	Access	11000110
	BlockWrite	11000111
	BlockErase	11001000
	BlockPermalock	11001001
Custom	ChgAreaGroupPwd	1110000000000100
	ReadLock	1110000000000111
Proprietary	Initialize	1110000100001111

Differences from EPCglobal C1G2 Ver. 1.2.0

- CRC-16

When the R/W writes the entire or part of the PC or EPC area of the Tag, CRC-16 stored in EPC memory 00_H to $0F_H$ of the Tag is disabled until an ACK command is received and a response that is not truncated (PC, EPC, CRC-16) is returned. After the completion of responding to ACK command, the correct CRC-16 value calculated during responding is written to EPC memory (00_H to $0F_H$) as well. If a truncated response to the ACK command is requested before CRC-16 is enabled, the CRC-16 value in the EPC memory, which has not been enabled, is returned as is.

- T4 time (time duration between commands sent by R/W)

The minimum value of T4 time is different from the value defined in EPC standards depending on the length of RTcal.

Length of RTcal	Minimum value of T4 time
44usec ≤ RTcal	2.0RTcal (EPC standards compliant)
22usec ≤ RTcal < 44usec	4.0RTcal
RTcal < 22usec	6.0RTcal

(1) BlockWrite (Optional command)

The following table shows the format of the BlockWrite command. Parts of the function of BlockWrite command are different form the EPCglobal C1G2 Ver.1.2.0 as following.

- MemBank : BlockWrite command can be executed in EPC and User memory bank. If BlockWrite command executed to the Reserved and TID bank, the LSI reply an error code.
- WordCount : If the WordCount is specified over 17 (11_H), the LSI will reply an error code.

If part of the words to be written is locked by the BlockPermaLock, the LSI reply an error code.

- BlockWrite command

	Command	MemBank	WordPtr	WordCount	Data	RN	CRC-16
# of bits	16	2	EBV	8	WordCount × 16	16	16
Description	1100 0111	01: EPC 11: User	Starting Address Pointer	Number of word to write	Data to be written	Handle	

(2) BlockErase (Optional command)

The following table shows the format of the BlockErase command. Parts function of BlockErase command are different form the EPCglobal C1G2 Ver.1.2.0 as described as follows.

- MemBank : BlockErase command can be executed in EPC and User memory bank. If BlockErase executed to the Reserved and TID bank, the LSI reply an error code.
- WordCount : If the WordCount is specified over 17 (11_H), this LSI will reply an error code.

If part of the words to be erased is locked by the BlockPermaLock, the LSI reply an error code.

- BlockErase command

	Command	MemBank	WordPtr	WordCount	RN	CRC-16
# of bits	16	2	EBV	8	16	16
Description	1100 1000	01: EPC 11: User	Starting Address Pointer	Number of word to erase	Handle	

(3) BlockPermaLock (Optional command)

This LSI, the unit of 1 Block is defined as 16 bits. The format of the BlockPermaLock command is shown in the table below. Parts function of the BlockPermaLock command are different form the EPCglobal C1G2 Ver.1.2.0 as described as follows.

- MemBank : BlockPermaLock command can be executed for User memory bank. If BlockPermaLock command executed to the EPC, Reserved and TID bank, the LSI reply an error code.
- BlockRange : If the BlockRange is specified over 17 (11_H), the LSI reply an error code.

- BlockPermaLock command

	Command	RFU	Read / Lock	MemBank	BlockPtr	Block Range	Mask	RN	CRC-16
# of bits	16	8	1	2	EBV	8	Variable	16	16
Description	1100 1001	00_H	0: Read 1: PermaLock	11:User	Mask starting address, specified in units of 16 blocks	Mask range, specified in units of 16 blocks	0: Retain current permalock setting 1: Assert permalock	Handle	

(4) ChgAreaGroupPwd (Custom command)

The following table “ChgAreaGroupPwd command” shows the format of the ChgAreaGroupPwd command. The R/W can use ChgAreaGroupPwd to change the password of each AreaGroup. To change the password of the AreaGroup, the R/W shall send the existing and new passwords. The initial password set as “0” at shipment stage from factory.
Only the tag in the secured or open state can execute the ChgBlockGroupPwd command.
ChgAreaGroupPwd has the following fields:

- AreaGroupPtr : This LSI has four 4 AreaGroup (01 to 03), which is specified with 2 bit value. 3 bit values from MSB shall be padded with Zero “0”
- Data: specifies the new password.
- Passwd specifies the current password.

The ChgBlockGroupPwd command also includes the Tag handle and CRC-16. The CRC-16 is calculated over the first command code bit to the last handle bit.
If a Tag in the open or secured state receives ChgAreaGroupPwd with a valid CRC-16 but an invalid handle, it shall ignore the ChgAreaGroupPwd and remain in its current state. If the password set in the Passwd field does not correspond to the stored value, the new password is not written. The Tag will not reply and return to the arbitrate state.

A ChgAreaGroupPwd shall be prepended with a frame-sync.

After issuing ChgAreaGroupPwd, the R/W transmit CW for the lesser of Treply or 20 ms, where Treply is the time between the R/W's ChgAreaGroupPwd command and Tag's backscattered reply. The R/W may observe several possible incomes from a ChgAreaGroupPwd, depending on the success or failure of the Tag's password change operation.

- ChgBlockGroupPwd succeeds: After complete the ChgAreaGroupPwd, the Tag return the response shown in table “• Tag reply to ChgAreaGroupPwd command”. The reply includes a header (“0” bit), Tag handle, and CRC-16 calculated over the “0” bit and handle. If the R/W observes this reply within 20 ms then the ChgAreaGroupPwd is completed successfully.
- The tag encounters an error: Tag returns an error code during the CW period rather than the reply shown in table “• Tag reply to ChgAreaGroupPwd command” (See “■COMMAND 4. Error of Serial communication mode” for the error code definition and reply format).
- Failure: If the R/W does not observe a reply within 20 ms then the ChgAreaGroupPwd does not complete successfully. The R/W may issue a Req_RN command (containing the Tag's handle) to verify that the tag is still in the R/W filed, and may reissue the ChgAreaGroupPwd.

Upon receiving a valid ChgAreaGroupPwd command, the Tag rewrites the AreaGroup password with the specified data. The new password is valid immediately after rewriting. The tag's reply to a ChgAreaGroupPwd use the extended preamble. (i.e., the Tag reply as if TRext = 1 regardless of the TRext value in the Query that initiated the round).

- ChgAreaGroupPwd command

	Command	AreaGroupPtr	Data	Password	RN	CRC-16
# of bits	16	5	32	32	16	16
Description	1110 0000 0000 0100	AreaGroupPtr	New Passwd	Current Passwd	Handle	

- Tag reply to ChgAreaGroupPwd command

	Header	RN	CRC-16
# of bits	1	16	16
Description	0	Handle	

(5) ReadLock (Custom command)

This LSI has the ReadLock function. The ReadLock command specifies the ReadLock status in the unit of Area (256 bits). The format of ReadLock command is shown in table "• ReadLock command".
Only the tag in the secured or open state can execute the ReadLock command.
ReadLock has the following fields:

- AreaGroupPtr : This LSI has four 4 AreaGroup (1 to 6), which is specified with 3 bit value. 2 bit values from MSB shall be padded with Zero "0".
- ReadLock contains a 32-bit payload defined as follows.
  - MASK0-15 0: Ignore the associated Action field and retain the current setting.
    1: Implement the associated Action field and overwrite the current ReadLock setting.
  - Action0-15 : Set the ReadLock status (1: Assert ReadLock, 0: Deassert ReadLock)
- Password: Set the corresponding password to the AreaGroup specified by the AreaGroupPtr. If the password is wrong, the ReadLock status can not be changed.

The AreaGroup6 does not contain Area 11 to Area 15, the setting toward these area is ignored.

The ReadLock command also includes the Tag handle and CRC-16. The CRC-16 is calculated over the first command code bit to the last handle bit.

If a Tag in the open or secured state receives ReadLock with a valid CRC-16 but an invalid handle, it shall ignore the ReadLock and remain in its current state.

A ReadLock shall be prepended with a frame-sync.

After issuing ReadLock, the R/W transmit CW for the lesser of Treply or 20 ms, where Treply is the time between the R/W's ReadLock command and Tag's backscattered reply. The R/W may observe several possible incomes from a ReadLock, depending on the success or failure of the Tag's memory lock operation.

- ReadLock succeeds : After complete the ReadLock, the Tag return the response shown in table "• Tag reply to ReadLock command". The reply includes a header ("0" bit), Tag handle, and CRC-16 calculated over the "0" bit and handle. If the R/W observes this reply within 20 ms then the ReadLock is completed successfully.
- The tag encounters an error: Tag returns an error code during the CW period rather than the reply shown in Table "• Tag reply to ReadLock command" (See "■COMMAND 4. Error of Serial communication mode" for the error code definition and reply format).
- Failure : If the R/W does not observe a reply within 20 ms then the ReadLock does not complete successfully. The R/W may issue a Req_RN command (containing the Tag's handle) to verify that the tag is still in the R/W filed, and may reissue the ReadLock.

Upon receiving a valid ReadLock command, the Tag perform the lock operation.

The tag's reply to a ReadLock use the extended preamble. (i.e., the Tag reply as if TRext = 1 regardless of the TRext value in the Query that initiated the round).

• ReadLock command

	Command	AreaGroupPtr	Payload	Password	RN	CRC-16
# of bits	16	5	32	32	16	16
Description	1110 0000 0000 0111	AreaGroupPtr	Mask/Action (See the table below)	32 bit password	Handle	

• ReadLock command payload

Payload																														
MASK																Action														
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

• Tag reply to ReadLock command

	Header	RN	CRC-16
# of bits	1	16	16
Description	0	Handle	

(6) Initialize (Proprietary command)

The following table shows the format of the Initialize command. This command is provided for manufacturer to initialize the memory area excepting TID bank and part of system area after the IR reflow during tag assembly process. Data area and Lock information area are overwriten with data zero(0) and disabled to be intialized again. Once this command is executed, the System Lock status becomes to be Normal.
Initialize command shall be prepended with a frame-sync. Return link frequency is specified by Query command issued previously.
Initialize command can be executed from all the state excepting Kill state, and no tag is idetified by inventory sequence. Therefore it is not allowed to execute Initialize command if multiple tags are existed in the RF communication fields of reader/writer.
The command sequence is described as following.

1. R/W issues Query, in which DR value and M value specifies return link frequency.
2. R/W issues initialize command. Data field in the command has to be "00h".
3. Tag confirms CRC16. If the CRC16 is invalid, tag ignores the command.
4. If SYSLOCK information is NORMAL or KILL, tag ignores the commad.
5. The memory area excepting TID bank and part of system area is initialized (data zero(0) is overwritten.)
6. NOMAL value is stored in SYSLOCK information.
7. Tag responds to the command as shown in the following table.

• Initialize command

	Command	Data	CRC-16
# of bits	16	8	16
Description	1110 0001 0000 1111	00H	

• Tag reply to Initialize command

	Header	CRC-16
# of bits	1	16
Description	0	

2. Error code of RF communication mode

The error code is compliant with EPCglobal C1G2 Ver. 1.2.0 (Annex I).

3. Command of Serial communication mode

This LSI accepts 2 commands specified in Op-code. Op-code is an 8 bits code as shown in the table below. If other codes are inputted, the command is ignored. If XCS is risen during the input sequence of Op-code, the command cant be executed.

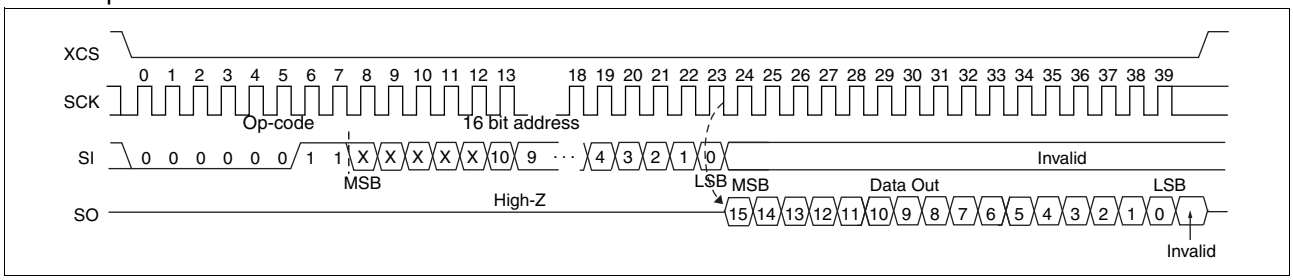
• Op-code of Serial interface

Name	Function	Op-code
READ	Read from memory area in unit of 16 bits	0000 0011
WRITE	Write to memory area in unit of 16 bits	0000 0010

(1) READ

The READ command is executed in units of 16 bits (1 word).
The memory addressing is described as table "■ MEMORY 2. Memory map • Memory map". The sequence of READ command is shown in the figure below.
Op-code and 16 bits address are input through SI. synchronously to the rising edge of SCK.
The upper 5 address bits don't care. Then, the data is read through SO synchronously to the falling edge of SCK.
During the data is read, the SI value is invalid. The reading address is automatically incremented by each 16-cycle clock input until XCS is rising. If the most significant address is reached, the counter rolls over to "0000_H".
The rising edge of XCS terminate the READ operation.
The READ command can be executed in the User memory, TID, EPC, and Lock status areas. If the specified areas are in Read Locked, "0000_H" is output instead of the data. If this LSI is in Kill status, the READ command is ignored.

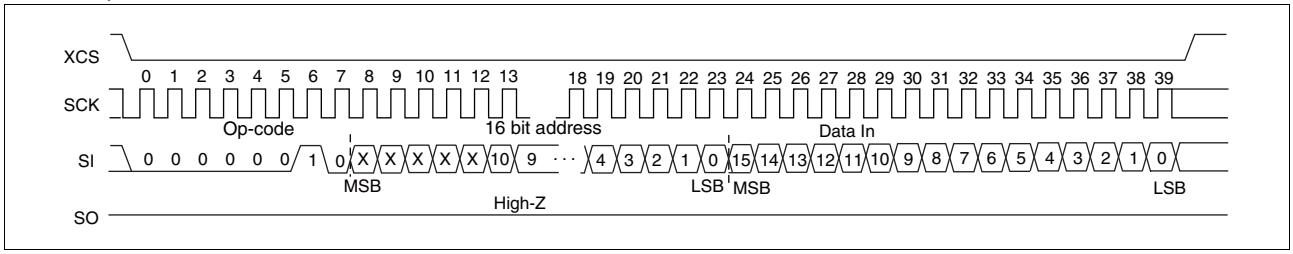
• Sequence of READ command.



(2) WRITE

The WRITE command is executed in units of 16 bits (1 word). The memory addressing is described as table"■ MEMORY 2. Memory map • Memory map".
The sequence of WRITE command is shown in the figure below.
Op-code, 16 bits address and 16 bits of writing data are input through SI synchronously to the rising edge of SCK.
The upper 5 address bits don't care. The writing address is automatically incremented by the following 16 bits data input until XCS is rising. If the most significant address is reached, the counter rolls over to "0000_H".
The rising edge of XCS terminate the write operation.
The WRITE command can be executed in the User memory areas. It writes error information to the SPI Error Information Register. (The error code is described in " ■COMMAND 4. Error of Serial communication mode")
If this LSI is in Kill status, the WRITE command is ignored.

• Sequence of WRITE command



4. Error of Serial Communication Mode

In Serial communication mode, if the LSI encounters an error when executing a READ/WRITE command, the error codes will be stored in the SPI Error Information Register.
When reading error occurred, “0000_H” is output instead of the data. When writing error occurred.

• SPI Error Information Register

The following table shows the format of error information that stored in the SPI Error Information Register (SPI_ERR_Info:address = 8000_H, see table “■ MEMORY 2. Memory map • Memory map”). The information can be read by the READ command. If the start bit of addresses for the following command is "0", the error information register will be cleared after an error occurs.

- SPI Error Information Register format

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	0	0	0	0	0	0	0	0	0	0	0	0	ERROR*			

* : ERROR
b1000 : Low voltage detection
b0100 : Write NG
b0010 : Read NG
b0001 : NG because RF occurred
b0000 : Finished successfully

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

Parameter	Symbol	Rating			Unit	Remarks
		Min	Typ	Max		
Maximum input voltage	Vmax	—	—	3.0	V	Between PWRP-PWRM
Power supply voltage	V_{DD}	− 0.5	—	+ 4.0	V	
Input voltage	V_{IN}	− 0.5	—	V_{DD} + 0.5	V	
Output voltage	V_{OUT}	− 0.5	—	V_{DD} + 0.5	V	
ESD voltage immunity	V_{ESD}	− 2	—	+ 2	kV	Human Body Model
	V_{ESD}	− 100	—	+ 100	V	Machine Model
Storage temperature	Tstg	− 40	—	+ 85	°C	Excluding FRAM data retention guarantee

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operation Conditions

Parameter		Symbol	Value			Unit	Remarks
			Min	Typ	Max		
Operating junction temperature		Tj	-20	—	+85	°C	
Retention guarantee temperature		Trtn1	-20	—	+55	°C	Retention guarantee period: 10years
RF communication	Antenna input frequency	Fclk	860	—	960	MHz	According to the Radio Law
	Reception modulation depth	(A-B)/A	80	90	100	%	
	Receiving bit rate	F_fwd	26.7	—	128	kbps	PIE code: mark rate = 1/2
	Receiving waveform rise time	Tr	1	—	500	µs	
	Receiving waveform settling time	Ts	—	—	1500	µs	
	Receiving waveform fall time	Tf	1	—	500	µs	
Serial communication	Power supply voltage	V_{DD}	2.3	3.3	3.6	V	
	“H” level input voltage	V_{IH}	V_{DD} − 0.2	—	V_{DD} + 0.3	V	
	“L”level input voltage	V_{IL}	− 0.3	—	+ 0.4	V	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. RF Communication Characteristics

Parameter		Symbol	Value			Unit	Conditionas/Remarks
			Min	Typ	Max		
Minimum operating power when reading		P_{R_MIN}	—	–6	—	dBm	Measured for TSSOP16 PKG Tari=25us, RTcal=3Tari,TRcal=2.6RTcal, DR=8,FM0,BLF=41kbps, DSB-ASK, Modulation depth=90%*
Minimum operating power when writing		P_{W_MIN}	—	–6	—	dBm	
Maximum operating power		P_{MAX}		18		dBm	
MB97R803A (Wafer)	Equivalent input capacitance	C_P	—	0.47	—	pF	Input power = -6dBm, paralel model (At 953MHz)
	Equivalent input resistance	R_P	—	2	—	KΩ	Input power = -6dBm, paralel model (At 953MHz)
MB97R804B (TSSOP)	Equivalent input capacitance	C_P	—	0.69	—	pF	Input power = -6dBm, paralel model (At 953MHz)
	Equivalent input resistance	R_P	—	1.7	—	KΩ	Input power = -6dBm, paralel model (At 953MHz)
Returning bit rate		F_rtrn	40		640	kbps	
Error of returning bit rate		Ftolerance	± 5		± 22	%	
Bit rate change during returning		Fvariation	–21		14	%	This is different from the value defined in EPC standards.

* : These characteristics are the values for the standalone LSI, and do not specify the values when the LSI is connected to other circuits such as a microcomputer.

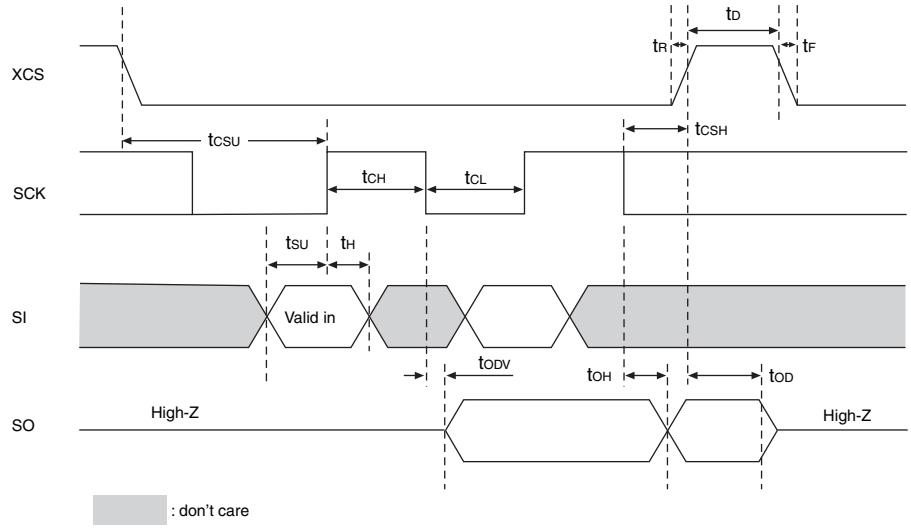
4. Serial Communication DC Characteristics

Parameter		Symbol	Value			Unit	Remarks
			Min	Typ	Max		
Input leakage current		I_{LI}	—	—	± 5	µA	V_{IN} = 0V to V_{DD}
Output leakage current		I_{LO}	—	—	± 5	µA	V_{OUT} = 0V to V_{DD}, when output pin is Hi-Z
Power supply	Operating current	I_{CC}	—	70	200	µA	SCK = 2MHz, Vdd=3.0V
	Power down current 1	I_{PD1}	—	0.01	5	µA	SPI = 0V or open XCS, XWP, SCK, SI = 0V or V_{DD} No RF reception
	Power down current 2	I_{PD2}	—	3	5	uA	SPI = 0V or open XCS, XWP, SCK, SI = 0V or V_{DD} RF receiving
	Standby current	I_{SB}	—	10	50	µA	SPI = V--$_{DD}$ XCS, XWP, SCK, SI = 0V or V_{DD}
Output voltage at “H” level		V_{OH}	V_{DD} × 0.8	—	V_{DD}	V	I_{OH} = –1mA
Output voltage at “L” level		V_{OL}	0	—	0.4	V	I_{OL} = 2mA
SPI pin pull-down resistance		R_{IN}	0.8	1	1.2	MΩ	V_{IN} = V_{DD}

5. Serial Communication AC Characteristics

Parameter	Symbol	Value		Unit
		Min	Max	
SCK clock frequency	f_{CK}	—	2	MHz
Clock high time	t_{CH}	200	—	ns
Clock low time	t_{CL}	30	—	ns
Chip select set time	t_{CSU}	10	—	ns
Chip select hold time	t_{CSH}	10	—	ns
Output disable time	t_{OD}	—	20	ns
Output data valid time	t_{ODV}	—	35	ns
Output hold time	t_{OH}	0	—	ns
Deselect time	t_D	200	—	ns
Data rise time	t_R	—	50	ns
Data fall time	t_F	—	50	ns
Data set up time	t_{SU}	10	—	ns
Data hold time	t_H	10	—	ns

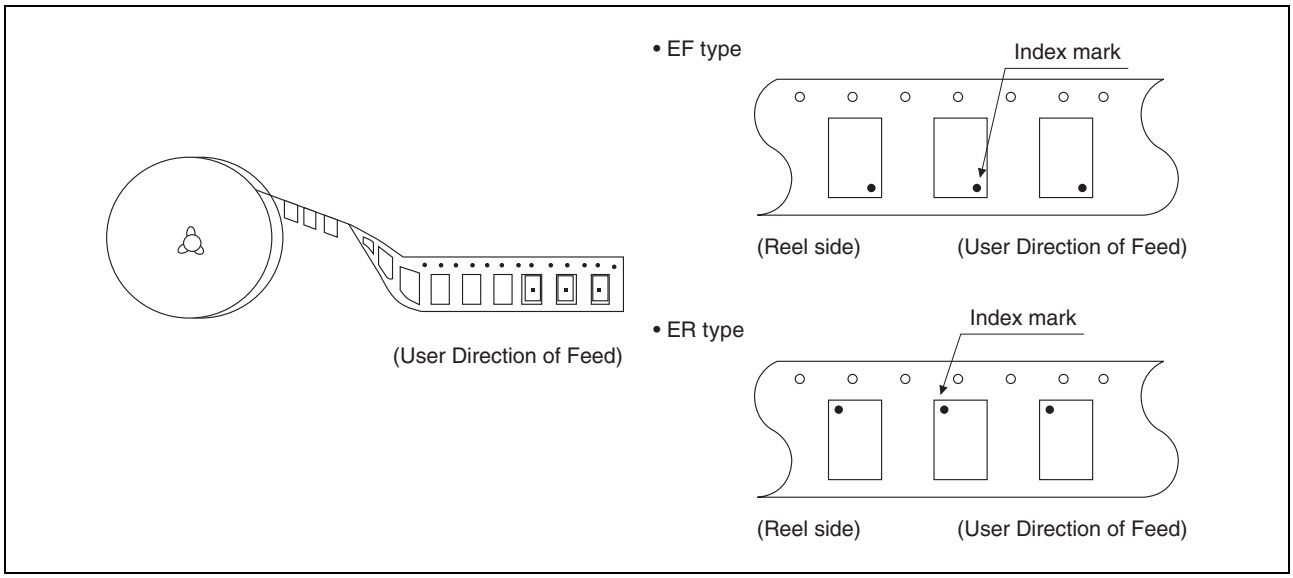
- Serial data timing



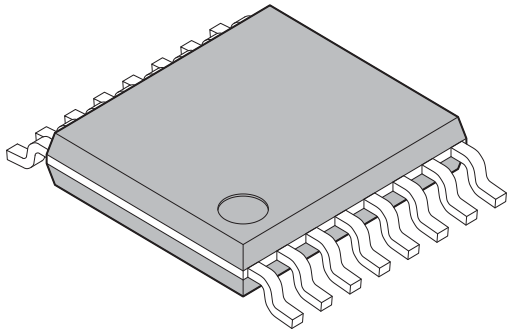
■ ORDERING INFORMATION

Part number	Interface	Shipping method	Wafer thickness	Remarks
MB97R803A-DIAP15	RF	Wafer (After dicing)	150 µm ± 25.4 µm	
MB97R804BPFT-G-JNEFE1	RF + SPI	TSSOP16 (Tape & Reel)	—	EF type*
MB97R804BPFT-G-JNERE1				ER type*

* : IC orientation

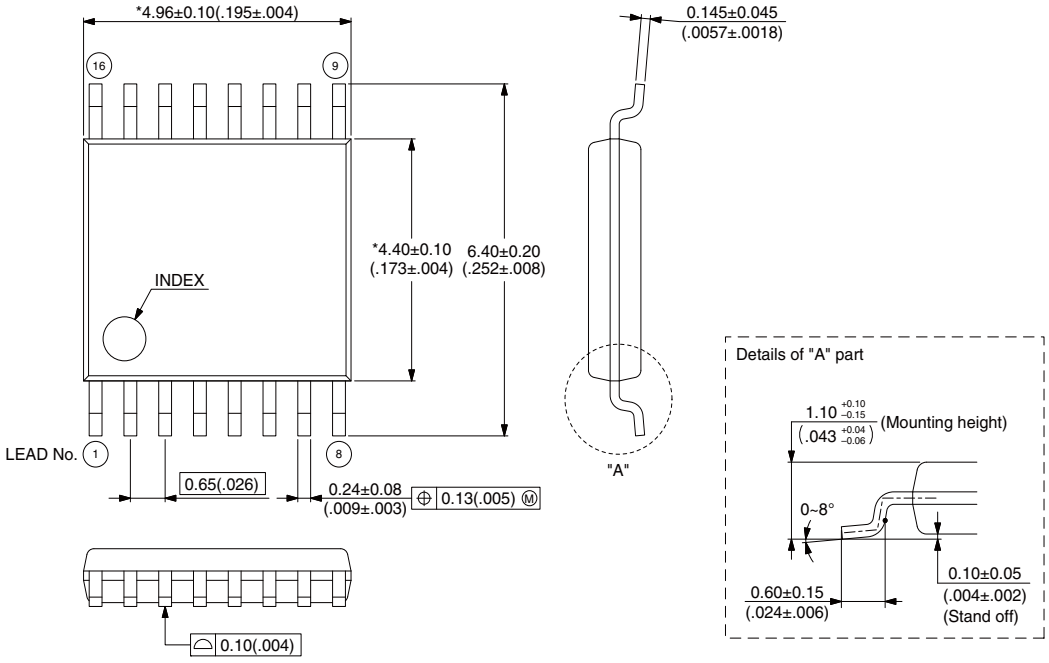


■ PACKAGE DIMENSION

16-pin plastic TSSOP		
	Lead pitch	0.65 mm
	Package width package length	4.40 mm 4.96 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm Max
	Weight	0.06 g
(FPT-16P-M08)		

16-pin plastic TSSOP
(FPT-16P-M08)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) * : These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

MEMO

MEMO

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Edited: Sales Promotion Department