FUJITSU SEMICONDUCTOR
DATA SHEET

DS704-00003-1v0-E

*16-bit Proprietary Microcontroller*

# F²MC-16FX MB96650 Series

## MB96F653R/A, MB96F655R/A
## MB96F656R, MB96F657R

### ■ DESCRIPTION

MB96650 series is based on FUJITSU's advanced F²MC-16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established F²MC-16LX family thus allowing for easy migration of F²MC-16LX Software to the new F²MC-16FX products. F²MC-16FX product improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For high processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 32MHz operation frequency from an external 4MHz to 8MHz resonator. The result is a minimum instruction cycle time of 31.2ns going together with excellent EMI behavior. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows selecting suitable operation frequencies for peripheral resources independent of the CPU speed.

Note: F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

FUJITSU SEMICONDUCTOR provides information facilitating product development via the following website. The website contains information useful for customers.

http://edevice.fujitsu.com/micom/en-support/


2012.12

FUJITSU

## ■ FEATURES

- Technology
  0.18µm CMOS

- CPU
  - $F^2$MC-16FX CPU
  - Optimized instruction set for controller applications
    (bit, byte, word and long-word data types, 23 different addressing modes, barrel shift, variety of pointers)
  - 8-byte instruction queue
  - Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available

- System clock
  - On-chip PLL clock multiplier (×1 to ×8, ×1 when PLL stop)
  - 4MHz to 8MHz crystal oscillator
    (maximum frequency when using ceramic resonator depends on Q-factor)
  - Up to 8MHz external clock for devices with fast clock input feature
  - 32.768kHz subsystem quartz clock
  - 100kHz/2MHz internal RC clock for quick and safe startup, clock stop detection function, watchdog
  - Clock source selectable from mainclock oscillator, subclock oscillator and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals
  - The subclock oscillator is enabled by the Boot ROM program controlled by a configuration marker after a Power or External reset
  - Low Power Consumption - 13 operating modes (different Run, Sleep, Timer, Stop modes)

- On-chip voltage regulator
  Internal voltage regulator supports a wide MCU supply voltage range (Min=2.7V), offering low power consumption

- Low voltage detection function
  Reset is generated when supply voltage falls below programmable reference voltage

- Code Security
  Protects Flash Memory content from unintended read-out

- DMA
  Automatic transfer function independent of CPU, can be assigned freely to resources

- Interrupts
  - Fast Interrupt processing
  - 8 programmable priority levels
  - Non-Maskable Interrupt (NMI)

- CAN
  - Supports CAN protocol version 2.0 part A and B
  - ISO16845 certified
  - Bit rates up to 1Mbps
  - 32 message objects
  - Each message object has its own identifier mask
  - Programmable FIFO mode (concatenation of message objects)
  - Maskable interrupt
  - Disabled Automatic Retransmission mode for Time Triggered CAN applications
  - Programmable loop-back mode for self-test operation

- USART
  - Full duplex USARTs (SCI/LIN)
  - Wide range of baud rate settings using a dedicated reload timer
  - Special synchronous options for adapting to different synchronous serial protocols
  - LIN functionality working either as master or slave LIN device
  - Extended support for LIN-Protocol to reduce interrupt load

- $I^2C$
  - Up to 400kbps
  - Master and Slave functionality, 7-bit and 10-bit addressing

- A/D converter
  - SAR-type
  - 8/10-bit resolution
  - Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
  - Range Comparator Function
  - Scan Disable Function

- Source Clock Timers

  Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)

- Hardware Watchdog Timer
  - Hardware watchdog timer is active after reset
  - Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval

- Reload Timers
  - 16-bit wide
  - Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
  - Event count function

- Free-Running Timers
  - Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
  - Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency

- Input Capture Units
  - 16-bit wide
  - Signals an interrupt upon external event
  - Rising edge, Falling edge or Both (rising & falling) edges sensitive

- Output Compare Units
  - 16-bit wide
  - Signals an interrupt when a match with Free-running Timer occurs
  - A pair of compare registers can be used to generate an output signal

- Programmable Pulse Generator
  - 16-bit down counter, cycle and duty setting registers
  - Can be used as $2 \times 8$-bit PPG
  - Interrupt at trigger, counter borrow and/or duty match
  - PWM operation and one-shot operation
  - Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock or of selected Reload timer underflow as clock input
  - Can be triggered by software or reload timer
  - Can trigger ADC conversion
  - Timing point capture
  - Start delay

- Quadrature Position/Revolution Counter (QPRC)
  - Up/down count mode, Phase difference count mode, Count mode with direction
  - 16-bit position counter
  - 16-bit revolution counter
  - Two 16-bit compare registers with interrupt
  - Detection edge of the three external event input pins AIN, BIN and ZIN is configurable

- Real Time Clock
  - Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
  - Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
  - Read/write accessible second/minute/hour registers
  - Can signal interrupts every half second/second/minute/hour/day
  - Internal clock divider and prescaler provide exact 1s clock

- External Interrupts
  - Edge or Level sensitive
  - Interrupt mask bit per channel
  - Each available CAN channel RX has an external interrupt for wake-up
  - Selected USART channels SIN have an external interrupt for wake-up

- Non Maskable Interrupt
  - Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
  - Once enabled, can not be disabled other than by reset
  - High or Low level sensitive
  - Pin shared with external interrupt 0

- I/O Ports
  - Most of the external pins can be used as general purpose I/O
  - All push-pull outputs (except when used as $I^2C$ SDA/SCL line)
  - Bit-wise programmable as input/output or peripheral signal
  - Bit-wise programmable input enable
  - One input level per GPIO-pin (either Automotive or CMOS hysteresis)
  - Bit-wise programmable pull-up resistor

- Built-in On Chip Debugger (OCD)
  - One-wire debug tool interface
  - Break function:
    - Hardware break: 6 points (shared with code event)
    - Software break: 4096 points
  - Event function
    - Code event: 6 points (shared with hardware break)
    - Data event: 6 points
    - Event sequencer: 2 levels + reset
  - Execution time measurement function
  - Trace function: 42 branches
  - Security function

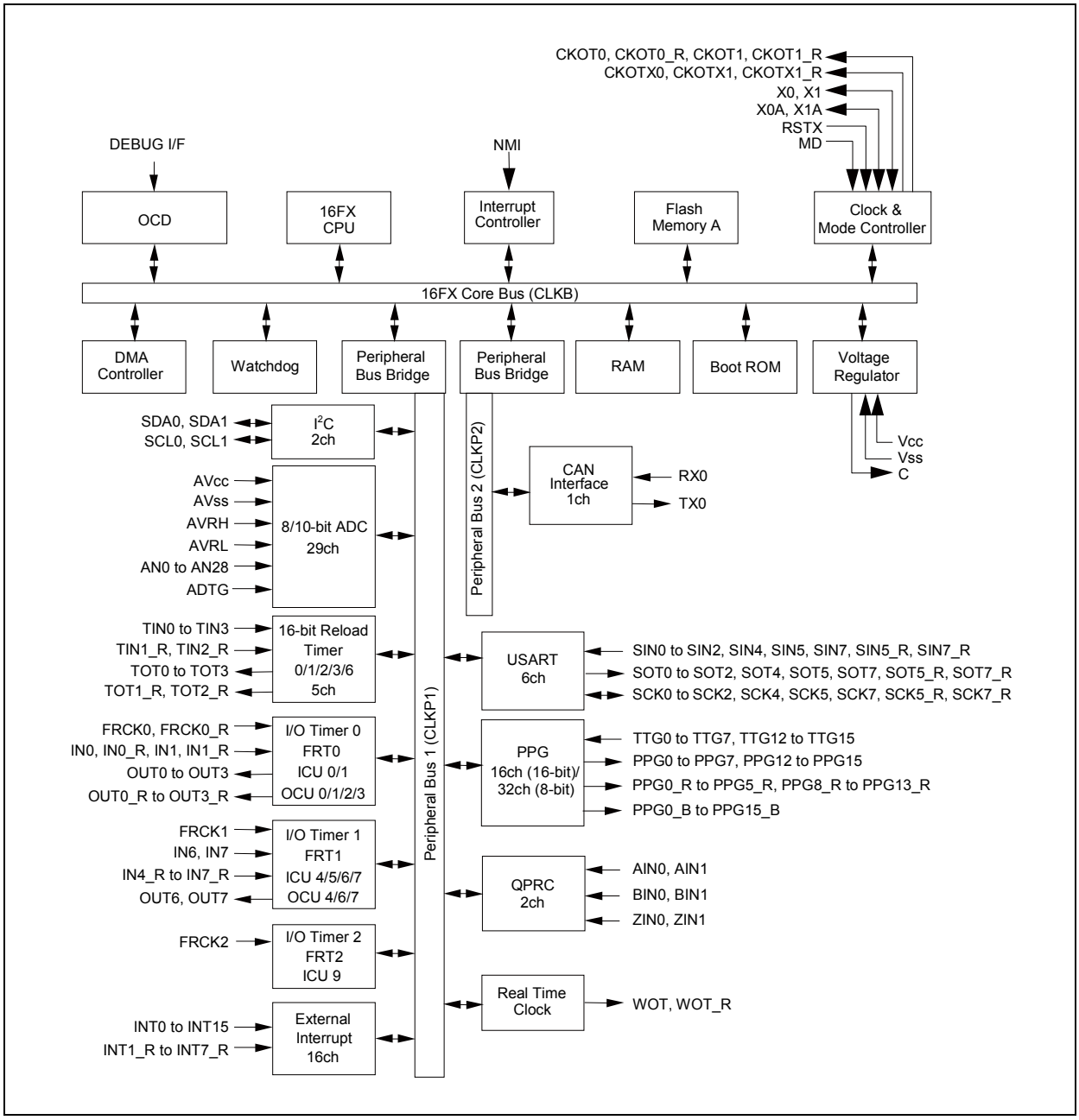
- Flash Memory
  - Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
  - Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
  - Supports automatic programming, Embedded Algorithm
  - Write/Erase/Erase-Suspend/Resume commands
  - A flag indicating completion of the automatic algorithm
  - Erase can be performed on each sector individually
  - Sector protection
  - Flash Security feature to protect the content of the Flash
  - Low voltage detection during Flash erase or write

## ■ PRODUCT LINEUP

| Features | | MB96650 | Remark |
|---|---|---|---|
| Product Type | | Flash Memory Product | |
| Subclock | | Subclock can be set by software | |
| Dual Operation Flash Memory | RAM | - | |
| 64.5KB + 32KB | 10KB | MB96F653R, MB96F653A | Product Options<br>R: MCU with CAN<br>A: MCU without CAN |
| 128.5KB + 32KB | 16KB | MB96F655R, MB96F655A | |
| 256.5KB + 32KB | 24KB | MB96F656R | |
| 384.5KB + 32KB | 28KB | MB96F657R | |
| Package | | LQFP-120<br>FPT-120P-M21 | |
| DMA | | 4ch | |
| USART | | 6ch | LIN-USART 0 to 2/4/5/7 |
| | with automatic LIN-Header transmission/reception | Yes (only 1ch) | LIN-USART 0 |
| | with 16 byte RX- and TX-FIFO | No | |
| $I^2C$ | | 2ch | $I^2C$ 0/1 |
| 8/10-bit A/D Converter | | 29ch | AN 0 to 28 |
| | with Data Buffer | No | |
| | with Range Comparator | Yes | |
| | with Scan Disable | Yes | |
| | with ADC Pulse Detection | No | |
| 16-bit Reload Timer (RLT) | | 5ch | RLT 0 to 3/6 |
| 16-bit Free-Running Timer (FRT) | | 3ch | FRT 0 to 2 |
| 16-bit Input Capture Unit (ICU) | | 7ch<br>(1 channel for LIN-USART) | ICU 0/1/4 to 7/9<br>ICU 9 for LIN-USART |
| 16-bit Output Compare Unit (OCU) | | 7ch | OCU 0 to 4/6/7<br>(OCU 4 for FRT clear) |
| 8/16-bit Programmable Pulse Generator (PPG) | | 16ch (16-bit) / 32ch (8-bit) | PPG 0 to 15 |
| | with Timing point capture | Yes | |
| | with Start delay | Yes | |
| | with Ramp | No | |
| Quadrature Position/Revolution Counter (QPRC) | | 2ch | QPRC 0/1 |
| CAN Interface | | 1ch | CAN 0<br>32 Message Buffers |
| External Interrupts (INT) | | 16ch | INT 0 to 15 |
| Non-Maskable Interrupt (NMI) | | 1ch | |
| Real Time Clock (RTC) | | 1ch | |
| I/O Ports | | 99 (Dual clock mode)<br>101 (Single clock mode) | |
| Clock Calibration Unit (CAL) | | 1ch | |
| Clock Output Function | | 2ch | |
| Low Voltage Detection Function | | Yes | Low voltage detection function can be disabled by software |
| Hardware Watchdog Timer | | Yes | |
| On-chip RC-oscillator | | Yes | |
| On-chip Debugger | | Yes | |

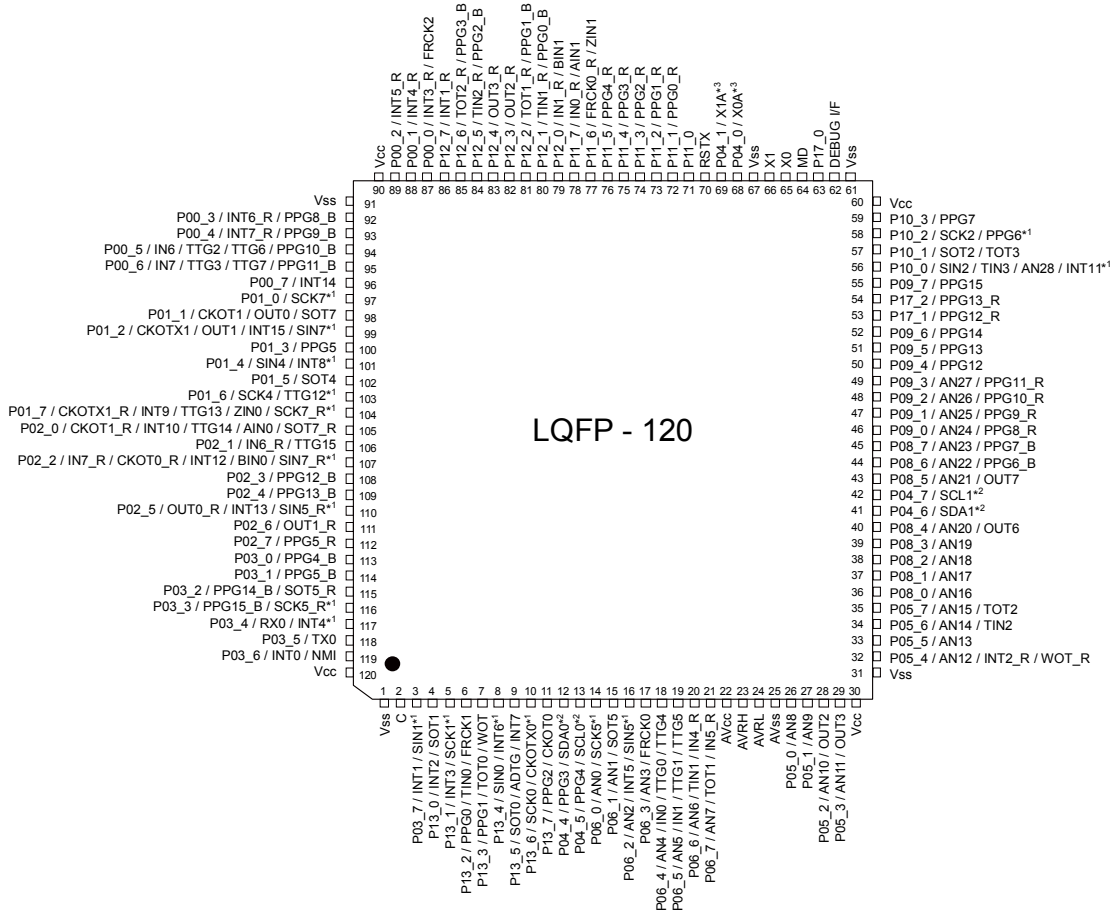
Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the general I/O port according to your function use.

## ■ BLOCK DIAGRAM



## ■ PIN ASSIGNMENT

(Top view)




(FPT-120P-M21)

*1: CMOS input level only
*2: CMOS input level only for $I^2C$
*3: Please set ROM Configuration Block (RCB) to use the subclock.
Other than those above, general-purpose pins have only Automotive input level.

## ■ PIN DESCRIPTION

| Pin name | Feature | Description |
|---|---|---|
| ADTG | ADC | A/D converter trigger input pin |
| AINn | QPRC | Quadrature Position/Revolution Counter Unit n input pin |
| ANn | ADC | A/D converter channel n input pin |
| AVcc | Supply | Analog circuits power supply pin |
| AVRH | ADC | A/D converter high reference voltage input pin |
| AVRL | ADC | A/D converter low reference voltage input pin |
| AVss | Supply | Analog circuits power supply pin |
| BINn | QPRC | Quadrature Position/Revolution Counter Unit n input pin |
| C | Voltage regulator | Internally regulated power supply stabilization capacitor pin |
| CKOTn | Clock Output function | Clock Output function n output pin |
| CKOTn_R | Clock Output function | Relocated Clock Output function n output pin |
| CKOTXn | Clock Output function | Clock Output function n inverted output pin |
| CKOTXn_R | Clock Output function | Relocated Clock Output function n inverted output pin |
| DEBUG I/F | OCD | On Chip Debugger input/output pin |
| FRCKn | Free-Running Timer | Free-Running Timer n input pin |
| FRCKn_R | Free-Running Timer | Relocated Free-Running Timer n input pin |
| INn | ICU | Input Capture Unit n input pin |
| INn_R | ICU | Relocated Input Capture Unit n input pin |
| INTn | External Interrupt | External Interrupt n input pin |
| INTn_R | External Interrupt | Relocated External Interrupt n input pin |
| MD | Core | Input pin for specifying the operating mode |
| NMI | External Interrupt | Non-Maskable Interrupt input pin |
| OUTn | OCU | Output Compare Unit n waveform output pin |
| OUTn_R | OCU | Relocated Output Compare Unit n waveform output pin |
| Pnn_m | GPIO | General purpose I/O pin |
| PPGn | PPG | Programmable Pulse Generator n output pin (16bit/8bit) |
| PPGn_R | PPG | Relocated Programmable Pulse Generator n output pin (16bit/8bit) |
| PPGn_B | PPG | Programmable Pulse Generator n output pin (16bit/8bit) |
| RSTX | Core | Reset input pin |
| RXn | CAN | CAN interface n RX input pin |
| SCKn | USART | USART n serial clock input/output pin |
| SCKn_R | USART | Relocated USART n serial clock input/output pin |
| SCLn | $I^2C$ | $I^2C$ interface n clock I/O input/output pin |
| SDAn | $I^2C$ | $I^2C$ interface n serial data I/O input/output pin |
| SINn | USART | USART n serial data input pin |
| SINn_R | USART | Relocated USART n serial data input pin |
| SOTn | USART | USART n serial data output pin |
| SOTn_R | USART | Relocated USART n serial data output pin |
| TINn | Reload Timer | Reload Timer n event input pin |
| TINn_R | Reload Timer | Relocated Reload Timer n event input pin |
| TOTn | Reload Timer | Reload Timer n output pin |
| TOTn_R | Reload Timer | Relocated Reload Timer n output pin |
| TTGn | PPG | Programmable Pulse Generator n trigger input pin |
| TXn | CAN | CAN interface n TX output pin |

| Pin name | Feature | Description |
|---|---|---|
| Vcc | Supply | Power supply pin |
| Vss | Supply | Power supply pin |
| WOT | RTC | Real Time clock output pin |
| WOT_R | RTC | Relocated Real Time clock output pin |
| X0 | Clock | Oscillator input pin |
| X0A | Clock | Subclock Oscillator input pin |
| X1 | Clock | Oscillator output pin |
| X1A | Clock | Subclock Oscillator output pin |
| ZINn | QPRC | Quadrature Position/Revolution Counter Unit n input pin |

## ■ PIN CIRCUIT TYPE

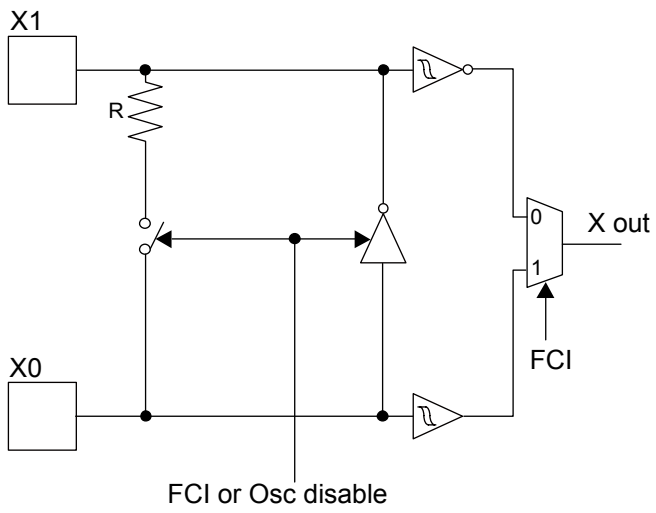
| Pin no. | I/O circuit type* | Pin name |
|---|---|---|
| 1 | Supply | Vss |
| 2 | F | C |
| 3 | M | P03_7 / INT1 / SIN1 |
| 4 | H | P13_0 / INT2 / SOT1 |
| 5 | M | P13_1 / INT3 / SCK1 |
| 6 | H | P13_2 / PPG0 / TIN0 / FRCK1 |
| 7 | H | P13_3 / PPG1 / TOT0 / WOT |
| 8 | M | P13_4 / SIN0 / INT6 |
| 9 | H | P13_5 / SOT0 / ADTG / INT7 |
| 10 | M | P13_6 / SCK0 / CKOTX0 |
| 11 | H | P13_7 / PPG2 / CKOT0 |
| 12 | N | P04_4 / PPG3 / SDA0 |
| 13 | N | P04_5 / PPG4 / SCL0 |
| 14 | I | P06_0 / AN0 / SCK5 |
| 15 | K | P06_1 / AN1 / SOT5 |
| 16 | I | P06_2 / AN2 / INT5 / SIN5 |
| 17 | K | P06_3 / AN3 / FRCK0 |
| 18 | K | P06_4 / AN4 / IN0 / TTG0 / TTG4 |
| 19 | K | P06_5 / AN5 / IN1 / TTG1 / TTG5 |
| 20 | K | P06_6 / AN6 / TIN1 / IN4_R |
| 21 | K | P06_7 / AN7 / TOT1 / IN5_R |
| 22 | Supply | AVcc |
| 23 | G | AVRH |
| 24 | G | AVRL |
| 25 | Supply | AVss |
| 26 | K | P05_0 / AN8 |
| 27 | K | P05_1 / AN9 |
| 28 | K | P05_2 / AN10 / OUT2 |
| 29 | K | P05_3 / AN11 / OUT3 |
| 30 | Supply | Vcc |
| 31 | Supply | Vss |
| 32 | K | P05_4 / AN12 / INT2_R / WOT_R |
| 33 | K | P05_5 / AN13 |
| 34 | K | P05_6 / AN14 / TIN2 |
| 35 | K | P05_7 / AN15 / TOT2 |
| 36 | K | P08_0 / AN16 |
| 37 | K | P08_1 / AN17 |
| 38 | K | P08_2 / AN18 |
| 39 | K | P08_3 / AN19 |
| 40 | K | P08_4 / AN20 / OUT6 |

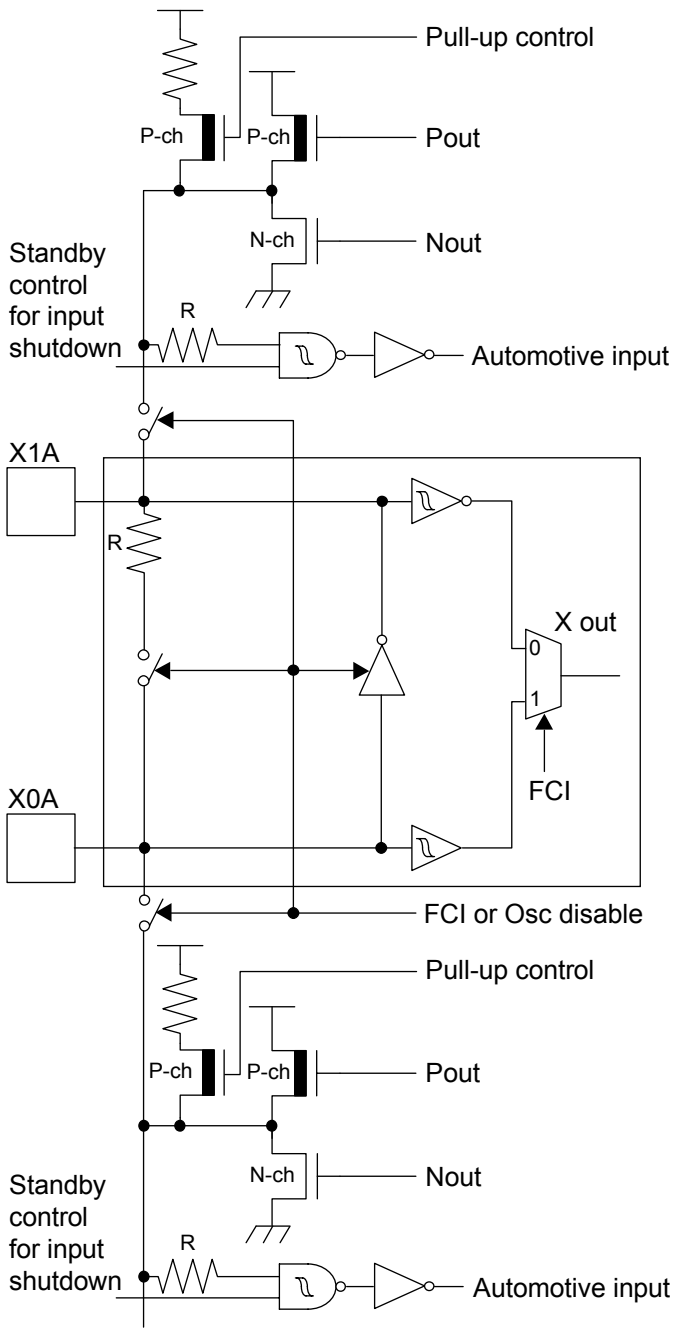
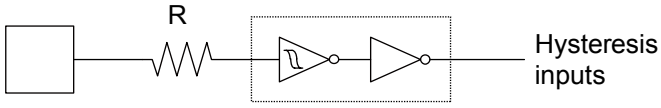
| Pin no. | I/O circuit type* | Pin name |
|---|---|---|
| 41 | N | P04_6 / SDA1 |
| 42 | N | P04_7 / SCL1 |
| 43 | K | P08_5 / AN21 / OUT7 |
| 44 | K | P08_6 / AN22 / PPG6_B |
| 45 | K | P08_7 / AN23 / PPG7_B |
| 46 | K | P09_0 / AN24 / PPG8_R |
| 47 | K | P09_1 / AN25 / PPG9_R |
| 48 | K | P09_2 / AN26 / PPG10_R |
| 49 | K | P09_3 / AN27 / PPG11_R |
| 50 | H | P09_4 / PPG12 |
| 51 | H | P09_5 / PPG13 |
| 52 | H | P09_6 / PPG14 |
| 53 | H | P17_1 / PPG12_R |
| 54 | H | P17_2 / PPG13_R |
| 55 | H | P09_7 / PPG15 |
| 56 | I | P10_0 / SIN2 / TIN3 / AN28 / INT11 |
| 57 | H | P10_1 / SOT2 / TOT3 |
| 58 | M | P10_2 / SCK2 / PPG6 |
| 59 | H | P10_3 / PPG7 |
| 60 | Supply | Vcc |
| 61 | Supply | Vss |
| 62 | O | DEBUG I/F |
| 63 | H | P17_0 |
| 64 | C | MD |
| 65 | A | X0 |
| 66 | A | X1 |
| 67 | Supply | Vss |
| 68 | B | P04_0 / X0A |
| 69 | B | P04_1 / X1A |
| 70 | C | RSTX |
| 71 | H | P11_0 |
| 72 | H | P11_1 / PPG0_R |
| 73 | H | P11_2 / PPG1_R |
| 74 | H | P11_3 / PPG2_R |
| 75 | H | P11_4 / PPG3_R |
| 76 | H | P11_5 / PPG4_R |
| 77 | H | P11_6 / FRCK0_R / ZIN1 |
| 78 | H | P11_7 / IN0_R / AIN1 |
| 79 | H | P12_0 / IN1_R / BIN1 |
| 80 | H | P12_1 / TIN1_R / PPG0_B |

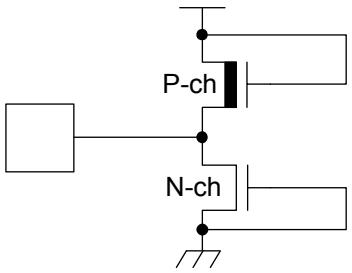
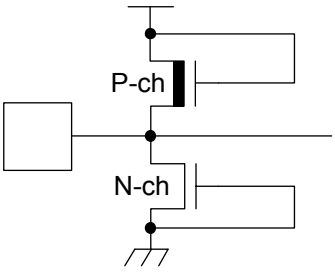
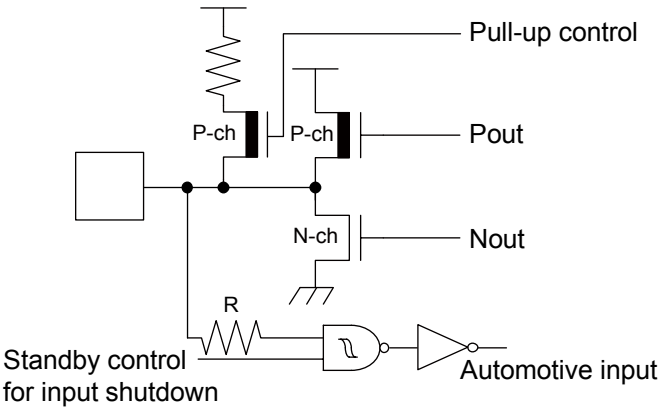
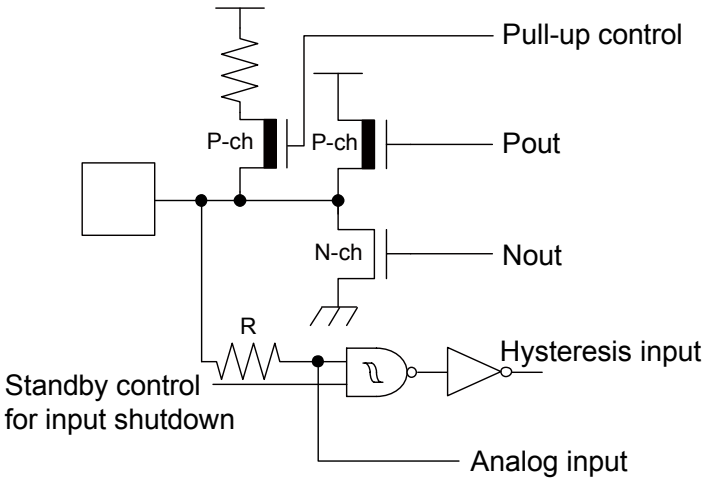
| Pin no. | I/O circuit type* | Pin name |
|---|---|---|
| 81 | H | P12_2 / TOT1_R / PPG1_B |
| 82 | H | P12_3 / OUT2_R |
| 83 | H | P12_4 / OUT3_R |
| 84 | H | P12_5 / TIN2_R / PPG2_B |
| 85 | H | P12_6 / TOT2_R / PPG3_B |
| 86 | H | P12_7 / INT1_R |
| 87 | H | P00_0 / INT3_R / FRCK2 |
| 88 | H | P00_1 / INT4_R |
| 89 | H | P00_2 / INT5_R |
| 90 | Supply | Vcc |
| 91 | Supply | Vss |
| 92 | H | P00_3 / INT6_R / PPG8_B |
| 93 | H | P00_4 / INT7_R / PPG9_B |
| 94 | H | P00_5 / IN6 / TTG2 / TTG6 / PPG10_B |
| 95 | H | P00_6 / IN7 / TTG3 / TTG7 / PPG11_B |
| 96 | H | P00_7 / INT14 |
| 97 | M | P01_0 / SCK7 |
| 98 | H | P01_1 / CKOT1 / OUT0 / SOT7 |
| 99 | M | P01_2 / CKOTX1 / OUT1 / INT15 / SIN7 |
| 100 | H | P01_3 / PPG5 |
| 101 | M | P01_4 / SIN4 / INT8 |
| 102 | H | P01_5 / SOT4 |
| 103 | M | P01_6 / SCK4 / TTG12 |
| 104 | M | P01_7 / CKOTX1_R / INT9 / TTG13 / ZIN0 / SCK7_R |
| 105 | H | P02_0 / CKOT1_R / INT10 / TTG14 / AIN0 / SOT7_R |
| 106 | H | P02_1 / IN6_R / TTG15 |
| 107 | M | P02_2 / IN7_R / CKOT0_R / INT12 / BIN0 / SIN7_R |
| 108 | H | P02_3 / PPG12_B |
| 109 | H | P02_4 / PPG13_B |
| 110 | M | P02_5 / OUT0_R / INT13 / SIN5_R |
| 111 | H | P02_6 / OUT1_R |
| 112 | H | P02_7 / PPG5_R |
| 113 | H | P03_0 / PPG4_B |
| 114 | H | P03_1 / PPG5_B |
| 115 | H | P03_2 / PPG14_B / SOT5_R |
| 116 | M | P03_3 / PPG15_B / SCK5_R |
| 117 | M | P03_4 / RX0 / INT4 |
| 118 | H | P03_5 / TX0 |
| 119 | H | P03_6 / INT0 / NMI |
| 120 | Supply | Vcc |

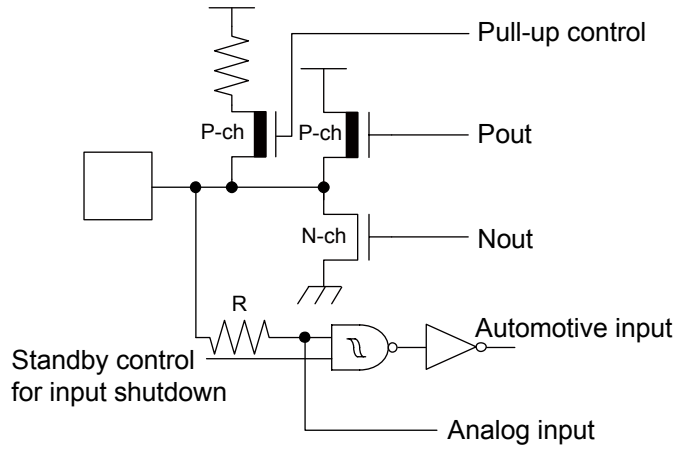
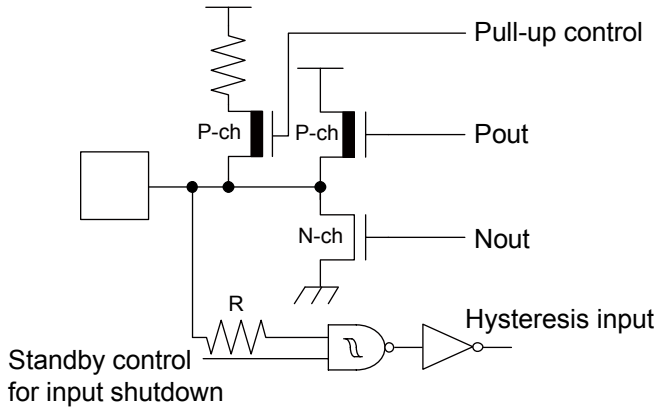
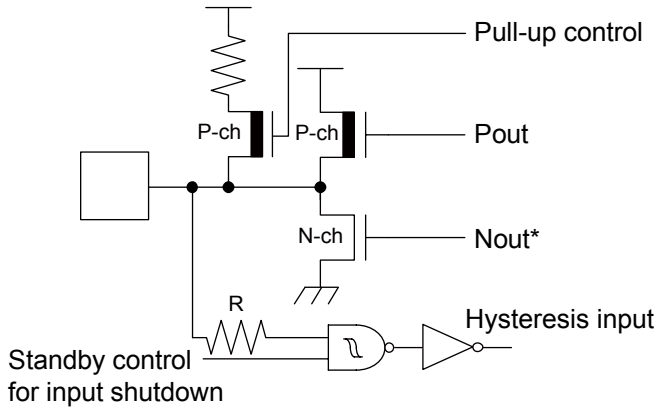
*: See “■ I/O CIRCUIT TYPE” for details on the I/O circuit types.

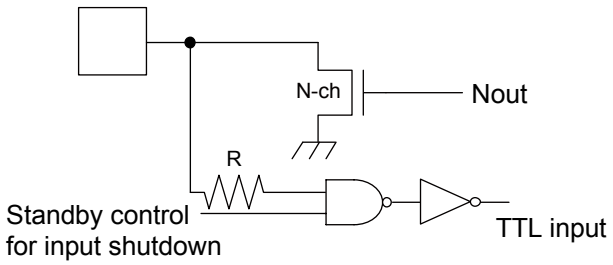
## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A |  | High-speed oscillation circuit:<br>• Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin)<br>• Feedback resistor = approx. 1.0MΩ<br>• The amplitude: 1.8V±0.15V to operate by the internal supply voltage |

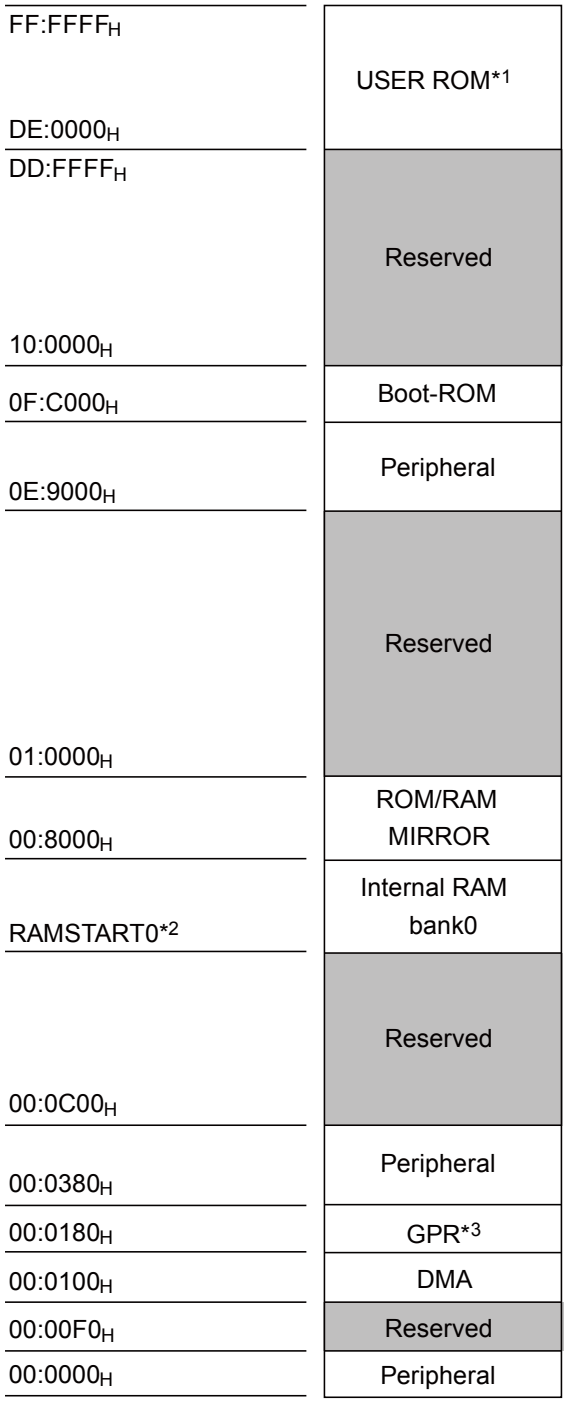
| Type | Circuit | Remarks |
|---|---|---|
| B |  | Low-speed oscillation circuit shared with GPIO functionality:<br>• Feedback resistor = approx. 5.0MΩ<br>• GPIO functionality selectable (CMOS level output ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA), Automotive input with input shutdown function and programmable pull-up resistor) |
| C |  | CMOS hysteresis input pin |

| Type | Circuit | Remarks |
|---|---|---|
| F |  | Power supply input protection circuit |
| G |  | • A/D converter ref+ (AVRH)/ ref- (AVRL) power supply input pin with protection circuit<br>• Without protection circuit against $V_{CC}$ for pins AVRH/AVRL |
| H |  | • CMOS level output ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA)<br>• Automotive input with input shutdown function<br>• Programmable pull-up resistor |
| I |  | • CMOS level output ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA)<br>• CMOS hysteresis input with input shutdown function<br>• Programmable pull-up resistor<br>• Analog input |

| Type | Circuit | Remarks |
|---|---|---|
| K |  | • CMOS level output ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA)<br>• Automotive input with input shutdown function<br>• Programmable pull-up resistor<br>• Analog input |
| M |  | • CMOS level output ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA)<br>• CMOS hysteresis input with input shutdown function<br>• Programmable pull-up resistor |
| N |  | • CMOS level output ($I_{OL}$ = 3mA, $I_{OH}$ = -3mA)<br>• CMOS hysteresis input with input shutdown function<br>• Programmable pull-up resistor<br>*: N-channel transistor has slew rate control according to $I^2C$ spec, irrespective of usage. |

| Type | Circuit | Remarks |
|---|---|---|
| O |  | • Open-drain I/O<br>• Output 25mA, Vcc = 2.7V<br>• TTL input |

## ■ MEMORY MAP




*1: For details about USER ROM area, see "■USER ROM MEMORY MAP FOR FLASH DEVICES" on the following pages.
*2: For RAMSTART addresses, see the table on the next page.
*3: Unused GPR banks can be used as RAM area.
GPR: General-Purpose Register
The DMA area is only available if the device contains the corresponding resource.
The available RAM and ROM area depends on the device.

## ■ RAMSTART ADDRESSES

| Devices | Bank 0<br>RAM size | RAMSTART0 |
|---|---|---|
| MB96F653 | 10KB | $00:5A00_H$ |
| MB96F655 | 16KB | $00:4200_H$ |
| MB96F656 | 24KB | $00:2200_H$ |
| MB96F657 | 28KB | $00:1200_H$ |

## ■ USER ROM MEMORY MAP FOR FLASH DEVICES

| CPU mode address | Flash memory mode address | MB96F653 Flash size 64.5KB + 32KB | MB96F655 Flash size 128.5KB + 32KB | MB96F656 Flash size 256.5KB + 32KB | MB96F657 Flash size 384.5KB + 32KB | |
|---|---|---|---|---|---|---|
| $FF:FFFF_H$<br>$FF:0000_H$ | $3F:FFFF_H$<br>$3F:0000_H$ | SA39 - 64KB | SA39 - 64KB | SA39 - 64KB | SA39 - 64KB | Bank A of Flash A |
| $FE:FFFF_H$<br>$FE:0000_H$ | $3E:FFFF_H$<br>$3E:0000_H$ | Reserved | SA38 - 64KB | SA38 - 64KB | SA38 - 64KB | |
| $FD:FFFF_H$<br>$FD:0000_H$ | $3D:FFFF_H$<br>$3D:0000_H$ | | Reserved | SA37 - 64KB | SA37 - 64KB | |
| $FC:FFFF_H$<br>$FC:0000_H$ | $3C:FFFF_H$<br>$3C:0000_H$ | | | SA36 - 64KB | SA36 - 64KB | |
| $FB:FFFF_H$<br>$FB:0000_H$ | $3B:FFFF_H$<br>$3B:0000_H$ | | | Reserved | SA35 - 64KB | |
| $FA:FFFF_H$<br>$FA:0000_H$ | $3A:FFFF_H$<br>$3A:0000_H$ | | | | SA34 - 64KB | |
| $F9:FFFF_H$<br>$DF:A000_H$ | | | | | Reserved | |
| $DF:9FFF_H$<br>$DF:8000_H$ | $1F:9FFF_H$<br>$1F:8000_H$ | SA4 - 8KB | SA4 - 8KB | SA4 - 8KB | SA4 - 8KB | Bank B of Flash A |
| $DF:7FFF_H$<br>$DF:6000_H$ | $1F:7FFF_H$<br>$1F:6000_H$ | SA3 - 8KB | SA3 - 8KB | SA3 - 8KB | SA3 - 8KB | |
| $DF:5FFF_H$<br>$DF:4000_H$ | $1F:5FFF_H$<br>$1F:4000_H$ | SA2 - 8KB | SA2 - 8KB | SA2 - 8KB | SA2 - 8KB | |
| $DF:3FFF_H$<br>$DF:2000_H$ | $1F:3FFF_H$<br>$1F:2000_H$ | SA1 - 8KB | SA1 - 8KB | SA1 - 8KB | SA1 - 8KB | |
| $DF:1FFF_H$<br>$DF:0000_H$ | $1F:1FFF_H$<br>$1F:0000_H$ | SAS - 512B* | SAS - 512B* | SAS - 512B* | SAS - 512B* | Bank A of Flash A |
| $DE:FFFF_H$<br>$DE:0000_H$ | | Reserved | Reserved | Reserved | Reserved | |

*: Physical address area of SAS-512B is from $DF:0000_H$ to $DF:01FF_H$.
Others (from $DF:0200_H$ to $DF:1FFF_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address $DF:0000_H$ -$DF:01FF_H$.
SAS can not be used for $E^2$PROM emulation.

## ■ SERIAL PROGRAMMING COMMUNICATION INTERFACE

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

| MB96650 | | |
|---|---|---|
| Pin Number | USART Number | Normal Function |
| 8 | USART0 | SIN0 |
| 9 | | SOT0 |
| 10 | | SCK0 |
| 3 | USART1 | SIN1 |
| 4 | | SOT1 |
| 5 | | SCK1 |
| 56 | USART2 | SIN2 |
| 57 | | SOT2 |
| 58 | | SCK2 |
| 101 | USART4 | SIN4 |
| 102 | | SOT4 |
| 103 | | SCK4 |

## ■ INTERRUPT VECTOR TABLE

| Vector number | Offset in vector table | Vector name | Cleared by DMA | Index in ICR to program | Description |
|---|---|---|---|---|---|
| 0 | $3FC_H$ | CALLV0 | No | - | CALLV instruction |
| 1 | $3F8_H$ | CALLV1 | No | - | CALLV instruction |
| 2 | $3F4_H$ | CALLV2 | No | - | CALLV instruction |
| 3 | $3F0_H$ | CALLV3 | No | - | CALLV instruction |
| 4 | $3EC_H$ | CALLV4 | No | - | CALLV instruction |
| 5 | $3E8_H$ | CALLV5 | No | - | CALLV instruction |
| 6 | $3E4_H$ | CALLV6 | No | - | CALLV instruction |
| 7 | $3E0_H$ | CALLV7 | No | - | CALLV instruction |
| 8 | $3DC_H$ | RESET | No | - | Reset vector |
| 9 | $3D8_H$ | INT9 | No | - | INT9 instruction |
| 10 | $3D4_H$ | EXCEPTION | No | - | Undefined instruction execution |
| 11 | $3D0_H$ | NMI | No | - | Non-Maskable Interrupt |
| 12 | $3CC_H$ | DLY | No | 12 | Delayed Interrupt |
| 13 | $3C8_H$ | RC_TIMER | No | 13 | RC Clock Timer |
| 14 | $3C4_H$ | MC_TIMER | No | 14 | Main Clock Timer |
| 15 | $3C0_H$ | SC_TIMER | No | 15 | Sub Clock Timer |
| 16 | $3BC_H$ | LVDI | No | 16 | Low Voltage Detector |
| 17 | $3B8_H$ | EXTINT0 | Yes | 17 | External Interrupt 0 |
| 18 | $3B4_H$ | EXTINT1 | Yes | 18 | External Interrupt 1 |
| 19 | $3B0_H$ | EXTINT2 | Yes | 19 | External Interrupt 2 |
| 20 | $3AC_H$ | EXTINT3 | Yes | 20 | External Interrupt 3 |
| 21 | $3A8_H$ | EXTINT4 | Yes | 21 | External Interrupt 4 |
| 22 | $3A4_H$ | EXTINT5 | Yes | 22 | External Interrupt 5 |
| 23 | $3A0_H$ | EXTINT6 | Yes | 23 | External Interrupt 6 |
| 24 | $39C_H$ | EXTINT7 | Yes | 24 | External Interrupt 7 |
| 25 | $398_H$ | EXTINT8 | Yes | 25 | External Interrupt 8 |
| 26 | $394_H$ | EXTINT9 | Yes | 26 | External Interrupt 9 |
| 27 | $390_H$ | EXTINT10 | Yes | 27 | External Interrupt 10 |
| 28 | $38C_H$ | EXTINT11 | Yes | 28 | External Interrupt 11 |
| 29 | $388_H$ | EXTINT12 | Yes | 29 | External Interrupt 12 |
| 30 | $384_H$ | EXTINT13 | Yes | 30 | External Interrupt 13 |
| 31 | $380_H$ | EXTINT14 | Yes | 31 | External Interrupt 14 |
| 32 | $37C_H$ | EXTINT15 | Yes | 32 | External Interrupt 15 |
| 33 | $378_H$ | CAN0 | No | 33 | CAN Controller 0 |
| 34 | $374_H$ | - | - | 34 | Reserved |
| 35 | $370_H$ | - | - | 35 | Reserved |
| 36 | $36C_H$ | - | - | 36 | Reserved |
| 37 | $368_H$ | - | - | 37 | Reserved |
| 38 | $364_H$ | PPG0 | Yes | 38 | Programmable Pulse Generator 0 |
| 39 | $360_H$ | PPG1 | Yes | 39 | Programmable Pulse Generator 1 |
| 40 | $35C_H$ | PPG2 | Yes | 40 | Programmable Pulse Generator 2 |

| Vector number | Offset in vector table | Vector name | Cleared by DMA | Index in ICR to program | Description |
|---|---|---|---|---|---|
| 41 | $358_H$ | PPG3 | Yes | 41 | Programmable Pulse Generator 3 |
| 42 | $354_H$ | PPG4 | Yes | 42 | Programmable Pulse Generator 4 |
| 43 | $350_H$ | PPG5 | Yes | 43 | Programmable Pulse Generator 5 |
| 44 | $34C_H$ | PPG6 | Yes | 44 | Programmable Pulse Generator 6 |
| 45 | $348_H$ | PPG7 | Yes | 45 | Programmable Pulse Generator 7 |
| 46 | $344_H$ | PPG8 | Yes | 46 | Programmable Pulse Generator 8 |
| 47 | $340_H$ | PPG9 | Yes | 47 | Programmable Pulse Generator 9 |
| 48 | $33C_H$ | PPG10 | Yes | 48 | Programmable Pulse Generator 10 |
| 49 | $338_H$ | PPG11 | Yes | 49 | Programmable Pulse Generator 11 |
| 50 | $334_H$ | PPG12 | Yes | 50 | Programmable Pulse Generator 12 |
| 51 | $330_H$ | PPG13 | Yes | 51 | Programmable Pulse Generator 13 |
| 52 | $32C_H$ | PPG14 | Yes | 52 | Programmable Pulse Generator 14 |
| 53 | $328_H$ | PPG15 | Yes | 53 | Programmable Pulse Generator 15 |
| 54 | $324_H$ | - | - | 54 | Reserved |
| 55 | $320_H$ | - | - | 55 | Reserved |
| 56 | $31C_H$ | - | - | 56 | Reserved |
| 57 | $318_H$ | - | - | 57 | Reserved |
| 58 | $314_H$ | RLT0 | Yes | 58 | Reload Timer 0 |
| 59 | $310_H$ | RLT1 | Yes | 59 | Reload Timer 1 |
| 60 | $30C_H$ | RLT2 | Yes | 60 | Reload Timer 2 |
| 61 | $308_H$ | RLT3 | Yes | 61 | Reload Timer 3 |
| 62 | $304_H$ | - | - | 62 | Reserved |
| 63 | $300_H$ | - | - | 63 | Reserved |
| 64 | $2FC_H$ | RLT6 | Yes | 64 | Reload Timer 6 |
| 65 | $2F8_H$ | ICU0 | Yes | 65 | Input Capture Unit 0 |
| 66 | $2F4_H$ | ICU1 | Yes | 66 | Input Capture Unit 1 |
| 67 | $2F0_H$ | - | - | 67 | Reserved |
| 68 | $2EC_H$ | - | - | 68 | Reserved |
| 69 | $2E8_H$ | ICU4 | Yes | 69 | Input Capture Unit 4 |
| 70 | $2E4_H$ | ICU5 | Yes | 70 | Input Capture Unit 5 |
| 71 | $2E0_H$ | ICU6 | Yes | 71 | Input Capture Unit 6 |
| 72 | $2DC_H$ | ICU7 | Yes | 72 | Input Capture Unit 7 |
| 73 | $2D8_H$ | - | - | 73 | Reserved |
| 74 | $2D4_H$ | ICU9 | Yes | 74 | Input Capture Unit 9 |
| 75 | $2D0_H$ | - | - | 75 | Reserved |
| 76 | $2CC_H$ | - | - | 76 | Reserved |
| 77 | $2C8_H$ | OCU0 | Yes | 77 | Output Compare Unit 0 |
| 78 | $2C4_H$ | OCU1 | Yes | 78 | Output Compare Unit 1 |
| 79 | $2C0_H$ | OCU2 | Yes | 79 | Output Compare Unit 2 |
| 80 | $2BC_H$ | OCU3 | Yes | 80 | Output Compare Unit 3 |

| Vector number | Offset in vector table | Vector name | Cleared by DMA | Index in ICR to program | Description |
|---|---|---|---|---|---|
| 81 | $2B8_H$ | OCU4 | Yes | 81 | Output Compare Unit 4 |
| 82 | $2B4_H$ | - | - | 82 | Reserved |
| 83 | $2B0_H$ | OCU6 | Yes | 83 | Output Compare Unit 6 |
| 84 | $2AC_H$ | OCU7 | Yes | 84 | Output Compare Unit 7 |
| 85 | $2A8_H$ | - | - | 85 | Reserved |
| 86 | $2A4_H$ | - | - | 86 | Reserved |
| 87 | $2A0_H$ | - | - | 87 | Reserved |
| 88 | $29C_H$ | - | - | 88 | Reserved |
| 89 | $298_H$ | FRT0 | Yes | 89 | Free-Running Timer 0 |
| 90 | $294_H$ | FRT1 | Yes | 90 | Free-Running Timer 1 |
| 91 | $290_H$ | FRT2 | Yes | 91 | Free-Running Timer 2 |
| 92 | $28C_H$ | - | - | 92 | Reserved |
| 93 | $288_H$ | RTC0 | No | 93 | Real Time Clock |
| 94 | $284_H$ | CAL0 | No | 94 | Clock Calibration Unit |
| 95 | $280_H$ | - | - | 95 | Reserved |
| 96 | $27C_H$ | IIC0 | Yes | 96 | $I^2C$ interface 0 |
| 97 | $278_H$ | IIC1 | Yes | 97 | $I^2C$ interface 1 |
| 98 | $274_H$ | ADC0 | Yes | 98 | A/D Converter 0 |
| 99 | $270_H$ | - | - | 99 | Reserved |
| 100 | $26C_H$ | - | - | 100 | Reserved |
| 101 | $268_H$ | LINR0 | Yes | 101 | LIN USART 0 RX |
| 102 | $264_H$ | LINT0 | Yes | 102 | LIN USART 0 TX |
| 103 | $260_H$ | LINR1 | Yes | 103 | LIN USART 1 RX |
| 104 | $25C_H$ | LINT1 | Yes | 104 | LIN USART 1 TX |
| 105 | $258_H$ | LINR2 | Yes | 105 | LIN USART 2 RX |
| 106 | $254_H$ | LINT2 | Yes | 106 | LIN USART 2 TX |
| 107 | $250_H$ | - | - | 107 | Reserved |
| 108 | $24C_H$ | - | - | 108 | Reserved |
| 109 | $248_H$ | LINR4 | Yes | 109 | LIN USART 4 RX |
| 110 | $244_H$ | LINT4 | Yes | 110 | LIN USART 4 TX |
| 111 | $240_H$ | LINR5 | Yes | 111 | LIN USART 5 RX |
| 112 | $23C_H$ | LINT5 | Yes | 112 | LIN USART 5 TX |
| 113 | $238_H$ | - | - | 113 | Reserved |
| 114 | $234_H$ | - | - | 114 | Reserved |
| 115 | $230_H$ | LINR7 | Yes | 115 | LIN USART 7 RX |
| 116 | $22C_H$ | LINT7 | Yes | 116 | LIN USART 7 TX |
| 117 | $228_H$ | - | - | 117 | Reserved |
| 118 | $224_H$ | - | - | 118 | Reserved |
| 119 | $220_H$ | - | - | 119 | Reserved |
| 120 | $21C_H$ | - | - | 120 | Reserved |

| Vector number | Offset in vector table | Vector name | Cleared by DMA | Index in ICR to program | Description |
|---|---|---|---|---|---|
| 121 | $218_H$ | - | - | 121 | Reserved |
| 122 | $214_H$ | - | - | 122 | Reserved |
| 123 | $210_H$ | - | - | 123 | Reserved |
| 124 | $20C_H$ | - | - | 124 | Reserved |
| 125 | $208_H$ | - | - | 125 | Reserved |
| 126 | $204_H$ | - | - | 126 | Reserved |
| 127 | $200_H$ | - | - | 127 | Reserved |
| 128 | $1FC_H$ | - | - | 128 | Reserved |
| 129 | $1F8_H$ | - | - | 129 | Reserved |
| 130 | $1F4_H$ | - | - | 130 | Reserved |
| 131 | $1F0_H$ | - | - | 131 | Reserved |
| 132 | $1EC_H$ | - | - | 132 | Reserved |
| 133 | $1E8_H$ | FLASHA | Yes | 133 | Flash memory A interrupt |
| 134 | $1E4_H$ | - | - | 134 | Reserved |
| 135 | $1E0_H$ | - | - | 135 | Reserved |
| 136 | $1DC_H$ | - | - | 136 | Reserved |
| 137 | $1D8_H$ | QPRC0 | Yes | 137 | Quad Position/Revolution counter 0 |
| 138 | $1D4_H$ | QPRC1 | Yes | 138 | Quad Position/Revolution counter 1 |
| 139 | $1D0_H$ | ADCRC0 | No | 139 | A/D Converter 0 - Range Comparator |
| 140 | $1CC_H$ | - | - | 140 | Reserved |
| 141 | $1C8_H$ | - | - | 141 | Reserved |
| 142 | $1C4_H$ | - | - | 142 | Reserved |
| 143 | $1C0_H$ | - | - | 143 | Reserved |

## ■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU SEMICONDUCTOR semiconductor devices.

### 1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- Absolute Maximum Ratings

  Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- Recommended Operating Conditions

  Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

  Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

  No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- Processing and Protection of Pins

  These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

  (1) Preventing Over-Voltage and Over-Current Conditions

  Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

  (2) Protection of Output Pins

  Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
  Therefore, avoid this type of connection.

  (3) Handling of Unused Input Pins

  Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- Latch-up

  Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

  CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

  (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

  (2) Be sure that abnormal current flows do not occur during the power-on sequence.

- Observance of Safety Regulations and Standards

  Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- Fail-Safe Design

  Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- Precautions Related to Usage of Devices

  FUJITSU SEMICONDUCTOR semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

  CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

   Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under FUJITSU SEMICONDUCTOR's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- Lead Insertion Type

  Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

  Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to FUJITSU SEMICONDUCTOR recommended mounting conditions.

  If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- Surface Mount Type

  Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

  You must use appropriate mounting techniques. FUJITSU SEMICONDUCTOR recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with FUJITSU SEMICONDUCTOR ranking of recommended conditions.

- Lead-Free Packaging

  CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- Storage of Semiconductor Devices

  Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

  (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

  (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
  When you open Dry Package that recommends humidity 40% to 70% relative humidity.

  (3) When necessary, FUJITSU SEMICONDUCTOR packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

  (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- Baking

  Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the FUJITSU SEMICONDUCTOR recommended conditions for baking.

  Condition: 125°C/24 h

- Static Electricity

  Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

  (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

  (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

  (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
  Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

  (4) Ground all fixtures and instruments, or protect with anti-static measures.

  (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.
Customers considering the use of FUJITSU SEMICONDUCTOR products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.
http://edevice.fujitsu.com/fj/handling-e.pdf

## ■ HANDLING DEVICES

**Special care is required for the following when handling the device:**
• Latch-up prevention
• Unused pins handling
• External clock usage
• Notes on PLL clock mode operation
• Power supply pins (Vcc/Vss)
• Crystal oscillator and ceramic resonator circuit
• Turn on sequence of power supply to A/D converter and analog inputs
• Pin handling when not using the A/D converter
• Notes on Power-on
• Stabilization of power supply voltage
• Serial communication
• Mode Pin (MD)

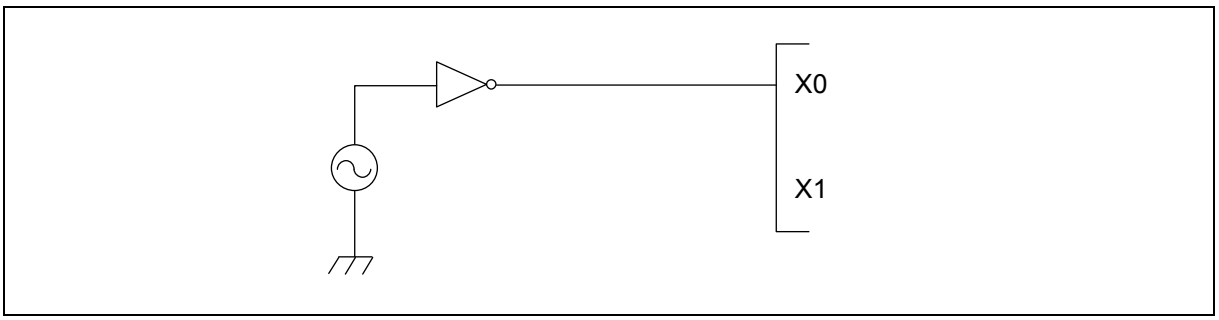
**1. Latch-up prevention**
CMOS IC chips may suffer latch-up under the following conditions:
- A voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between Vcc pins and Vss pins.
- The $AV_{CC}$ power supply is applied before the $V_{CC}$ voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.
For the same reason, extra care is required to not let the analog power-supply voltage ($AV_{CC}$, AVRH) exceed the digital power-supply voltage.

**2. Unused pins handling**
Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).
Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. To prevent latch-up, they must therefore be pulled up or pulled down through resistors which should be more than 2kΩ.
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

**3. External clock usage**
The permitted frequency range of an external clock depends on the oscillator type and configuration.
See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

**(1) Single phase external clock for Main oscillator**
When using a single phase external clock for the Main oscillator, X0 pin must be driven and X1 pin left open.
And supply 1.8V power to the external clock.

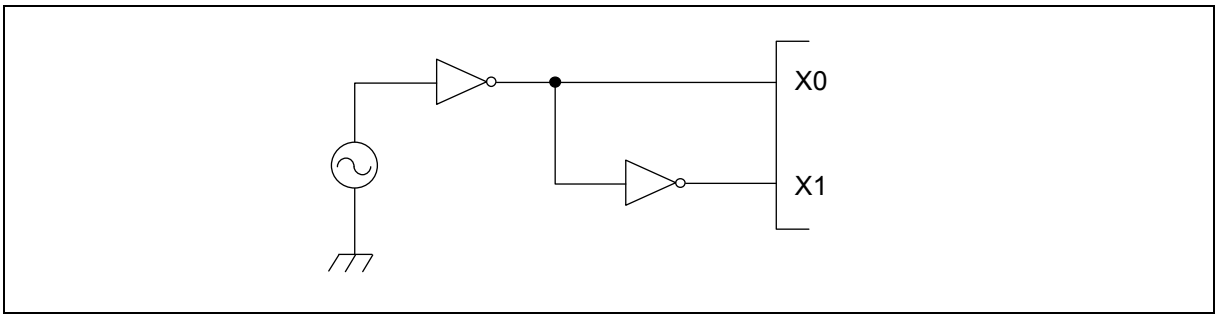


**(2) Single phase external clock for Sub oscillator**

When using a single phase external clock for the Sub oscillator, “External clock mode” must be selected and X0A/P04_0 pin must be driven. X1A/P04_1 pin can be configured as GPIO.

**(3) Opposite phase external clock**

When using an opposite phase external clock, X1 (X1A) pins must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. Supply level on X0 and X1 pins must be 1.8V.




**4. Notes on PLL clock mode operation**

If the microcontroller is operated with PLL clock mode and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

**5. Power supply pins (Vcc/Vss)**

It is required that all $V_{CC}$-level as well as all $V_{SS}$-level power supply pins are at the same potential. If there is more than one $V_{CC}$ or $V_{SS}$ level, the device may operate incorrectly or be damaged even within the guaranteed operating range.
Vcc and Vss pins must be connected to the device from the power supply with lowest possible impedance.
The smoothing capacitor at Vcc pin must use the one of a capacity value that is larger than Cs.
Besides this, as a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1µF between Vcc and Vss pins as close as possible to Vcc and Vss pins.

**6. Crystal oscillator and ceramic resonator circuit**

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.
It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.
It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

**7. Turn on sequence of power supply to A/D converter and analog inputs**

It is required to turn the A/D converter power supply ($AV_{CC}$, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply ($V_{CC}$) on.
It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, AVRH must not exceed $AV_{CC}$ . Input voltage for ports shared with analog input ports also must not exceed $AV_{CC}$ (turning the analog and digital power supplies simultaneously on or off is acceptable).

**8. Pin handling when not using the A/D converter**

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as $AV_{CC}$ = $V_{CC}$, $AV_{SS}$ = AVRH =AVRL = $V_{SS}$.

**9. Notes on Power-on**

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2V to 2.7V.

**10. Stabilization of power supply voltage**

If the power supply voltage varies acutely even within the operation safety range of the $V_{CC}$ power supply voltage, a malfunction may occur. The $V_{CC}$ power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that $V_{CC}$ ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard $V_{CC}$ power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

**11. Serial communication**

There is a possibility to receive wrong data due to noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.
Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

**12. Mode Pin (MD)**

Connect the mode pin directly to Vcc or Vss pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to Vcc or Vss pin and provide a low-impedance connection.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Power supply voltage*[1] | $V_{CC}$ | - | $V_{SS}$ - 0.3 | $V_{SS}$ + 6.0 | V | |
| Analog power supply voltage*[1] | $AV_{CC}$ | - | $V_{SS}$ - 0.3 | $V_{SS}$ + 6.0 | V | $V_{CC} = AV_{CC}$*[2] |
| Analog reference voltage*[1] | AVRH, AVRL | - | $V_{SS}$ - 0.3 | $V_{SS}$ + 6.0 | V | $AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH > AVRL, AVRL $\geq AV_{SS}$ |
| Input voltage*[1] | $V_I$ | - | $V_{SS}$ - 0.3 | $V_{SS}$ + 6.0 | V | $V_I \leq V_{CC}$ + 0.3V*[3] |
| Output voltage*[1] | $V_O$ | - | $V_{SS}$ - 0.3 | $V_{SS}$ + 6.0 | V | $V_O \leq V_{CC}$ + 0.3V*[3] |
| Maximum Clamp Current | $I_{CLAMP}$ | - | -4.0 | +4.0 | mA | Applicable to general purpose I/O pins *[4] |
| Total Maximum Clamp Current | $\Sigma\lvert I_{CLAMP}\rvert$ | - | - | 33 | mA | Applicable to general purpose I/O pins *[4] |
| "L" level maximum output current | $I_{OL}$ | - | - | 15 | mA | |
| "L" level average output current | $I_{OLAV}$ | - | - | 4 | mA | |
| "L" level maximum overall output current | $\Sigma I_{OL}$ | - | - | 82 | mA | |
| "L" level average overall output current | $\Sigma I_{OLAV}$ | - | - | 41 | mA | |
| "H" level maximum output current | $I_{OH}$ | - | - | -15 | mA | |
| "H" level average output current | $I_{OHAV}$ | - | - | -4 | mA | |
| "H" level maximum overall output current | $\Sigma I_{OH}$ | - | - | -82 | mA | |
| "H" level average overall output current | $\Sigma I_{OHAV}$ | - | - | -41 | mA | |
| Power consumption*[5] | $P_D$ | $T_A$= +125°C | - | 446*[6] | mW | |
| Operating ambient temperature | $T_A$ | - | -40 | +125*[7] | °C | |
| Storage temperature | $T_{STG}$ | - | -55 | +150 | °C | |

*1: This parameter is based on $V_{SS} = AV_{SS} = 0V$.

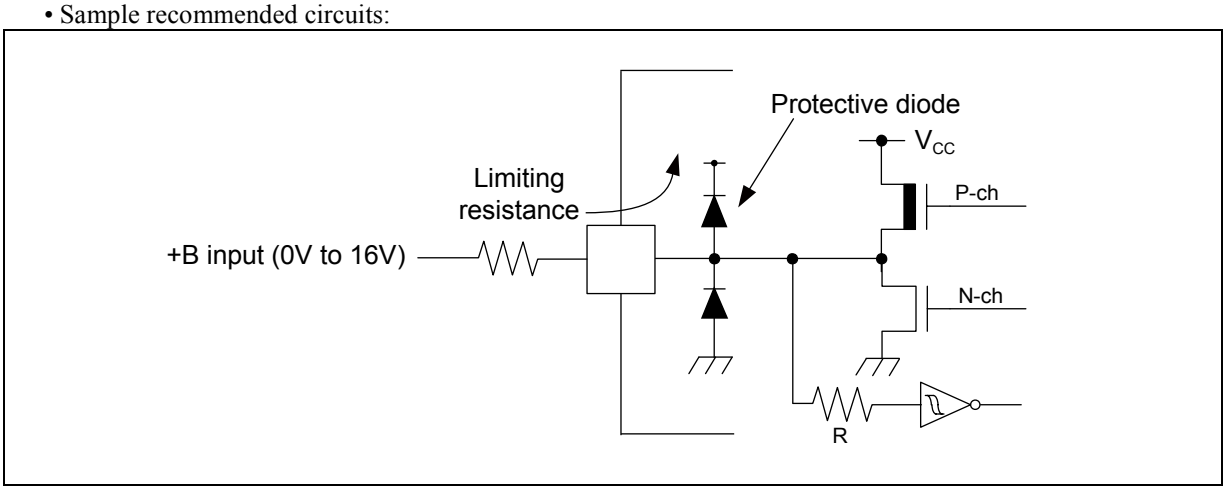
*2: $AV_{CC}$ and $V_{CC}$ must be set to the same voltage. It is required that $AV_{CC}$ does not exceed $V_{CC}$ and that the voltage at the analog inputs does not exceed $AV_{CC}$ when the power is switched on.

*3: $V_I$ and $V_O$ should not exceed $V_{CC}$ + 0.3V. $V_I$ should also not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the $I_{CLAMP}$ rating supersedes the $V_I$ rating. Input/Output voltages of standard ports depend on $V_{CC}$.

*4:
- Applicable to all general purpose I/O pins (Pnn_m).
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.

- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset.
- The DEBUG I/F pin has only a protective diode against $V_{SS}$. Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.

• Sample recommended circuits:




*5: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$ (I/O load power dissipation, sum is performed on all I/O ports)
$P_{INT} = V_{CC} \times (I_{CC} + I_A)$ (internal power dissipation)
$I_{CC}$ is the total core current consumption into $V_{CC}$ as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.
$I_A$ is the analog current consumption into $AV_{CC}$.
*6: Worst case value for a package mounted on single layer PCB at specified $T_A$ without air flow.
*7: Write/erase to a large sector in flash memory is warranted with $T_A \leq +105°C$.

**<WARNING>**

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

($V_{SS}$ = $AV_{SS}$ = 0V)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Power supply voltage | $V_{CC}$, $AV_{CC}$ | 2.7 | - | 5.5 | V | |
| | | 2.0 | - | 5.5 | V | Maintains RAM data in stop mode |
| Smoothing capacitor at C pin | $C_S$ | 0.5 | 1.0 to 3.9 | 4.7 | µF | 1.0µF (Allowance within ± 50%)<br>3.9µF (Allowance within ± 20%)<br>Please use the ceramic capacitor or the capacitor of the frequency response of this level.<br>The smoothing capacitor at $V_{CC}$ must use the one of a capacity value that is larger than $C_S$. |

**<WARNING>**

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## 3. DC Characteristics

### (1) Current Rating

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current in Run modes*1 | $I_{CCPLL}$ | Vcc | PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz<br>Flash 0 wait<br>(CLKRC and CLKSC stopped) | - | 27 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 37 | mA | $T_A$ = +105°C |
| | | | | - | - | 38.5 | mA | $T_A$ = +125°C |
| | $I_{CCMAIN}$ | | Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz<br>Flash 0 wait<br>(CLKPLL, CLKSC and CLKRC stopped) | - | 3.5 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 8 | mA | $T_A$ = +105°C |
| | | | | - | - | 9.5 | mA | $T_A$ = +125°C |
| | $I_{CCRCH}$ | | RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz<br>Flash 0 wait<br>(CLKMC, CLKPLL and CLKSC stopped) | - | 1.8 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 6 | mA | $T_A$ = +105°C |
| | | | | - | - | 7.5 | mA | $T_A$ = +125°C |
| | $I_{CCRCL}$ | | RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz<br>Flash 0 wait<br>(CLKMC, CLKPLL and CLKSC stopped) | - | 0.16 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 3.5 | mA | $T_A$ = +105°C |
| | | | | - | - | 5 | mA | $T_A$ = +125°C |
| | $I_{CCSUB}$ | | Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz<br>Flash 0 wait<br>(CLKMC, CLKPLL and CLKRC stopped) | - | 0.1 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 3.3 | mA | $T_A$ = +105°C |
| | | | | - | - | 4.8 | mA | $T_A$ = +125°C |

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current in Sleep modes*1 | $I_{CCSPLL}$ | Vcc | PLL Sleep mode with CLKS1/2 = CLKP1/2 = 32MHz (CLKRC and CLKSC stopped) | - | 8.5 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 14 | mA | $T_A$ = +105°C |
| | | | | - | - | 15.5 | mA | $T_A$ = +125°C |
| | $I_{CCSMAIN}$ | | Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped) | - | 1 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 4.5 | mA | $T_A$ = +105°C |
| | | | | - | - | 6 | mA | $T_A$ = +125°C |
| | $I_{CCSRCH}$ | | RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped) | - | 0.6 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 3.8 | mA | $T_A$ = +105°C |
| | | | | - | - | 5.3 | mA | $T_A$ = +125°C |
| | $I_{CCSRCL}$ | | RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 100kHz (CLKMC, CLKPLL and CLKSC stopped) | - | 0.07 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 2.8 | mA | $T_A$ = +105°C |
| | | | | - | - | 4.3 | mA | $T_A$ = +125°C |
| | $I_{CCSSUB}$ | | Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz, (CLKMC, CLKPLL and CLKRC stopped) | - | 0.04 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 2.5 | mA | $T_A$ = +105°C |
| | | | | - | - | 4 | mA | $T_A$ = +125°C |

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current in Timer modes*2 | $I_{CCTPLL}$ | Vcc | PLL Timer mode with CLKPLL = 32MHz (CLKRC and CLKSC stopped) | - | 2485 | 2715 | µA | $T_A$ = +25°C |
| | | | | - | - | 4095 | µA | $T_A$ = +105°C |
| | | | | - | - | 5065 | µA | $T_A$ = +125°C |
| | $I_{CCTMAIN}$ | | Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped) | - | 285 | 330 | µA | $T_A$ = +25°C |
| | | | | - | - | 1195 | µA | $T_A$ = +105°C |
| | | | | - | - | 2165 | µA | $T_A$ = +125°C |
| | $I_{CCTRCH}$ | | RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped) | - | 160 | 215 | µA | $T_A$ = +25°C |
| | | | | - | - | 1095 | µA | $T_A$ = +105°C |
| | | | | - | - | 2075 | µA | $T_A$ = +125°C |
| | $I_{CCTRCL}$ | | RC Timer mode with CLKRC = 100kHz (CLKPLL, CLKMC and CLKSC stopped) | - | 35 | 75 | µA | $T_A$ = +25°C |
| | | | | - | - | 905 | µA | $T_A$ = +105°C |
| | | | | - | - | 1880 | µA | $T_A$ = +125°C |
| | $I_{CCTSUB}$ | | Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped) | - | 25 | 65 | µA | $T_A$ = +25°C |
| | | | | - | - | 885 | µA | $T_A$ = +105°C |
| | | | | - | - | 1850 | µA | $T_A$ = +125°C |

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current in Stop mode*3 | $I_{CCH}$ | Vcc | - | - | 20 | 60 | µA | $T_A$ = +25°C |
| | | | | - | - | 880 | µA | $T_A$ = +105°C |
| | | | | - | - | 1845 | µA | $T_A$ = +125°C |
| Flash Power Down current | $I_{CCFLASHPD}$ | | - | - | 36 | 70 | µA | |
| Power supply current for active Low Voltage detector*4 | $I_{CCLVD}$ | | Low voltage detector enabled | - | 5 | - | µA | $T_A$ = +25°C |
| | | | | - | - | 12.5 | µA | $T_A$ = +125°C |
| Flash Write/ Erase current*5 | $I_{CCFLASH}$ | | - | - | 12.5 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 20 | mA | $T_A$ = +125°C |

*1: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control. Current for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current.

*2: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode. When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current. The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. The current for "On Chip Debugger" part is not included.

*3: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode. When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

*4: When low voltage detector is enabled, $I_{CCLVD}$ must be added to Power supply current.

*5: When Flash Write / Erase program is executed, $I_{CCFLASH}$ must be added to Power supply current.

(2) Pin Characteristics

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | $V_{IH}$ | Port inputs Pnn_m | - | $V_{CC}$ × 0.7 | - | $V_{CC}$ + 0.3 | V | CMOS Hysteresis input |
| | | | - | $V_{CC}$ × 0.8 | - | $V_{CC}$ + 0.3 | V | AUTOMOTIVE Hysteresis input |
| | $V_{IHX0S}$ | X0 | External clock in "Fast Clock Input mode" | VD × 0.8 | - | VD | V | VD=1.8V±0.15V |
| | $V_{IHX0AS}$ | X0A | External clock in "Oscillation mode" | $V_{CC}$ × 0.8 | - | $V_{CC}$ + 0.3 | V | |
| | $V_{IHR}$ | RSTX | - | $V_{CC}$ × 0.8 | - | $V_{CC}$ + 0.3 | V | CMOS Hysteresis input |
| | $V_{IHM}$ | MD | - | $V_{CC}$ - 0.3 | - | $V_{CC}$ + 0.3 | V | CMOS Hysteresis input |
| | $V_{IHD}$ | DEBUG I/F | - | 2.0 | - | $V_{CC}$ + 0.3 | V | TTL Input |
| "L" level input voltage | $V_{IL}$ | Port inputs Pnn_m | - | $V_{SS}$ - 0.3 | - | $V_{CC}$ × 0.3 | V | CMOS Hysteresis input |
| | | | - | $V_{SS}$ - 0.3 | - | $V_{CC}$ × 0.5 | V | AUTOMOTIVE Hysteresis input |
| | $V_{ILX0S}$ | X0 | External clock in "Fast Clock Input mode" | $V_{SS}$ | - | VD × 0.2 | V | VD=1.8V±0.15V |
| | $V_{ILX0AS}$ | X0A | External clock in "Oscillation mode" | $V_{SS}$ - 0.3 | - | $V_{CC}$ × 0.2 | V | |
| | $V_{ILR}$ | RSTX | - | $V_{SS}$ - 0.3 | - | $V_{CC}$ × 0.2 | V | CMOS Hysteresis input |
| | $V_{ILM}$ | MD | - | $V_{SS}$ - 0.3 | - | $V_{SS}$ + 0.3 | V | CMOS Hysteresis input |
| | $V_{ILD}$ | DEBUG I/F | - | $V_{SS}$ - 0.3 | - | 0.8 | V | TTL Input |

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level output voltage | $V_{OH4}$ | 4mA type | $4.5V \le V_{CC} \le 5.5V$<br>$I_{OH} = -4mA$<br>$2.7V \le V_{CC} < 4.5V$<br>$I_{OH} = -1.5mA$ | $V_{CC}$ - 0.5 | - | $V_{CC}$ | V | |
| | $V_{OH3}$ | 3mA type | $4.5V \le V_{CC} \le 5.5V$<br>$I_{OH} = -3mA$<br>$2.7V \le V_{CC} < 4.5V$<br>$I_{OH} = -1.5mA$ | $V_{CC}$ - 0.5 | - | $V_{CC}$ | V | |
| "L" level output voltage | $V_{OL4}$ | 4mA type | $4.5V \le V_{CC} \le 5.5V$<br>$I_{OL} = +4mA$<br>$2.7V \le V_{CC} < 4.5V$<br>$I_{OL} = +1.7mA$ | - | - | 0.4 | V | |
| | $V_{OL3}$ | 3mA type | $2.7V \le V_{CC} < 5.5V$<br>$I_{OL} = +3mA$ | - | - | 0.4 | V | |
| | $V_{OLD}$ | DEBUG I/F | $V_{CC} = 2.7V$<br>$I_{OL} = +25mA$ | 0 | - | 0.25 | V | |
| Input leak current | $I_{IL}$ | Pnn_m | $V_{SS} < V_I < V_{CC}$<br>$AV_{SS}$, AVRL < $V_I$ < $AV_{CC}$, AVRH | - 1 | - | + 1 | µA | |
| Pull-up resistance value | $R_{PU}$ | Pnn_m | $V_{CC} = 5.0V \pm 10\%$ | 25 | 50 | 100 | kΩ | |
| Input capacitance | $C_{IN}$ | Other than C, Vcc, Vss, AVcc, AVss, AVRH, AVRL | - | - | 5 | 15 | pF | |

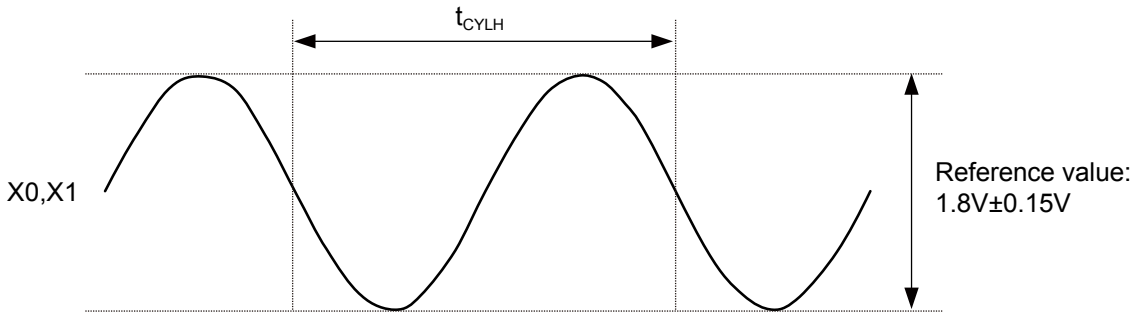
## 4. AC Characteristics

### (1) Main Clock Input Characteristics

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, VD=1.8V±0.15V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

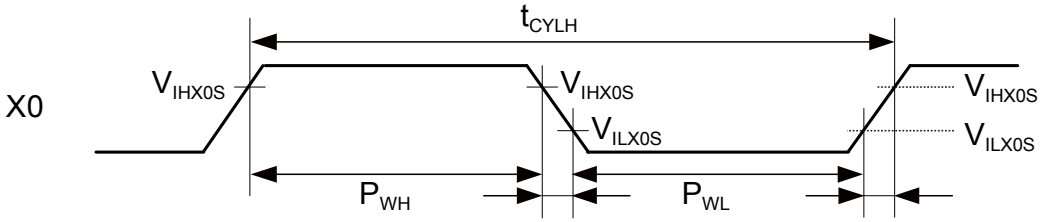
| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Input frequency | $f_C$ | X0, X1 | 4 | - | 8 | MHz | When using a crystal oscillator, PLL off |
| | | | - | - | 8 | MHz | When using an opposite phase external clock, PLL off |
| | | | 4 | - | 8 | MHz | When using a crystal oscillator or opposite phase external clock, PLL on |
| Input frequency | $f_{FCI}$ | X0 | - | - | 8 | MHz | When using a single phase external clock in “Fast Clock Input mode”, PLL off |
| | | | 4 | - | 8 | MHz | When using a single phase external clock in “Fast Clock Input mode”, PLL on |
| Input clock cycle | $t_{CYLH}$ | - | 125 | - | - | ns | |
| Input clock pulse width | $P_{WH}$, $P_{WL}$ | - | 55 | - | - | ns | |

When using the crystal oscillator




The amplitude changes by resistance, capacity which added outside or the difference of the device.

When using the external clock

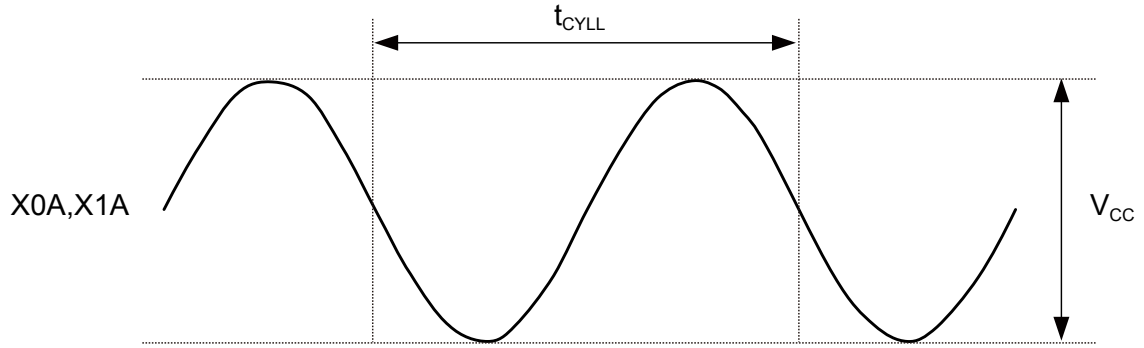


(2) Sub Clock Input Characteristics

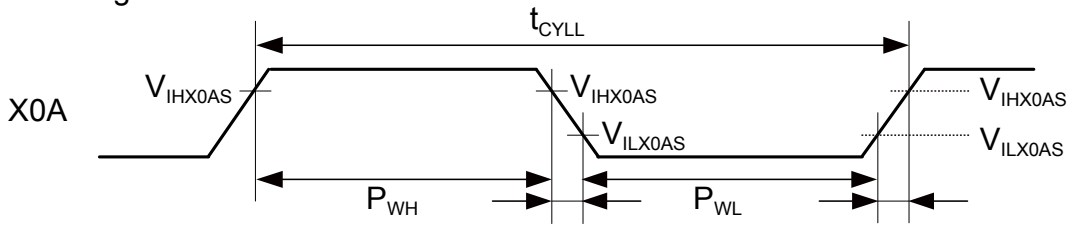
($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input frequency | $f_{CL}$ | X0A, X1A | - | - | 32.768 | - | kHz | When using an oscillation circuit |
| | | | - | - | - | 100 | kHz | When using an opposite phase external clock |
| | | X0A | - | - | - | 50 | kHz | When using a single phase external clock |
| Input clock cycle | $t_{CYLL}$ | - | - | 10 | - | - | µs | |
| Input clock pulse width | - | - | $P_{WH}/t_{CYLL}$, $P_{WL}/t_{CYLL}$ | 30 | - | 70 | % | |

When using the crystal oscillator




When using the external clock



(3) Built-in RC Oscillation Characteristics

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Clock frequency | $f_{RC}$ | 50 | 100 | 200 | kHz | When using slow frequency of RC oscillator |
| | | 1 | 2 | 4 | MHz | When using fast frequency of RC oscillator |
| RC clock stabilization time | $t_{RCSTAB}$ | 80 | 160 | 320 | µs | When using slow frequency of RC oscillator (16 RC clock cycles) |
| | | 64 | 128 | 256 | µs | When using fast frequency of RC oscillator (256 RC clock cycles) |

(4) Internal Clock Timing

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

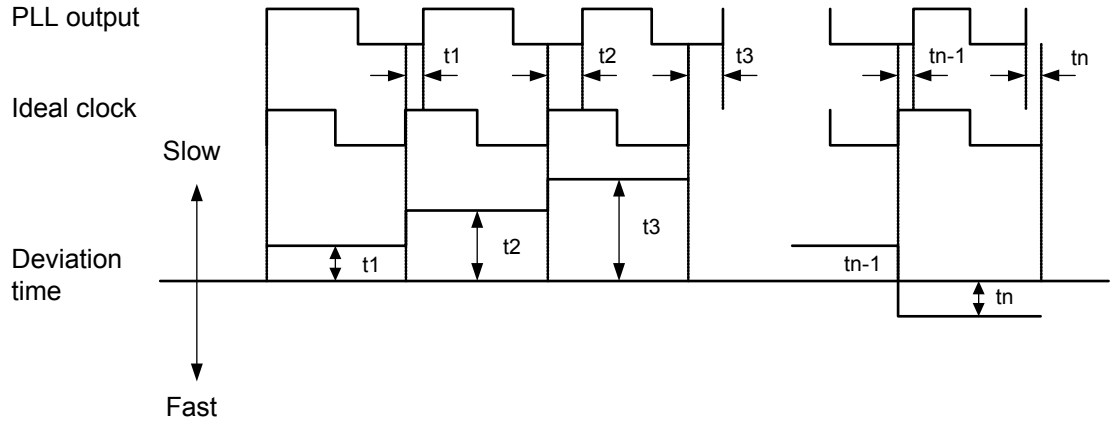
| Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Internal System clock frequency (CLKS1 and CLKS2) | $f_{CLKS1}$, $f_{CLKS2}$ | - | 54 | MHz |
| Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1) | $f_{CLKB}$, $f_{CLKP1}$ | - | 32 | MHz |
| Internal peripheral clock frequency (CLKP2) | $f_{CLKP2}$ | - | 32 | MHz |

(5) Operating Conditions of PLL

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| PLL oscillation stabilization wait time | $t_{LOCK}$ | 1 | - | 4 | ms | For CLKMC = 4MHz |
| PLL input clock frequency | $f_{PLLI}$ | 4 | - | 8 | MHz | |
| PLL oscillation clock frequency | $f_{CLKVCO}$ | 56 | - | 108 | MHz | Permitted VCO output frequency of PLL (CLKVCO) |
| PLL phase jitter | $t_{PSKEW}$ | -5 | - | +5 | ns | For CLKMC (PLL input clock) ≥ 4MHz |

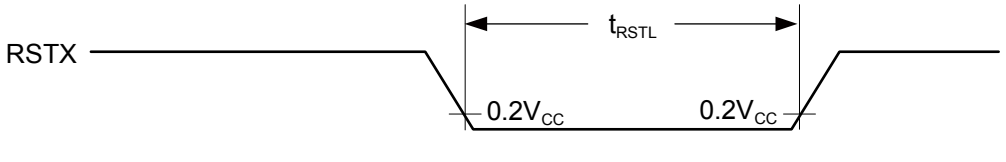
Deviation time from the ideal clock is assured per cycle out of 20,000 cycles.




(6) Reset Input

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

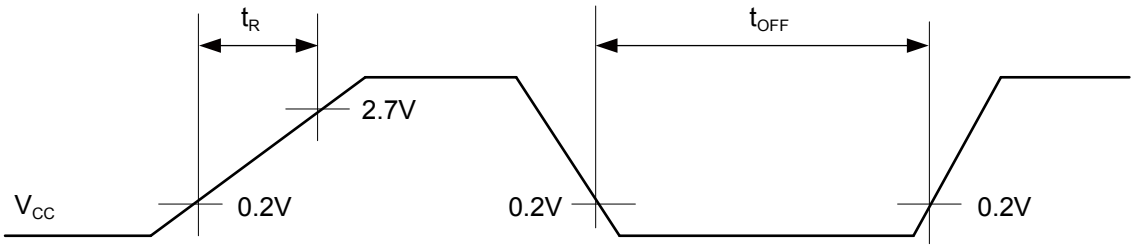
| Parameter | Symbol | Pin name | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Reset input time | $t_{RSTL}$ | RSTX | 10 | - | µs |
| Rejection of reset input time | | | 1 | - | µs |



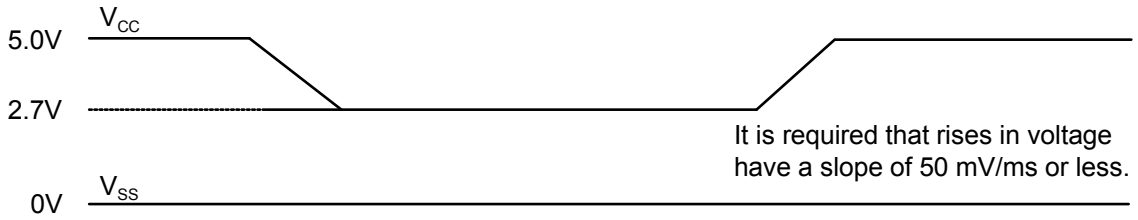
(7) Power-on Reset Timing

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

| Parameter | Symbol | Pin name | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Power on rise time | $t_R$ | Vcc | 0.05 | - | 30 | ms |
| Power off time | $t_{OFF}$ | Vcc | 1 | - | - | ms |




If the power supply is changed too rapidly, a power-on reset may occur. We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.




It is required that rises in voltage have a slope of 50 mV/ms or less.

(8) USART Timing

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C, $C_L$=50pF)

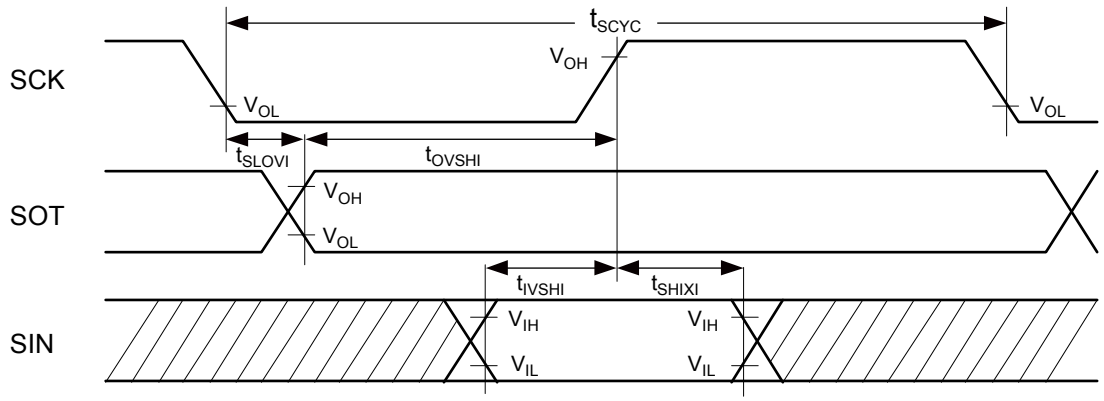
| Parameter | Symbol | Pin name | Conditions | 4.5V ≤ $V_{CC}$ < 5.5V | | 2.7V ≤ $V_{CC}$ < 4.5V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCKn | Internal shift clock mode | $4t_{CLKP1}$ | - | $4t_{CLKP1}$ | - | ns |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCKn, SOTn | | - 20 | + 20 | - 30 | + 30 | ns |
| SOT → SCK ↑ delay time | $t_{OVSHI}$ | SCKn, SOTn | | $N \times t_{CLKP1}$ – 20* | - | $N \times t_{CLKP1}$ – 30* | - | ns |
| SIN → SCK ↑ setup time | $t_{IVSHI}$ | SCKn, SINn | | $t_{CLKP1}$ + 45 | - | $t_{CLKP1}$ + 55 | - | ns |
| SCK ↑ → SIN hold time | $t_{SHIXI}$ | SCKn, SINn | | 0 | - | 0 | - | ns |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCKn | External shift clock mode | $t_{CLKP1}$ + 10 | - | $t_{CLKP1}$ + 10 | - | ns |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCKn | | $t_{CLKP1}$ + 10 | - | $t_{CLKP1}$ + 10 | - | ns |
| SCK ↓ → SOT delay time | $t_{SLOVE}$ | SCKn, SOTn | | - | $2t_{CLKP1}$ + 45 | - | $2t_{CLKP1}$ + 55 | ns |
| SIN → SCK ↑ setup time | $t_{IVSHE}$ | SCKn, SINn | | $t_{CLKP1}/2$ + 10 | - | $t_{CLKP1}/2$ + 10 | - | ns |
| SCK ↑ → SIN hold time | $t_{SHIXE}$ | SCKn, SINn | | $t_{CLKP1}$ + 10 | - | $t_{CLKP1}$ + 10 | - | ns |
| SCK fall time | $t_F$ | SCKn | | - | 20 | - | 20 | ns |
| SCK rise time | $t_R$ | SCKn | | - | 20 | - | 20 | ns |

Notes:
- AC characteristic in CLK synchronized mode.
- $C_L$ is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96600 series HARDWARE MANUAL”.
- $t_{CLKP1}$ indicates the peripheral clock 1 (CLKP1), Unit: ns
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKn and SOTn_R is not guaranteed.

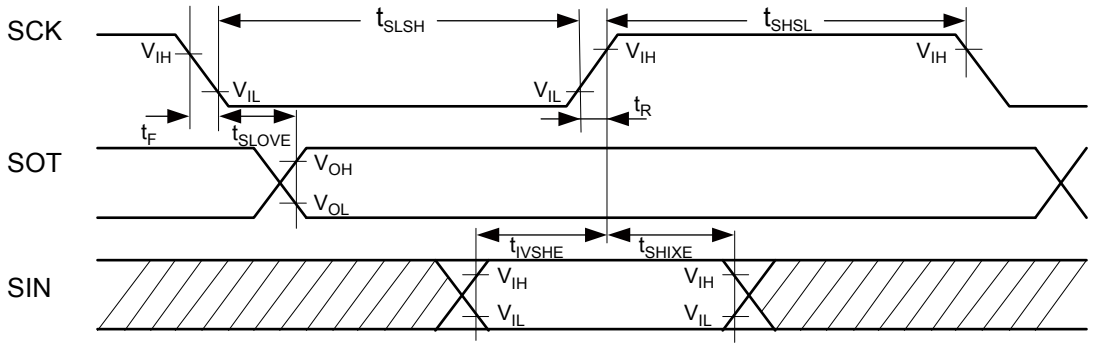
*: Parameter N depends on $t_{SCYC}$ and can be calculated as follows:
- If $t_{SCYC} = 2 \times k \times t_{CLKP1}$, then N = k, where k is an integer > 2
- If $t_{SCYC} = (2 \times k + 1) \times t_{CLKP1}$, then N = k + 1, where k is an integer > 1

Examples:

| $t_{SCYC}$ | N |
|---|---|
| $4 \times t_{CLKP1}$ | 2 |
| $5 \times t_{CLKP1}$, $6 \times t_{CLKP1}$ | 3 |
| $7 \times t_{CLKP1}$, $8 \times t_{CLKP1}$ | 4 |
| ... | ... |




Internal shift clock mode



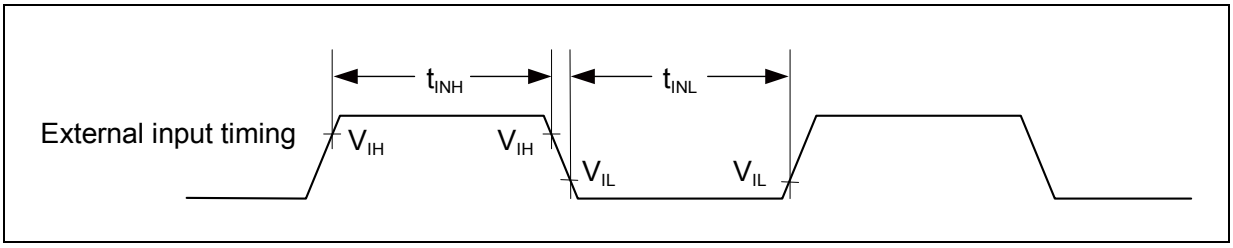

External shift clock mode

(9) External Input Timing

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Input pulse width | $t_{INH}$, $t_{INL}$ | Pnn_m | $2t_{CLKP1}$ +200 ($t_{CLKP1}$= $1/f_{CLKP1}$)* | - | ns | General Purpose I/O |
| | | ADTG | | | | A/D Converter trigger input |
| | | TINn, TINn_R | | | | Reload Timer |
| | | TTGn | | | | PPG trigger input |
| | | FRCKn, FRCKn_R | | | | Free-Running Timer input clock |
| | | INn, INn_R | | | | Input Capture |
| | | AINn, BINn, ZINn | | | | Quadrature Position/Revolution Counter |
| | | INTn, INTn_R | 200 | - | ns | External Interrupt |
| | | NMI | | | | Non-Maskable Interrupt |

*: $t_{CLKP1}$ indicates the peripheral clock1 (CLKP1) cycle time except stop when in stop mode.



(10) $I^2C$ Timing

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

| Parameter | Symbol | Conditions | Typical mode | | High-speed mode*4 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| SCL clock frequency | $f_{SCL}$ | $C_L$ = 50pF, R = (Vp/$I_{OL}$)*1 | 0 | 100 | 0 | 400 | kHz |
| (Repeated) START condition hold time SDA ↓ → SCL ↓ | $t_{HDSTA}$ | | 4.0 | - | 0.6 | - | µs |
| SCL clock "L" width | $t_{LOW}$ | | 4.7 | - | 1.3 | - | µs |
| SCL clock "H" width | $t_{HIGH}$ | | 4.0 | - | 0.6 | - | µs |
| (Repeated) START condition setup time SCL ↑ → SDA ↓ | $t_{SUSTA}$ | | 4.7 | - | 0.6 | - | µs |
| Data hold time SCL ↓ → SDA ↓ ↑ | $t_{HDDAT}$ | | 0 | 3.45*2 | 0 | 0.9*3 | µs |
| Data setup time SDA ↓ ↑ → SCL ↑ | $t_{SUDAT}$ | | 250 | - | 100 | - | ns |
| STOP condition setup time SCL ↑ → SDA ↑ | $t_{SUSTO}$ | | 4.0 | - | 0.6 | - | µs |
| Bus free time between "STOP condition" and "START condition" | $t_{BUS}$ | | 4.7 | - | 1.3 | - | µs |
| Pulse width of spikes which will be suppressed by input noise filter | $t_{SP}$ | - | 0 | (1-1.5) × $t_{CLKP1}$*5 | 0 | (1-1.5) × $t_{CLKP1}$*5 | ns |

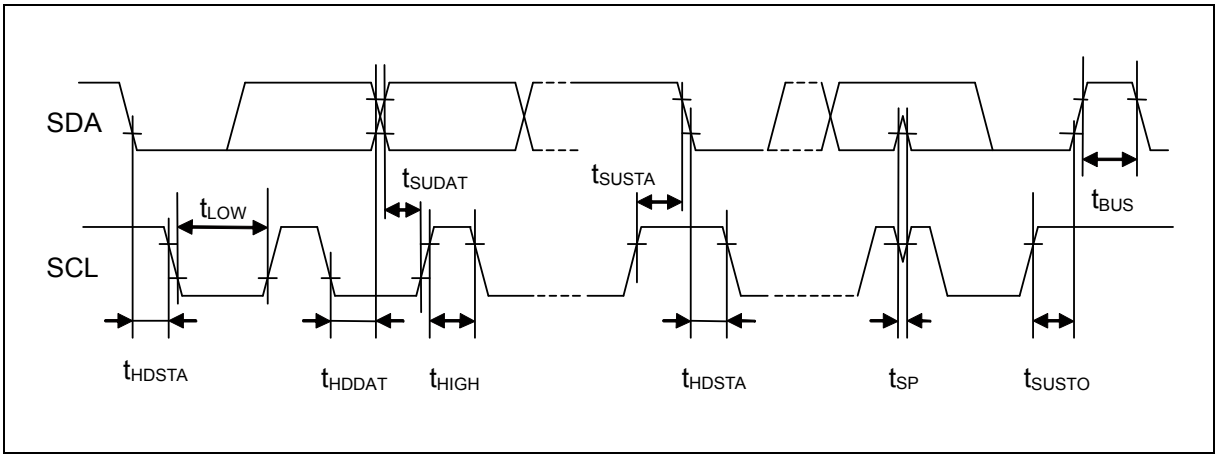
*1: R and $C_L$ represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and $I_{OL}$ indicates $V_{OL}$ guaranteed current.

*2: The maximum $t_{HDDAT}$ only has to be met if the device does not extend the "L" width ($t_{LOW}$) of the SCL signal.

*3: A high-speed mode $I^2C$ bus device can be used on a standard mode $I^2C$ bus system as long as the device satisfies the requirement of "$t_{SUDAT} \geq 250ns$".

*4: For use at over 100kHz, set the peripheral clock1 (CLKP1) to at least 6MHz.

*5: $t_{CLKP1}$ indicates the peripheral clock1 (CLKP1) cycle time.



## 5. A/D Converter

### (1) Electrical Characteristics for the A/D Converter

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

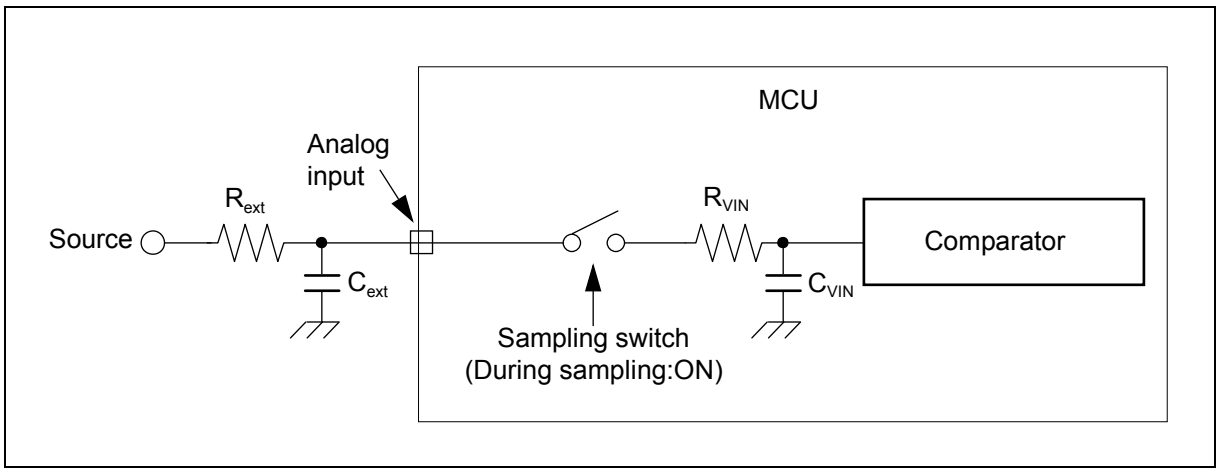
| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | - | - | - | - | 10 | bit | |
| Total error | - | - | - 3.0 | - | + 3.0 | LSB | |
| Nonlinearity error | - | - | - 2.5 | - | + 2.5 | LSB | |
| Differential Nonlinearity error | - | - | - 1.9 | - | + 1.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | ANn | Typ - 20 | AVRL + 0.5LSB | Typ + 20 | mV | |
| Full scale transition voltage | $V_{FST}$ | ANn | Typ - 20 | AVRH - 1.5LSB | Typ + 20 | mV | |
| Compare time* | - | - | 1.0 | - | 5.0 | µs | 4.5V ≤ $AV_{CC}$ ≤ 5.5V |
| | | | 2.2 | - | 8.0 | µs | 2.7V ≤ $AV_{CC}$ < 4.5V |
| Sampling time* | - | - | 0.5 | - | - | µs | 4.5V ≤ $AV_{CC}$ ≤ 5.5V |
| | | | 1.2 | - | - | µs | 2.7V ≤ $AV_{CC}$ < 4.5V |
| Power supply current | $I_A$ | $AV_{CC}$ | - | 2.0 | 3.1 | mA | A/D Converter active |
| | $I_{AH}$ | | - | - | 3.3 | µA | A/D Converter not operated |
| Reference power supply current (between AVRH and AVRL) | $I_R$ | AVRH | - | 520 | 810 | µA | A/D Converter active |
| | $I_{RH}$ | | - | - | 1.0 | µA | A/D Converter not operated |
| Analog input capacity | $C_{VIN}$ | ANn | - | - | 15.9 | pF | |
| Analog impedance | $R_{VIN}$ | ANn | - | - | 2050 | Ω | 4.5V ≤ $AV_{CC}$ ≤ 5.5V |
| | | | - | - | 3600 | Ω | 2.7V ≤ $AV_{CC}$ < 4.5V |
| Analog port input current (during conversion) | $I_{AIN}$ | ANn | - 0.3 | - | + 0.3 | µA | $AV_{SS}$ , AVRL < $V_{AIN}$ < $AV_{CC}$, AVRH |
| Analog input voltage | $V_{AIN}$ | ANn | AVRL | - | AVRH | V | |
| Reference voltage range | - | AVRH | $AV_{CC}$ - 0.1 | - | $AV_{CC}$ | V | |
| | - | AVRL | $AV_{SS}$ | - | $AV_{SS}$ + 0.1 | V | |
| Variation between channels | - | ANn | - | - | 4.0 | LSB | |

*: Time for each channel.

(2) Accuracy and Setting of the A/D Converter Sampling Time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time (Tsamp) depends on the external driving impedance $R_{ext}$, the board capacitance of the A/D converter input pin $C_{ext}$ and the $AV_{CC}$ voltage level. The following replacement model can be used for the calculation:




$R_{ext}$: External driving impedance

$C_{ext}$: Capacitance of PCB at A/D converter input

$C_{VIN}$: Analog input capacity (I/O, analog switch and ADC are contained)

$R_{VIN}$: Analog input impedance (I/O, analog switch and ADC are contained)

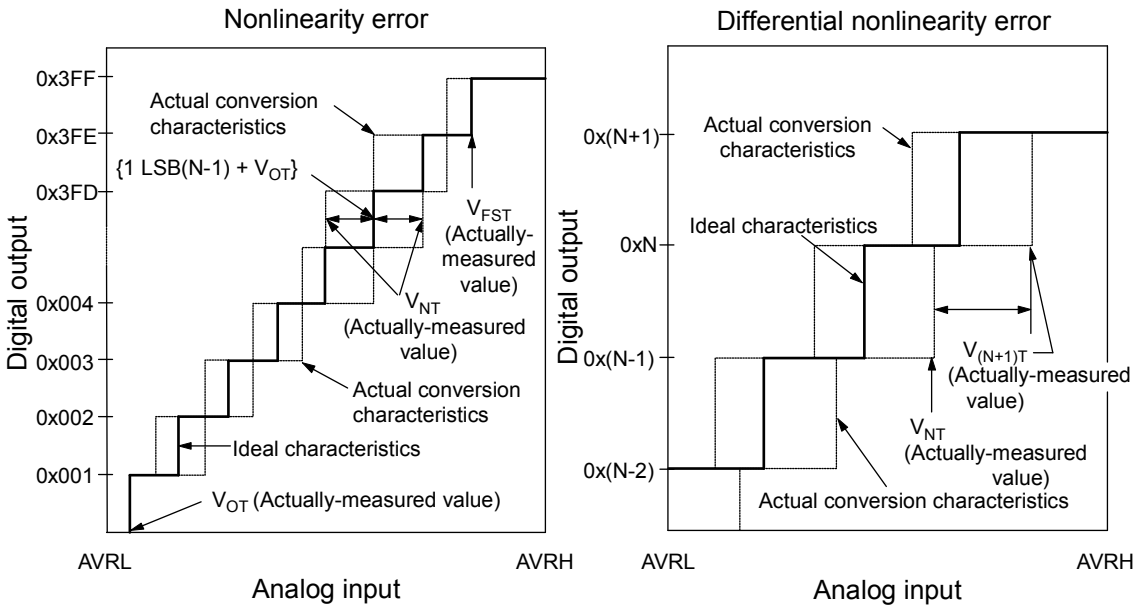
The following approximation formula for the replacement model above can be used:

$Tsamp = 7.62 \times (Rext \times Cext + (Rext + R_{VIN}) \times C_{VIN})$

- Do not select a sampling time below the absolute minimum permitted value.
  ($0.5\mu s$ for $4.5V \leq AV_{CC} \leq 5.5V$, $1.2\mu s$ for $2.7V \leq AV_{CC} < 4.5V$)
- If the sampling time cannot be sufficient, connect a capacitor of about $0.1\mu F$ to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current IIL (static current before the sampling switch) or the analog input leakage current IAIN (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current IIL cannot be compensated by an external capacitor.
- The accuracy gets worse as |AVRH - AVRL| becomes smaller.

(3) Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Nonlinearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ⟷ 0b0000000001) to the full-scale transition point (0b1111111110 ⟷ 0b1111111111).
- Differential nonlinearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- Zero transition voltage: Input voltage which results in the minimum conversion value.
- Full scale transition voltage: Input voltage which results in the maximum conversion value.

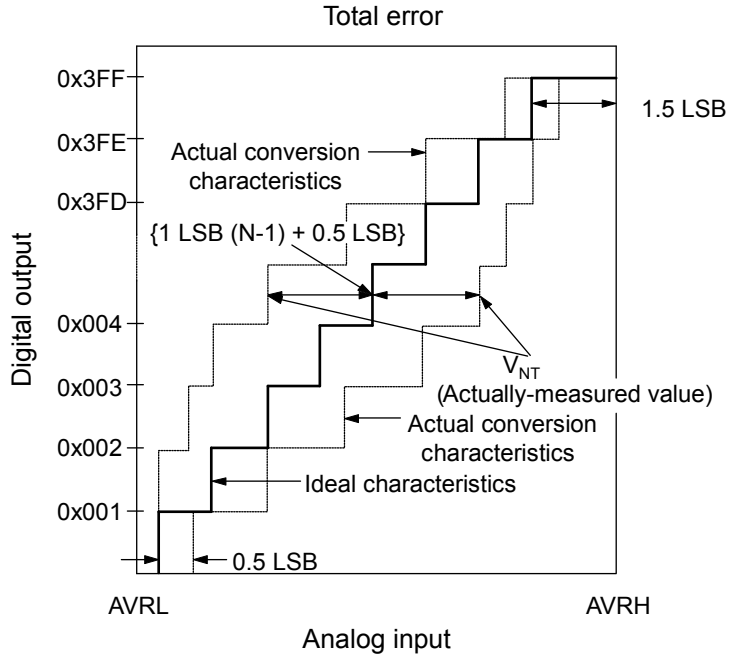



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022}$$

N : A/D converter digital output value.
$V_{OT}$ : Voltage at which the digital output changes from 0x000 to 0x001.
$V_{FST}$ : Voltage at which the digital output changes from 0x3FE to 0x3FF.
$V_{NT}$ : Voltage at which the digital output changes from 0x(N − 1) to 0xN.




$$1LSB\ (Ideal\ value) = \frac{AVRH - AVRL}{1024}\ [V]$$

$$Total\ error\ of\ digital\ output\ N = \frac{V_{NT} - \{1LSB \times (N - 1) + 0.5LSB\}}{1LSB}$$

N : A/D converter digital output value.
$V_{NT}$ : Voltage at which the digital output changes from 0x(N + 1) to 0xN.
$V_{OT}$ (Ideal value) = AVRL + 0.5LSB[V]
$V_{FST}$ (Ideal value) = AVRH - 1.5LSB[V]

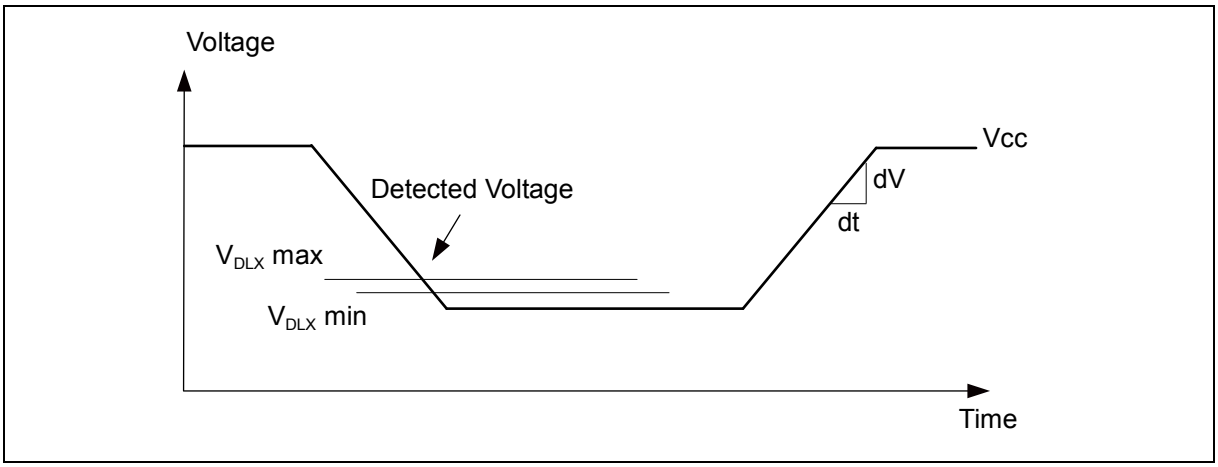
## 6. Low Voltage Detection Function Characteristics

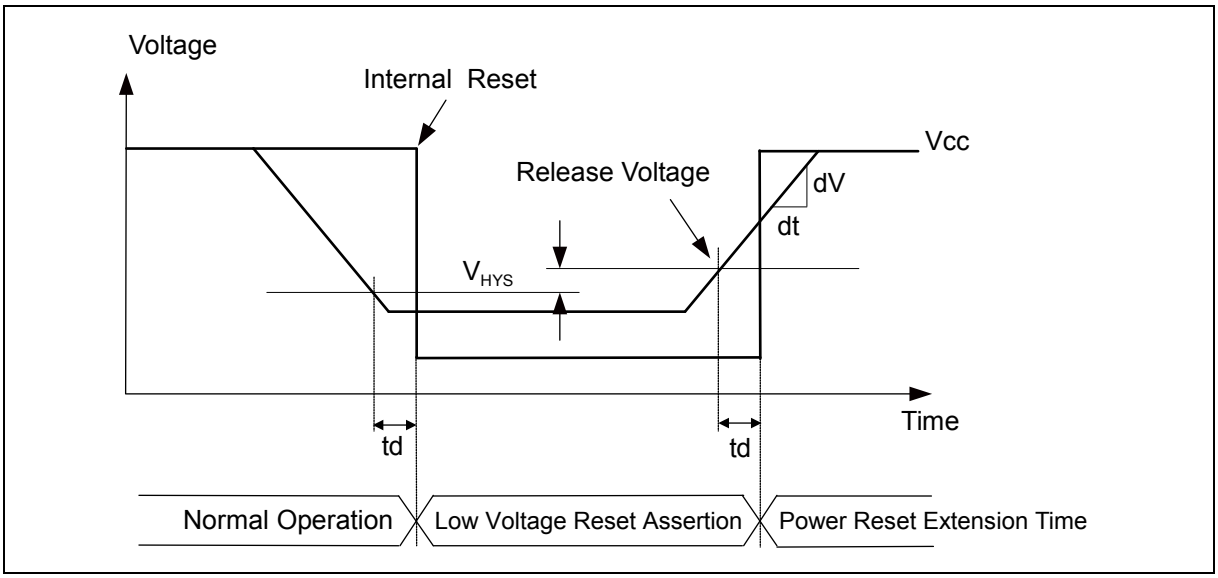
($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

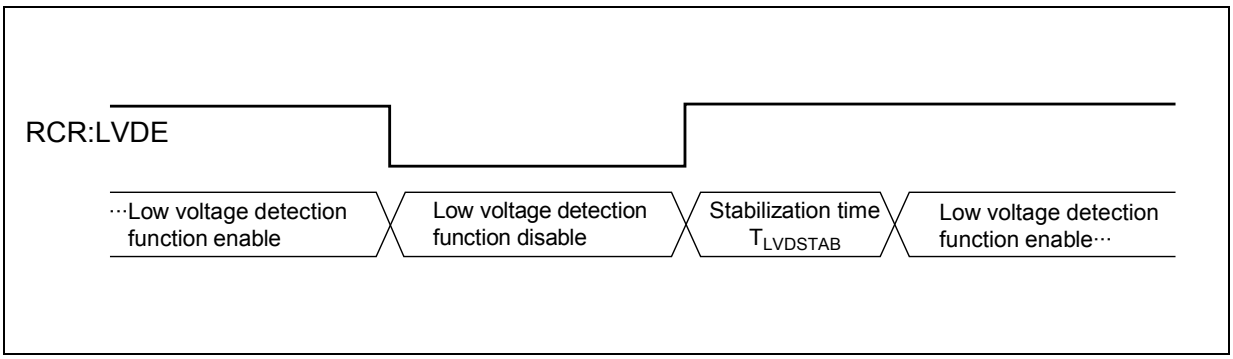
| Parameter | Symbol | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Detected voltage*1 | $V_{DL0}$ | CILCR:LVL = $0000_B$ | 2.70 | 2.90 | 3.10 | V |
| | $V_{DL1}$ | CILCR:LVL = $0001_B$ | 2.79 | 3.00 | 3.21 | V |
| | $V_{DL2}$ | CILCR:LVL = $0010_B$ | 2.98 | 3.20 | 3.42 | V |
| | $V_{DL3}$ | CILCR:LVL = $0011_B$ | 3.26 | 3.50 | 3.74 | V |
| | $V_{DL4}$ | CILCR:LVL = $0100_B$ | 3.45 | 3.70 | 3.95 | V |
| | $V_{DL5}$ | CILCR:LVL = $0111_B$ | 3.73 | 4.00 | 4.27 | V |
| | $V_{DL6}$ | CILCR:LVL = $1001_B$ | 3.91 | 4.20 | 4.49 | V |
| Power supply voltage change rate*2 | dV/dt | - | - 0.004 | - | + 0.004 | V/µs |
| Hysteresis width | $V_{HYS}$ | CILCR:LVHYS=0 | - | - | 50 | mV |
| | | CILCR:LVHYS=1 | 80 | 100 | 120 | mV |
| Stabilization time | $T_{LVDSTAB}$ | - | - | - | 75 | µs |
| Detection delay time | $t_d$ | - | - | - | 30 | µs |

*1: If the power supply voltage fluctuates within the time less than the detection delay time ($t_d$), there is a possibility that the low voltage detection will occur or stop after the power supply voltage passes the detection range.

*2: In order to perform the low voltage detection at the detection voltage ($V_{DLX}$), be sure to suppress fluctuation of the power supply voltage within the limits of the change ration of power supply voltage.


Voltage
Vcc
Detected Voltage
dV
dt
$V_{DLX}$ max
$V_{DLX}$ min
Time


Voltage
Internal Reset
Vcc
Release Voltage
dV
dt
$V_{HYS}$
Time
td
td
Normal Operation
Low Voltage Reset Assertion
Power Reset Extension Time


RCR:LVDE
···Low voltage detection function enable
Low voltage detection function disable
Stabilization time $T_{LVDSTAB}$
Low voltage detection function enable···

## 7. Flash Memory Write/Erase Characteristics

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

| Parameter | | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Sector erase time | Large Sector | $T_A \leq$ + 105°C | - | 1.6 | 7.5 | s | Includes write time prior to internal erase. |
| | Small Sector | - | - | 0.4 | 2.1 | s | |
| | Security Sector | - | - | 0.31 | 1.65 | s | |
| Word (16-bit) write time | Large Sector | $T_A \leq$ + 105°C | - | 25 | 400 | µs | Not including system-level overhead time. |
| | Small Sector | - | - | 25 | 400 | µs | |
| Chip erase time | | $T_A \leq$ + 105°C | - | 11.51 | 55.05 | s | Includes write time prior to internal erase. |

Note: While the Flash memory is written or erased, shutdown of the external power ($V_{CC}$) is prohibited. In the application system where the external power ($V_{CC}$) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.
To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage ($V_{DLX}$)[*1].

Write/Erase cycles and data hold time

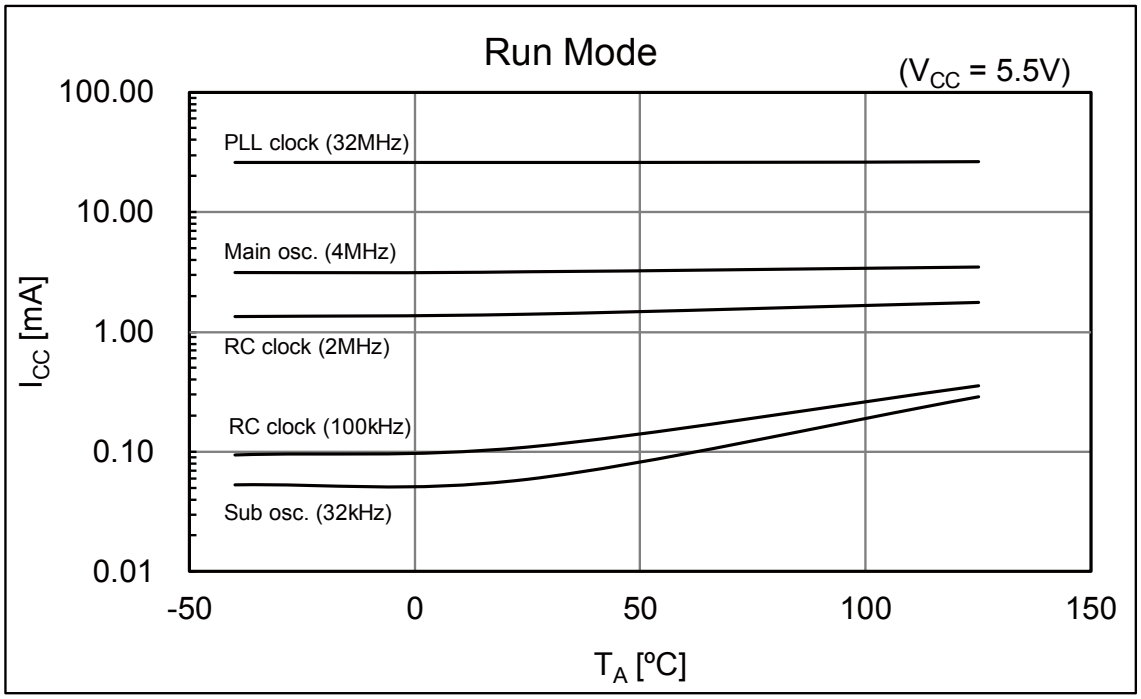
| Write/Erase cycles (cycle) | Data hold time (year) |
|---|---|
| 1,000 | 20 [*2] |
| 10,000 | 10 [*2] |
| 100,000 | 5 [*2] |

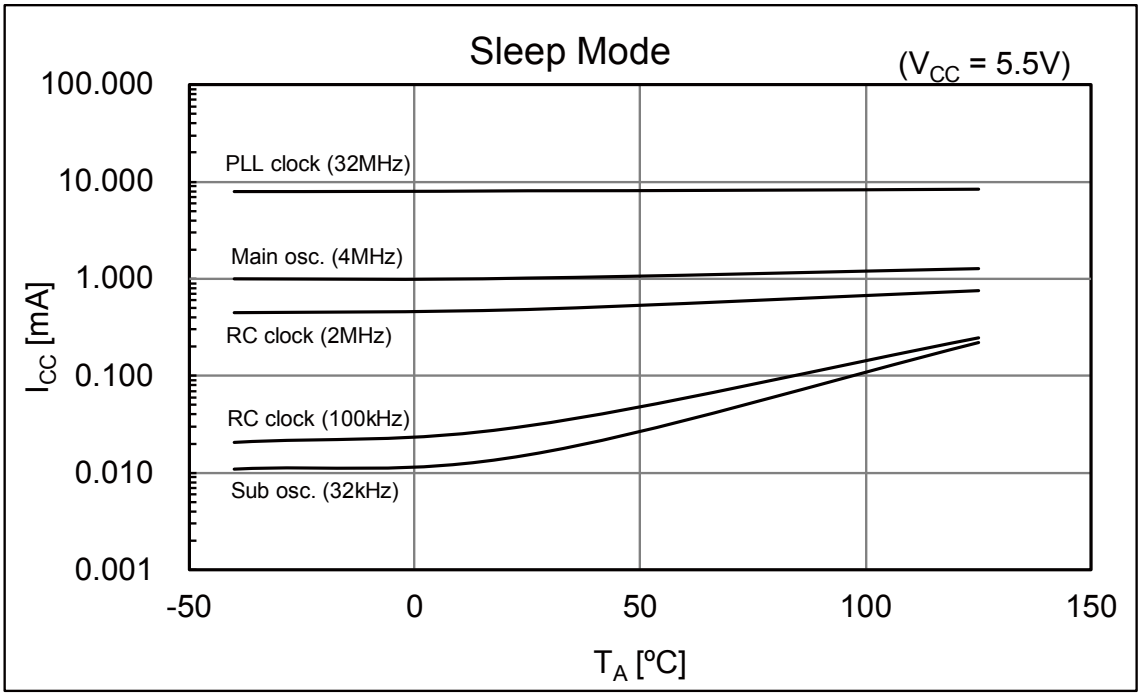
*1: See "6. Low Voltage Detection Function Characteristics".
*2: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

## ■ EXAMPLE CHARACTERISTICS

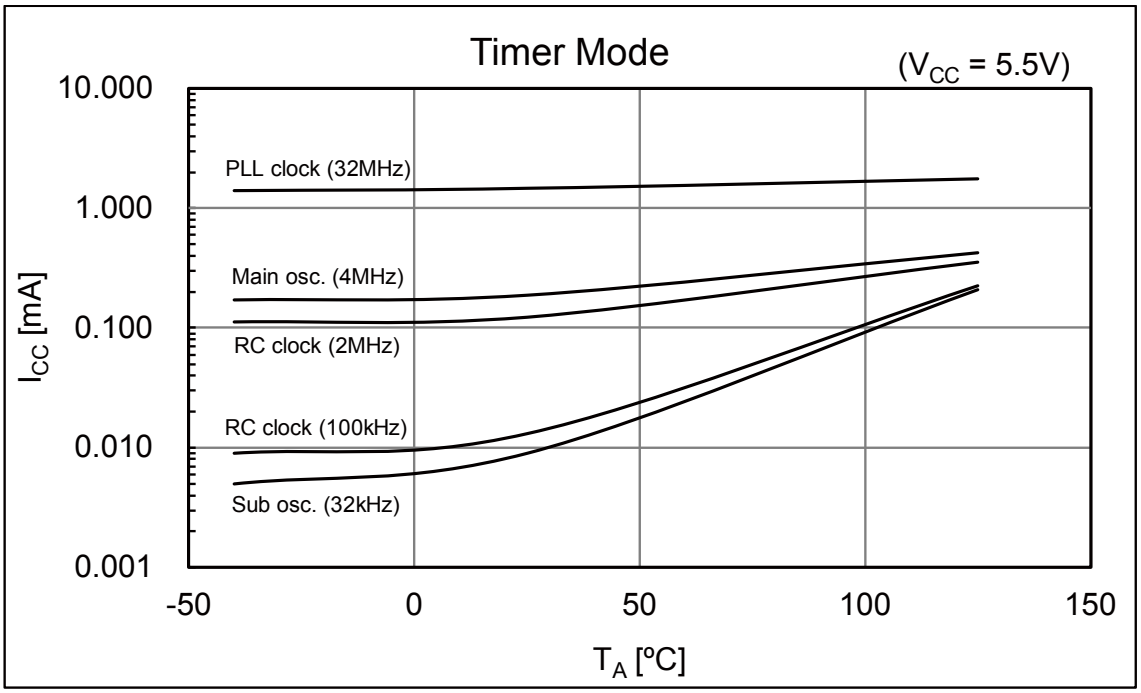
This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

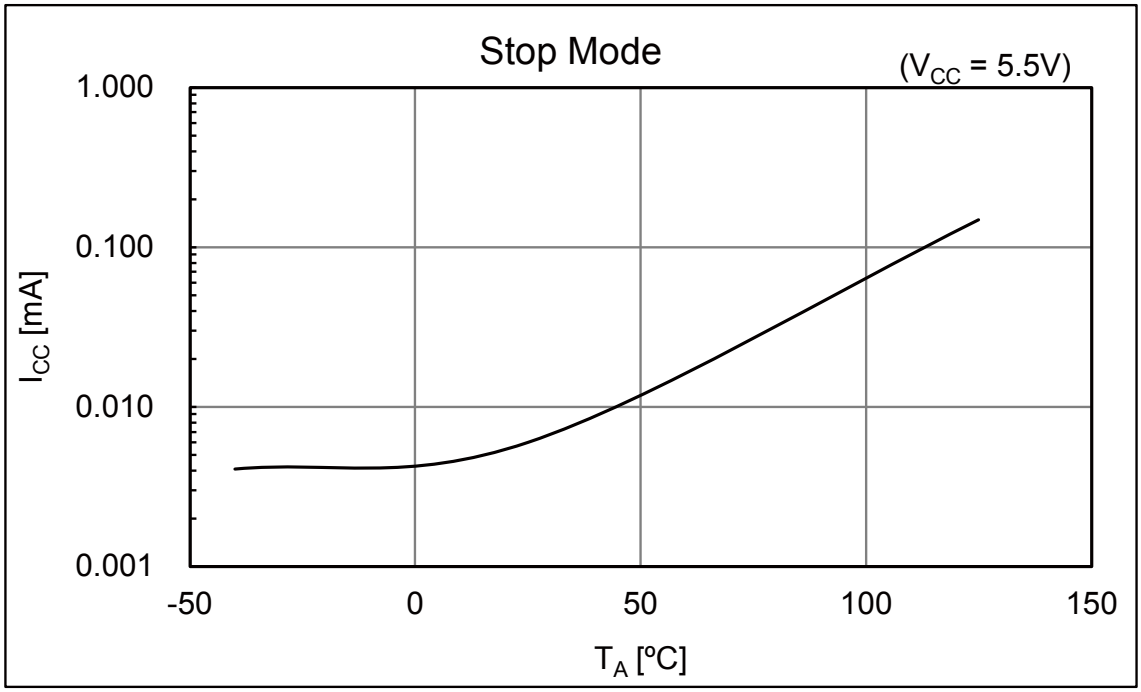
- MB96F657



• MB96F657


Timer Mode
($V_{CC}$ = 5.5V)
10.000
1.000
0.100
0.010
0.001
$I_{CC}$ [mA]
PLL clock (32MHz)
Main osc. (4MHz)
RC clock (2MHz)
RC clock (100kHz)
Sub osc. (32kHz)
-50
0
50
100
150
$T_A$ [ºC]


Stop Mode
($V_{CC}$ = 5.5V)
1.000
0.100
0.010
0.001
$I_{CC}$ [mA]
-50
0
50
100
150
$T_A$ [ºC]

• Used setting

| Mode | Selected Source Clock | Clock/Regulator and FLASH Settings |
|---|---|---|
| Run mode | PLL | CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32MHz |
| | Main osc. | CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4MHz |
| | RC clock fast | CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2MHz |
| | RC clock slow | CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100kHz |
| | Sub osc. | CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32kHz |
| Sleep mode | PLL | CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32MHz<br>Regulator in High Power Mode,<br>(CLKB is stopped in this mode) |
| | Main osc. | CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4MHz<br>Regulator in High Power Mode,<br>(CLKB is stopped in this mode) |
| | RC clock fast | CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2MHz<br>Regulator in High Power Mode,<br>(CLKB is stopped in this mode) |
| | RC clock slow | CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100kHz<br>Regulator in Low Power Mode,<br>(CLKB is stopped in this mode) |
| | Sub osc. | CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32kHz<br>Regulator in Low Power Mode,<br>(CLKB is stopped in this mode) |
| Timer mode | PLL | CLKMC = 4MHz, CLKPLL = 32MHz<br>(System clocks are stopped in this mode)<br>Regulator in High Power Mode,<br>FLASH in Power-down / reset mode |
| | Main osc. | CLKMC = 4MHz<br>(System clocks are stopped in this mode)<br>Regulator in High Power Mode,<br>FLASH in Power-down / reset mode |
| | RC clock fast | CLKMC = 2MHz<br>(System clocks are stopped in this mode)<br>Regulator in High Power Mode,<br>FLASH in Power-down / reset mode |
| | RC clock slow | CLKMC = 100kHz<br>(System clocks are stopped in this mode)<br>Regulator in Low Power Mode,<br>FLASH in Power-down / reset mode |
| | Sub osc. | CLKMC = 32 kHz<br>(System clocks are stopped in this mode)<br>Regulator in Low Power Mode,<br>FLASH in Power-down / reset mode |
| Stop mode | stopped | (All clocks are stopped in this mode)<br>Regulator in Low Power Mode,<br>FLASH in Power-down / reset mode |

## ■ ORDERING INFORMATION

MCU with CAN controller

| Part number | Flash memory | Package* |
|---|---|---|
| MB96F653RBPMC-GSE1 | Flash A (96.5KB) | 120-pin plastic LQFP (FPT-120P-M21) |
| MB96F653RBPMC-GSE2 | | |
| MB96F655RBPMC-GSE1 | Flash A (160.5KB) | 120-pin plastic LQFP (FPT-120P-M21) |
| MB96F655RBPMC-GSE2 | | |
| MB96F656RBPMC-GSE1 | Flash A (288.5KB) | 120-pin plastic LQFP (FPT-120P-M21) |
| MB96F656RBPMC-GSE2 | | |
| MB96F657RBPMC-GSE1 | Flash A (416.5KB) | 120-pin plastic LQFP (FPT-120P-M21) |
| MB96F657RBPMC-GSE2 | | |

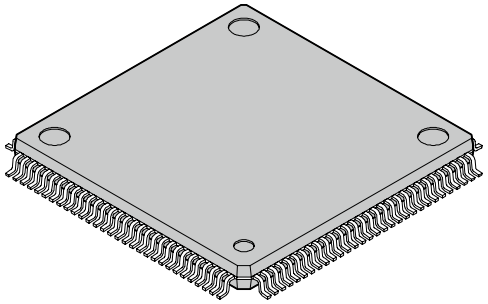
*: For details about package, see "■PACKAGE DIMENSION".

MCU without CAN controller

| Part number | Flash memory | Package* |
|---|---|---|
| MB96F653ABPMC-GSE1 | Flash A (96.5KB) | 120-pin plastic LQFP (FPT-120P-M21) |
| MB96F653ABPMC-GSE2 | | |
| MB96F655ABPMC-GSE1 | Flash A (160.5KB) | 120-pin plastic LQFP (FPT-120P-M21) |
| MB96F655ABPMC-GSE2 | | |

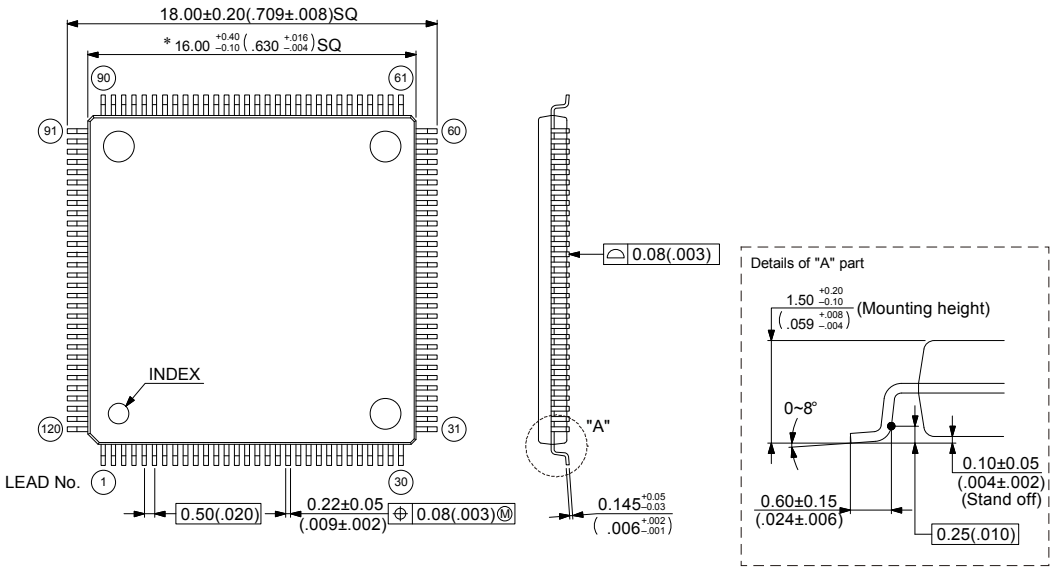
*: For details about package, see "■PACKAGE DIMENSION".

## ■ PACKAGE DIMENSION

| 120-pin plastic LQFP | | |
|---|---|---|
|  | Lead pitch | 0.50 mm |
| | Package width × package length | 16.0 × 16.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.88 g |
| (FPT-120P-M21) | Code (Reference) | P-LFQFP120-16×16-0.50 |

120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.






Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

## ■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

| Page | Section | Change Results |
|---|---|---|
| - | - | PRELIMINARY → Data sheet |
| 2 | ■FEATURES | Changed the description of "System clock"<br>Up to 16 MHz external clock for devices with fast clock input feature<br>→<br>Up to 8 MHz external clock for devices with fast clock input feature |
| 4 | | Changed the description of "External Interrupts"<br>Interrupt mask and pending bit per channel<br>→<br>Interrupt mask bit per channel |
| | | Changed the description of "Built-in On Chip Debugger"<br>- Event sequencer: 2 levels<br>→<br>- Event sequencer: 2 levels + reset |
| 5 | ■PRODUCT LINEUP | Added the Product |
| | | Changed the Remark of RLT<br>RLT 0/1/2/3/6 Only RLT6 can be used as PPG clock source<br>→<br>RLT 0 to 3/6 |
| 6 | ■BLOCK DIAGRAM | Deleted the block of RLT6 from PPG block |
| | | Changed the RLT block<br>4ch<br>→<br>0/1/2/3/6 5ch |
| 8 | ■PIN DESCRIPTION | Changed the Description of PPGn_B<br>Programmable Pulse Generator n output (8bit)<br>→<br>Programmable Pulse Generator n output (16bit/8bit) |
| 14 | ■I/O CIRCUIT TYPE | Changed the figure of type B |
| | | Changed the Remarks of type B<br>(CMOS hysteresis input with input shutdown function, $I_{OL}$ = 4mA, $I_{OH}$ = -4mA, Programmable pull-up resister)<br>→<br>(CMOS level output ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA), Automotive input with input shutdown function and programmable pull-up resistor) |
| 15 | | Changed the figure of type G |
| 18 | ■MEMORY MAP | Changed the START addresses of Boot-ROM<br>$0F:E000_H$<br>→<br>$0F:C000_H$ |

| Page | Section | Change Results |
|---|---|---|
| 20 | ■USER ROM MEMORY MAP FOR FLASH DEVICES | Changed the annotation<br>Others (from DF:$0200_H$ to DF:$1FFF_H$) are all mirror area of SAS-512B.<br>→<br>Others (from DF:$0200_H$ to DF:$1FFF_H$) is mirror area of SAS-512B. |
| 22 | ■INTERRUPT VECTOR TABLE | Changed the Description of CALLV0 to CALLV7<br>Reserved<br>→<br>CALLV instruction |
| | | Changed the Description of RESET<br>Reserved<br>→<br>Reset vector |
| | | Changed the Description of INT9<br>Reserved<br>→<br>INT9 instruction |
| | | Changed the Description of EXCEPTION<br>Reserved<br>→<br>Undefined instruction execution |
| 23 | | Changed the Vector name of Vector number 64<br>PPGRLT<br>→<br>RLT6 |
| | | Changed the Description of Vector number 64<br>Reload Timer 6 can be used as PPG clock source<br>→<br>Reload Timer 6 |
| 26 to 29 | ■HANDLING PRECAUTIONS | Added a section |
| 31 | ■HANDLING DEVICES | Added the description to “3. External clock usage”<br>(3) Opposite phase external clock |
| | | Changed the description in “7. Turn on sequence of power supply to A/D converter and analog inputs”<br><br>In this case, the voltage must not exceed AVRH or $AV_{CC}$<br>→<br>In this case, AVRH must not exceed $AV_{CC}$. Input voltage for ports shared with analog input ports also must not exceed $AV_{CC}$ |
| 32 | | Added the description “12. Mode Pin (MD)” |
| 34 | ■ELECTRICAL CHARACTERISTICS<br>1. Absolute Maximum Ratings | Changed the annotation *4<br>Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).<br>→<br>Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset. |

| Page | Section | Change Results |
|---|---|---|
| 34 | 1. Absolute Maximum Ratings | Added the annotation *4<br>The DEBUG I/F pin has only a protective diode against $V_{SS}$. Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V. |
| 36 | 2. Recommended Operating Conditions | Added the Value and Remarks to “Power supply voltage”<br>Min: 2.0V<br>Typ: -<br>Max: 5.5V<br>Remarks: Maintains RAM data in stop mode |
| | | Changed the Value of “Smoothing capacitor at C pin”<br>Typ: 1.0µF → 1.0µF to 3.9µF<br>Max: 1.5µF → 4.7µF |
| | | Changed the Remarks of “Smoothing capacitor at C pin”<br>Deleted “(Target value)”<br>Added “3.9µF (Allowance within ± 20%)” |
| 37 | 3. DC Characteristics<br>(1) Current Rating | Deleted “(Target value)” from Remarks |
| | | Added the Symbol to “Power supply current in Run modes”<br>$I_{CCRCH}$, $I_{CCRCL}$ |
| | | Changed the Conditions of $I_{CCPLL}$, $I_{CCMAIN}$, $I_{CCSUB}$ in “Power supply current in Run modes”<br>“Flash 0 wait” is added |
| | | Changed the Value of “Power supply current in Run modes”<br>$I_{CCPLL}$<br>Max: 37.5mA → 37mA ($T_A$ = +105°C)<br>Max: 39mA → 38.5mA ($T_A$ = +125°C)<br>$I_{CCMAIN}$<br>Max: 9mA → 8mA ($T_A$ = +105°C)<br>Max: 10.5mA → 9.5mA ($T_A$ = +125°C)<br>$I_{CCSUB}$<br>Max: 6mA → 3.3mA ($T_A$ = +105°C)<br>Max: 7.5mA → 4.8mA ($T_A$ = +125°C) |
| 38 | | Added the Symbol to “Power supply current in Sleep modes”<br>$I_{CCSRCH}$, $I_{CCSRCL}$ |
| | | Changed the Conditions of $I_{CCSMAIN}$ in “Power supply current in Sleep modes”<br>“SMCR:LPMSS=0” is added |
| | | Changed the Value of “Power supply current in Sleep modes”<br>$I_{CCSPLL}$<br>Typ: 10mA → 8.5mA ($T_A$ = +25°C)<br>Max : 15mA → 14mA ($T_A$ = +105°C)<br>Max : 16.5mA → 15.5mA ($T_A$ = +125°C)<br>$I_{CCSMAIN}$<br>Max: 7mA → 4.5m A ($T_A$ = +105°C)<br>Max : 8.5mA → 6mA ($T_A$ = +125°C)<br>$I_{CCSSUB}$<br>Typ: 0.08mA → 0.04m A ($T_A$ = +25°C)<br>Max: 4mA → 2.5m A ($T_A$ = +105°C)<br>Max : 5.5mA → 4mA ($T_A$ = +125°C) |

| Page | Section | Change Results |
|---|---|---|
| 39 | 3. DC Characteristics<br>(1) Current Rating | Added the Symbol to “Power supply current in Timer modes”<br>$I_{CCTPLL}$ |
| | | Changed the Conditions of $I_{CCTMAIN}$, $I_{CCTRCH}$ in “Power supply current in Timer modes”<br>“SMCR:LPMSS=0” is added |
| | | Changed the Value of “Power supply current in Timer modes”<br>$I_{CCTMAIN}$<br>Max: 355µA → 330µA ($T_A$ = +25°C)<br>Max: 1300µA → 1195µA ($T_A$ = +105°C)<br>Max: 2310µA → 2165µA ($T_A$ = +125°C)<br>$I_{CCTRCH}$<br>Max: 245µA → 215µA ($T_A$ = +25°C)<br>Max: 1215µA → 1095µA ($T_A$ = +105°C)<br>Max: 2215µA → 2075µA ($T_A$ = +125°C)<br>$I_{CCTRCL}$<br>Max: 105µA → 75µA ($T_A$ = +25°C)<br>Max: 1010µA → 905µA ($T_A$ = +105°C)<br>Max: 2015µA → 1880µA ($T_A$ = +125°C)<br>$I_{CCTSUB}$<br>Max: 90µA → 65µA ($T_A$ = +25°C)<br>Max: 985µA → 885µA ($T_A$ = +105°C)<br>Max: 1990µA → 1850µA ($T_A$ = +125°C) |
| 40 | | Changed the Value of “Power supply current in Stop modes”<br>$I_{CCH}$<br>Max: 90µA → 60µA ($T_A$ = +25°C)<br>Max: 985µA → 880µA ($T_A$ = +105°C)<br>Max: 1985µA → 1845µA ($T_A$ = +125°C) |
| | | Added the Symbol<br>$I_{CCFLASHPD}$ |
| | | Changed the Value and condition of “Power supply current for active Low Voltage detector”<br>$I_{CCLVD}$<br>Typ: 5µA, Max: 15µA, Remarks: nothing<br>→<br>Typ: 5µA, Max: -, Remarks: $T_A$ = +25°C<br>Typ: -, Max: 12.5µA, Remarks: $T_A$ = +125°C |
| | | Changed the condition of “Flash Write/Erase current”<br>$I_{CCFLASH}$<br>Typ: 12.5mA, Max: 20mA, Remarks: nothing<br>→<br>Typ: 12.5mA, Max: -, Remarks: $T_A$ = +25°C<br>Typ: -, Max: 20mA, Remarks: $T_A$ = +125°C |
| | | Changed the annotation *2<br>The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator.<br>→<br>When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.<br>The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. The current for "On Chip Debugger" part is not included. |

| Page | Section | Change Results |
|---|---|---|
| 42 | 3. DC Characteristics<br>(2) Pin Characteristics | Added the Symbol for DEBUG I/F pin<br>$V_{OLD}$ |
| | | Changed the Pin name of “Input capacitance”<br>Other than<br>Vcc,<br>Vss,<br>AVcc,<br>AVss,<br>AVRH<br>AVRL<br>→<br>Other than<br>C,<br>Vcc,<br>Vss,<br>AVcc,<br>AVss,<br>AVRH<br>AVRL |
| | | Deleted the annotation<br>“$I_{OH}$ and $I_{OL}$ are target value.” |
| 43 | 4. AC Characteristics<br>(1) Main Clock Input Characteristics | Changed MAX frequency for $f_{FCI}$ in all conditions<br>16→8<br>Changed MIN frequency for $t_{CYLH}$<br>62.5→125<br>Changed MIN, MAX and Unit for $P_{WH}$ , $P_{WL}$<br>MIN: 30→55<br>MAX: 70→-<br>Unit: %→ns |
| | | Added the figure ($t_{CYLH}$) when using the external clock |
| 44 | 4. AC Characteristics<br>(2) Sub Clock Input Characteristics | Added the figure ($t_{CYLL}$) when using the crystal oscillator clock |
| 45 | 4. AC Characteristics<br>(3) Built-in RC Oscillation Characteristics | Added “RC clock stabilization time” |
| 46 | 4. AC Characteristics<br>(5) Operating Conditions of PLL | Changed the Value of “PLL input clock frequency”<br>Max: 16MHz → 8MHz |
| | | Changed the Symbol of “PLL oscillation clock frequency”<br>$f_{PLLO}$ → $f_{CLKVCO}$ |
| | | Added Remarks to “PLL oscillation clock frequency” |
| | | Added “ PLL phase jitter” and the figure |
| | 4. AC Characteristics<br>(6) Reset Input | Added the figure for reset input time ($t_{RSTL}$) |
| 48 | 4. AC Characteristics<br>(8) USART Timing | Changed the condition<br>($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 105°C)<br>→<br>($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C, $C_L$=50pF) |
| | | Changed the HARDWARE MANUAL<br>“MB96650 series HARDWARE MANUAL”<br>→<br>“MB96600 series HARDWARE MANUAL” |
| 49 | | Changed the figure for “Internal shift clock mode” |

| Page | Section | Change Results |
|---|---|---|
| 51 | 4. AC Characteristics<br>(10) $I^2C$ timing | Added parameter, “Noise filter” and an annotation *5 for it |
| | | Added $t_{SP}$ to the figure |
| 52 | 5. A/D Converter<br>(1) Electrical Characteristics for the A/D Converter | Added “Analog impedance” |
| | | Added “Variation between channels” |
| | | Added the annotation |
| 53 | 5. A/D Converter<br>(2) Accuracy and Setting of the A/D Converter Sampling Time | Deleted the unit “[min]” from approximation formula of Sampling time |
| 54 | 5. A/D Converter<br>(3) Definition of A/D Converter Terms | Changed the Description and the figure<br>“Linearity” → “Nonlinearity”<br>“Differential linearity error”<br>→<br>“Differential nonlinearity error” |
| | | Changed the Description<br>Linearity error:<br>Deviation of the line between the zero-transition point (0b0000000000←→0b0000000001) and the full-scale transition point (0b1111111110←→0b1111111111) from the actual conversion characteristics.<br>→<br>Nonlinearity error:<br>Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ←→ 0b0000000001) to the full-scale transition point (0b1111111110 ←→ 0b1111111111). |
| | | Added the Description<br>“Zero transition voltage”<br>“Full scale transition voltage” |
| 56 | 6. Low Voltage Detection Function Characteristics | Added the Value of “ Power supply voltage change rate”<br>Max: +0.004 V/µs |
| | | Added “Hysteresis width” ($V_{HYS}$) |
| | | Added “Stabilization time” ($T_{LVDSTAB}$) |
| | | Added “Detection delay time” ($t_d$) |
| | | Deleted the Remarks |
| | | Added the annotation *1, *2 |
| 57 | | Added the figure for “Hysteresis width” |
| | | Added the figure for “Stabilization time” |
| 58 | 7. Flash Memory Write/Erase Characteristics | Changed the Value of “Sector erase time” |
| | | Added “Security Sector” to “Sector erase time” |
| | | Changed the Parameter<br>“Half word (16 bit) write time”<br>→<br>“Word (16-bit) write time” |
| | | Changed the Value of “Chip erase time” |
| | | Changed the Remarks of “Sector erase time”<br>Excludes write time prior to internal erase<br>→<br>Includes write time prior to internal erase |
| | | Added the Note and annotation *1 |
| | | Deleted “(targeted value)” from title “ Write/Erase cycles and data hold time” |
| 59 to 61 | ■EXAMPLE CHARACTERISTICS | Added a section |

| Page | Section | Change Results |
|---|---|---|
| 62 | ■ORDERING INFORMATION | Changed part number<br>• MCU with CAN controller<br>MB96F656RAPMC-GSE1* → MB96F656RBPMC-GSE1<br>MB96F656RAPMC-GSE2* → MB96F656RBPMC-GSE2<br>MB96F657RAPMC-GSE1* → MB96F657RBPMC-GSE1<br>MB96F657RAPMC-GSE2* → MB96F657RBPMC-GSE2 |
| | | Added part number<br>• MCU with CAN controller<br>MB96F653RBPMC-GSE1<br>MB96F653RBPMC-GSE2<br>MB96F655RBPMC-GSE1<br>MB96F655RBPMC-GSE2<br>• MCU without CAN controller<br>MB96F653ABPMC-GSE1<br>MB96F653ABPMC-GSE2<br>MB96F655ABPMC-GSE1<br>MB96F655ABPMC-GSE2 |

MEMO

# FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
Tel: +81-45-415-5858
*http://jp.fujitsu.com/fsl/en/*

*For further information please contact:*

**North and South America**
FUJITSU SEMICONDUCTOR AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
*http://us.fujitsu.com/micro/*

**Europe**
FUJITSU SEMICONDUCTOR EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
*http://emea.fujitsu.com/semiconductor/*

**Korea**
FUJITSU SEMICONDUCTOR KOREA LTD.
902 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
*http://kr.fujitsu.com/fsk/*

**Asia Pacific**
FUJITSU SEMICONDUCTOR ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
*http://sg.fujitsu.com/semiconductor/*

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.
30F, Kerry Parkside, 1155 Fang Dian Road,
Pudong District, Shanghai 201204, China
Tel : +86-21-6146-3688 Fax : +86-21-6146-3660
*http://cn.fujitsu.com/fss/*

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.
2/F, Green 18 Building, Hong Kong Science Park,
Shatin, N.T., Hong Kong
Tel : +852-2736-3232 Fax : +852-2314-4207
*http://cn.fujitsu.com/fsp/*



Edited: Sales Promotion Department