

16-bit Proprietary Microcontroller

F²MC-16FX MB96610 Series

**MB96F612R/A, MB96F613R/A,
MB96F615R/A**

■ DESCRIPTION

MB96610 series is based on FUJITSU's advanced F²MC-16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established F²MC-16LX family thus allowing for easy migration of F²MC-16LX Software to the new F²MC-16FX products. F²MC-16FX product improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For high processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 32MHz operation frequency from an external 4MHz resonator. The result is a minimum instruction cycle time of 31.2ns going together with excellent EMI behavior. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows selecting suitable operation frequencies for peripheral resources independent of the CPU speed.

Note: F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

FUJITSU SEMICONDUCTOR provides information facilitating product development via the following website. The website contains information useful for customers.

<http://edevice.fujitsu.com/micom/en-support/>

MB96610 Series

■ FEATURES

- Technology
 - 0.18 μ m CMOS
- CPU
 - F²MC-16FX CPU
 - Optimized instruction set for controller applications (bit, byte, word and long-word data types, 23 different addressing modes, barrel shift, variety of pointers)
 - 8-byte instruction execution queue
 - Signed multiply (16-bit \times 16-bit) and divide (32-bit/16-bit) instructions available
- System clock
 - On-chip PLL clock multiplier ($\times 1$ to $\times 8$, $\times 1$ when PLL stop)
 - 4MHz to 8MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor)
 - Up to 8MHz external clock for devices with fast clock input feature
 - 32.768kHz subsystem quartz clock
 - 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog
 - Clock source selectable from mainclock oscillator, subclock oscillator and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals
 - The subclock oscillator is enabled by the Boot ROM program controlled by a configuration marker after a Power or External reset
 - Low Power Consumption - 13 operating modes (different Run, Sleep, Timer modes, Stop mode)
- On-chip voltage regulator
 - Internal voltage regulator supports a wide MCU supply voltage range (Min=2.7V), offering low power consumption
- Low voltage reset
 - Reset is generated when supply voltage falls below programmable reference voltage
- Code Security
 - Protects Flash Memory content from unintended read-out
- DMA
 - Automatic transfer function independent of CPU, can be assigned freely to resources
- Interrupts
 - Fast Interrupt processing
 - 8 programmable priority levels
 - Non-Maskable Interrupt (NMI)
- CAN
 - Supports CAN protocol version 2.0 part A and B
 - ISO16845 certified
 - Bit rates up to 1Mbps
 - 32 message objects
 - Each message object has its own identifier mask
 - Programmable FIFO mode (concatenation of message objects)
 - Maskable interrupt
 - Disabled Automatic Retransmission mode for Time Triggered CAN applications
 - Programmable loop-back mode for self-test operation

- **USART**
 - Full duplex USARTs (SCI/LIN)
 - Wide range of baud rate settings using a dedicated reload timer
 - Special synchronous options for adapting to different synchronous serial protocols
 - LIN functionality working either as master or slave LIN device
 - Extended support for LIN-Protocol to reduce interrupt load
- **A/D converter**
 - SAR-type
 - 8/10-bit resolution
 - Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
 - Range Comparator Function
- **Source Clock Timers**
 - Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)
- **Hardware Watchdog Timer**
 - Hardware watchdog timer is active after reset
 - Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval
- **Reload Timers**
 - 16-bit wide
 - Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
 - Event count function
- **Free-Running Timers**
 - Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
 - Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency
- **Input Capture Units**
 - 16-bit wide
 - Signals an interrupt upon external event
 - Rising edge, Falling edge or Both (rising & falling) edges sensitive
- **Output Compare Units**
 - 16-bit wide
 - Signals an interrupt when a match with 16-bit I/O Timer occurs
 - A pair of compare registers can be used to generate an output signal
- **Programmable Pulse Generator**
 - 16-bit down counter, cycle and duty setting registers
 - Can be used as 2×8 -bit PPG
 - Interrupt at trigger, counter borrow and/or duty match
 - PWM operation and one-shot operation
 - Internal prescaler allows 1, $1/4$, $1/16$, $1/64$ of peripheral clock as counter clock or of selected Reload timer underflow as clock input
 - Can be triggered by software or reload timer
 - Can trigger ADC conversion
 - Timing point capture
- **Quadrature Position/Revolution Counter (QPRC)**
 - Edge count mode, Phase count mode, Level count mode
 - 16-bit position counter
 - 16-bit revolution counter
 - Two 16-bit compare registers with interrupt
 - Detection edge of the three external event input pins AIN, BIN and ZIN is configurable

- **Real Time Clock**
 - Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
 - Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
 - Read/write accessible second/minute/hour registers
 - Can signal interrupts every half second/second/minute/hour/day
 - Internal clock divider and prescaler provide exact 1s clock
- **External Interrupts**
 - Edge or Level sensitive
 - Interrupt mask and pending bit per channel
 - Each available CAN channel RX has an external interrupt for wake-up
 - Selected USART channels SIN have an external interrupt for wake-up
- **Non Maskable Interrupt**
 - Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
 - Once enabled, can not be disabled other than by reset
 - High or Low level sensitive
 - Pin shared with external interrupt 0
- **I/O Ports**
 - Most of the external pins can be used as general purpose I/O
 - All push-pull outputs
 - Bit-wise programmable as input/output or peripheral signal
 - Bit-wise programmable input enable
 - One input level per GPIO-pin (either Automotive or CMOS hysteresis)
 - Bit-wise programmable pull-up resistor
- **Built-in On Chip Debugger (OCD)**
 - One-wire debug tool interface
 - Break function:
 - Hardware break: 6 points (shared with code event)
 - Software break: 4096 points
 - Event function
 - Code event: 6 points (shared with hardware break)
 - Data event: 6 points
 - Event sequencer: 2 levels + reset
 - Execution time measurement function
 - Trace function: 42 branches
 - Security function
- **Flash Memory**
 - Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
 - Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
 - Supports automatic programming, Embedded Algorithm
 - Write/Erase/Erase-Suspend/Resume commands
 - A flag indicating completion of the automatic algorithm
 - Erase can be performed on each sector individually
 - Sector protection
 - Flash Security feature to protect the content of the Flash
 - Low voltage detection during Flash erase

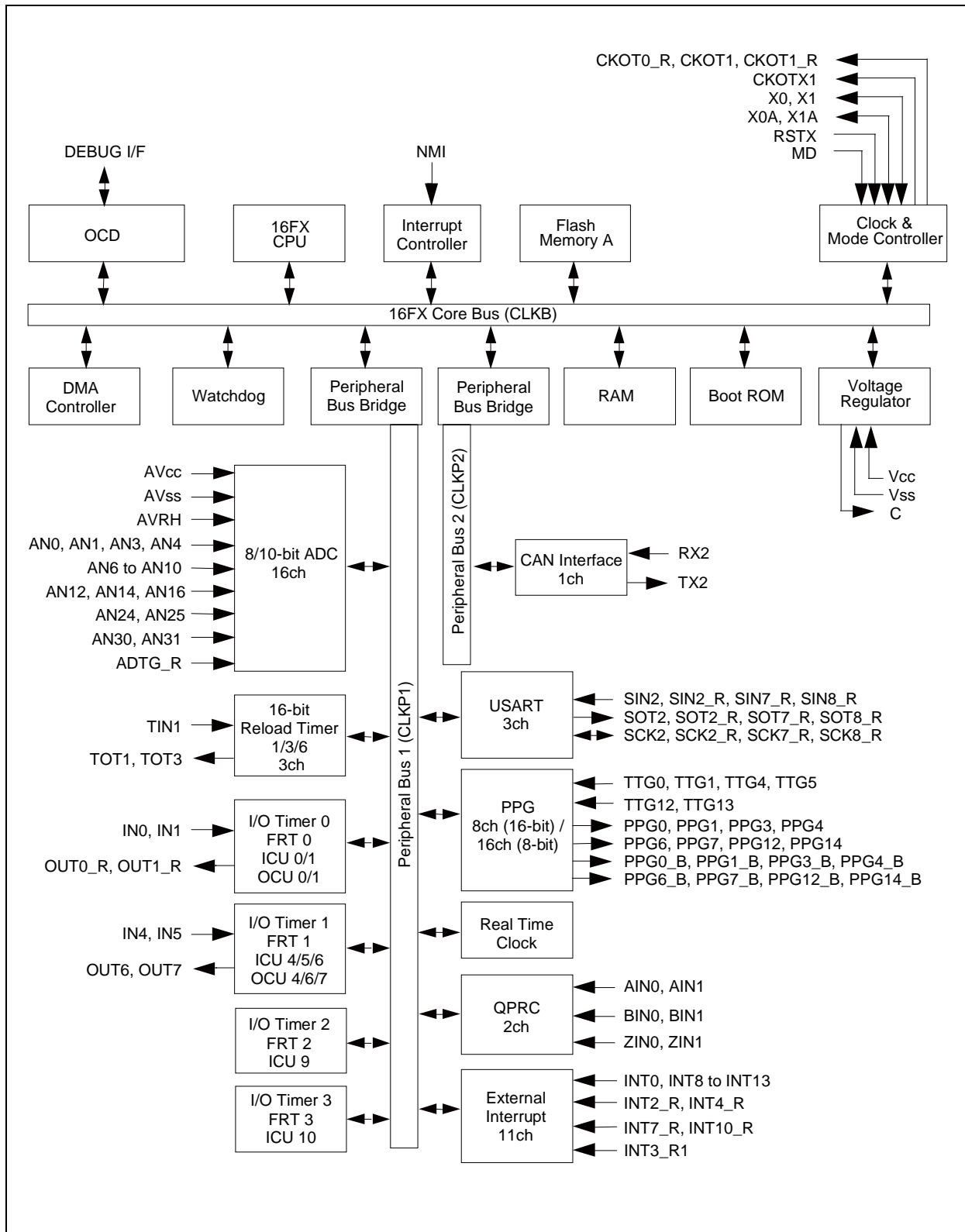
■ PRODUCT LINEUP

Features		MB96610	Remark
Product Type		Flash Memory Product	
Subclock		Subclock can be set by software	
Dual Operation Flash Memory	RAM	-	
32.5KB + 32KB	4KB	MB96F612R, MB96F612A	Product Options R: MCU with CAN A: MCU without CAN
64.5KB + 32KB	10KB	MB96F613R, MB96F613A	
128.5KB + 32KB	10KB	MB96F615R, MB96F615A	
Package		LQFP-48 FPT-48P-M26	
DMA		2ch	
USART		3ch	LIN-USART 2/7/8
with automatic LIN-Header transmission/reception		Yes (only 1ch)	LIN-USART 2
with 16 byte RX- and TX-FIFO		No	
8/10-bit A/D Converter		16ch	AN 0/1/3/4/6 to 10/ 12/14/16/24/25/30/31
with Data Buffer		No	
with Range Comparator		Yes	
with Scan Disable		No	
with ADC Pulse Detection		No	
16-bit Reload Timer (RLT)		3ch	RLT 1/3/6
16-bit Free-Running Timer (FRT)		4ch	FRT 0 to 3 FRT 0 to 3 does not have external clock input pin
16-bit Input Capture Unit (ICU)		7ch (3 channels for LIN-USART)	ICU 0/1/4 to 6/9/10 (ICU 6/9/10 for LIN-USART)
16-bit Output Compare Unit (OCU)		5ch	OCU 0/1/4/6/7 (OCU 4 for FRT clear)
8/16-bit Programmable Pulse Generator (PPG)		8ch (16-bit) / 16ch (8-bit)	PPG 0/1/3/4/6/7/12/14
with Timing point capture		Yes	
with Start delay		No	
with Ramp		No	
Quadrature Position/Revolution Counter (QPRC)		2ch	QPRC 0/1
CAN Interface		1ch	CAN 2 32 Message Buffers
External Interrupts (INT)		11ch	INT 0/2/3/4/7 to 13
Non-Maskable Interrupt (NMI)		1ch	
Real Time Clock (RTC)		1ch	
I/O Ports		35 (Dual clock mode) 37 (Single clock mode)	
Clock Calibration Unit (CAL)		1ch	
Clock Output Function		2ch	
Low Voltage Reset		Yes	Low Voltage Reset can be disabled by software
Hardware Watchdog Timer		Yes	
On-chip RC-oscillator		Yes	
On-chip Debugger		Yes	

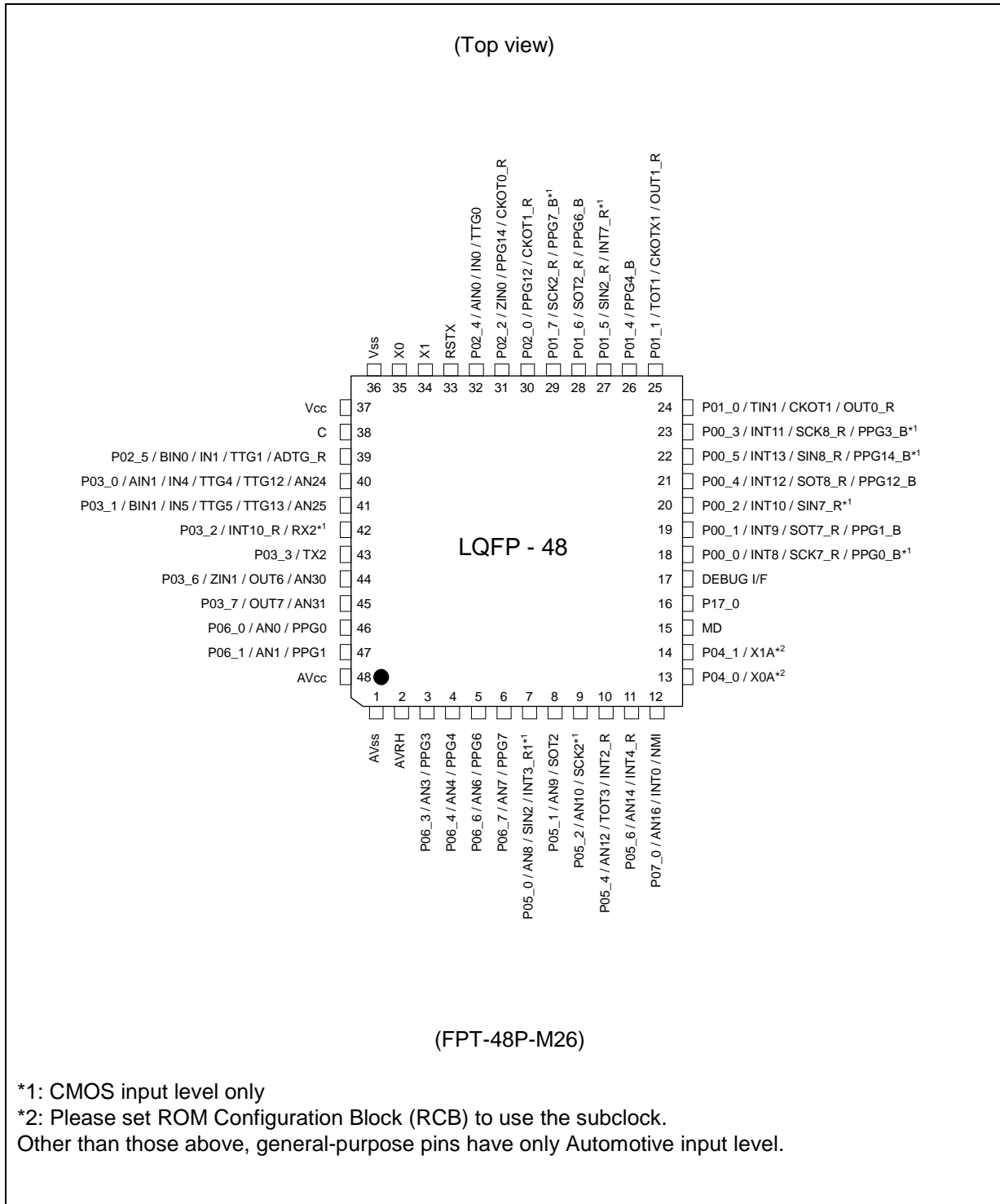
Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the General I/O port according to your function use.

MB96610 Series

■ BLOCK DIAGRAM



■ PIN ASSIGNMENTS



MB96610 Series

■ PIN FUNCTION DESCRIPTION

Pin name	Feature	Description
ADTG_R	ADC	Relocated A/D converter trigger input pin
AINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin
ANn	ADC	A/D converter channel n input pin
AVcc	Supply	Analog circuits power supply pin
AVRH	ADC	A/D converter high reference voltage input pin
AVss	Supply	Analog circuits power supply pin
BINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock Output function	Clock Output function n output pin
CKOTn_R	Clock Output function	Relocated Clock Output function n output pin
CKOTXn	Clock Output function	Clock Output function n inverted output pin
DEBUG I/F	OCD	On Chip Debugger input/output pin
INn	ICU	Input Capture Unit n input pin
INTn	External Interrupt	External Interrupt n input pin
INTn_R	External Interrupt	Relocated External Interrupt n input pin
INTn_R1	External Interrupt	Relocated External Interrupt n input pin
MD	Core	Input pin for specifying the operating mode
NMI	External Interrupt	Non-Maskable Interrupt input pin
OUTn	OCU	Output Compare Unit n waveform output pin
OUTn_R	OCU	Relocated Output Compare Unit n waveform output pin
Pnn_m	GPIO	General purpose I/O pin
PPGn	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_B	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
RSTX	Core	Reset input pin
RXn	CAN	CAN interface n RX input pin
SCKn	USART	USART n serial clock input/output pin
SCKn_R	USART	Relocated USART n serial clock input/output pin
SINn	USART	USART n serial data input pin
SINn_R	USART	Relocated USART n serial data input pin
SOTn	USART	USART n serial data output pin
SOTn_R	USART	Relocated USART n serial data output pin
TINn	Reload Timer	Reload Timer n event input pin
TOTn	Reload Timer	Reload Timer n output pin
TTGn	PPG	Programmable Pulse Generator n trigger input pin
TXn	CAN	CAN interface n TX output pin
Vcc	Supply	Power supply pin
Vss	Supply	Power supply pin
X0	Clock	Oscillator input pin
X0A	Clock	Subclock Oscillator input pin
X1	Clock	Oscillator output pin
X1A	Clock	Subclock Oscillator output pin
ZINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin

■ PIN CIRCUIT TYPE

Pin no.	I/O circuit type*	Pin name
1	Supply	AV _{ss}
2	G	AVRH
3	K	P06_3 / AN3 / PPG3
4	K	P06_4 / AN4 / PPG4
5	K	P06_6 / AN6 / PPG6
6	K	P06_7 / AN7 / PPG7
7	I	P05_0 / AN8 / SIN2 / INT3_R1
8	K	P05_1 / AN9 / SOT2
9	I	P05_2 / AN10 / SCK2
10	K	P05_4 / AN12 / TOT3 / INT2_R
11	K	P05_6 / AN14 / INT4_R
12	K	P07_0 / AN16 / INT0 / NMI
13	B	P04_0 / X0A
14	B	P04_1 / X1A
15	C	MD
16	H	P17_0
17	O	DEBUG I/F
18	M	P00_0 / INT8 / SCK7_R / PPG0_B
19	H	P00_1 / INT9 / SOT7_R / PPG1_B
20	M	P00_2 / INT10 / SIN7_R
21	H	P00_4 / INT12 / SOT8_R / PPG12_B
22	M	P00_5 / INT13 / SIN8_R / PPG14_B
23	M	P00_3 / INT11 / SCK8_R / PPG3_B
24	H	P01_0 / TIN1 / CKOT1 / OUT0_R
25	H	P01_1 / TOT1 / CKOTX1 / OUT1_R
26	H	P01_4 / PPG4_B
27	M	P01_5 / SIN2_R / INT7_R
28	H	P01_6 / SOT2_R / PPG6_B
29	M	P01_7 / SCK2_R / PPG7_B
30	H	P02_0 / PPG12 / CKOT1_R
31	H	P02_2 / ZIN0 / PPG14 / CKOT0_R
32	H	P02_4 / AIN0 / IN0 / TTG0

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Pin no.	I/O circuit type*	Pin name
33	C	RSTX
34	A	X1
35	A	X0
36	Supply	Vss
37	Supply	Vcc
38	F	C
39	H	P02_5 / BIN0 / IN1 / TTG1 / ADTG_R
40	K	P03_0 / AIN1 / IN4 / TTG4 / TTG12 / AN24
41	K	P03_1 / BIN1 / IN5 / TTG5 / TTG13 / AN25
42	M	P03_2 / INT10_R / RX2
43	H	P03_3 / TX2
44	K	P03_6 / ZIN1 / OUT6 / AN30
45	K	P03_7 / OUT7 / AN31
46	K	P06_0 / AN0 / PPG0
47	K	P06_1 / AN1 / PPG1
48	Supply	AVcc

*: See “■ I/O CIRCUIT TYPE” for details on the I/O circuit types.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		<p>High-speed oscillation circuit:</p> <ul style="list-style-type: none"> • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Feedback resistor = approx. 1.0MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode • The amplitude: 1.8V±0.15V to operate by the internal supply voltage

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Type	Circuit	Remarks
B	<p>The diagram for Type B shows a complex circuit. At the top, there is a pull-up resistor connected to a 'Pull-up control' line. Below this, a P-channel MOSFET (P-ch) is connected to a 'Pout' output. Another P-channel MOSFET (P-ch) is connected to a common node. An N-channel MOSFET (N-ch) is connected to a 'Nout' output. A 'Standby control for input shutdown' line is connected to a resistor 'R' and an AND gate. The AND gate's other input is connected to the common node between the two P-ch MOSFETs. The output of the AND gate is connected to an 'Automotive input' through an inverter. Below this, there is an oscillator circuit. It consists of two crystals, X1A and X0A, connected to a common node. A resistor 'R' is connected between this common node and the 'Automotive input' line. The oscillator circuit also includes two inverters and a multiplexer 'X out' with inputs 0 and 1, controlled by 'FCI'. A control line 'FCI or Osc disable' is connected to the oscillator circuit. At the bottom, there is another pull-up resistor and P-ch MOSFET connected to 'Pout', and an N-ch MOSFET connected to 'Nout'. A second 'Standby control for input shutdown' line is connected to a resistor 'R' and an AND gate, which is connected to the 'Automotive input' through an inverter.</p>	<p>Low-speed oscillation circuit shared with GPIO functionality:</p> <ul style="list-style-type: none"> • Feedback resistor = approx. 5.0MΩ. Feedback resistor is grounded in the center when the oscillator is disabled • GPIO functionality selectable (CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$), Automotive input with input shutdown function and programmable pull-up resistor)
C	<p>The diagram for Type C shows a simple circuit. An input pin is connected to a resistor 'R'. The other end of the resistor is connected to a CMOS hysteresis circuit, which consists of two inverters connected in a feedback loop. The output of this circuit is labeled 'Hysteresis inputs'.</p>	<p>CMOS hysteresis input pin</p>

Type	Circuit	Remarks
F		<p>Power supply input protection circuit</p>
G		<ul style="list-style-type: none"> • A/D converter ref+ (AVRH) power supply input pin with protection circuit • Without protection circuit against V_{CC} for pins AVRH
H		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) • Automotive input with input shutdown function • Programmable pull-up resistor
I		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor • Analog input

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Type	Circuit	Remarks
K		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) • Automotive input with input shutdown function • Programmable pull-up resistor • Analog input
M		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor
O		<ul style="list-style-type: none"> • I_{OL}: 25mA @ 2.7V • TTL input

■ MEMORY MAP

FF:FFF _H	USER ROM* ¹
DE:0000 _H DD:FFF _H	Reserved
10:0000 _H 0F:C000 _H	Boot-ROM
0E:9000 _H	Peripheral
	Reserved
01:0000 _H 00:8000 _H	ROM/RAM MIRROR
RAMSTART0* ²	Internal RAM bank0
	Reserved
00:0C00 _H	Peripheral
00:0380 _H	Peripheral
00:0180 _H	GPR* ³
00:0100 _H	DMA
00:00F0 _H	Reserved
00:0000 _H	Peripheral

*1: For details about USER ROM area, see “■USER ROM MEMORY MAP FOR FLASH DEVICES” on the following pages.
 *2: For RAMSTART addresses, see the table on the next page.
 *3: Unused GPR banks can be used as RAM area.
 GPR: General-Purpose Register
 The DMA area is only available if the device contains the corresponding resource.
 The available RAM and ROM area depends on the device.

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■ RAMSTART ADDRESSES

Devices	Bank 0 RAM size	RAMSTART0
MB96F612	4KB	00:7200 _H
MB96F613 MB96F615	10KB	00:5A00 _H

■ USER ROM MEMORY MAP FOR FLASH DEVICES

		MB96F612	MB96F613	MB96F615		
Alternative mode CPU address	Flash memory mode address	Flash size 32.5KB + 32KB	Flash size 64.5KB + 32KB	Flash size 128.5KB + 32KB		
FF:FFFF _H FF:8000 _H	3F:FFFF _H 3F:8000 _H	SA39 - 32KB	SA39 - 64KB	SA39 - 64KB	Bank A of Flash A	
FF:7FFF _H FF:0000 _H FE:FFFF _H	3F:7FFF _H 3F:0000 _H 3E:FFFF _H	Reserved				Reserved
FE:0000 _H FD:FFFF _H	3E:0000 _H		Reserved	Reserved		
DF:A000 _H DF:9FFF _H DF:8000 _H	1F:9FFF _H 1F:8000 _H	SA4 - 8KB	SA4 - 8KB	SA4 - 8KB	Bank B of Flash A	
DF:7FFF _H DF:6000 _H	1F:7FFF _H 1F:6000 _H	SA3 - 8KB	SA3 - 8KB	SA3 - 8KB		
DF:5FFF _H DF:4000 _H	1F:5FFF _H 1F:4000 _H	SA2 - 8KB	SA2 - 8KB	SA2 - 8KB		
DF:3FFF _H DF:2000 _H	1F:3FFF _H 1F:2000 _H	SA1 - 8KB	SA1 - 8KB	SA1 - 8KB		
DF:1FFF _H DF:0000 _H	1F:1FFF _H 1F:0000 _H	SAS - 512B*	SAS - 512B*	SAS - 512B*	Bank A of Flash A	
DE:FFFF _H DE:0000 _H		Reserved	Reserved	Reserved		

*: Physical address area of SAS-512B is from DF:0000_H to DF:01FF_H.
Others (from DF:0200_H to DF:1FFF_H) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000_H -DF:01FF_H.
SAS can not be used for E²PROM emulation.

MB96610 Series

■ SERIAL PROGRAMMING COMMUNICATION INTERFACE

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

MB96610		
Pin Number	USART Number	Normal Function
7	USART2	SIN2
8		SOT2
9		SCK2
20	USART7	SIN7_R
19		SOT7_R
18		SCK7_R
22	USART8	SIN8_R
21		SOT8_R
23		SCK8_R

■ INTERRUPT VECTOR TABLE

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	3FC _H	CALLV0	No	-	CALLV instruction
1	3F8 _H	CALLV1	No	-	CALLV instruction
2	3F4 _H	CALLV2	No	-	CALLV instruction
3	3F0 _H	CALLV3	No	-	CALLV instruction
4	3EC _H	CALLV4	No	-	CALLV instruction
5	3E8 _H	CALLV5	No	-	CALLV instruction
6	3E4 _H	CALLV6	No	-	CALLV instruction
7	3E0 _H	CALLV7	No	-	CALLV instruction
8	3DC _H	RESET	No	-	Reset vector
9	3D8 _H	INT9	No	-	INT9 instruction
10	3D4 _H	EXCEPTION	No	-	Undefined instruction execution
11	3D0 _H	NMI	No	-	Non-Maskable Interrupt
12	3CC _H	DLY	No	12	Delayed Interrupt
13	3C8 _H	RC_TIMER	No	13	RC Clock Timer
14	3C4 _H	MC_TIMER	No	14	Main Clock Timer
15	3C0 _H	SC_TIMER	No	15	Sub Clock Timer
16	3BC _H	LVDI	No	16	Low Voltage Detector
17	3B8 _H	EXTINT0	Yes	17	External Interrupt 0
18	3B4 _H	-	-	18	Reserved
19	3B0 _H	EXTINT2	Yes	19	External Interrupt 2
20	3AC _H	EXTINT3	Yes	20	External Interrupt 3
21	3A8 _H	EXTINT4	Yes	21	External Interrupt 4
22	3A4 _H	-	-	22	Reserved
23	3A0 _H	-	-	23	Reserved
24	39C _H	EXTINT7	Yes	24	External Interrupt 7
25	398 _H	EXTINT8	Yes	25	External Interrupt 8
26	394 _H	EXTINT9	Yes	26	External Interrupt 9
27	390 _H	EXTINT10	Yes	27	External Interrupt 10
28	38C _H	EXTINT11	Yes	28	External Interrupt 11
29	388 _H	EXTINT12	Yes	29	External Interrupt 12
30	384 _H	EXTINT13	Yes	30	External Interrupt 13
31	380 _H	-	-	31	Reserved
32	37C _H	-	-	32	Reserved
33	378 _H	-	-	33	Reserved
34	374 _H	-	-	34	Reserved
35	370 _H	CAN2	No	35	CAN Controller 2
36	36C _H	-	-	36	Reserved
37	368 _H	-	-	37	Reserved
38	364 _H	PPG0	Yes	38	Programmable Pulse Generator 0
39	360 _H	PPG1	Yes	39	Programmable Pulse Generator 1
40	35C _H	-	-	40	Reserved

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Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
41	358 _H	PPG3	Yes	41	Programmable Pulse Generator 3
42	354 _H	PPG4	Yes	42	Programmable Pulse Generator 4
43	350 _H	-	-	43	Reserved
44	34C _H	PPG6	Yes	44	Programmable Pulse Generator 6
45	348 _H	PPG7	Yes	45	Programmable Pulse Generator 7
46	344 _H	-	-	46	Reserved
47	340 _H	-	-	47	Reserved
48	33C _H	-	-	48	Reserved
49	338 _H	-	-	49	Reserved
50	334 _H	PPG12	Yes	50	Programmable Pulse Generator 12
51	330 _H	-	-	51	Reserved
52	32C _H	PPG14	Yes	52	Programmable Pulse Generator 14
53	328 _H	-	-	53	Reserved
54	324 _H	-	-	54	Reserved
55	320 _H	-	-	55	Reserved
56	31C _H	-	-	56	Reserved
57	318 _H	-	-	57	Reserved
58	314 _H	-	-	58	Reserved
59	310 _H	RLT1	Yes	59	Reload Timer 1
60	30C _H	-	-	60	Reserved
61	308 _H	RLT3	Yes	61	Reload Timer 3
62	304 _H	-	-	62	Reserved
63	300 _H	-	-	63	Reserved
64	2FC _H	RLT6	Yes	64	Reload Timer 6
65	2F8 _H	ICU0	Yes	65	Input Capture Unit 0
66	2F4 _H	ICU1	Yes	66	Input Capture Unit 1
67	2F0 _H	-	-	67	Reserved
68	2EC _H	-	-	68	Reserved
69	2E8 _H	ICU4	Yes	69	Input Capture Unit 4
70	2E4 _H	ICU5	Yes	70	Input Capture Unit 5
71	2E0 _H	ICU6	Yes	71	Input Capture Unit 6
72	2DC _H	-	-	72	Reserved
73	2D8 _H	-	-	73	Reserved
74	2D4 _H	ICU9	Yes	74	Input Capture Unit 9
75	2D0 _H	ICU10	Yes	75	Input Capture Unit 10
76	2CC _H	-	-	76	Reserved
77	2C8 _H	OCU0	Yes	77	Output Compare Unit 0
78	2C4 _H	OCU1	Yes	78	Output Compare Unit 1
79	2C0 _H	-	-	79	Reserved
80	2BC _H	-	-	80	Reserved

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Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
81	2B8 _H	OCU4	Yes	81	Output Compare Unit 4
82	2B4 _H	-	-	82	Reserved
83	2B0 _H	OCU6	Yes	83	Output Compare Unit 6
84	2AC _H	OCU7	Yes	84	Output Compare Unit 7
85	2A8 _H	-	-	85	Reserved
86	2A4 _H	-	-	86	Reserved
87	2A0 _H	-	-	87	Reserved
88	29C _H	-	-	88	Reserved
89	298 _H	FRT0	Yes	89	Free-Running Timer 0
90	294 _H	FRT1	Yes	90	Free-Running Timer 1
91	290 _H	FRT2	Yes	91	Free-Running Timer 2
92	28C _H	FRT3	Yes	92	Free-Running Timer 3
93	288 _H	RTC0	No	93	Real Time Clock
94	284 _H	CAL0	No	94	Clock Calibration Unit
95	280 _H	-	-	95	Reserved
96	27C _H	-	-	96	Reserved
97	278 _H	-	-	97	Reserved
98	274 _H	ADC0	Yes	98	A/D Converter 0
99	270 _H	-	-	99	Reserved
100	26C _H	-	-	100	Reserved
101	268 _H	-	-	101	Reserved
102	264 _H	-	-	102	Reserved
103	260 _H	-	-	103	Reserved
104	25C _H	-	-	104	Reserved
105	258 _H	LINR2	Yes	105	LIN USART 2 RX
106	254 _H	LINT2	Yes	106	LIN USART 2 TX
107	250 _H	-	-	107	Reserved
108	24C _H	-	-	108	Reserved
109	248 _H	-	-	109	Reserved
110	244 _H	-	-	110	Reserved
111	240 _H	-	-	111	Reserved
112	23C _H	-	-	112	Reserved
113	238 _H	-	-	113	Reserved
114	234 _H	-	-	114	Reserved
115	230 _H	LINR7	Yes	115	LIN USART 7 RX
116	22C _H	LINT7	Yes	116	LIN USART 7 TX
117	228 _H	LINR8	Yes	117	LIN USART 8 RX
118	224 _H	LINT8	Yes	118	LIN USART 8 TX
119	220 _H	-	-	119	Reserved
120	21C _H	-	-	120	Reserved

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Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
121	218 _H	-	-	121	Reserved
122	214 _H	-	-	122	Reserved
123	210 _H	-	-	123	Reserved
124	20C _H	-	-	124	Reserved
125	208 _H	-	-	125	Reserved
126	204 _H	-	-	126	Reserved
127	200 _H	-	-	127	Reserved
128	1FC _H	-	-	128	Reserved
129	1F8 _H	-	-	129	Reserved
130	1F4 _H	-	-	130	Reserved
131	1F0 _H	-	-	131	Reserved
132	1EC _H	-	-	132	Reserved
133	1E8 _H	FLASHA	Yes	133	Flash memory A interrupt
134	1E4 _H	-	-	134	Reserved
135	1E0 _H	-	-	135	Reserved
136	1DC _H	-	-	136	Reserved
137	1D8 _H	QPRC0	Yes	137	Quadrature Position/Revolution counter 0
138	1D4 _H	QPRC1	Yes	138	Quadrature Position/Revolution counter 1
139	1D0 _H	ADCRC0	No	139	A/D Converter 0 - Range Comparator
140	1CC _H	-	-	140	Reserved
141	1C8 _H	-	-	141	Reserved
142	1C4 _H	-	-	142	Reserved
143	1C0 _H	-	-	143	Reserved

■ HANDLING DEVICES

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator and ceramic resonator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on Power-on
- Stabilization of power supply voltage
- Serial communication
- Mode Pin (MD)

1. Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC} , $AVRH$) exceed the digital power-supply voltage.

2. Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register $PIER = 0$).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than $2k\Omega$.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

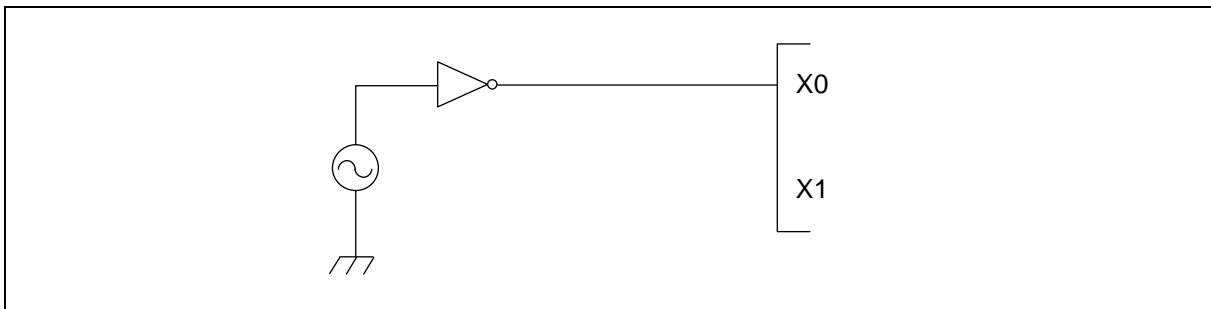
3. External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration.

See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

(1) Single phase external clock for Main oscillator

When using a single phase external clock for the Main oscillator, X0 pin must be driven and X1 pin left open. And supply 1.8V power to the external clock.



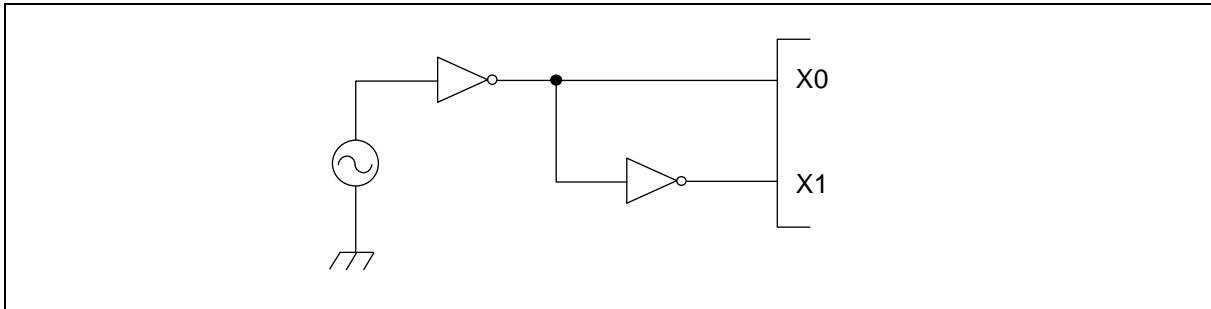
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(2) Single phase external clock for Sub oscillator

When using a single phase external clock for the Sub oscillator, “External clock mode” must be selected and X0A/P04_0 pin must be driven. X1A/P04_1 pin must be configured as GPIO.

(3) Opposite phase external clock

When using an opposite phase external clock, X1 (X1A) pins must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. Supply level on X0 and X1 pins must be 1.8V.



4. Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

5. Power supply pins (Vcc/Vss)

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} pins must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1μF between V_{CC} and V_{SS} pins as close as possible to V_{CC} and V_{SS} pins.

6. Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

7. Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, AVRH must not exceed AV_{CC}. Input voltage for ports shared with analog input ports also must not exceed AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

8. Pin handling when not using the A/D converter

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as AV_{CC} = V_{CC}, AV_{SS} = AVRH = V_{SS}.

9. Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50 μ s from 0.2V to 2.7V.

10. Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/ μ s or less in instantaneous fluctuation for power supply switching.

11. Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise. Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

12. Mode Pin (MD)

Connect the mode pin directly to Vcc or Vss pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to Vcc or Vss pin and provide a low-impedance connection.

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■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage* ¹	V _{CC}	-	V _{SS} - 0.3	V _{SS} + 6.0	V	
Analog power supply voltage* ¹	AV _{CC}	-	V _{SS} - 0.3	V _{SS} + 6.0	V	V _{CC} = AV _{CC} * ²
Analog reference voltage* ¹	AVRH	-	V _{SS} - 0.3	V _{SS} + 6.0	V	AV _{CC} ≥ AVRH, AVRH ≥ AV _{SS}
Input voltage* ¹	V _I	-	V _{SS} - 0.3	V _{SS} + 6.0	V	V _I ≤ V _{CC} + 0.3V* ³
Output voltage* ¹	V _O	-	V _{SS} - 0.3	V _{SS} + 6.0	V	V _O ≤ V _{CC} + 0.3V* ³
Maximum Clamp Current	I _{CLAMP}	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins * ⁴
Total Maximum Clamp Current	Σ I _{CLAMP}	-	-	13	mA	Applicable to general purpose I/O pins * ⁴
"L" level maximum output current	I _{OL}	-	-	15	mA	
"L" level average output current	I _{OLAV}	-	-	4	mA	
"L" level maximum overall output current	ΣI _{OL}	-	-	32	mA	
"L" level average overall output current	ΣI _{OLAV}	-	-	16	mA	
"H" level maximum output current	I _{OH}	-	-	-15	mA	
"H" level average output current	I _{OHAV}	-	-	-4	mA	
"H" level maximum overall output current	ΣI _{OH}	-	-	-32	mA	
"H" level average overall output current	ΣI _{OHAV}	-	-	-16	mA	
Power consumption* ⁵	P _D	T _A = +125°C	-	284* ⁶	mW	
Operating ambient temperature	T _A	-	-40	+125* ⁷	°C	
Storage temperature	T _{STG}	-	-55	+150	°C	

*1: This parameter is based on V_{SS} = AV_{SS} = 0V.

*2: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

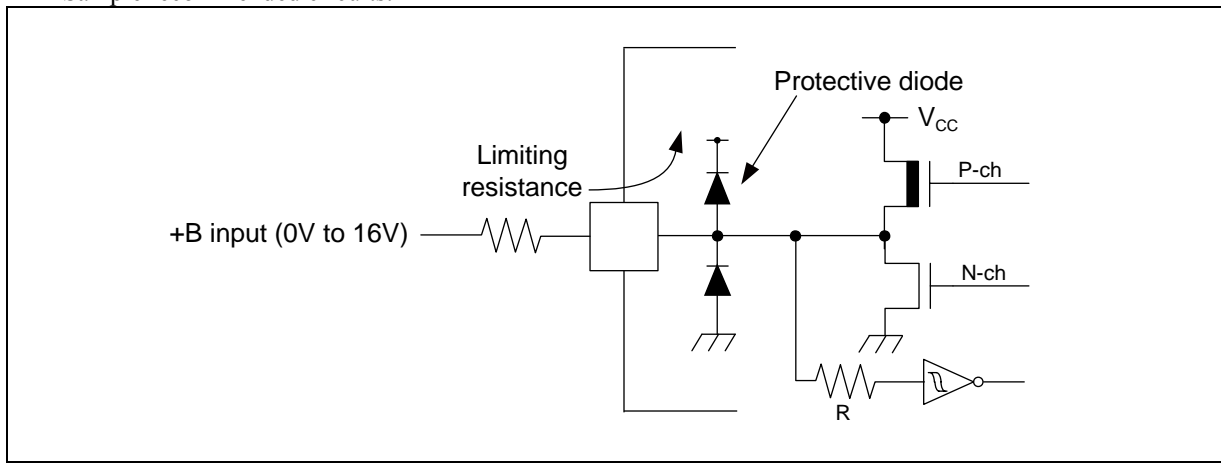
*3: V_I and V_O should not exceed V_{CC} + 0.3V. V_I should also not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/Output voltages of standard ports depend on V_{CC}.

*4: • Applicable to all general purpose I/O pins (Pnn_m).

- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.

- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset.
- The DEBUG I/F pin has only a protective diode against V_{SS} . Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.

- Sample recommended circuits:



*5: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.

The actual power dissipation depends on the customer application and can be calculated as follows:

$$P_D = P_{IO} + P_{INT}$$

$$P_{IO} = \sum (V_{OL} \times I_{OL} + V_{OH} \times I_{OH}) \text{ (I/O load power dissipation, sum is performed on all I/O ports)}$$

$$P_{INT} = V_{CC} \times (I_{CC} + I_A) \text{ (internal power dissipation)}$$

I_{CC} is the total core current consumption into V_{CC} as described in the "DC characteristics" and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.

I_A is the analog current consumption into AV_{CC} .

*6: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

*7: Write/erase to a large sector in flash memory is warranted with $T_A \leq +105^\circ\text{C}$.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

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2. Recommended Operating Conditions

($V_{SS} = AV_{SS} = 0V$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	2.7	-	5.5	V	
		2.0	-	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor at C pin	C_S	0.5	1.0 to 3.9	4.7	μF	1.0 μF (Allowance within $\pm 50\%$) 3.9 μF (Allowance within $\pm 20\%$) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at V_{CC} must use the one of a capacity value that is larger than C_S .

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.

Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(1) Current Rating

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes*1	I _{CCPLL}	V _{CC}	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz	-	25	-	mA	T _A = +25°C
			Flash 0 wait	-	-	34	mA	T _A = +105°C
			(CLKRC and CLKSC stopped)	-	-	35	mA	T _A = +125°C
	I _{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz	-	3.5	-	mA	T _A = +25°C
			Flash 0 wait	-	-	7.5	mA	T _A = +105°C
			(CLKPLL, CLKSC and CLKRC stopped)	-	-	8.5	mA	T _A = +125°C
	I _{CCRCH}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz	-	1.7	-	mA	T _A = +25°C
			Flash 0 wait	-	-	5.5	mA	T _A = +105°C
			(CLKMC, CLKPLL and CLKSC stopped)	-	-	6.5	mA	T _A = +125°C
	I _{CCRCL}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz	-	0.15	-	mA	T _A = +25°C
			Flash 0 wait	-	-	3.2	mA	T _A = +105°C
			(CLKMC, CLKPLL and CLKSC stopped)	-	-	4.2	mA	T _A = +125°C
	I _{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz	-	0.1	-	mA	T _A = +25°C
			Flash 0 wait	-	-	3	mA	T _A = +105°C
			(CLKMC, CLKPLL and CLKRC stopped)	-	-	4	mA	T _A = +125°C

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Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Sleep modes *1	I _{CCSPLL}	V _{CC}	PLL Sleep mode with CLKS1/2 = CLKP1/2 = 32MHz (CLKRC and CLKSC stopped)	-	6.5	-	mA	T _A = +25°C
				-	-	13	mA	T _A = +105°C
				-	-	14	mA	T _A = +125°C
	I _{CCSMAN}		Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	0.9	-	mA	T _A = +25°C
				-	-	4	mA	T _A = +105°C
				-	-	5	mA	T _A = +125°C
	I _{CCSRCH}		RC Sleep mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped)	-	0.5	-	mA	T _A = +25°C
				-	-	3.5	mA	T _A = +105°C
				-	-	4.5	mA	T _A = +125°C
	I _{CCSRCL}		RC Sleep mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz (CLKMC, CLKPLL and CLKSC stopped)	-	0.06	-	mA	T _A = +25°C
				-	-	2.7	mA	T _A = +105°C
				-	-	3.7	mA	T _A = +125°C
	I _{CCSSUB}		Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz, (CLKMC, CLKPLL and CLKRC stopped)	-	0.04	-	mA	T _A = +25°C
				-	-	2.5	mA	T _A = +105°C
				-	-	3.5	mA	T _A = +125°C

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Timer modes ^{*2}	I _{CCTPLL}	V _{CC}	PLL Timer mode with CLKP1 = 32MHz (CLKRC and CLKSC stopped)	-	2480	2710	μA	T _A = +25°C
				-	-	3985	μA	T _A = +105°C
				-	-	4830	μA	T _A = +125°C
	I _{CCTMAIN}		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	285	325	μA	T _A = +25°C
				-	-	1085	μA	T _A = +105°C
				-	-	1930	μA	T _A = +125°C
	I _{CCTRCH}		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped)	-	160	210	μA	T _A = +25°C
				-	-	1025	μA	T _A = +105°C
				-	-	1840	μA	T _A = +125°C
	I _{CCTRCL}		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped)	-	35	75	μA	T _A = +25°C
				-	-	855	μA	T _A = +105°C
				-	-	1640	μA	T _A = +125°C
	I _{CCTSUB}		Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	-	25	65	μA	T _A = +25°C
				-	-	830	μA	T _A = +105°C
				-	-	1620	μA	T _A = +125°C

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Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Stop mode*3	I _{CCH}	V _{CC}	-	-	20	55	μA	T _A = +25°C
				-	-	825	μA	T _A = +105°C
				-	-	1615	μA	T _A = +125°C
Flash Power Down current	I _{CCFLASHPD}		-	-	36	70	μA	
Power supply current for active Low Voltage detector*4	I _{CCLVD}		Low voltage detector enabled	-	5	-	μA	T _A = +25°C
				-	-	12.5	μA	T _A = +125°C
Flash Write/ Erase current*5	I _{CCFLASH}	-	-	12.5	-	mA	T _A = +25°C	
			-	-	20	mA	T _A = +125°C	

*1: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter "Standby mode and voltage regulator control circuit" of the Hardware Manual for further details about voltage regulator control. Current for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current.

*2: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode. When Flash is not in Power-down / reset mode, I_{CCFLASHPD} must be added to the Power supply current. The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. Power supply for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current.

*3: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode. When Flash is not in Power-down / reset mode, I_{CCFLASHPD} must be added to the Power supply current.

*4: When low voltage detector is enabled, I_{CCLVD} must be added to Power supply current.

*5: When Flash Write / Erase program is executed, I_{CCFLASH} must be added to Power supply current.

(2) Pin Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Port inputs Pnn_m	-	$V_{CC} \times 0.7$	-	$V_{CC} + 0.3$	V	CMOS Hysteresis input
			-	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	AUTOMOTIVE Hysteresis input
	V_{IHx0S}	X0	External clock in "Fast Clock Input mode"	$VD \times 0.8$	-	VD	V	$VD=1.8V \pm 0.15V$
	V_{IHx0AS}	X0A	External clock in "Oscillation mode"	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	
	V_{IHR}	RSTX	-	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	CMOS Hysteresis input
	V_{IHM}	MD	-	$V_{CC} - 0.3$	-	$V_{CC} + 0.3$	V	CMOS Hysteresis input
	V_{IHD}	DEBUG I/F	-	2.0	-	$V_{CC} + 0.3$	V	TTL Input
"L" level input voltage	V_{IL}	Port inputs Pnn_m	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.3$	V	CMOS Hysteresis input
			-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.5$	V	AUTOMOTIVE Hysteresis input
	V_{ILx0S}	X0	External clock in "Fast Clock Input mode"	V_{SS}	-	$VD \times 0.2$	V	$VD=1.8V \pm 0.15V$
	V_{ILx0AS}	X0A	External clock in "Oscillation mode"	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
	V_{ILR}	RSTX	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	CMOS Hysteresis input
	V_{ILM}	MD	-	$V_{SS} - 0.3$	-	$V_{SS} + 0.3$	V	CMOS Hysteresis input
	V_{ILD}	DEBUG I/F	-	$V_{SS} - 0.3$	-	0.8	V	TTL Input

MB96610 Series

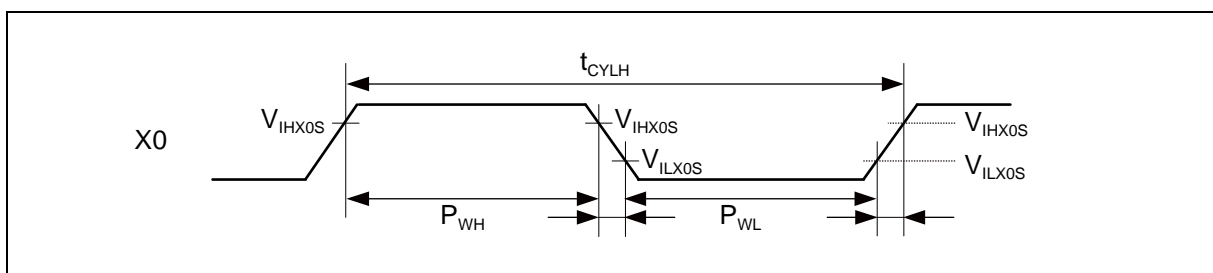
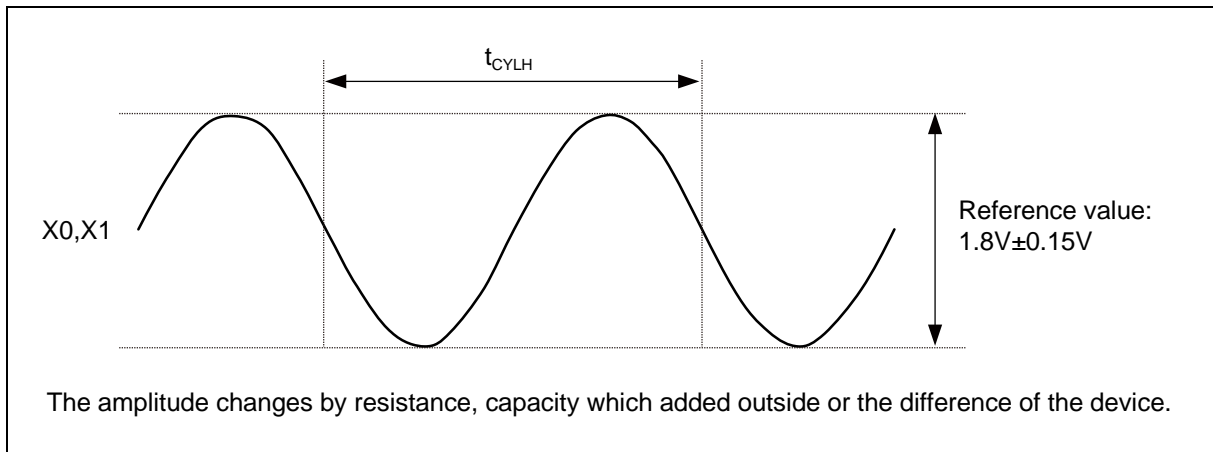
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V _{OH4}	4mA type	4.5V ≤ V _{CC} ≤ 5.5V I _{OH} = -4mA	V _{CC} - 0.5	-	V _{CC}	V	
			2.7V ≤ V _{CC} < 4.5V I _{OH} = -1.5mA					
"L" level output voltage	V _{OL4}	4mA type	4.5V ≤ V _{CC} ≤ 5.5V I _{OL} = +4mA	-	-	0.4	V	
			2.7V ≤ V _{CC} < 4.5V I _{OL} = +1.7mA					
	V _{OLD}	DEBUG I/F	V _{CC} = 2.7V I _{OL} = +25mA	0	-	0.25	V	
Input leak current	I _{IL}	Pnn_m	V _{SS} < V _I < V _{CC} AV _{SS} < V _I < AV _{CC} , AVRH	- 1	-	+ 1	μA	
Pull-up resistance value	R _{PU}	Pnn_m	V _{CC} = 5.0V ±10%	25	50	100	kΩ	
Input capacitance	C _{IN}	Other than C, V _{CC} , V _{SS} , AV _{CC} , AV _{SS} , AVRH	-	-	5	15	pF	

4. AC Characteristics

(1) Main Clock Input Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_D = 1.8V \pm 0.15V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Input frequency	f_C	X0, X1	4	-	8	MHz	When using a crystal oscillator, PLL off
			-	-	8	MHz	When using an opposite phase external clock, PLL off
			4	-	8	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Input frequency	f_{FCI}	X0	-	-	8	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL off
			4	-	8	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL on
Input clock cycle	t_{CYLH}	-	125	-	-	ns	
Input clock pulse width	P_{WH} , P_{WL}	-	55	-	-	ns	

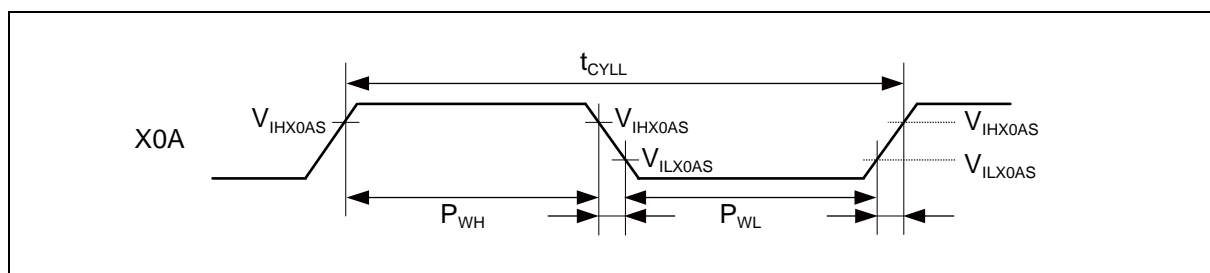
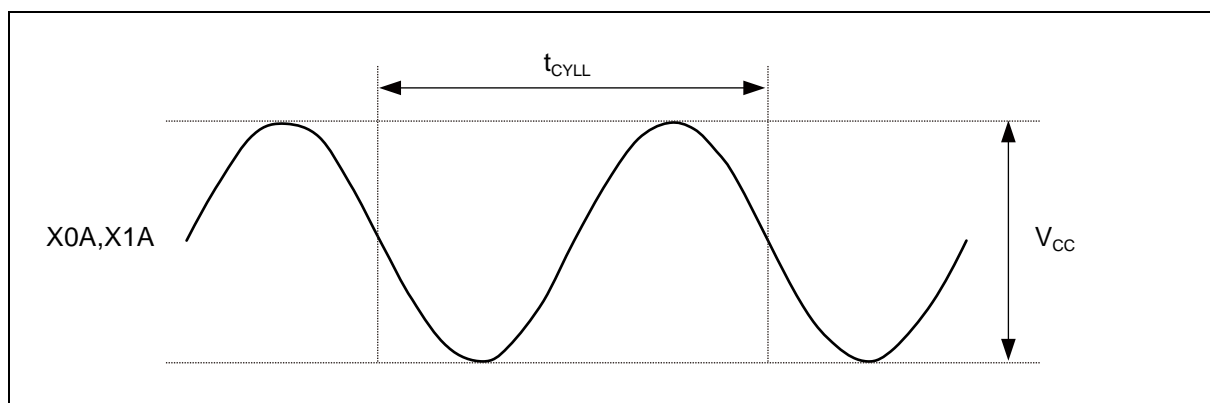


MB96610 Series

(2) Sub Clock Input Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100		kHz
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	μs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL} , P_{WL}/t_{CYLL}	30	-	70	%	



(3) Built-in RC Oscillation Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock frequency	f_{RC}	50	100	200	kHz	When using slow frequency of RC oscillator
		1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	80	160	320	μs	When using slow frequency of RC oscillator (16 RC clock cycles)
		64	128	256	μs	When using fast frequency of RC oscillator (256 RC clock cycles)

(4) Internal Clock Timing

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

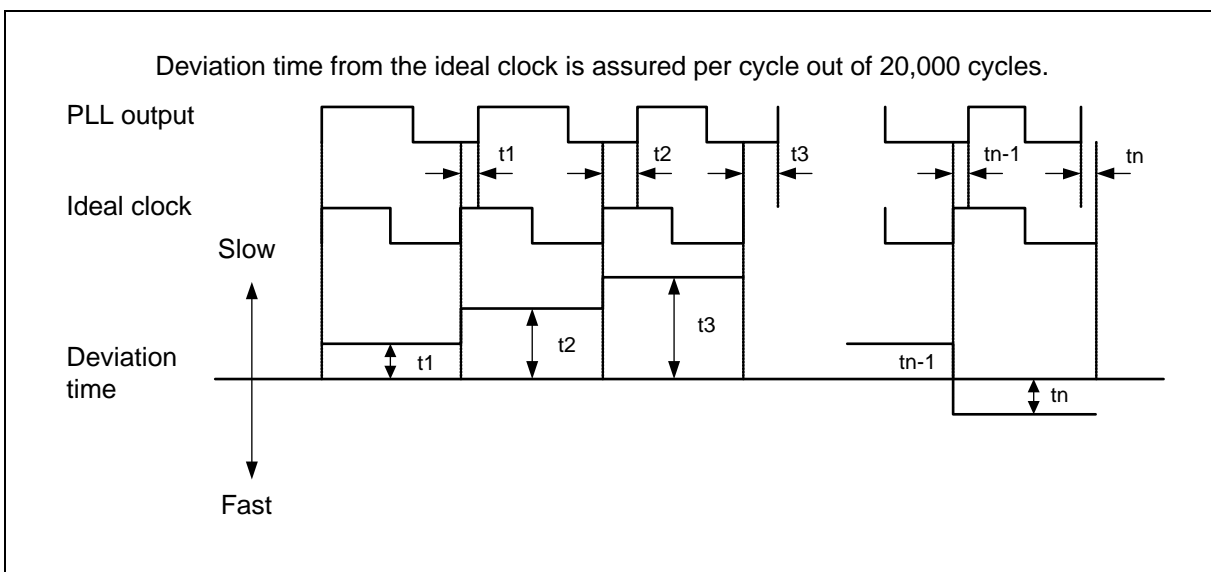
Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	-	54	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	-	32	MHz
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	-	32	MHz

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(5) Operating Conditions of PLL

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

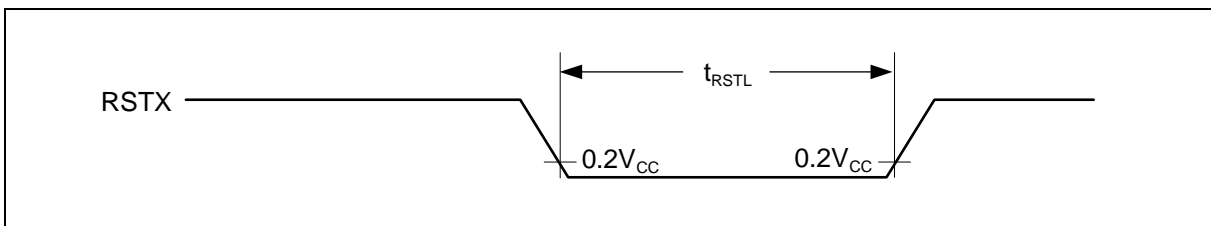
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) $\geq 4MHz$



(6) Reset Input

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

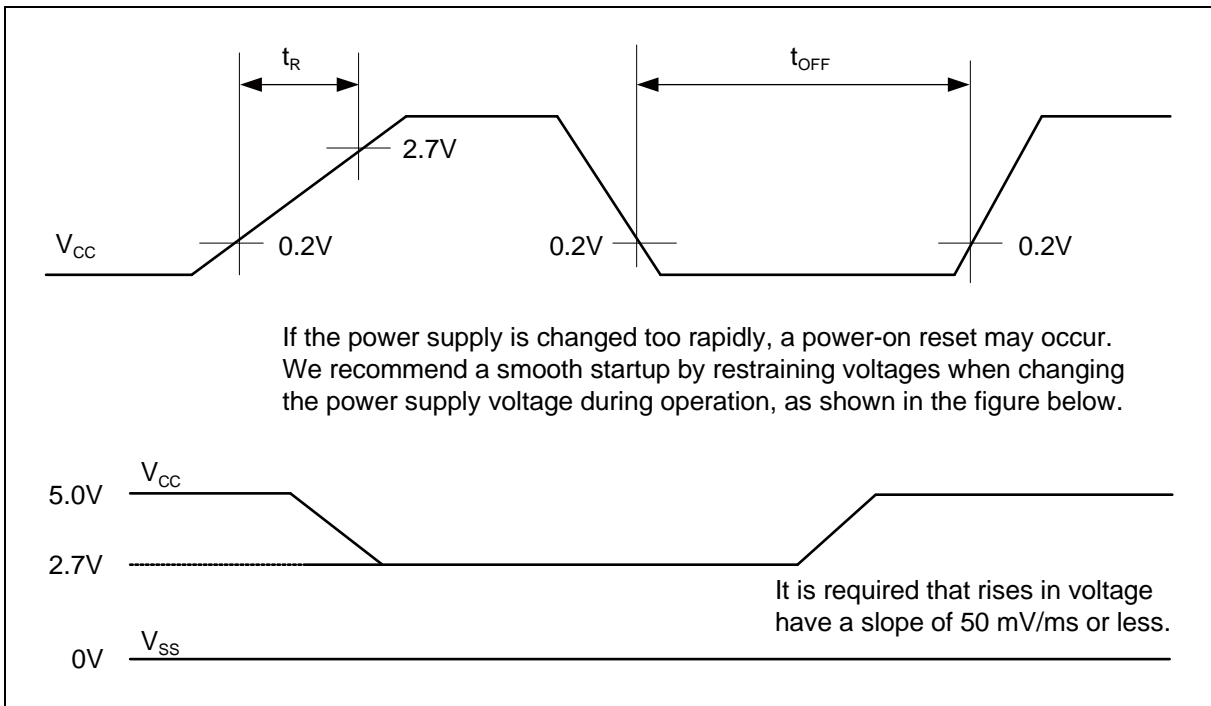
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	μs
Rejection of reset input time			1	-	μs



(7) Power-on Reset Timing

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Power on rise time	t_R	Vcc	0.05	-	30	ms
Power off time	t_{OFF}	Vcc	1	-	-	ms



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(8) USART Timing

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, $C_L = 50pF$)

Parameter	Symbol	Pin name	Conditions	4.5V ≤ V _{CC} < 5.5V		2.7V ≤ V _{CC} < 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t _{SCYC}	SCKn	Internal shift clock mode	4t _{CLKP1}	-	4t _{CLKP1}	-	ns
SCK ↓ → SOT delay time	t _{SLOV1}	SCKn, SOTn		- 20	+ 20	- 30	+ 30	ns
SOT → SCK ↑ delay time	t _{OVSHI}	SCKn, SOTn		N×t _{CLKP1} - 20*	-	N×t _{CLKP1} - 30*	-	ns
SIN → SCK ↑ setup time	t _{IVSHI}	SCKn, SINn		t _{CLKP1} + 45	-	t _{CLKP1} + 55	-	ns
SCK ↑ → SIN hold time	t _{SHIX1}	SCKn, SINn		0	-	0	-	ns
Serial clock "L" pulse width	t _{SLSH}	SCKn	External shift clock mode	t _{CLKP1} + 10	-	t _{CLKP1} + 10	-	ns
Serial clock "H" pulse width	t _{SHSL}	SCKn		t _{CLKP1} + 10	-	t _{CLKP1} + 10	-	ns
SCK ↓ → SOT delay time	t _{SLOVE}	SCKn, SOTn		-	2t _{CLKP1} + 45	-	2t _{CLKP1} + 55	ns
SIN → SCK ↑ setup time	t _{IVSHE}	SCKn, SINn		t _{CLKP1} /2 + 10	-	t _{CLKP1} /2 + 10	-	ns
SCK ↑ → SIN hold time	t _{SHIXE}	SCKn, SINn		t _{CLKP1} + 10	-	t _{CLKP1} + 10	-	ns
SCK fall time	t _F	SCKn		-	20	-	20	ns
SCK rise time	t _R	SCKn		-	20	-	20	ns

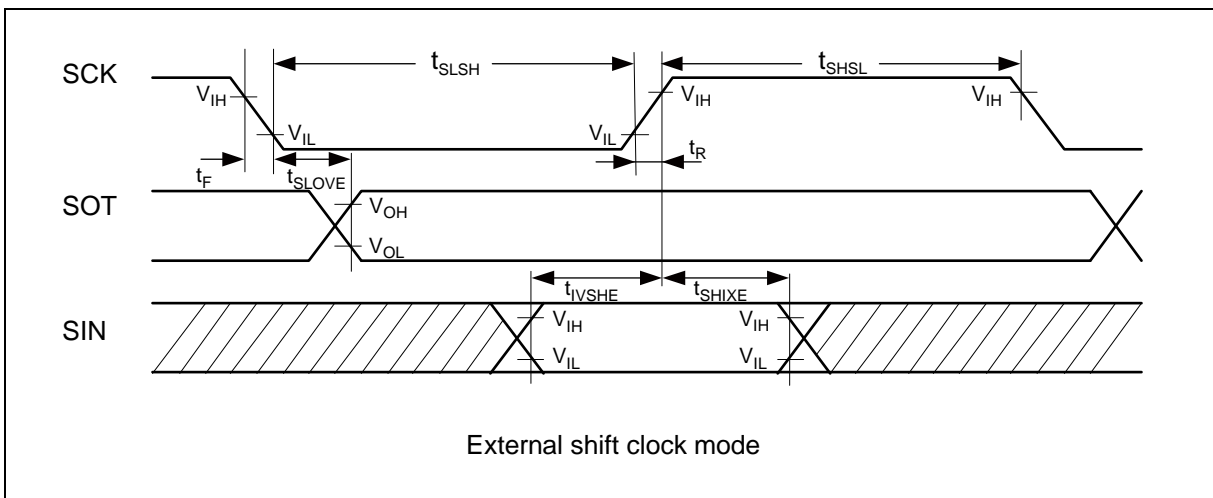
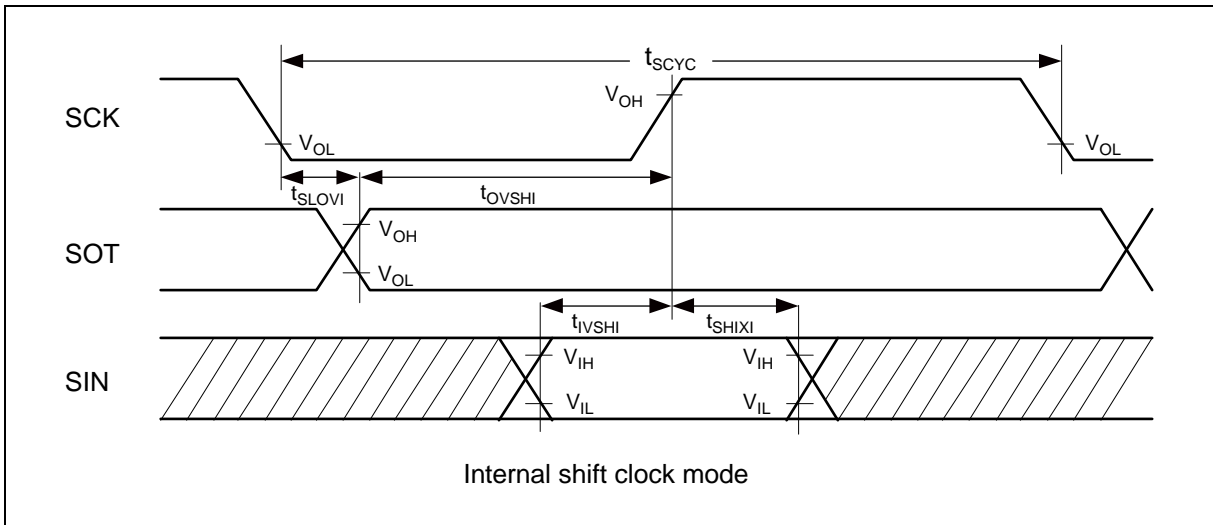
- Notes:
- AC characteristic in CLK synchronized mode.
 - C_L is the load capacity value of pins when testing.
 - Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "MB96600 series HARDWARE MANUAL".
 - t_{CLKP1} indicates the peripheral clock 1 (CLKP1), Unit: ns
 - These characteristics only guarantee the same relocate port number.
For example, the combination of SCKn and SOTn_R is not guaranteed.

*: Parameter N depends on t_{SCYC} and can be calculated as follows:

- If t_{SCYC} = 2 × k × t_{CLKP1}, then N = k, where k is an integer > 2
- If t_{SCYC} = (2 × k + 1) × t_{CLKP1}, then N = k + 1, where k is an integer > 1

Examples:

t _{SCYC}	N
4 × t _{CLKP1}	2
5 × t _{CLKP1} , 6 × t _{CLKP1}	3
7 × t _{CLKP1} , 8 × t _{CLKP1}	4
...	...



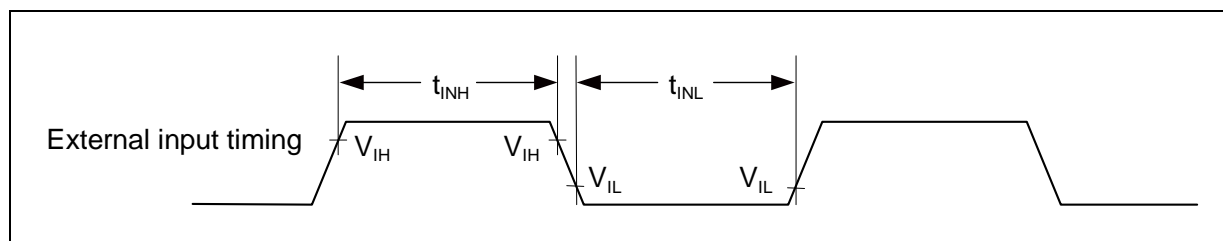
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(9) External Input Timing

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{INH} , t_{INL}	Pnn_m	$2t_{CLKP1} + 200$ ($t_{CLKP1} = 1/f_{CLKP1}$)*	-	ns	General Purpose I/O
		ADTG_R				A/D Converter trigger input
		TINn				Reload Timer
		TTGn				PPG trigger input
		INn				Input Capture
		AINn, BINn, ZINn				Quadrature Position/Revolution Counter
		INTn, INTn_R, INTn_R1	200	-	ns	External Interrupt
		NMI				Non-Maskable Interrupt

*: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time except stop when in stop mode.



5. A/D Converter

(1) Electrical Characteristics for the A/D Converter

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

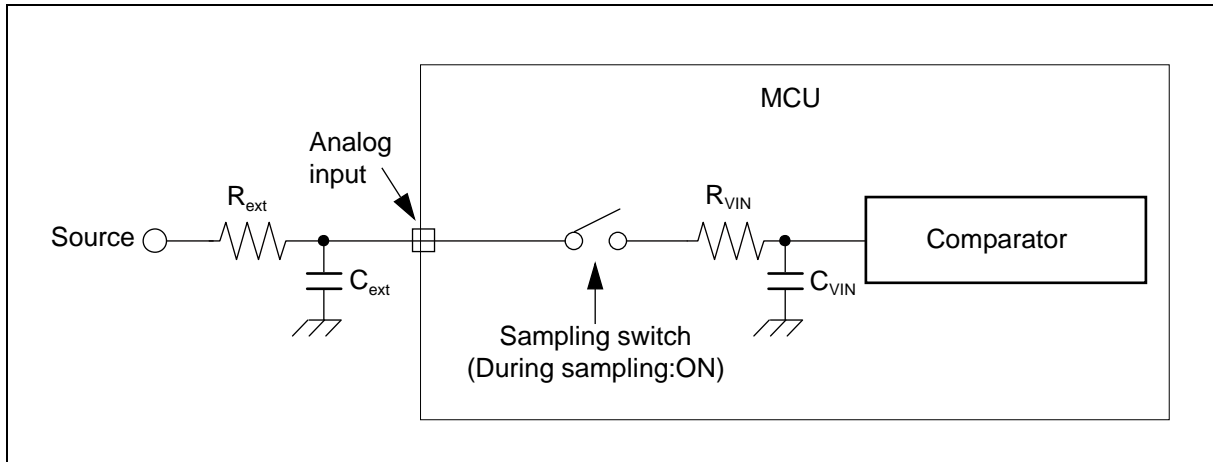
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	- 3.0	-	+ 3.0	LSB	
Nonlinearity error	-	-	- 2.5	-	+ 2.5	LSB	
Differential Nonlinearity error	-	-	- 1.9	-	+ 1.9	LSB	
Zero transition voltage	V_{OT}	ANn	Typ - 20	$AV_{SS} + 0.5LSB$	Typ + 20	mV	
Full scale transition voltage	V_{FST}	ANn	Typ - 20	$AVRH - 1.5LSB$	Typ + 20	mV	
Compare time*	-	-	1.0	-	5.0	μs	$4.5V \leq AV_{CC} \leq 5.5V$
			2.2	-	8.0	μs	$2.7V \leq AV_{CC} < 4.5V$
Sampling time*	-	-	0.5	-	-	μs	$4.5V \leq AV_{CC} \leq 5.5V$
			1.2	-	-	μs	$2.7V \leq AV_{CC} < 4.5V$
Power supply current	I_A	AV_{CC}	-	2.0	3.1	mA	A/D Converter active
	I_{AH}		-	-	3.3	μA	A/D Converter not operated
Reference power supply current (between AVRH and AV_{SS})	I_R	AVRH	-	520	810	μA	A/D Converter active
	I_{RH}		-	-	1.0	μA	A/D Converter not operated
Analog input capacity	C_{VIN}	ANn	-	-	15.6	pF	
Analog impedance	R_{VIN}	ANn	-	-	2050	Ω	$4.5V \leq AV_{CC} \leq 5.5V$
			-	-	3600	Ω	$2.7V \leq AV_{CC} < 4.5V$
Analog port input current (during conversion)	I_{AIN}	ANn	- 0.3	-	+ 0.3	μA	$AV_{SS} < V_{AIN} < AV_{CC}, AVRH$
Analog input voltage	V_{AIN}	ANn	AV_{SS}	-	AVRH	V	
Reference voltage range	-	AVRH	$AV_{CC} - 0.1$	-	AV_{CC}	V	
Variation between channels	-	ANn	-	-	4.0	LSB	

*: Time for each channel.

(2) Accuracy and Setting of the A/D Converter Sampling Time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time depends on the external driving impedance R_{ext} , the board capacitance of the A/D converter input pin C_{ext} and the AV_{CC} voltage level. The following replacement model can be used for the calculation:



R_{ext} : External driving impedance

C_{ext} : Capacitance of PCB at A/D converter input

C_{VIN} : Analog input capacity (I/O, analog switch and ADC are contained)

R_{VIN} : Analog input impedance (I/O, analog switch and ADC are contained)

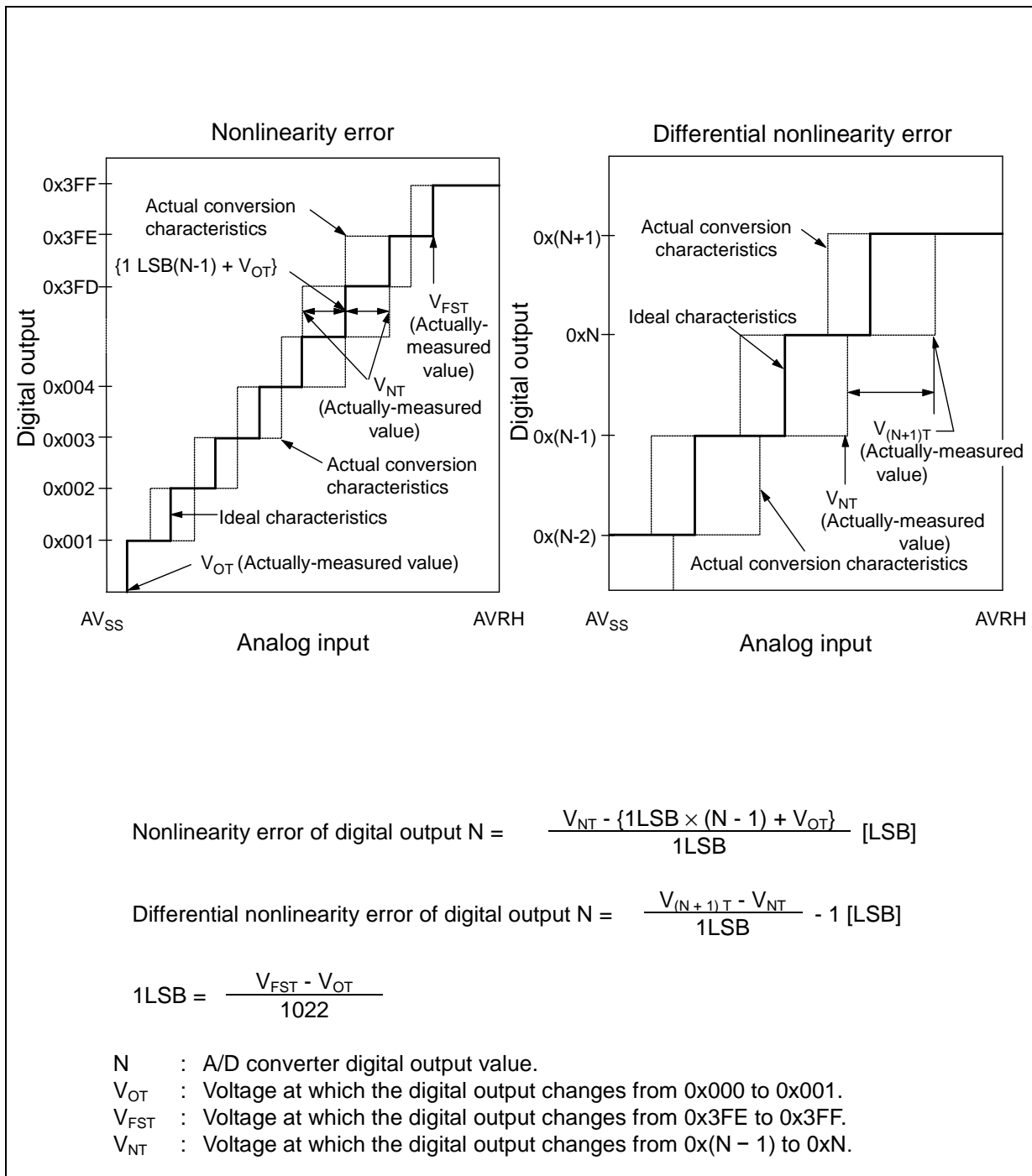
The following approximation formula for the replacement model above can be used:

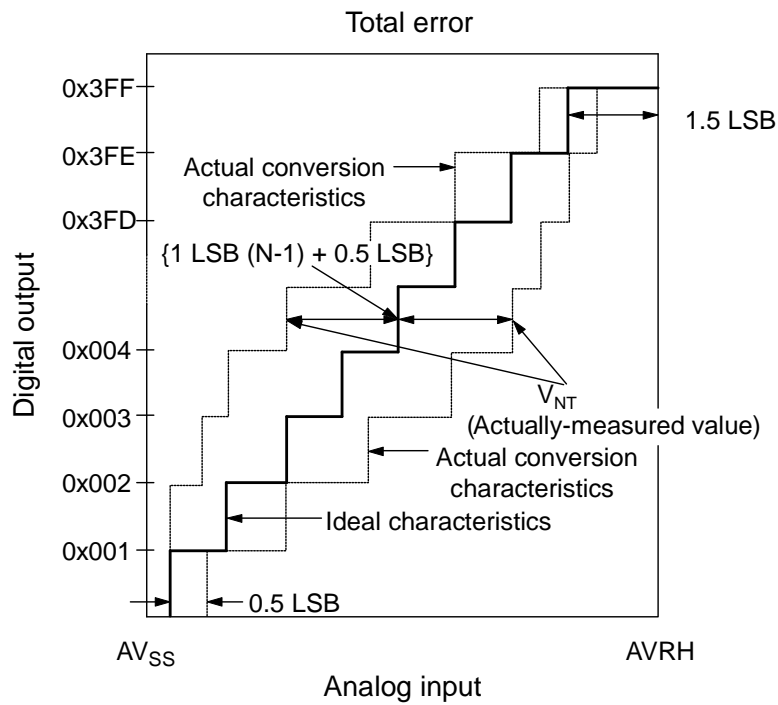
$$T_{smp} [\text{Min}] = 7.62 \times (R_{ext} \times C_{ext} + (R_{ext} + R_{VIN}) \times C_{VIN})$$

- Do not select a sampling time below the absolute minimum permitted value.
($0.5\mu\text{s}$ for $4.5\text{V} \leq AV_{CC} \leq 5.5\text{V}$, $1.2\mu\text{s}$ for $2.7\text{V} \leq AV_{CC} < 4.5\text{V}$)
- If the sampling time cannot be sufficient, connect a capacitor of about $0.1\mu\text{F}$ to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current I_{IL} (static current before the sampling switch) or the analog input leakage current I_{AIN} (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current I_{IL} cannot be compensated by an external capacitor.
- The accuracy gets worse as $|AV_{RH} - AV_{SS}|$ becomes smaller.

(3) Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Nonlinearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ←→ 0b0000000001) to the full-scale transition point (0b1111111110 ←→ 0b1111111111).
- Differential nonlinearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- Zero transition voltage: Input voltage which results in the minimum conversion value.
- Full scale transition voltage: Input voltage which results in the maximum conversion value.





$$1\text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AV}_{\text{SS}}}{1024} \text{ [V]}$$

$$\text{Total error of digital output N} = \frac{V_{\text{NT}} - \{1\text{LSB} \times \square(N - 1) + 0.5\text{LSB}\}}{1\text{LSB}}$$

- N : A/D converter digital output value.
- V_{NT} : Voltage at which the digital output changes from 0x(N + 1) to 0xN.
- V_{OT} (Ideal value) = AV_{SS} + 0.5LSB[V]
- V_{FST} (Ideal value) = AV_{RH} - 1.5LSB[V]

6. Low Voltage Detection Characteristics

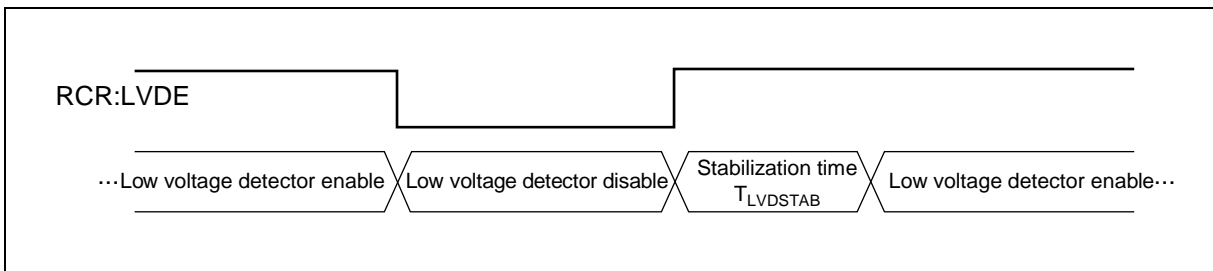
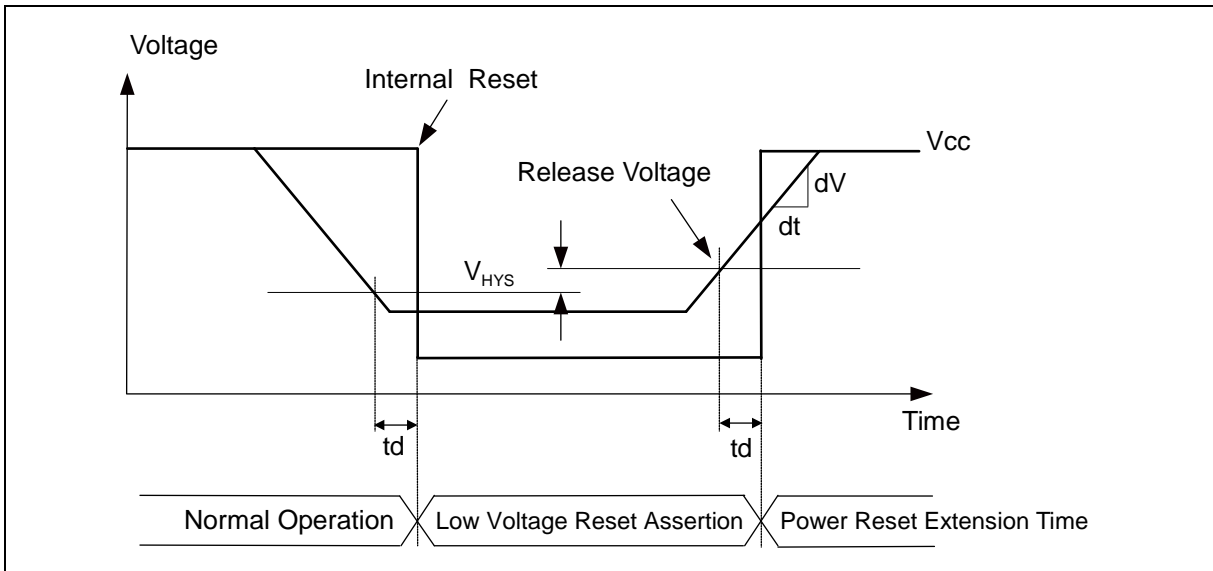
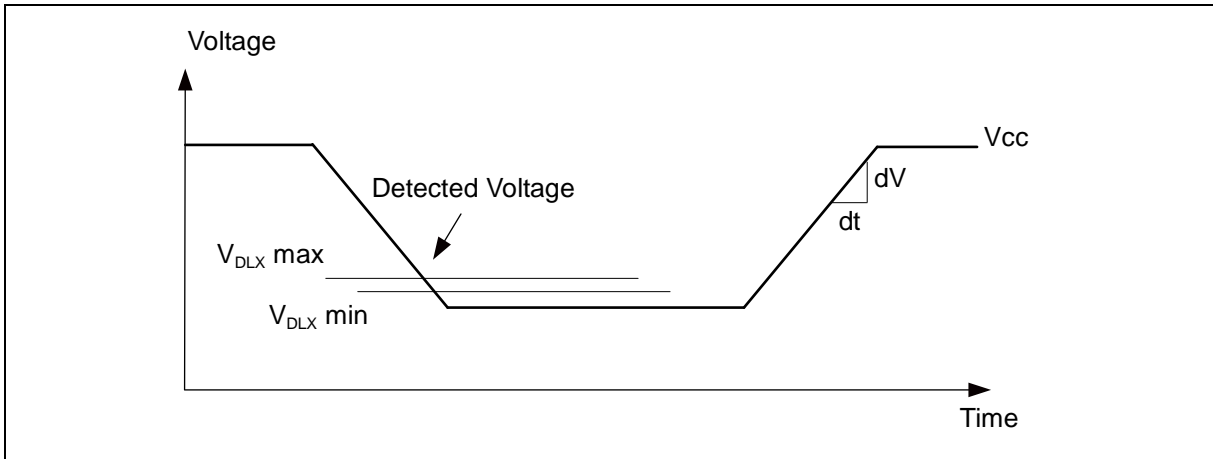
($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Detected voltage ^{*1}	V_{DL0}	CILCR:LVL = 0000 _B	2.70	2.90	3.10	V
	V_{DL1}	CILCR:LVL = 0001 _B	2.79	3.00	3.21	V
	V_{DL2}	CILCR:LVL = 0010 _B	2.98	3.20	3.42	V
	V_{DL3}	CILCR:LVL = 0011 _B	3.26	3.50	3.74	V
	V_{DL4}	CILCR:LVL = 0100 _B	3.45	3.70	3.95	V
	V_{DL5}	CILCR:LVL = 0111 _B	3.73	4.00	4.27	V
	V_{DL6}	CILCR:LVL = 1001 _B	3.91	4.20	4.49	V
Power supply voltage change rate ^{*2}	dV/dt	-	- 0.004	-	+ 0.004	V/ μ s
Hysteresis width	V_{HYS}	CILCR:LVHYS=0	-	-	50	mV
		CILCR:LVHYS=1	80	100	120	mV
Stabilization time	$T_{LVDSTAB}$	-	-	-	75	μ s
Detection delay time	t_d	-	-	-	30	μ s

*1: If the power supply voltage fluctuates within the time less than the detection delay time (t_d), there is a possibility that the low voltage detection will occur or stop after the power supply voltage passes the detection range.

*2: In order to perform the low voltage detection at the detection voltage (V_{DLX}), be sure to suppress fluctuation of the power supply voltage within the limits of the change ration of power supply voltage.

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7. Flash Memory Write/Erase Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_D = 1.8V \pm 0.15V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	$T_A \leq +105^\circ C$	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time	Large Sector	$T_A \leq +105^\circ C$	-	25	400	μs	Not including system-level overhead time.
	Small Sector	-	-	25	400	μs	
Chip erase time		$T_A \leq +105^\circ C$	-	5.11	25.05	s	Includes write time prior to internal erase.

Note: While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing, be sure to turn the power off by using an external voltage detector.

To put it concrete, change the external power in the range of change ration of power supply voltage ($-0.004V/\mu s$ to $+0.004V/\mu s$) after the external power falls below the detection voltage (V_{DLX})^{*1}.

Write/Erase cycles and data hold time

Write/Erase cycles (cycle)	Data hold time (year)
1,000	20 ^{*2}
10,000	10 ^{*2}
100,000	5 ^{*2}

*1: See "6. Low Voltage Detection Characteristics".

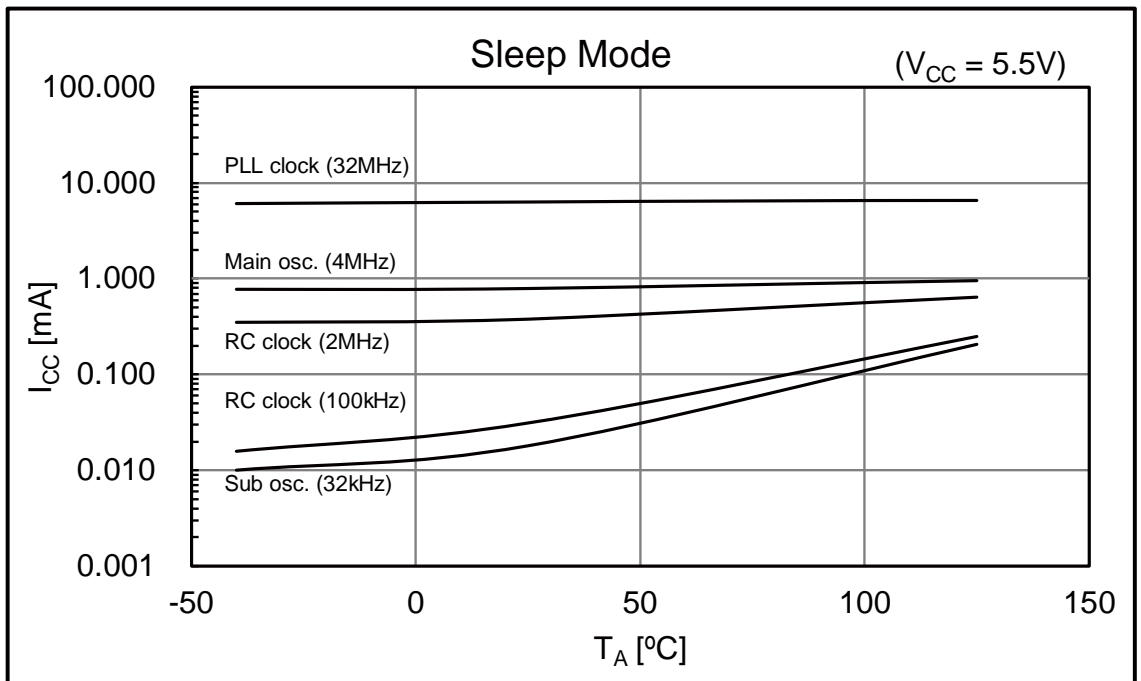
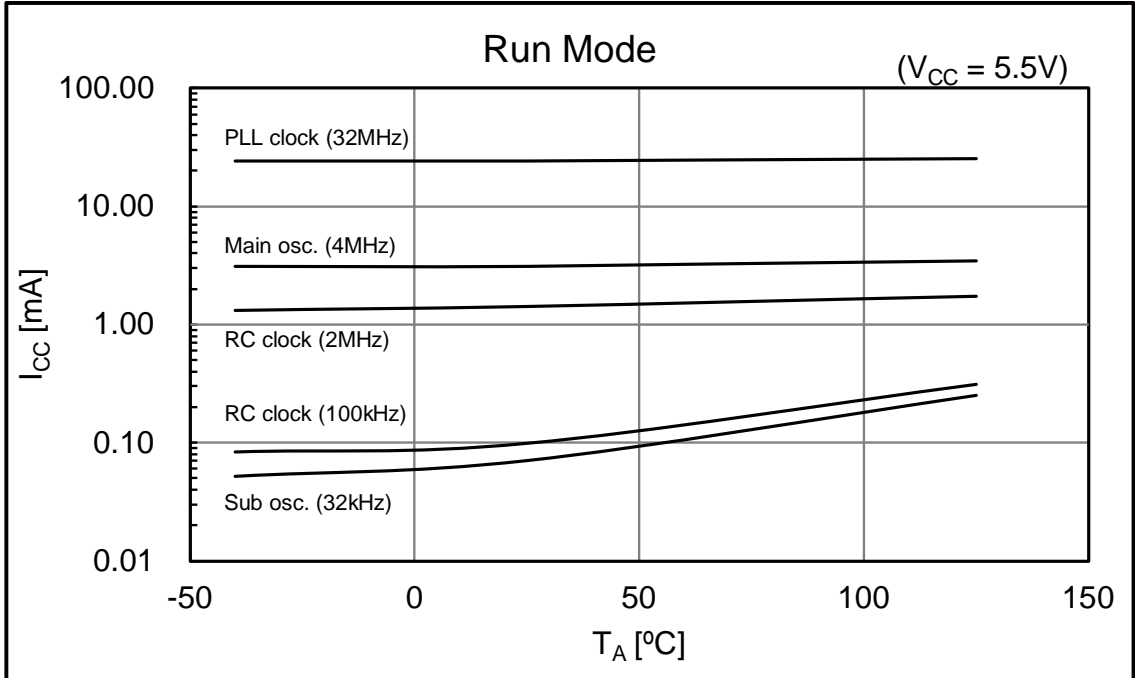
*2: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at $+85^\circ C$).

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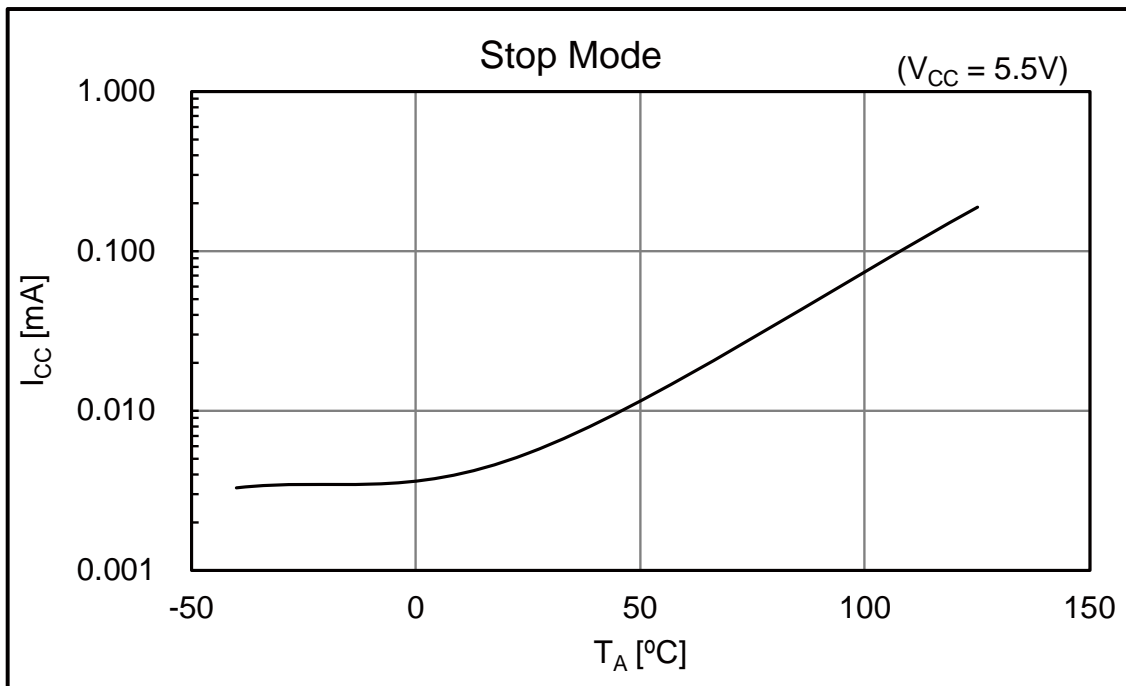
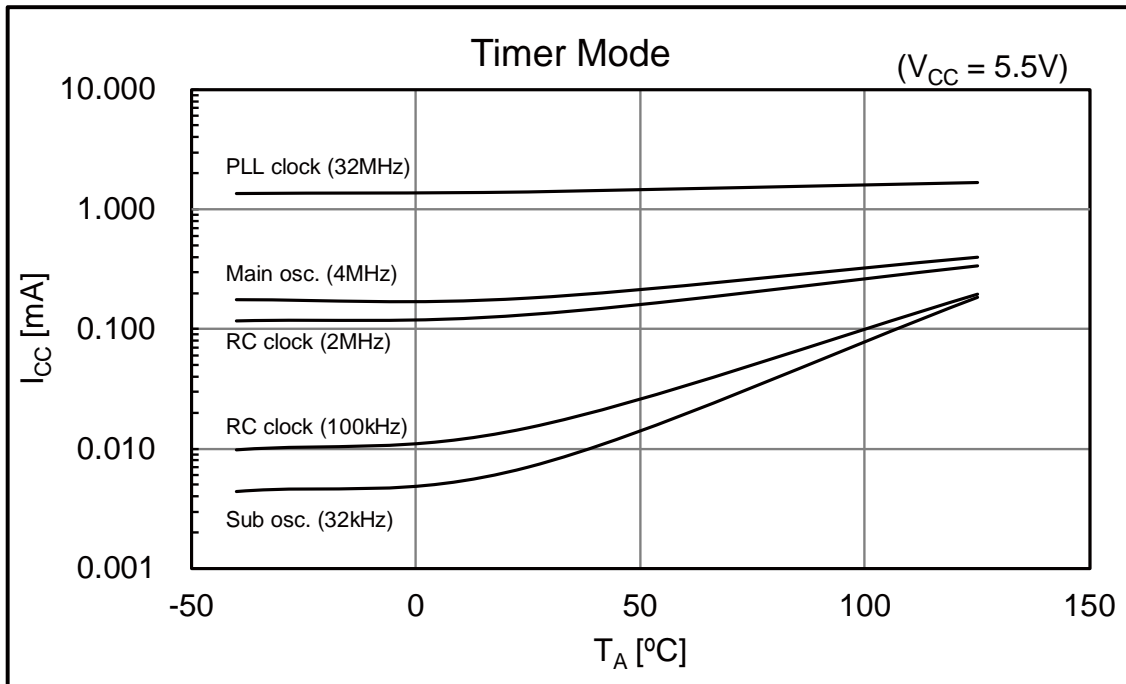
■ EXAMPLE CHARACTERISTICS

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

- MB96F615



• MB96F615



MB96610 Series

• Used setting

Mode	Selected Source Clock	Clock/Regulator and FLASH Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32MHz
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4MHz
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2MHz
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100kHz
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32kHz
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
Timer mode	PLL	CLKMC = 4MHz, CLKPLL = 32MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	Main osc.	CLKMC = 4MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock fast	CLKMC = 2MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock slow	CLKMC = 100kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
	Sub osc.	CLKMC = 32 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode

■ ORDERING INFORMATION

MCU with CAN controller

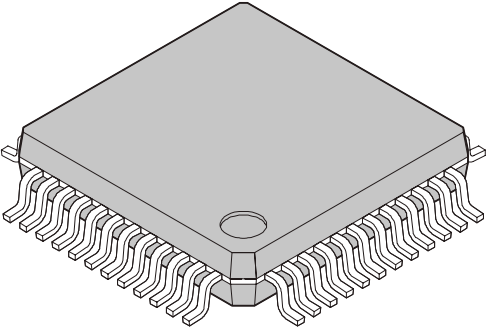
Part number	Flash memory	Package
MB96F612RBPMC-GSE1	Flash A (64.5KB)	48-pin plastic LQFP (FPT-48P-M26)
MB96F612RBPMC-GSE2		
MB96F612RBPMC-GTE1		
MB96F612RBPMC-GTE2		
MB96F613RBPMC-GSE1	Flash A (96.5KB)	48-pin plastic LQFP (FPT-48P-M26)
MB96F613RBPMC-GSE2		
MB96F613RBPMC-GTE1		
MB96F613RBPMC-GTE2		
MB96F615RBPMC-GSE1	Flash A (160.5KB)	48-pin plastic LQFP (FPT-48P-M26)
MB96F615RBPMC-GSE2		
MB96F615RBPMC-GTE1		
MB96F615RBPMC-GTE2		

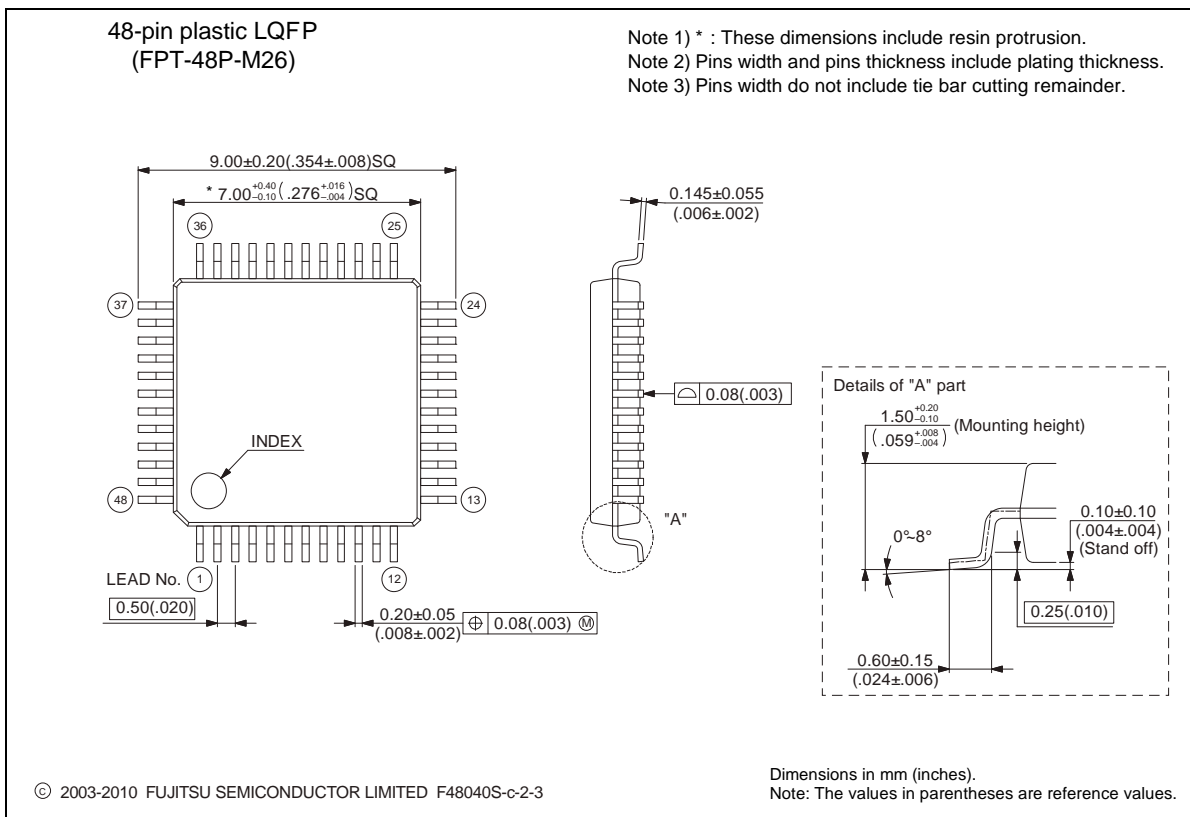
MCU without CAN controller

Part number	Flash memory	Package
MB96F612ABPMC-GSE1	Flash A (64.5KB)	48-pin plastic LQFP (FPT-48P-M26)
MB96F612ABPMC-GSE2		
MB96F612ABPMC-GTE1		
MB96F612ABPMC-GTE2		
MB96F613ABPMC-GSE1	Flash A (96.5KB)	48-pin plastic LQFP (FPT-48P-M26)
MB96F613ABPMC-GSE2		
MB96F613ABPMC-GTE1		
MB96F613ABPMC-GTE2		
MB96F615ABPMC-GSE1	Flash A (160.5KB)	48-pin plastic LQFP (FPT-48P-M26)
MB96F615ABPMC-GSE2		
MB96F615ABPMC-GTE1		
MB96F615ABPMC-GTE2		

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■ PACKAGE DIMENSION

 <p>48-pin plastic LQFP</p> <p>(FPT-48P-M26)</p>	Lead pitch	0.50 mm
	Package width x package length	7 mm x 7 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g
	Code (Reference)	P-LFQFP48-7x7-0.50



Please check the latest package dimension at the following URL.
<http://edevice.fujitsu.com/package/en-search/>

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
-	-	PRELIMINARY → Data sheet
2	■FEATURES	Changed the description of “System clock” Up to 16 MHz external clock for devices with fast clock input feature → Up to 8 MHz external clock for devices with fast clock input feature
4		Changed the description of “Built-in On Chip Debugger” - Event sequencer: 2 levels → - Event sequencer: 2 levels + reset
5	■PRODUCT LINEUP	Changed the Remark of RLT RLT 1/3/6 Only RLT6 can be used as PPG clock source → RLT 1/3/6
6	■BLOCK DIAGRAM	Deleted the block of RLT6 from PPG block
		Changed the RLT block 2ch → 1/3/6 3ch
8	■PIN FUNCTION DESCRIPTION	Changed the Description of PPGn_B Programmable Pulse Generator n output (8bit) → Programmable Pulse Generator n output (16bit/8bit)
12	■I/O CIRCUIT TYPE	Changed the figure of type B
		Changed the Remarks of type B (CMOS hysteresis input with input shutdown function, I _{OL} = 4mA, I _{OH} = -4mA, Programmable pull-up resistor) → (CMOS level output (I _{OL} = 4mA, I _{OH} = -4mA), Automotive input with input shutdown function and programmable pull-up resistor)
13		Changed the figure of type G
15	■MEMORY MAP	Changed the START addresses of Boot-ROM 0F:E000 _H → 0F:C000 _H
17	■USER ROM MEMORY MAP FOR FLASH DEVICES	Changed the annotation Others (from DF:0200 _H to DF:1FFF _H) are all ROM Mirror area for SAS-512B. → Others (from DF:0200 _H to DF:1FFF _H) is mirror area of SAS-512B.
19	■INTERRUPT VECTOR TABLE	Changed the Description of CALLV0 to CALLV7 Reserved → CALLV instruction
		Changed the Description of RESET Reserved → Reset vector

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Page	Section	Change Results
19	■INTERRUPT VECTOR TABLE	Changed the Description of INT9 Reserved → INT9 instruction
		Changed the Description of EXCEPTION Reserved → Undefined instruction execution
20		Changed the Vector name of Vector number 64 PPGRLT → RLT6
		Changed the Description of Vector number 64 Reload Timer 6 can be used as PPG clock source → Reload Timer 6
24	■HANDLING DEVICES	Added the description to “3. External clock usage” (3) Opposite phase external clock
		Changed the description in “7. Turn on sequence of power supply to A/D converter and analog inputs” It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVR _H or AV _{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable). → It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, AVR _H must not exceed AV _{CC} . Input voltage for ports shared with analog input ports also must not exceed AV _{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).
25		Added the description “12. Mode Pin (MD)”
27	■ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	Changed the annotation *4 Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode). → Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset.
		Added the annotation *4 The DEBUG I/F pin has only a protective diode against V _{SS} . Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.

Page	Section	Change Results
28	2. Recommended Operating Conditions	Added the Value and Remarks to “Power supply voltage” Min: 2.0V Typ: - Max: 5.5V Remarks: Maintains RAM data in stop mode
		Changed the Value of “Smoothing capacitor at C pin” Typ: 1.0μF → 1.0μF to 3.9μF Max: 1.5μF → 4.7μF
		Changed the Remarks of “Smoothing capacitor at C pin” Deleted “(Target value)” Added “3.9μF (Allowance within ± 20%)”
29	3. DC Characteristics (1) Current Rating	Deleted “(Target value)” from Remarks
		Added the Symbol to “Power supply current in Run modes” I_{CCRCH} , I_{CCRCL}
		Changed the Conditions of I_{CCPLL} , I_{CCMAIN} , I_{CCSUB} in “Power supply current in Run modes” “Flash 0 wait” is added
		Changed the Value of “Power supply current in Run modes” I_{CCPLL} TYP:27mA → 25mA ($T_A = +25^\circ\text{C}$) Max: 36mA → 34mA ($T_A = +105^\circ\text{C}$) Max: 37mA → 35mA ($T_A = +125^\circ\text{C}$) I_{CCMAIN} TYP:5mA → 3.5mA ($T_A = +25^\circ\text{C}$) Max: 10mA → 7.5mA ($T_A = +105^\circ\text{C}$) Max: 11.5mA → 8.5mA ($T_A = +125^\circ\text{C}$) I_{CCSUB} TYP:0.5mA → 0.1mA ($T_A = +25^\circ\text{C}$) Max: 5mA → 3mA ($T_A = +105^\circ\text{C}$) Max: 6.5mA → 4mA ($T_A = +125^\circ\text{C}$)
30		Added the Symbol to “Power supply current in Sleep modes” I_{CCSRCH} , I_{CCSRCL}
		Changed the Conditions of $I_{CCSMAIN}$ in “Power supply current in Sleep modes” “SMCR:LPMSS=0” is added
		Changed the Value of “Power supply current in Sleep modes” I_{CCSPLL} Typ: 10mA → 6.5mA ($T_A = +25^\circ\text{C}$) Max : 15mA → 13mA ($T_A = +105^\circ\text{C}$) Max : 16.5mA → 14mA ($T_A = +125^\circ\text{C}$) $I_{CCSMAIN}$ Typ: 3mA → 0.9mA ($T_A = +25^\circ\text{C}$) Max: 8mA → 4mA ($T_A = +105^\circ\text{C}$) Max: 9.5mA → 5mA ($T_A = +125^\circ\text{C}$) I_{CCSSUB} Typ: 0.3mA → 0.04mA ($T_A = +25^\circ\text{C}$) Max: 4.5mA → 2.5mA ($T_A = +105^\circ\text{C}$) Max: 6mA → 3.5mA ($T_A = +125^\circ\text{C}$)

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Page	Section	Change Results
31	3. DC Characteristics (1) Current Rating	Added the Symbol to “Power supply current in Timer modes” I_{CCTPLL}
		Changed the Conditions of $I_{CCTMAIN}$, I_{CCTRCH} , I_{CCTRCL} in “Power supply current in Timer modes” “SMCR:LPMSS=0” is added
		Changed the Value of “Power supply current in Timer modes” I_{CCTRCL} Typ: $45\mu A \rightarrow 35\mu A$ ($T_A = +25^\circ C$) I_{CCTSUB} Typ: $30\mu A \rightarrow 25\mu A$ ($T_A = +25^\circ C$)
		Changed the Value of “Power supply current in Stop mode” I_{CCH} Typ: $30\mu A \rightarrow 20\mu A$ ($T_A = +25^\circ C$) Max: $830\mu A \rightarrow 825\mu A$ ($T_A = +105^\circ C$)
32		Added the Symbol $I_{CCFLASHPD}$
		Changed the Value and condition of “Power supply current for active Low Voltage detector” I_{CCLVD} Typ: $5\mu A$, Max: $15\mu A$, Remarks: nothing → Typ: $5\mu A$, Max: -, Remarks: $T_A = +25^\circ C$ Typ: -, Max: $12.5\mu A$, Remarks: $T_A = +125^\circ C$
		Changed the condition of “Flash Write/Erase current” $I_{CCFLASH}$ Typ: $12.5mA$, Max: $20mA$, Remarks: nothing → Typ: $12.5mA$, Max: -, Remarks: $T_A = +25^\circ C$ Typ: -, Max: $20mA$, Remarks: $T_A = +125^\circ C$
34	3. DC Characteristics (2) Pin Characteristics	Added the Symbol for DEBUG I/F pin V_{OLD}
		Changed the Pin name of “Input capacitance” Other than V_{CC} , V_{SS} , AV_{CC} , AV_{SS} , AV_{RH} → Other than C , V_{CC} , V_{SS} , AV_{CC} , AV_{SS} , AV_{RH}
		Deleted the annotation “ I_{OH} and I_{OL} are target value.”
35	4. AC Characteristics (1) Main Clock Input Characteristics	Added the figure (t_{CYLH}) when using the external clock
36	(2) Sub Clock Input Characteristics	Added the figure (t_{CYLL}) when using the crystal oscillator clock
37	(3) Built-in RC Oscillation Characteristics	Added “RC clock stabilization time”

Page	Section	Change Results
38	4. AC Characteristics (5) Operating Conditions of PLL	Changed the Value of “PLL input clock frequency” Max: 16MHz → 8MHz
		Changed the Symbol of “PLL macro oscillation clock frequency” $f_{\text{PLLO}} \rightarrow f_{\text{CLKVCO}}$
		Added Remarks to “PLL macro oscillation clock frequency” Added “PLL phase jitter” and the figure
	(6) Reset Input	Added the figure for reset input time (t_{RSTL})
40	(8) USART Timing	Changed the condition ($V_{\text{CC}} = AV_{\text{CC}} = 2.7\text{V}$ to 5.5V , $V_{\text{SS}} = AV_{\text{SS}} = 0\text{V}$, $T_{\text{A}} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$) → ($V_{\text{CC}} = AV_{\text{CC}} = 2.7\text{V}$ to 5.5V , $V_{\text{SS}} = AV_{\text{SS}} = 0\text{V}$, $T_{\text{A}} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $C_{\text{L}}=50\text{pF}$)
		Changed the HARDWARE MANUAL “MB96610 series HARDWARE MANUAL” → “MB96600 series HARDWARE MANUAL”
41		Changed the figure for “Internal shift clock mode”
43	5. A/D Converter (1) Electrical Characteristics for the A/D Converter	Added “Analog impedance”
		Added “Variation between channels”
		Added the annotation
45	5. A/D Converter (3) Definition of A/D Converter Terms	Changed the Description and the figure “Linearity” → “Nonlinearity” “Differential linearity error” → “Differential nonlinearity error”
		Changed the Description Linearity error: Deviation of the line between the zero-transition point (0b0000000000 ←→ 0b0000000001) and the full-scale transition point (0b1111111110 ←→ 0b1111111111) from the actual conversion characteristics. → Nonlinearity error: Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ←→ 0b0000000001) to the full-scale transition point (0b1111111110 ←→ 0b1111111111).
		Added the Description “Zero transition voltage” “Full scale transition voltage”
47	6. Low Voltage Detection Characteristics	Added the Value of “Power supply voltage change rate” Max: $+0.004\text{ V}/\mu\text{s}$
		Added “Hysteresis width” (V_{HYS})
		Added “Stabilization time” ($T_{\text{LV DSTAB}}$)
		Added “Detection delay time” (t_{d})
		Deleted the Remarks
48		Added the annotation *1/*2
		Added the figure for “Hysteresis width” Added the figure for “Stabilization time”

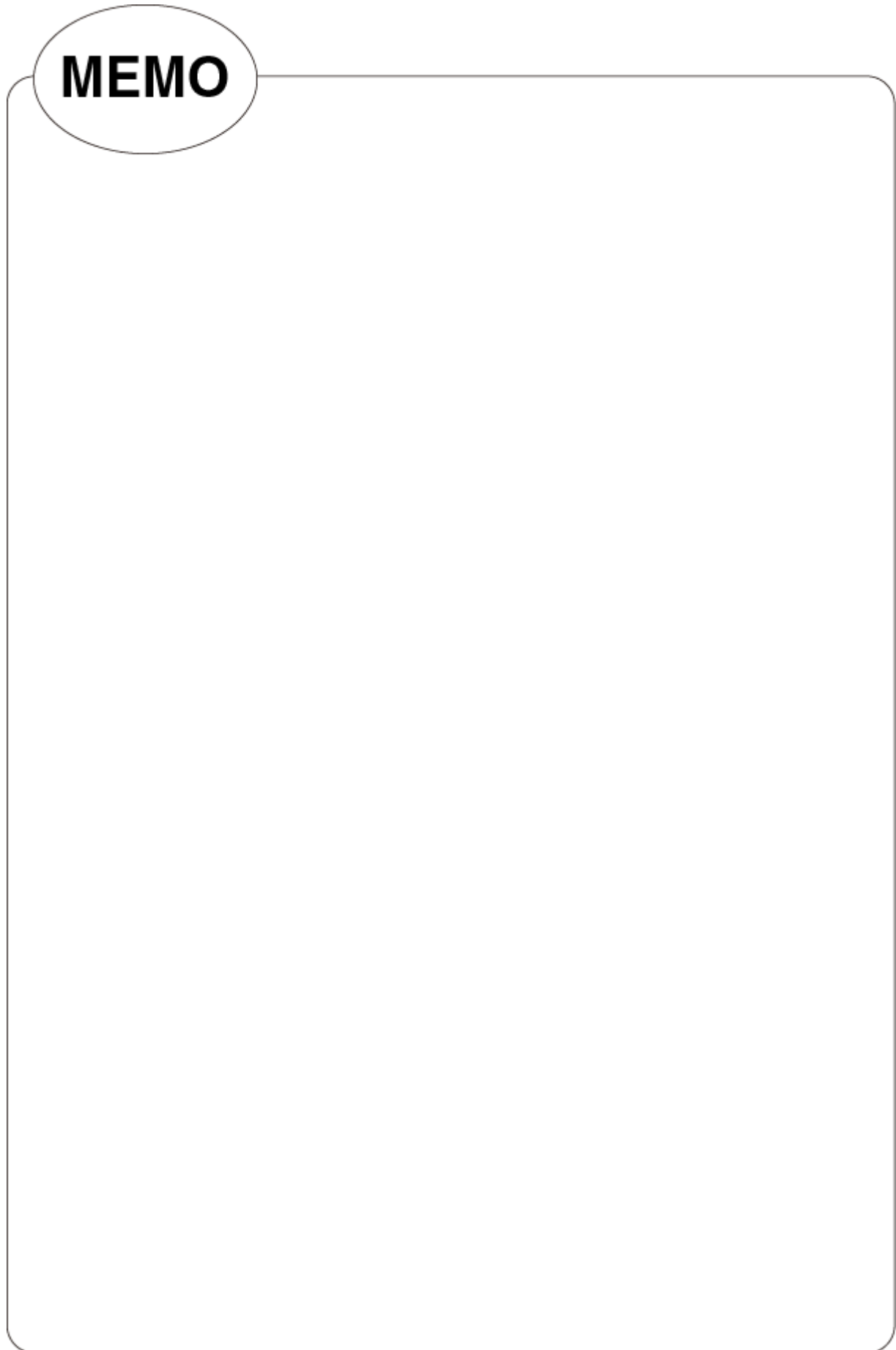
MB96610 Series

Page	Section	Change Results
49	7. Flash Memory Write/Erase Characteristics	Changed the Value of “Sector erase time”
		Added “Security Sector” to “Sector erase time”
		Changed the Parameter “Half word (16 bit) write time” → “Word (16-bit) write time”
		Changed the Value of “Chip erase time”
		Changed the Remarks of “Sector erase time” Excludes write time prior to internal erase → Includes write time prior to internal erase
		Added the Note and annotation *1
		Deleted “(targeted value)” from title “ Write/Erase cycles and data hold time”
50 to 52	■EXAMPLE CHARACTERISTICS	Added section

MEMO

MEMO

MEMO



MB96610 Series

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