IES5521A

Simple Zero-Crossing Triac Control Circuit with Adjustable Time-out

1 FEATURES

- Time-out function stops triac operation after a set time
- Reset time-out by turning mains supply off and on
- Low external component count
- Constant ON period time, with proportional OFF time
- All ON periods are an integral number of mains cycles
- No DC component in the mains supply
- On chip circuit protection against triac gate spikes
- Low supply current requirement
- Sensor AC powered, thus minimising DC supply and filtering needs
- Separate power supply input, allowing easy gate pulse width adjustment
- Accurate time-out using the mains frequency, or widely adjustable external “RC” time-out

2 TYPICAL APPLICATIONS

- Temperature control of cooking or heating appliances.
- Hair styling tools (straighteners, driers, curling wands ..)
- Electric Irons
- Toaster Ovens, Rice Cookers, Hotplates, Fry Pans, etc.
- Electric Blankets, Heating Pads, etc.
- or other appliances where a safety time-out is required.

3 GENERAL DESCRIPTION

The IES5521A is a derivative of the OM1654A, but offering the extra safety feature of a nominal 1 hour time-out. This is a key safety requirement for a range of personal and home appliance applications. The time-out function will stop the triac operation and thus prevent power from being applied to the heating elements.

Time-out can be accurately controlled from the AC supply frequency for a period of 1 hour (60Hz, or 71minutes at 50Hz), or can be adjusted by adding external resistor and capacitor components to set the frequency of an on-chip RC oscillator. In this manner, time-out periods from 1 minute to more than 5 hours, are possible.

The IES5521A is a monolithic bipolar control circuit for zero-crossing triggering of a triac in applications where it is controlled by a resistive sensor such as an NTC thermistor. In a typical application it can be used for the temperature control of a heating element in a cooker or another home heating appliance.

It is designed to control a suitable triac with a resistive load ranging from 400 watts on a nominal 220/250 volt mains supply. It can also be easily applied to 120Vac mains applications.

4 BLOCK DIAGRAM

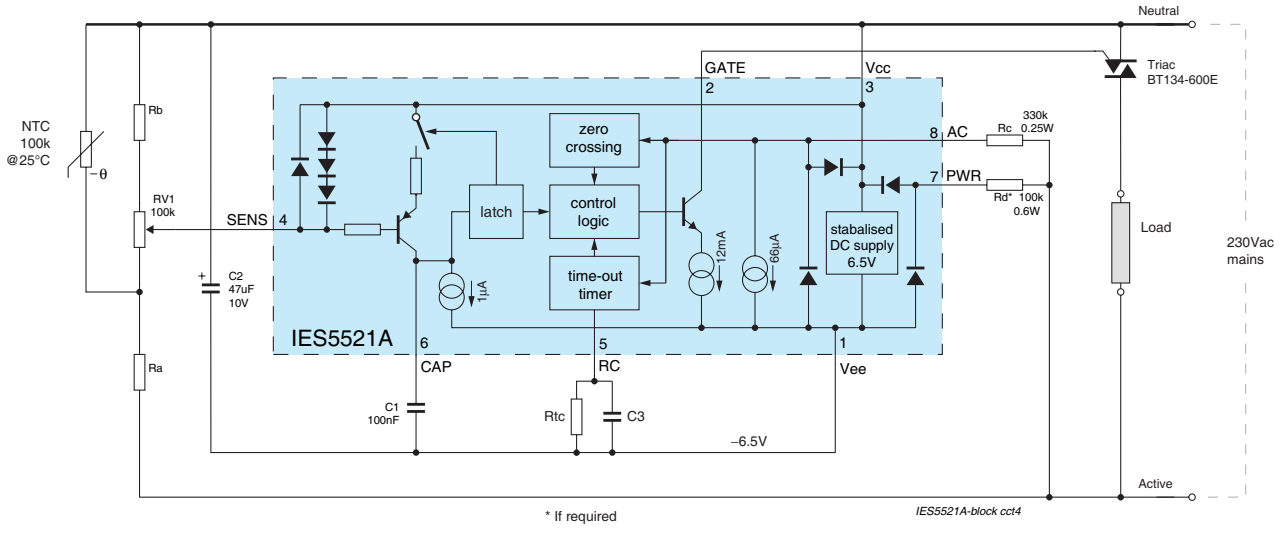

Fig.1 Block diagram

Contents are subject to the Disclaimer

5 PINNING INFORMATION

5.1 Pinning layout (8 pin)

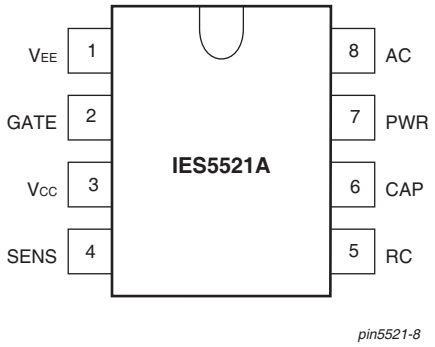

Fig.2 Pinning diagram (DIL-8 and SO-8)

5.2 Pin description (8 pin)

SYMBOL	PIN	DESCRIPTION
V_{EE}	1	Negative supply
GATE	2	Triac gate drive
V_{CC}	3	Common, Positive supply
SENS	4	Temperature sense
RC	5	RC oscillator input
CAP	6	Timing capacitor
PWR	7	Power supply input
AC	8	Mains supply

6 FUNCTIONAL DESCRIPTION

6.1 V_{CC} – Common, positive DC supply

The positive DC supply rail for the control IC IES5521A is used as the Common reference. This is connected to the T1 terminal of the triac, and being the positive supply rail enables negative gate drive to the triac in both positive and negative supply half cycles on T2. By driving the triac in this way the insensitive quadrant (negative T2 voltage, and positive gate triggering signal) is avoided.

6.2 V_{EE} – Substrate, negative DC supply

The substrate connection is the negative DC power supply terminal of the IES5521A. This should be bypassed to V_{CC} by a filtering capacitor of 47 microfarads. The operating voltage is typically –6.5 volts. This capacitor needs to be sufficiently large to maintain the operating voltage during the half cycle when it is not being charged, as well as to provide the energy to drive the triac gate during the gate pulse.

6.3 AC – AC signal, power supply and synchronisation

For the IES5521A the AC input is connected to the active mains supply rail via a resistor chosen to give the required gate pulse width, to ensure that during zero crossing of the mains cycle, the gate signal is applied from before the load current falls below the triac holding current, until after the load current has increased to a value greater than the triac latching current. A resistor from AC to V_{CC} may be required to ensure the gate drive pulse is still present when the negative mains voltage is insufficient for the load current to have reached the negative latching current.

In the simplest application (optimised for a 400W load), the AC input is connected via a160 kΩ resistor to the 220/250 volt AC mains supply line.

The AC input signal is rectified to provide some of the internal supply voltage, and also provides the synchronising information required by the IES5521A to generate the zero crossing signal.

6.4 PWR – Power supply

The pin (PWR) allows a further resistor to be used to provide an adequate DC power supply while also permitting easy adjustment of the gate pulse width via the AC pin.

The PWR pin is driven by a resistor from the mains Active. This resistor is chosen to ensure that the DC power supply is sufficient to provide the power supply necessary for the function of the IES5521A, and in addition to provide the energy needed for the gate drive. These calculations are described in the OM1654 application note AN002, and an application example is given in section 9.

6.5 GATE – Triac gate drive

The triac gate drive output is designed to be connected directly to the triac gate without the need for an external current setting resistor. It has inbuilt protection to withstand transient signals which may be induced on the gate of the triac by mains transients during firing. The gate drive is designed for a triac with a gate sensitivity which requires less than 10 mA of triggering current, and a suitable latching current. One triac with suitable characteristics is the BT137 series E when used with a load of more than 400 watts.

The gate drive has a negative temperature coefficient designed to match the gate temperature characteristic of typical triacs.

6.6 CAP – Timing capacitor

The timing capacitor is connected between this pin and V_{EE}. The discharge time of this capacitor sets the triac ON time, and is proportional to the capacitance value (approximately 4 seconds per micro farad). The charging period, or OFF time, varies with the magnitude of the input signal from the sensor. The ON period is synchronised with the mains zero crossing signals so that an integral number of full cycles makes up the ON period, and no nett DC signal is generated in the supply line. The initiation of an ON period is suppressed until the chip power supply reaches its regulated value.

After reaching a valid V_{EE} the chip will stay in operation even if the supply falls to about 4 volts. Triac gate pulses will not start until the internal voltage limiting “zener” begins to conduct.

6.7 SENS – Sensor input

The sensor input is designed to accept an input which is an AC signal referenced to common; thereby avoiding problems associated with the power dissipation involved in generating sufficient DC current to drive the sensor over its full operating resistance range. If a suitable resistive sensor is used with a parallel level setting potentiometer to apply a proportion of the AC sensor signal to the SENS input, a typical circuit will power this via a 160 kΩ resistor from the AC supply. The SENS input signal threshold is one VBE below the V_{CC} rail. Signals with a magnitude greater than this VBE charge the timing capacitor towards the V_{CC} rail until it reaches the threshold which initiates an ON cycle. Signals with a magnitude less than this do not charge the capacitor, and the triac drive remains OFF.

External circuits may be used to give greater temperature linearity and accuracy, and improved performance with variation in ambient temperature. The SENS input is only active on negative signals with respect to V_{CC}, and therefore either a full AC input may be used, or a signal that is only negatively going with respect to V_{CC}.

6.8 RC – Setting the time-out period

6.8.1 USING THE AC MAINS FREQUENCY

The RC oscillator can be disabled by connecting the RC pin to the V_{CC} pin through a 470 kΩ pull-up resistor (figure 5). The resistor tolerance is not critical. This resistor acts to limit current into pin 5 to approximately 4 / 470 kΩ = 8.5 µA. Other values may be used, however, this current must be accounted for in the determination of the appropriate power supply resistor R3 (figure 5).

With the RC oscillator disabled, the time-out circuit will run from the AC supply frequency, counting down 212992 cycles, whereupon it disables the gate signal to the triac. The time-out period is thus determined by the frequency of the AC supply, but is precisely controlled for a particular frequency.

Should a different accurate time-out period be required for a particular mains frequency (other than described here), please contact Integrated Electronic Solutions to discuss your needs.

6.8.2 USING THE RC OSCILLATOR

A period other than this may be chosen by removing the pull-up resistor between RC and V_{CC}, and replacing it with parallel resistor and capacitor network between the RC pin and V_{EE} (figure 6).

A typical resistor value would be 470 kΩ, with a corresponding capacitor chosen to give the desired time-out period. Lower resistances (for example, 100 kΩ) are possible but will cause a small shift in the oscillator frequency compared to the above calculation, while timing at larger resistances may be affected by leakage currents on the printed circuit board.

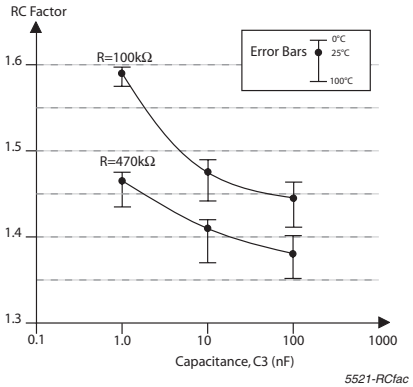

Fig.3 RC period multiplication factor

Figure 3 shows the multiplication factor for the period of the oscillation

associated with the circuit. For the application circuit of figure 6, the oscillation frequency (f_{OSC}) is therefore:

$$f_{OSC} \approx \frac{1}{1.38 \times R \times C} \quad (Hz)$$

The tolerance of the RC components determines the accuracy of the time-out period, with the RC oscillator itself having an accuracy of < 3% over the operating temperature range. The time-out period can be roughly calculated as 53248 cycles of the RC oscillator, though other factors also impact on this timing.

To calculate a more exact timing, a deeper understanding of the operation of the time-out function is required. Upon completion of the power-on-reset (POR), the timer circuit will start counting down using the AC mains frequency as the clock.

This circuit will continue counting down on the AC mains frequency until four cycles of RC oscillation are received at the RC input (pin 5). At this point it will switch over to counting down using the RC oscillator.

Therefore, the first part of the timing is performed using the AC mains frequency, and the total effect of this on the time-out depends upon the relative frequency and phasing of the mains and RC clock signals. For most combinations of values, this will have very minimal effect on the time-out period, and can usually be ignored.

The RC oscillator input also has a four-times frequency multiplier internal to the IC, therefore a 60 Hz RC oscillation at pin 5 will result in a time-out of around 15 minutes, compared to 59 minutes for the same frequency AC mains clock.

Additionally, the last 16 cycles of the count are always performed from the AC mains clock frequency (f_{MAINS}).

A closer approximation of the time-out period (t_{TO}) using the RC oscillator for the IES5521A is therefore:

$$t_{TO} \approx \frac{212976}{4 \times f_{OSC}} + \frac{16}{f_{MAINS}} \quad (s)$$

6.8.3 Resetting the time-out condition

To reset the IES5521A from the time-out condition, AC power must be removed until such time as the external supply capacitor (C2, figure 5) is fully discharged. This constraint ensures that short term losses of power and "brown-outs", will not cause the timer to be undesirably reset.

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are specified with respect to pin 3 (V_{CC})

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EE}	Supply voltage range (V_{EE})	V_{1-3}	−7.6	+0.5	V
V_{AC}	Voltage range (AC)	V_{8-3}	−7.6	+0.5	V
V_{PWR}	Voltage range (PWR)	V_{7-3}	−7.6	+0.5	V
V_{CAP}	Voltage range (CAP)	V_{6-3}	V_1−0.8	+0.8	V
V_{SENS}	Voltage range (SENS)	V_{4-3}	−1.6	+0.8	V
V_{GATE}	Voltage range (GATE)	V_{2-3}	V_1−30	+50	V
V_{RC}	Voltage range (RC)	V_{5-3}	−7.6	+0.5	V
I	DC current (any pin)		−	20	mA
P_{tot}	total power dissipation		−	300	mW
T_{stg}	storage temperature		−40	+125	°C
T_{amb}	operating ambient temperature		−25	+100	°C

8 CHARACTERISTICS

At T_{amb} = 25°C; Voltages are specified with respect to pin 3 (V_{CC})

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Power supply						
$-V_{EE}$	supply voltage (operating)		6.3	6.9	7.6	V
$-I_{EE}$	supply current (operating)	excluding gate drive. 470kΩ pull-up on RC.	–	210	270	µA
Gate drive						
I_{GATE}	gate current (triac T1 to V_{CC})	$V_{GATE} = V_{CC}$	10	12.5	-	mA
Zero crossing detection						
I_{AC}	+ve threshold		–	66	–	µA
$-V_{AC}$	–ve threshold		–	–6.4	–	V
Timing capacitor						
$-I_{CAP}$	discharge current		–	1	2.2	µA
$-V_{UT}$	upper threshold		–	1100	–	mV
$-V_{LT}$	lower threshold		–	V_{EE}+1100	–	mV
I_{CAP}	charge current	I_{SENS} = –20 µA	–	150	–	µA
Sense input (Figure 4)						
$-V_{SENS}$	sense voltage	I_{SENS} = –20 µA	–	1000	–	mV
$-V_{SENS}$	sense voltage	duty cycle = 50%	–	575	–	mV
$-\Delta V_{SENS}/ ^oC$	temperature sensitivity		–	2.2	–	mV/°C
$V_{SENS(rms)}$	AC sense voltage	Duty cycle = 5%	–	0.47	–	$V_{(rms)}$
$V_{SENS(rms)}$	AC sense voltage	Duty cycle = 25%	–	0.48	–	$V_{(rms)}$
$V_{SENS(rms)}$	AC sense voltage	Duty cycle = 50%	–	0.50	–	$V_{(rms)}$
$V_{SENS(rms)}$	AC sense voltage	Duty cycle = 75%	–	0.53	–	$V_{(rms)}$
$V_{SENS(rms)}$	AC sense voltage	Duty cycle = 95%	–	0.65	–	$V_{(rms)}$
$V_{SENS(rms)}$	AC sense voltage	Duty cycle = 100%	–	0.73	–	$V_{(rms)}$
RC input (Figure 6)						
$-I_{RC}$	charging current	At RC pin	–	340	810	µA
$-V_{RCTU}$	RC threshold - upper		–	2.4	3.0	V
$-V_{RCTL}$	RC threshold - lower		0.4	0.6	–	V
f_{OSC}	oscillator frequency	R4=470k, C3=100nF	–	15.42	–	Hz
t_{TO}	time-out time, IES5521A	R4=470k, C3=100nF	–	3454	–	s
Mains Frequency Timing (R4=470k, Figure 5)						
t_{TO}	time-out time, IES5521A	f_{MAINS} = 60Hz	3550	–	3550	s
		f_{MAINS} = 50Hz	4260	–	4260	s

9 APPLICATION INFORMATION

9.1 Design considerations

Figure 5 shows a typical simple circuit for a load of greater than 400W. In this application the PWR pin is not used.

The power supply resistance of 160 kΩ sets the DC power supply current available for the operation of the circuit. When it is required to fire the triac the gate pulse width must be sufficiently long to ensure that the triac load current is greater than the latching current when the gate pulse is removed. Hence the need to specify a minimum operating load for this circuit. At the same time most of the operating DC current derived through the resistor is used in providing the gate signal, thereby putting a tight limit on the upper value of the width of the gate pulse. The width of the gate pulse is derived from the supply voltage and the instantaneous value of the current flowing through the power supply resistor.

In figure 6 an application circuit is shown for a 60W load, using the PWR pin as well as the AC input pin.

Using a BT134 600E triac for a 60W load on 220V means an 805Ω load. At 20mA latching current (positive), then the mains voltage for latching is 16V (with a margin use 20V) at a phase angle of 3.7 degrees. For 66μA in R3 when the mains voltage is 20V, then

$$R3 = 330k\Omega$$

The supply current at mains peak voltage in R3 is

$$(220 \times \sqrt{2})/(330k) = 943\mu A .$$

The negative latching current of the BT134 600E is –15mA, giving a mains voltage at this time of –15V. Thus when the mains voltage is –15V, from the ratio of R3 and R5, the voltage on pin AC must be –6V. Therefore R5 = 220kΩ, and the firing angle 2.8 degrees.

The gate pulse width is 6.5 degrees, with a duty cycle of 3.6%. That is 722μA average for a peak (cold plus margin) gate current of – 20mA.

Therefore the average current needed from the power supply is the sum of the average gate current ($I_{GATE\text{-}AVG}$), the maximum supply current (I_{EE}), the positive threshold current averaged over the two half cycles ($I_{AC\text{-}AVG}$), and the average current in the RC network ($V_{RCTU}/R4$) :

$$722 + 270 + \frac{66}{2} + \frac{3.0}{470k} = 1071\mu A$$

Of this $943/\pi = 300\mu A$ is supplied via R3, so R6 must supply a further 768 μA average through the PWR pin. Therefore R6 is

$$220/(771 \times \pi) = 91k\Omega$$

A number of important characteristics of the triac are temperature sensitive. It is essential that the controlling integrated circuit exhibits comparable sensitivity to temperature change so that its characteristics vary in the same way as those of the triac, ensuring proper triggering over the full operating range.

9.2 Negative half cycle

A typical triac has a maximum latching current for the negative half cycle of 25 mA. If the gate pulse is terminated when the supply voltage falls below –6 volts, the minimum load can be calculated for which the holding current is reached before the supply voltage falls to this value. However, with the addition of resistors to V_{EE} and V_{CC} from the AC pin, other threshold voltages can be achieved, allowing other loads.

9.3 Positive half cycle

A typical positive half cycle latching current is 35 mA. Considering chip resistor tolerances, and from the value of the mains power supply resistor of 160 kΩ in figure 5 the end of the gate pulse can be calculated using the threshold current of nominally 66 μA where the gate drive is turned off.

9.4 Gate current

In assuming a triac gate current of 10 mA minimum an on chip margin has to be allowed for component tolerances, and a suitable variation with ambient temperature. Also it must be realised that most of the supply current is used in providing the gate current.

Thus in characterising the IES5521A the design has taken into account the availability of suitably sensitive triacs, and used this to employ design figures enabling operation in specific applications with minimum external component count, and yet ensuring reliable triggering and proper operation over normal operating temperature and supply voltage conditions.

9.5 Temperature sensing

The application circuit in figure 6 is the simplest configuration in which a negative temperature coefficient (NTC) thermistor or another resistive sensing element can be used. Note that at the low temperature end of the potentiometer travel no sensing signal is available at all. However simple resistor networks are usually needed to linearise the response of the setting resistor against control temperature, and can easily be designed to allow for maximum and minimum operating points. Alternatively these might be set mechanically by stops inherent in the mechanical construction of the product using the IES5521A.

Some applications require more accurate control over a limited temperature range; for example the control of fish tank heaters or water

bed thermostats. Use of an input bridge circuit with gain will permit greater accuracy, and exhibit less ambient temperature dependence (for example by using one external transistor). These circuits still use an AC sensing circuit, and therefore do not provide any additional loading on the DC power supply.

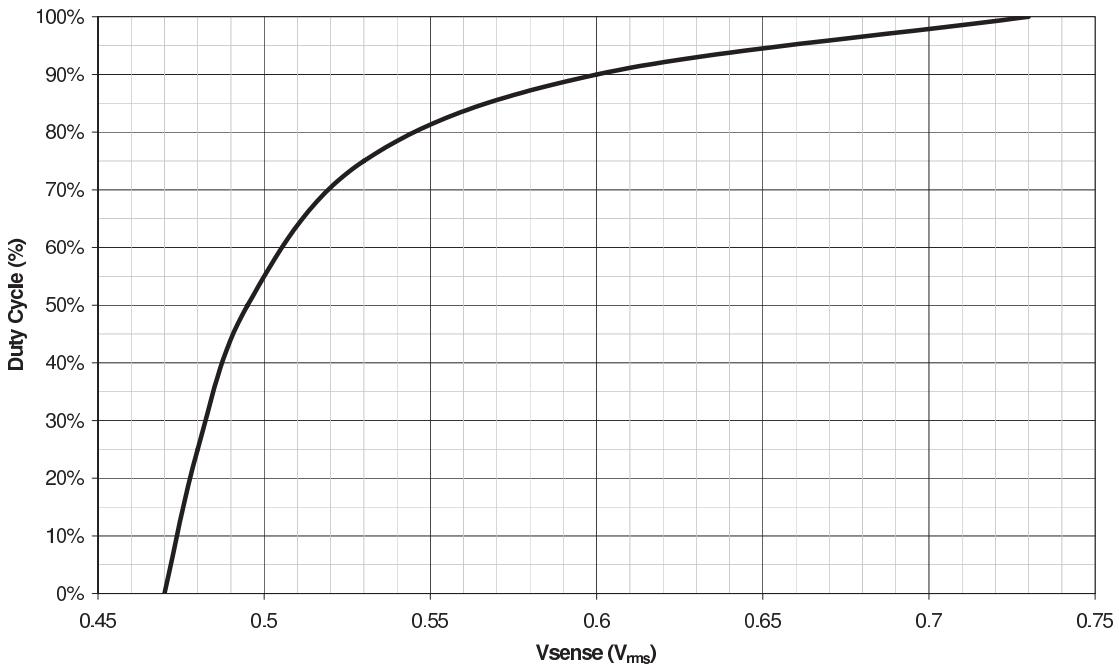

Fig.4 Duty Cycle versus Vsense

9.6 Application circuits

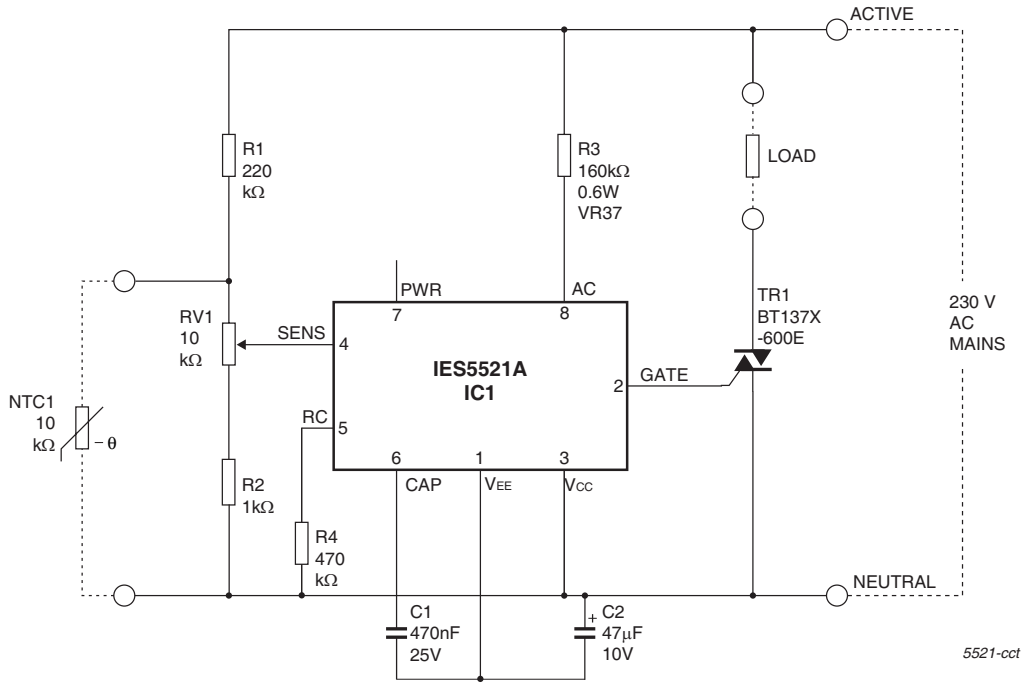

Fig.5 IES5521A application diagram: 400 W resistive heating load, referenced to mains, with fixed time-out period

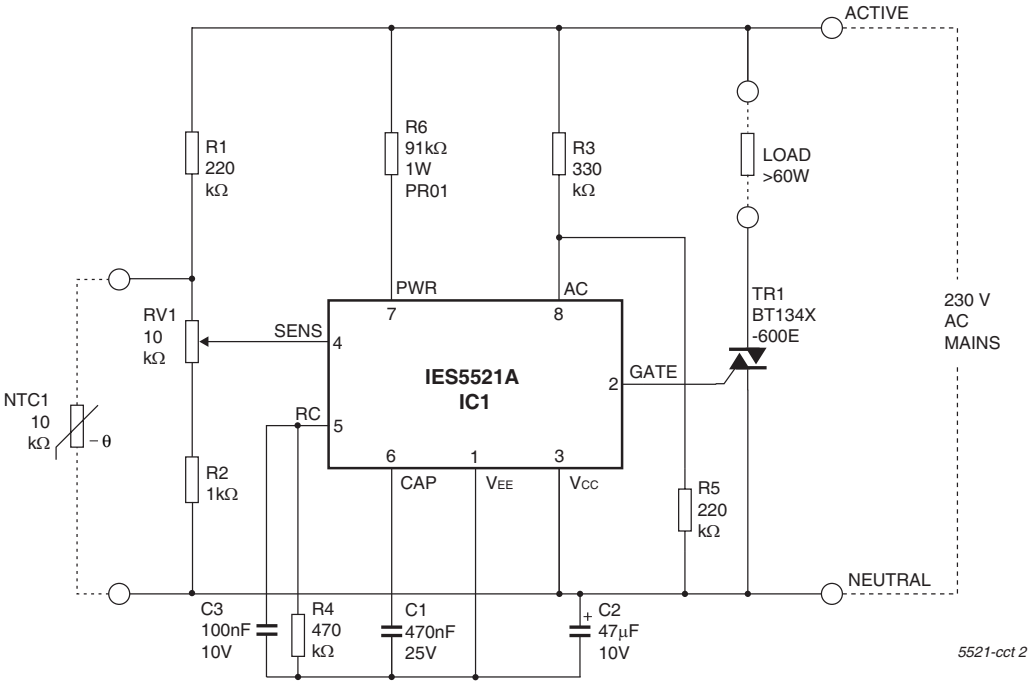

Fig.6 IES5521A application diagram: 60W resistive heating load, with time-out period set by RC components

10 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	NAME	DESCRIPTION	VERSION	ROHS
IES5521A P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1	Yes
IES5521A T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1	Yes

For more information on packages, please refer to the document “Integrated Circuit Packaging and Soldering Information”, available from Integrated Electronic Solutions.

Other package options are available. Contact Integrated Electronic Solutions for details.

11 ESD CAUTION

Electrostatic Discharge (ESD) sensitive device. ESD can cause permanent damage or degradation in the performance of this device. This device contains ESD protection structures aimed at minimising the impact of ESD. However, it is the users responsibility to ensure that proper ESD precautions are observed during the handling, placement and operation of this device.

12 DOCUMENT HISTORY

REVISION	DATE	DESCRIPTION
1.0	20051212	Product Release
0.2	20060901	HS formatting & ESD caution

13 DEFINITIONS

Data sheet status	
Engineering sample information	This contains draft information describing an engineering sample provided to demonstrate possible function and feasibility.Engineering samples have no guarantee that they will perform as described in all details.
Objective specification	This data sheet contains target or goal specifications for product development. Engineering samples have no guarantee that they will function as described in all details.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later. Products to this data may not yet have been fully tested, and their performance fully documented.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

14 COMPANY INFORMATION

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