Document Number: AFT23H200−4S2L
Rev. 1, 5/2013

RoHS

RF Power LDMOS Transistor

N−Channel Enhancement−Mode Lateral MOSFET

This 45 watt asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 2300 to 2400 MHz.

- Typical Doherty Single−Carrier W−CDMA Performance: V_{DD} = 28 Volts, I_{DQA} = 500 mA, V_{GSB} = 0.5 Vdc, P_{out} = 45 Watts Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

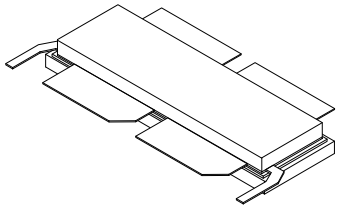
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2300 MHz	15.3	42.8	8.4	−27.6
2350 MHz	15.4	43.3	8.3	−31.1
2400 MHz	15.2	42.8	8.3	−33.9

Features

- Advanced High Performance In−Package Doherty
- Greater Negative Gate−Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- In Tape and Reel. R6 Suffix = 150 Units, 56 mm Tape Width, 13−inch Reel.

AFT23H200−4S2LR6

2300−2400 MHz, 45 W AVG., 28 V



NI−1230−4LS2L

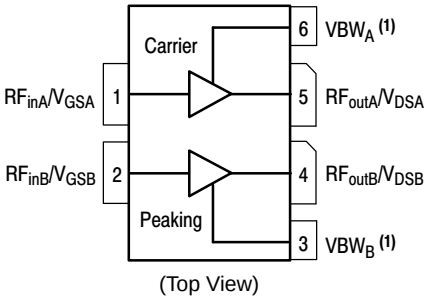


Figure 1. Pin Connections

1. Device cannot operate with the V_{DD} current supplied through pin 3 and pin 6.

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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	−0.5, +65	Vdc
Gate−Source Voltage	V_{GS}	−6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Case Operating Temperature Range	T_C	−40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	−40 to +225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	294 1.7	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 75°C, 45 W W−CDMA, 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.5 Vdc, 2350 MHz	$R_{\theta JC}$	0.32	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22−A114)	2
Machine Model (per EIA/JESD22−A115)	B
Charge Device Model (per JESD22−C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate−Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics − Side A (4) (Carrier)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 140 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DA} = 500 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.4	1.8	2.2	Vdc
Drain−Source On−Voltage (V_{GS} = 6 Vdc, I_D = 1.4 Adc)	$V_{DS(on)}$	0.1	0.14	0.4	Vdc
On Characteristics − Side B (4) (Peaking)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain−Source On−Voltage (V_{GS} = 6 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	0.1	0.14	0.4	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes − AN1955.
4. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2,3) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.5 Vdc, P_{out} = 45 W Avg., f = 2300 MHz, Single−Carrier W−CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	14.6	15.3	17.6	dB
Drain Efficiency	η_D	38.0	42.8	—	%
Output Peak−to−Average Ratio @ 0.01% Probability on CCDF	PAR	7.6	8.4	—	dB
Adjacent Channel Power Ratio	ACPR	—	−27.6	−25.0	dBc
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQA} = 500 mA, f = 2350 MHz					
VSWR 10:1 at 32 Vdc, 330 W CW (4) Output Power (3 dB Input Overdrive from 200 W CW (4) Rated Power)	No Device Degradation				
Typical Performances (2) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.5 Vdc, 2300−2400 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	210 (4)	—	W
P_{out} @ 3 dB Compression Point (5)	P3dB	—	290	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2300−2400 MHz frequency range)	Φ	—	34	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	150	—	MHz
Gain Flatness in 100 MHz Bandwidth @ P_{out} = 45 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (−30°C to +85°C)	ΔG	—	0.007	—	dB/°C
Output Power Variation over Temperature (−30°C to +85°C) (4)	ΔP1dB	—	0.002	—	dB/°C

1. Part internally matched both on input and output.
2. V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.
3. Measurements made with device in an asymmetrical Doherty configuration.
4. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
5. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W−CDMA single−carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

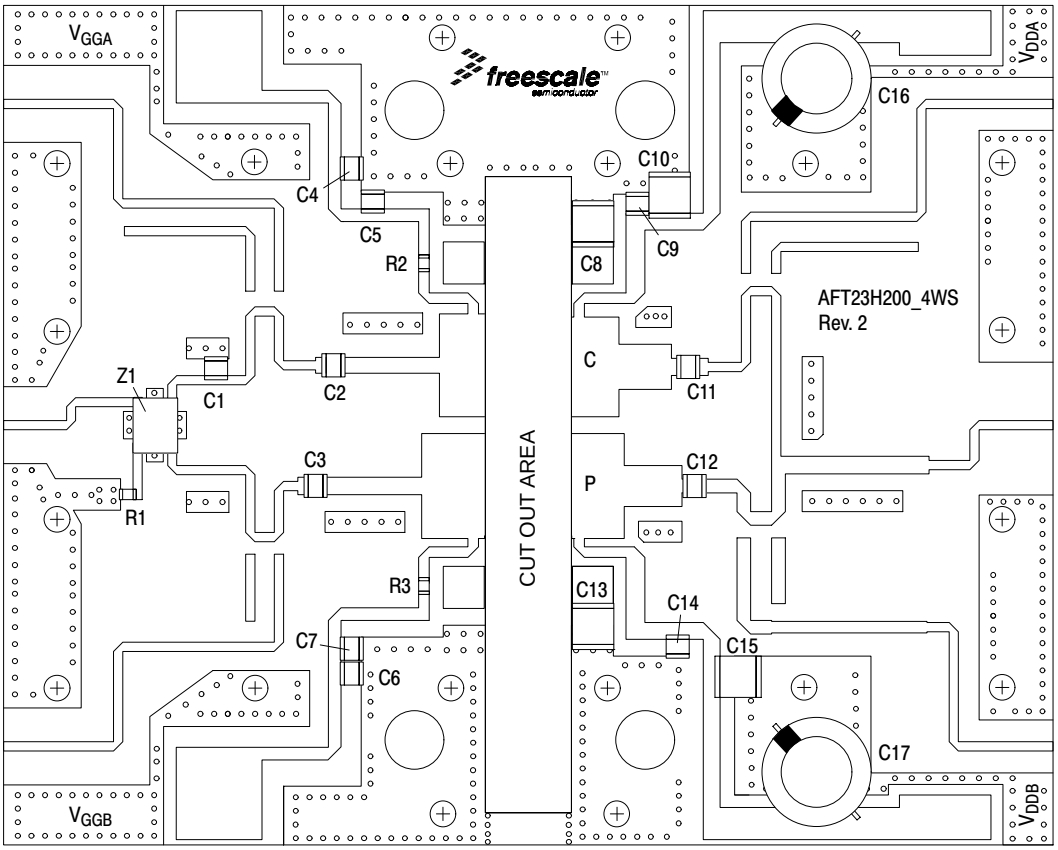


Figure 2. AFT23H200−4S2LR6 Test Circuit Component Layout

Table 5. AFT23H200−4S2LR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
C2, C3, C5, C7, C9, C12, C14	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C4, C6	2.2 μF Chip Capacitors	GRM55DR72H225KA88L	Murata
C8, C10, C13, C15	10 μF Chip Capacitors	GRM55DR61H106KA88L	Murata
C11	5.1 pF Chip Capacitor	ATC100B5R1CT500XT	ATC
C16, C17	220 μF, 50 V Electrolytic Capacitors	MVY50VC221MJ10TP	United Chem
R1	50 Ω, 10 W Chip Resistor	060120A15Z50−2	Anaren
R2, R3	2.7 Ω, 1/16 W Chip Resistors	CR10-120J-B	Kyocera
Z1	2300−2700 MHz Band, 90°, 3 dB Hybrid Coupler	X3C25P1-05S	Anaren
PCB	0.020″, ε_r = 3.5	RO4350B	Rogers

TYPICAL CHARACTERISTICS

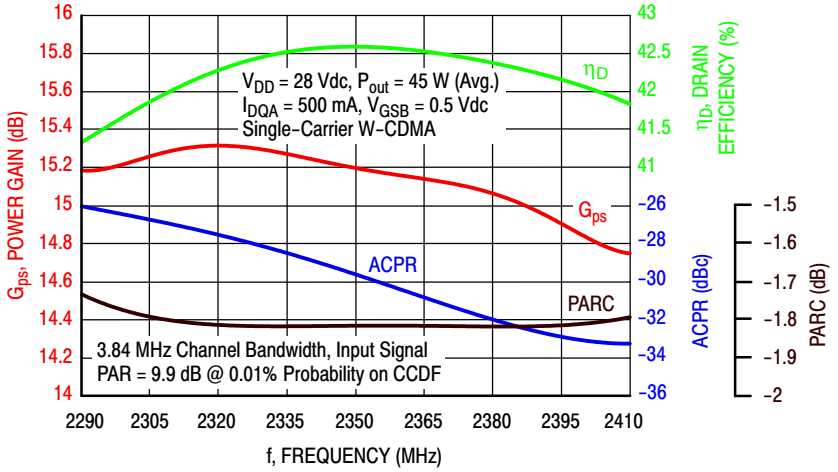


Figure 3. Single−Carrier Output Peak−to−Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 45 Watts Avg.

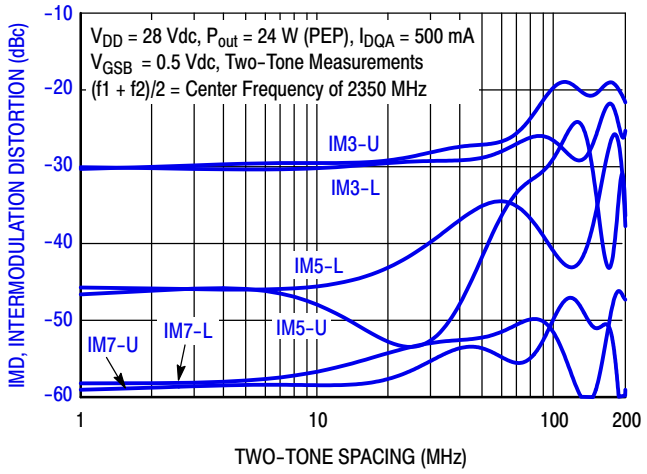


Figure 4. Intermodulation Distortion Products versus Two−Tone Spacing

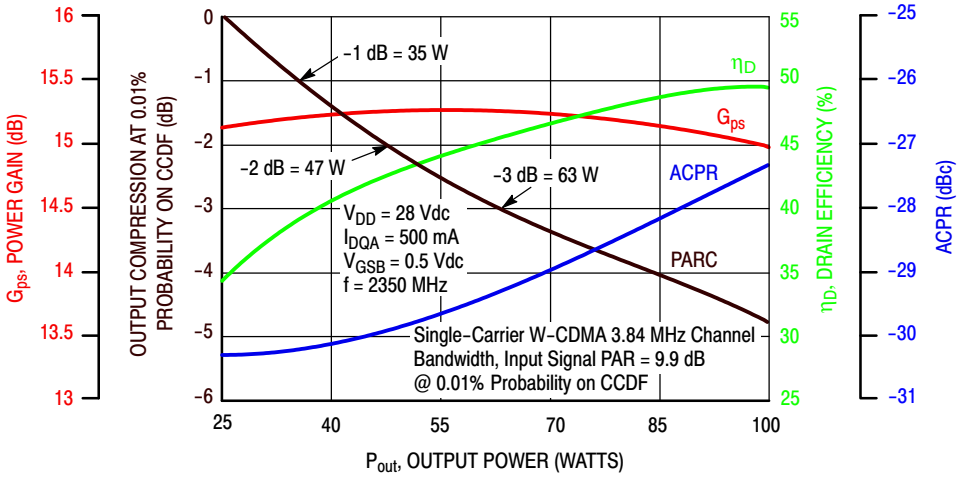


Figure 5. Output Peak−to−Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

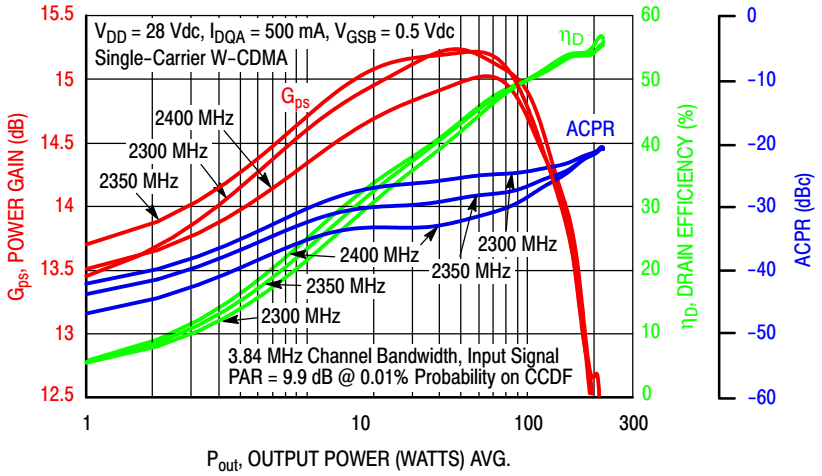


Figure 6. Single−Carrier W−CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

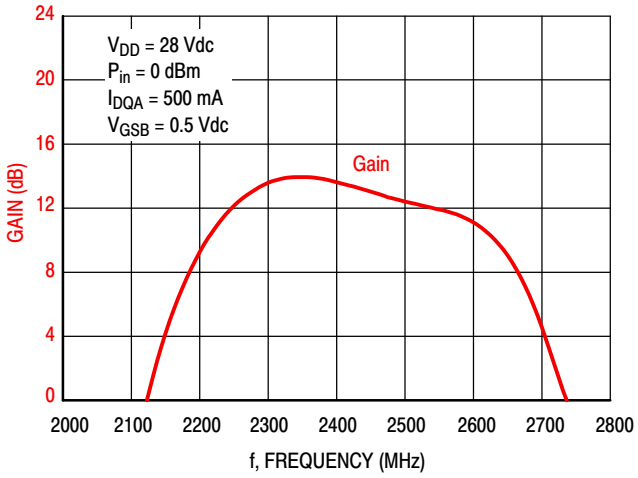


Figure 7. Broadband Frequency Response

V_{DD} = 28 Vdc, I_{DQA} = 734 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	4.98 - j10.2	5.10 + j9.68	2.07 - j3.84	18.4	51.9	154	57.8	-12
2350	8.15 - j11.4	7.40 + j10.5	2.02 - j3.81	18.4	51.8	153	57.3	-13
2400	12.1 - j11.3	11.0 + j10.5	1.89 - j3.59	18.3	51.8	153	56.7	-13

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	4.98 - j10.2	5.13 + j10.4	1.89 - j3.98	16.1	52.7	186	58.3	-17
2350	8.15 - j11.4	7.86 + j11.5	1.83 - j4.03	16.0	52.6	184	57.4	-17
2400	12.1 - j11.3	12.4 + j11.6	1.78 - j3.84	16.1	52.6	183	57.2	-18

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 8. Carrier Side Load Pull Performance — Maximum Power Tuning

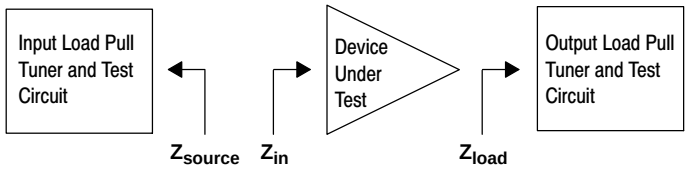
V_{DD} = 28 Vdc, I_{DQA} = 734 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	4.98 - j10.2	5.15 + j10.1	4.33 - j3.62	20.4	50.4	110	65.8	-17
2350	8.15 - j11.4	7.45 + j11.2	3.92 - j2.92	20.3	50.5	113	65.8	-18
2400	12.1 - j11.3	11.4 + j11.0	3.72 - j2.68	20.3	50.4	111	65.5	-18

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	4.98 - j10.2	5.00 + j10.7	3.99 - j3.52	18.2	51.3	136	66.6	-24
2350	8.15 - j11.4	7.58 + j12.1	3.77 - j2.92	18.2	51.2	133	66.3	-25
2400	12.1 - j11.3	12.3 + j12.3	3.44 - j2.68	18.2	51.3	134	66.1	-26

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 9. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning



V_{DD} = 28 Vdc, V_{GSB} = 1.8 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	4.16 - j8.18	3.52 + j7.55	2.12 - j4.32	17.5	53.0	200	54.8	-11
2350	6.03 - j8.44	4.66 + j8.11	2.09 - j4.32	17.7	53.0	201	55.0	-11
2400	8.93 - j7.56	6.30 + j8.25	2.07 - j4.25	17.8	53.0	201	55.0	-11

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	4.16 - j8.18	3.48 + j8.04	2.02 - j4.65	15.2	53.8	242	55.8	-15
2350	6.03 - j8.44	4.76 + j8.79	2.00 - j4.52	15.5	53.8	241	55.8	-15
2400	8.93 - j7.56	6.76 + j9.07	2.02 - j4.47	15.5	53.8	239	55.5	-16

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 10. Peaking Side Load Pull Performance — Maximum Power Tuning

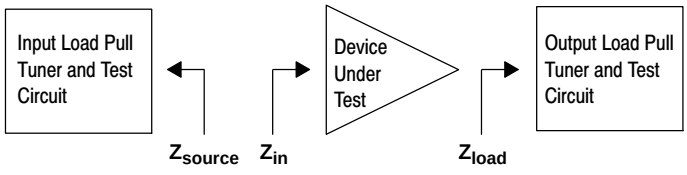
V_{DD} = 28 Vdc, V_{GSB} = 1.8 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	4.16 - j8.18	3.44 + j7.85	4.02 - j2.94	19.5	51.7	148	63.4	-16
2350	6.03 - j8.44	4.63 + j8.38	3.77 - j2.78	19.7	51.7	147	63.7	-17
2400	8.93 - j7.56	6.25 + j8.53	3.29 - j2.37	19.8	51.5	142	63.7	-18

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	4.16 - j8.18	3.31 + j8.22	3.97 - j3.19	17.4	52.5	176	64.4	-22
2350	6.03 - j8.44	4.53 + j8.99	3.45 - j2.78	17.6	52.4	175	64.6	-24
2400	8.93 - j7.56	6.50 + j9.33	3.17 - j2.43	17.8	52.2	166	64.2	-25

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 11. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning



P1dB − TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2350 MHz

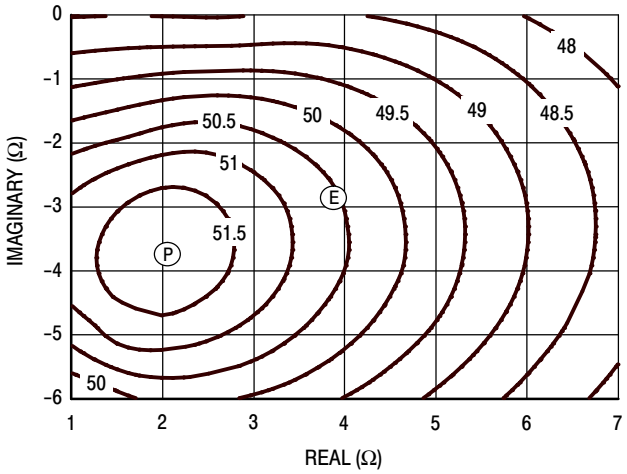


Figure 12. P1dB Load Pull Output Power Contours (dBm)

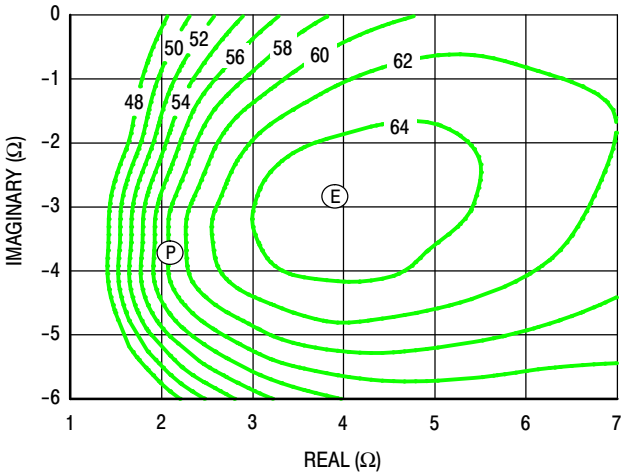


Figure 13. P1dB Load Pull Efficiency Contours (%)

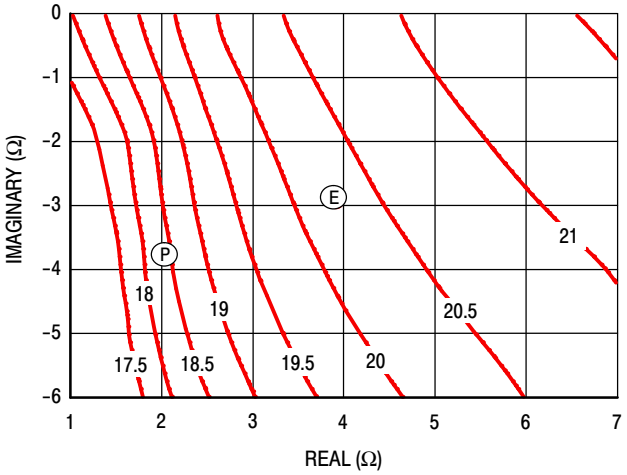


Figure 14. P1dB Load Pull Gain Contours (dB)

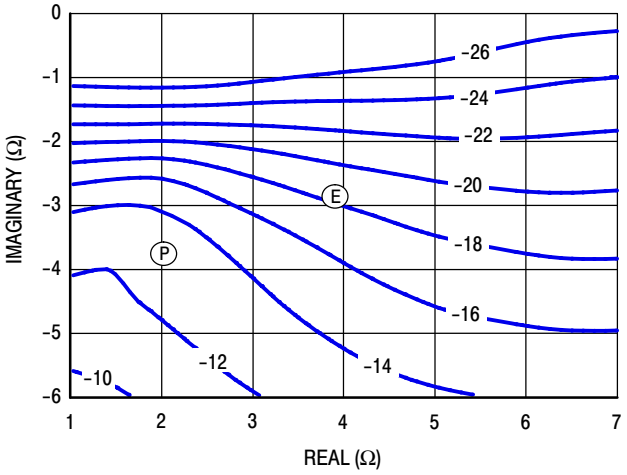


Figure 15. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain

Drain Efficiency

Linearity

Output Power

P3dB − TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2350 MHz

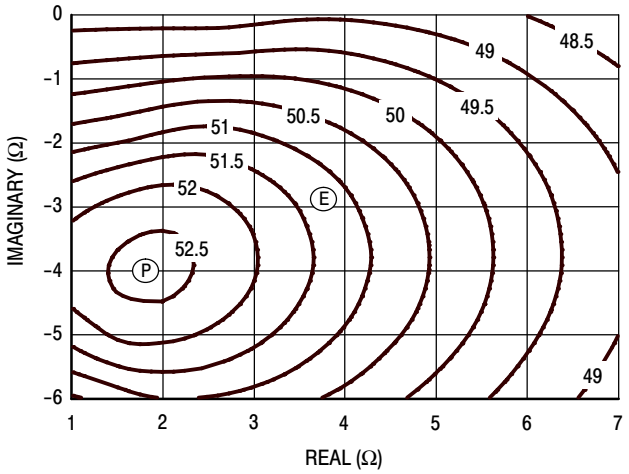


Figure 16. P3dB Load Pull Output Power Contours (dBm)

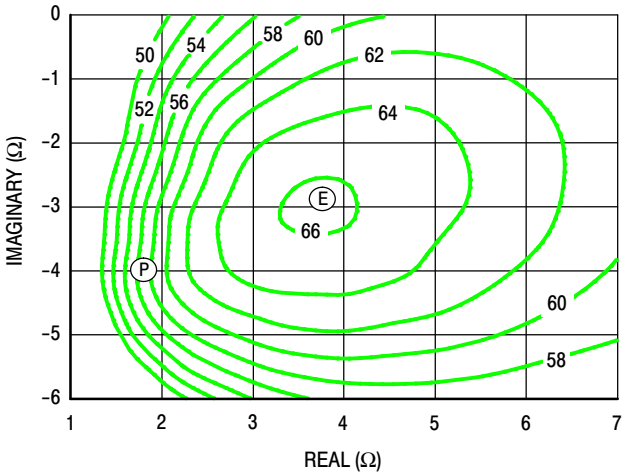


Figure 17. P3dB Load Pull Efficiency Contours (%)

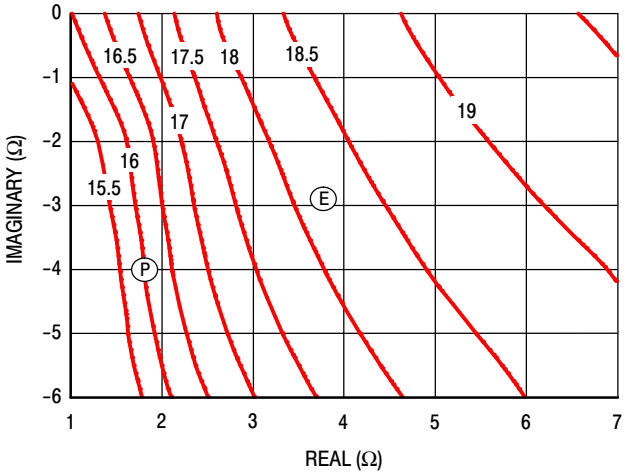


Figure 18. P3dB Load Pull Gain Contours (dB)

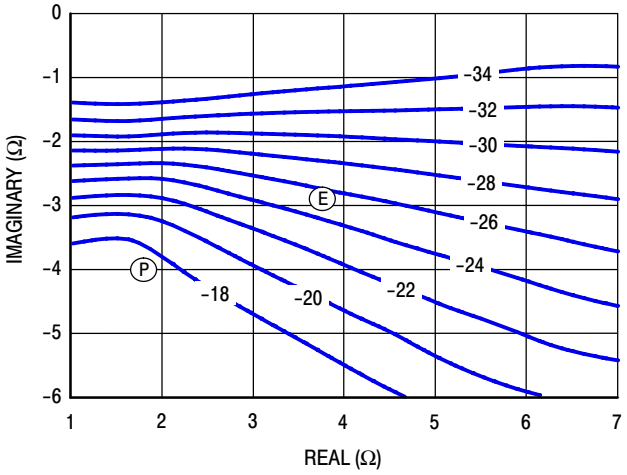


Figure 19. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain

Drain Efficiency

Linearity

Output Power

P1dB − TYPICAL PEAKING LOAD PULL CONTOURS — 2350 MHz

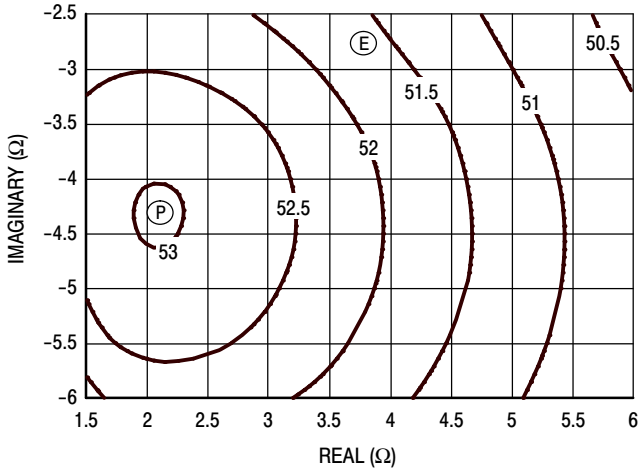


Figure 20. P1dB Load Pull Output Power Contours (dBm)

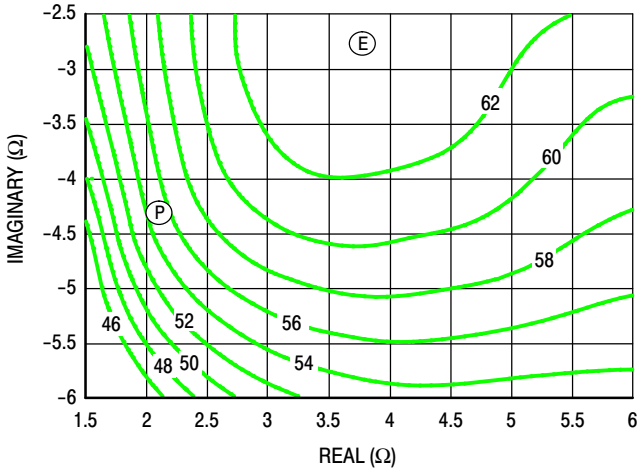


Figure 21. P1dB Load Pull Efficiency Contours (%)

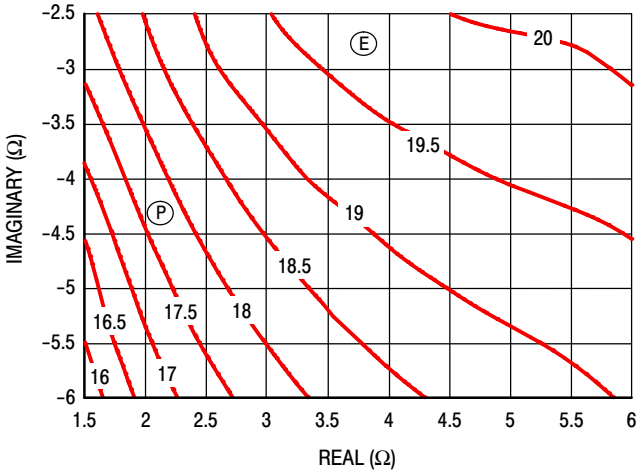


Figure 22. P1dB Load Pull Gain Contours (dB)

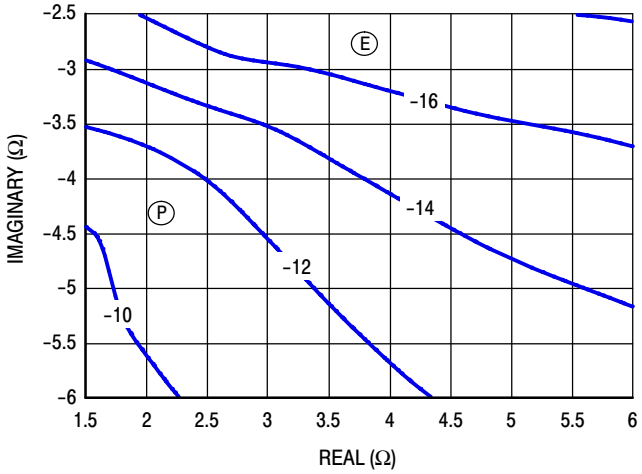


Figure 23. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain

Drain Efficiency

Linearity

Output Power

P3dB − TYPICAL PEAKING LOAD PULL CONTOURS — 2350 MHz

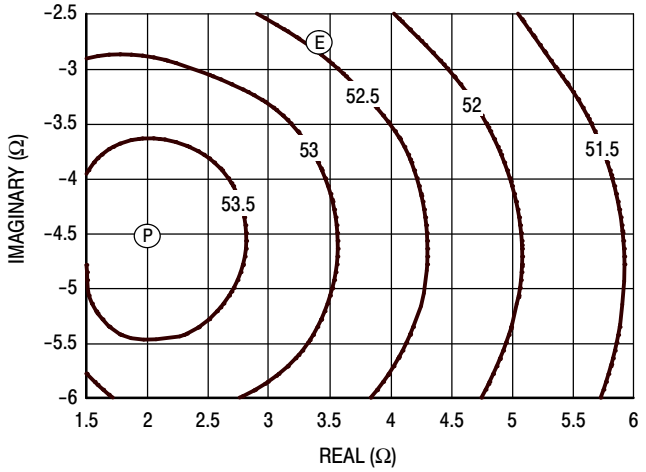


Figure 24. P3dB Load Pull Output Power Contours (dBm)

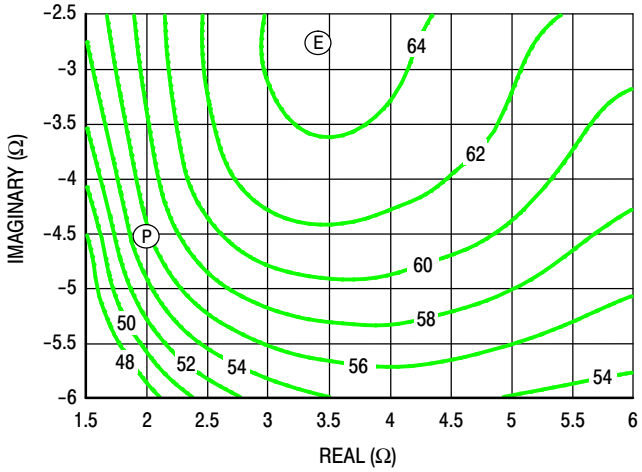


Figure 25. P3dB Load Pull Efficiency Contours (%)

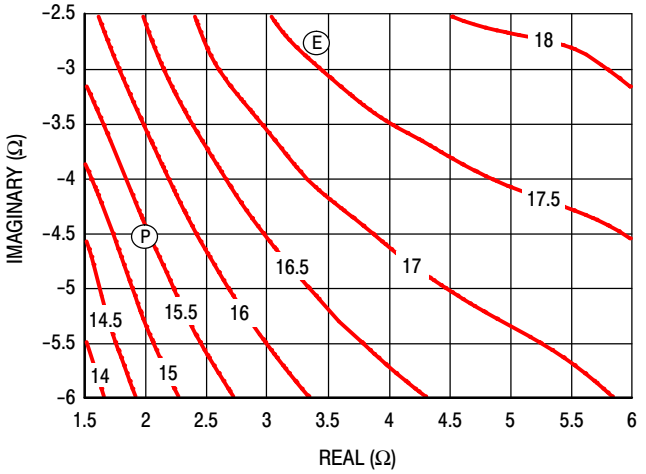


Figure 26. P3dB Load Pull Gain Contours (dB)

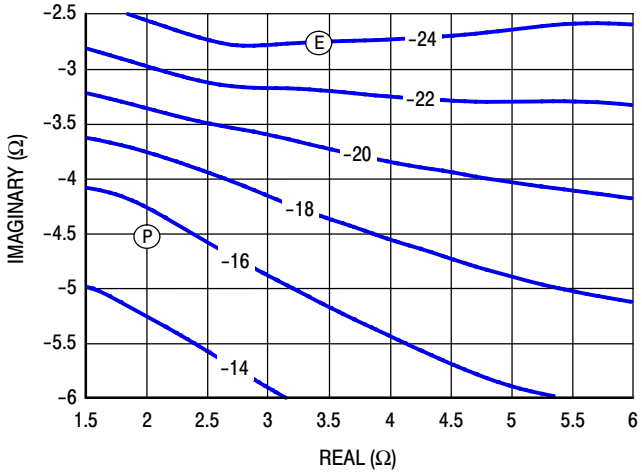


Figure 27. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

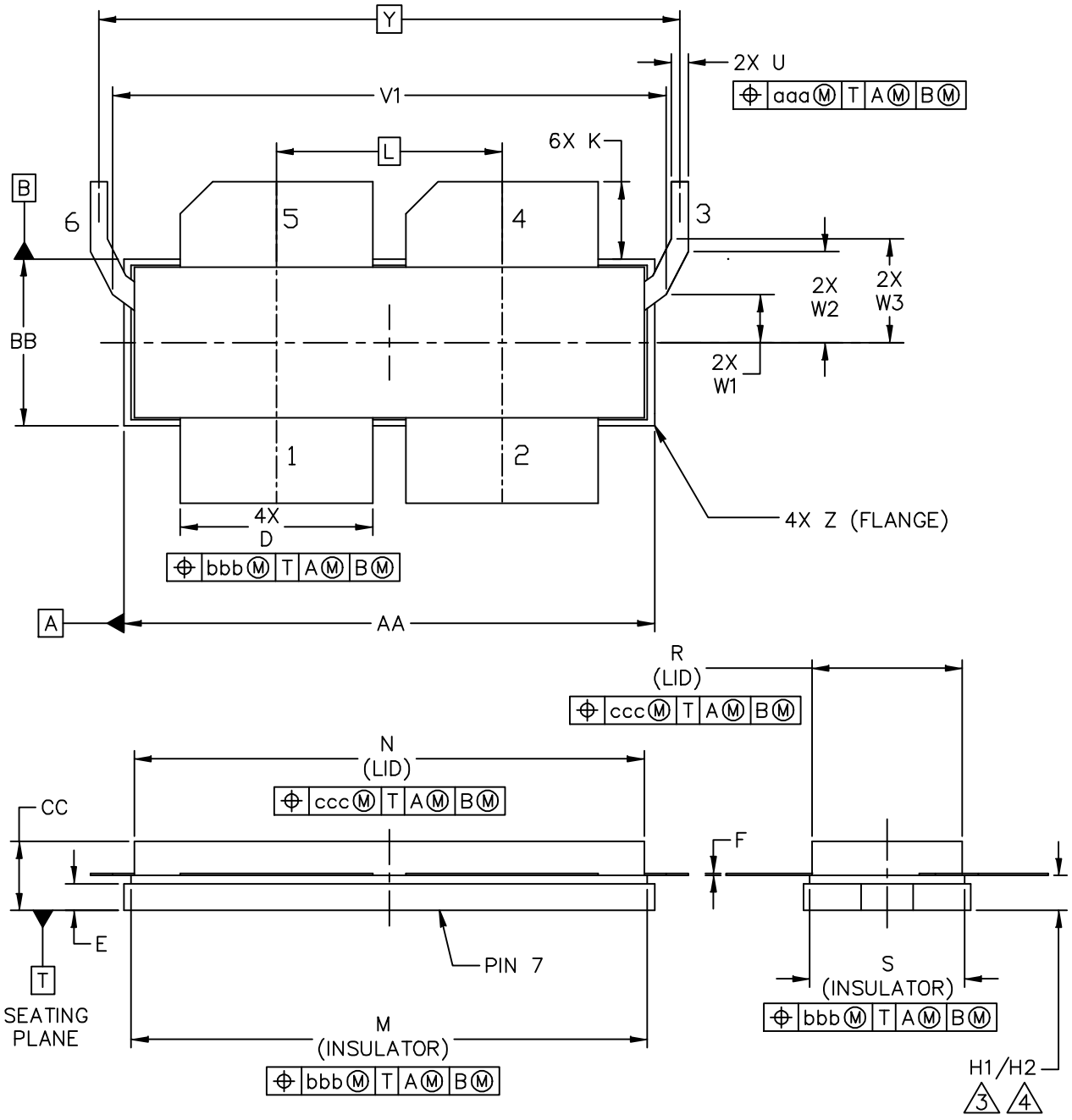
Power Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE AND COULD CHANGE ONCE SUFFICIENT MANUFACTURING DATA IS AVAILABLE.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	1.265	1.275	32.13	32.39	N	1.218	1.242	30.94	31.55
BB	.395	.405	10.03	10.29	R	.365	.375	9.27	9.53
CC	.170	.190	4.32	4.83	S	.365	.375	9.27	9.53
D	.455	.465	11.56	11.81	U	.035	.045	0.89	1.14
E	.062	.066	1.57	1.68	V1	1.320	1.330	33.53	33.78
F	.004	.007	0.10	0.18	W1	.110	.120	2.79	3.05
H1	.082	.090	2.08	2.29	W2	.213	.223	5.41	5.66
H2	.078	.094	1.98	2.39	W3	.243	.253	6.17	6.43
K	.175	.195	4.45	4.95	Y	1.390 BSC		35.31 BSC	
L	.540 BSC		13.72 BSC		Z	R.000	R.040	R0.00	R1.02
M	1.219	1.241	30.96	31.52	aaa	.015		0.38	
					bbb	.010		0.25	
					ccc	.020		0.51	

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2013	• Initial Release of Data Sheet
1	May 2013	• On Characteristics tables: Gate threshold voltage, $V_{GS(th)}$, updated to reflect actual test condition, V_{DS} = 10 Vdc, p. 2

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