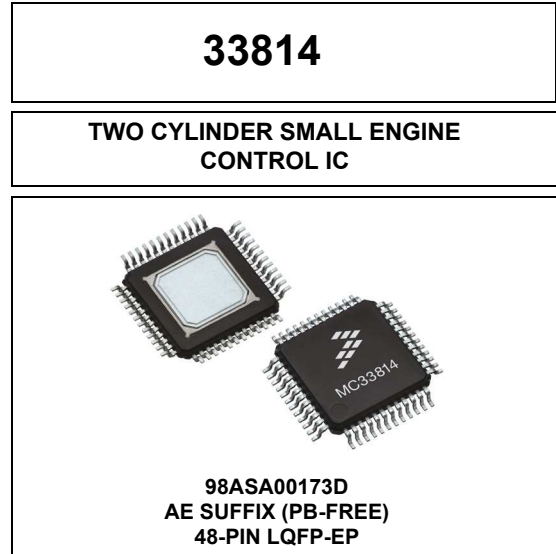


Two Cylinder Small Engine Control IC

The 33814 is an engine control analog power IC intended for two cylinder motorcycle and other small engine control applications. The IC consists of six integrated low side drivers, three pre-drivers, a Variable Reluctance Sensor (VRS) input circuit, a voltage pre-regulator using an external pass transistor, and two 5 volt internal regulators, one for the microcontroller unit (MCU) VCC supply, and one for use as a protected sensor supply. Also included is an MCU reset control circuit with watchdog, an ISO 9141 K-Line interface for diagnostic communication and a Serial Peripheral Interface (SPI). The six low side drivers are intended for driving two fuel injectors, a lamp, two relays or other loads, and a tachometer. The pre-drivers are intended to drive IGBT or MOSFET transistors to control ignition coils, and a HEGO heater. The device is packaged in a 48 pin LQFP-EP with an exposed pad.

Features:

- Operates over supply voltage range of $4.5\text{ V} \leq V_{PWR} \leq 36\text{ V}$
- Logic stability guaranteed down to 2.5 V
- Two fuel injector drivers - typical of 1.3 A each
- Two ignition IGBT or general purpose gate pre-drivers
- One O2 sensor (HEGO) heater general purpose gate pre-driver
- Relay 1 driver, typically 2.0 A, can be used for fuel pump control
- Relay 2 driver, typically 1.0 A, can be used as power relay control
- Lamp driver, typically 1.0 A can also be used to drive an LED
- V_{PROT} protected sensor supply tracks $V_{CC} + 5.0\text{ V}$ regulator
- MCU reset generator - system integrity monitor (watchdog)
- V_{PP} pre-regulator provides power for V_{CC} and V_{PROT} regulators
- Independent fault protection with all faults reported via the SPI
- ISO 9141 K-line interface for communicating diagnostic messages
- Start-up/shut-down control and power sequence logic
- Interfaces directly to MCU using a 5.0 V SPI and logic I/O
- Differential/single-ended VRS conditioning circuit with auto/manual selected thresholds and filter times with digital and tachometer outputs



Applications:

Small Engine Control for:

- Lawn Mowers
- Motor Scooters
- Small Motorcycles
- Lawn Trimmers
- Snow Blowers
- Chain Saws
- Gasoline-driven Electrical Generators
- Outboard Motors

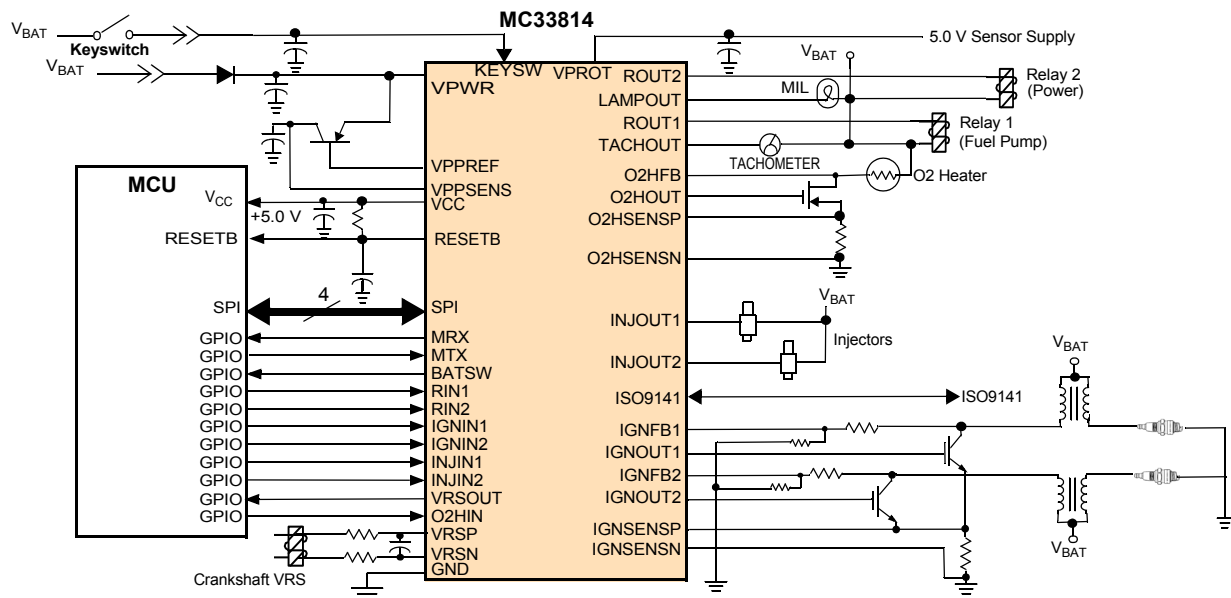


Figure 1. 33814 Simplified Application Diagram

* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

1 Orderable Parts

Table 1. Orderable Part Variations

| Part Number ⁽¹⁾ | Notes | Temperature (T _A) | Package |
|----------------------------|-------|-------------------------------|------------|
| MC33814AE | | -40 to 125 °C | 48 LQFP-EP |

Notes

1. To Order parts in Tape & Reel, add the R2 suffix to the part number.

Table of Contents

| | | |
|-----|---|----|
| 1 | Orderable Parts | 2 |
| 2 | Internal Block Diagram | 4 |
| 3 | Pin Connections | 5 |
| 3.1 | Pinout Diagram | 5 |
| 3.2 | Pin Definitions | 5 |
| 4 | General Product Characteristics | 8 |
| 4.1 | Maximum Ratings | 8 |
| 4.2 | Static Electrical Characteristics | 10 |
| 4.3 | Dynamic Electrical Characteristics | 15 |
| 4.4 | Timing Diagrams | 17 |
| 4.5 | Typical Electrical Characteristics | 18 |
| 5 | General IC Functional Description and Application Information | 20 |
| 5.1 | Functional Pin Description | 20 |
| 5.2 | MCU SPI Interface Description | 31 |
| 5.3 | Functional Device Operation | 32 |
| 6 | Typical Applications | 44 |
| 7 | Packaging | 45 |
| 7.1 | Package Mechanical Dimensions | 45 |
| 8 | Revision History | 49 |

2 Internal Block Diagram

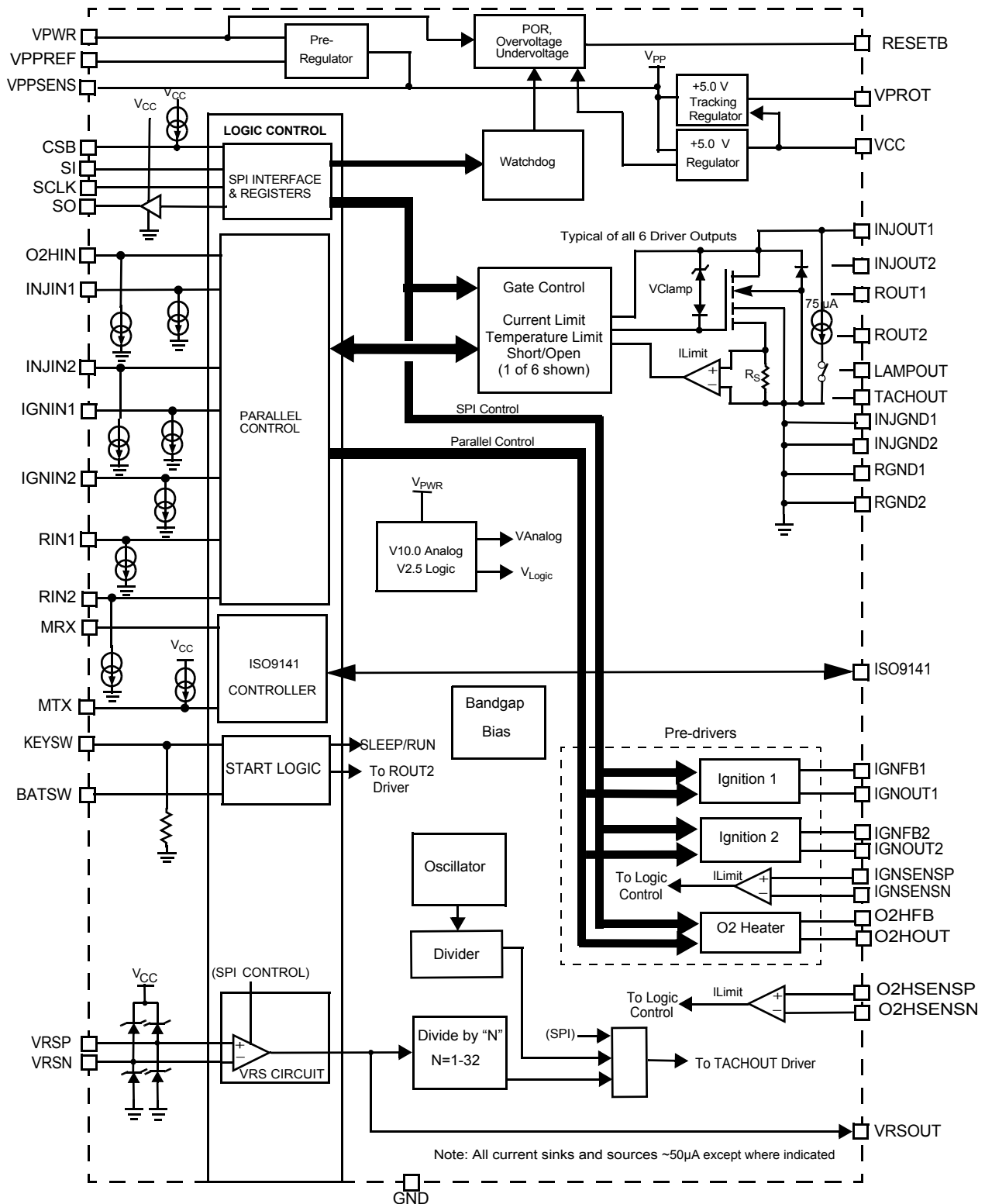


Figure 2. Simplified Internal Block Diagram

3 Pin Connections

3.1 Pinout Diagram

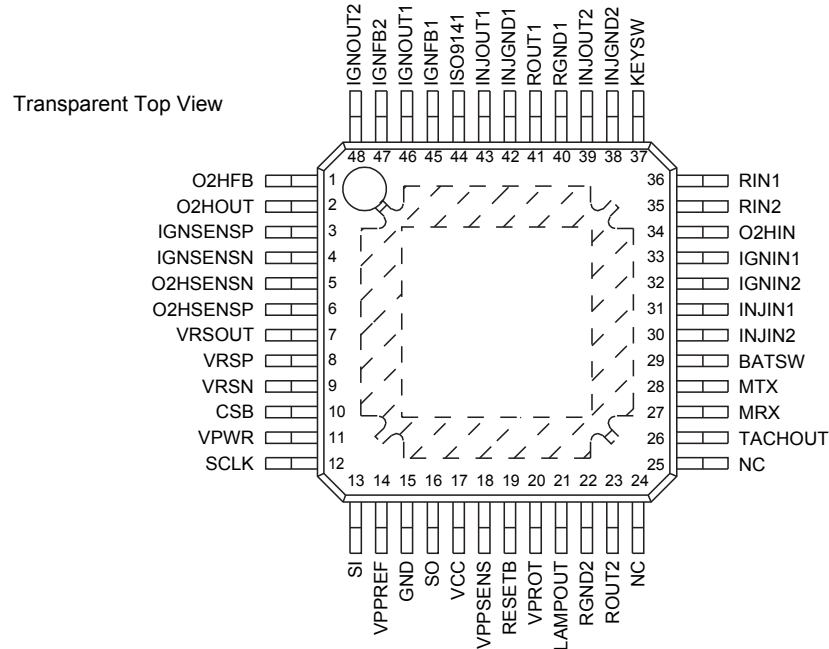


Figure 3. 33814 Pin Connections

3.2 Pin Definitions

Table 2. 33814 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page [20](#).

| Pin | Pin Name | Pin Function | Formal Name | Description |
|-----|----------|--------------|--|---|
| 1 | O2HFB | Input | O2 Sensor Heater Feedback Input | Voltage feedback from drain of O2 Sensor Heater driver FET |
| 2 | O2HOUT | Output | O2 Sensor Heater Output | Pre-driver output for O2 Sensor Heater driven by SPI input or O2HIN pin |
| 3 | IGNSENSP | Input | Ignition Current Sense Input Positive | Positive input to the ignition current sense differential amplifier Used to measure current in IGBT emitter resistor for IGNOUT1 and IGNOUT2, if used. |
| 4 | IGNSNSN | Input | Ignition Current Sense Input Negative | Negative input to the ignition current sense differential amplifier Used to measure current in IGBT emitter resistor for IGNOUT1 and IGNOUT2, if used |
| 5 | O2HSENSN | Input | O2 Heater Current Sense Input Negative | Negative input to the O2 heater current sense differential amplifier Used to measure current in of O2 heater driver MOSFET source resistor, if used. |

Table 2. 33814 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page [20](#).

| Pin | Pin Name | Pin Function | Formal Name | Description |
|-----|----------|--------------|---|---|
| 6 | O2HSENSP | Input | O2 Heater Current Sense Input Positive | Positive input to the O2 heater current sense differential amplifier Used to measure current in of O2 heater driver MOSFET source resistor, if used. |
| 7 | VRSOUT | Output | VRS Conditioned Output | 5.0 V Logic Level Output from conditioned VRS differential inputs VRSP, VRSN |
| 8 | VRSP | Input | Variable Reluctance Sensor Positive Input | The VRSP and VRSN form a differential input for the Variable Reluctance Sensor attached to the crankshaft toothed wheel. |
| 9 | VRSN | Input | Variable Reluctance Sensor Negative Input | The VRSP and VRSN form a differential input for the Variable Reluctance Sensor attached to the crankshaft toothed wheel. |
| 10 | CSB | Input | SPI Chip Select | The Chip Select input pin is an active low signal sent by the MCU to indicate that the device is being addressed. |
| 11 | VPWR | Supply Input | Main Voltage Supply Input | VPWR is the main voltage supply input for the device. Connected to a 12 Volt battery (Should have reverse battery protection and adequate transient protection.) |
| 12 | SCLK | Input | SPI Clock Input | The SCLK input pin is used to clock in and out the serial data on the SI and SO pins while being addressed by the CSB. |
| 13 | SI | Input | SPI Data Input | The SI input pin is used to receive serial data into the device from the MCU. |
| 14 | VPPREF | Output | VPP Reference Base Drive | Base drive for external PNP pass transistor |
| 15 | GND | Ground | Ground | Ground pin, return for all voltage supplies |
| 16 | SO | Output | SPI Data Output | The SO output pin is used to transmit serial data from the device to the MCU. |
| 17 | VCC | Supply | VCC Supply Protected Output | 5.0 Volt supply output for MCU V _{CC} . This output supplies the V _{CC} voltage for 5.0 Volt MCUs. It is short-circuit and overcurrent protected. |
| 18 | VPPSENS | Input | Voltage Sense from VPP | Feedback to internal V _{PP} 6.5 Volt regulator from external pass transistor |
| 19 | RESETB | Output | RESETB Output to MCU | 5.0 V Logic level reset signal used to reset the MCU during under and overvoltage conditions and for initial power-up, down and watchdog timeouts |
| 20 | VPROT | Output | Sensor Supply Protected Output | The VPROT Output is a protected 5.0 Volt output that tracks the V _{CC} voltage but isolates the VCC output against shorts to ground and to battery. It is intended to supply sensors which are located off of the ECU board. |
| 21 | LAMPOUT | Output | Warning Lamp Output | Low side driver output for MIL (warning lamp) driven by SPI input command |
| 22 | RGND2 | Ground | ROUT2 Power Ground | Ground connection for ROUT 2 low side driver. Must be tied to VPWR Ground. |
| 23 | ROUT2 | Output | Relay Driver 2 Output | Low side relay driver output # 2 driven by SPI input command or RIN2 logic input |
| 24 | N.C. | No Connect | Unused pin | For future expansion |
| 25 | N.C. | No Connect | Unused pin | For future expansion |
| 26 | TACHOUT | Output | Tachometer output | This pin provides the low side drive for a tachometer gauge or alternatively as a SPI controlled low side driver, or oscillator output. |
| 27 | MRX | Output | Low Side Driver Output | Output 5.0 V logic level ISO9141 data to the MCU from the ISO9141 IN/OUT pin |
| 28 | MTX | Input | ISO9141 MCU Data Input | Input 5.0 V logic level ISO9141 data from the MCU to the ISO9141 IN/OUT pin |

Table 2. 33814 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page [20](#).

| Pin | Pin Name | Pin Function | Formal Name | Description |
|-----|----------|--------------|---|--|
| 29 | BATSW | Output | Battery Switch | This output is a 5.0 V logic level that is high when KEYSW is high. It is only low when KEYSW is low. It can also be controlled via the SPI. The BATSW output may not be present in a different package but it's function can be read by the SPI. |
| 30 | INJIN2 | Input | Injector Driver Input 2 | 5.0 V logic level input from the MCU to control the injector 2 driver output. (Can also be controlled via the SPI) |
| 31 | INJIN1 | Input | Injector Driver Input 1 | 5.0 V logic level input from the MCU to control the injector 1 driver output. (Can also be controlled via the SPI) |
| 32 | IGNIN2 | Input | Ignition Input 2 | 5.0 V logic level input from MCU controlling the ignition coil # 2 current flow and spark. (Can also be controlled via the SPI) |
| 33 | IGNIN1 | Input | Ignition Input 1 | 5.0 V logic level input from MCU controlling the ignition coil # 1 current flow and spark. (Can also be controlled via the SPI) |
| 34 | O2HIN | Input | O2 Sensor Heater Input | 5.0 V logic level input used to turn on and off the O2HOUT driver. The O2HOUT driver can also be turned on and off via the SPI if this pin is not present in a different package. |
| 35 | RIN2 | Input | Relay Driver Input 2 | 5.0 V logic level input from the MCU to control the relay 2 driver output ROUT2. The ROUT2 driver can also be turned on and off via the SPI if this pin is not present in a different package. |
| 36 | RIN1 | Input | Relay Driver Input 1 | 5.0 V logic level input from the MCU to control the relay 1 driver output ROUT1. The ROUT1 driver can also be turned on and off via the SPI if this pin is not present in a different package. |
| 37 | KEYSW | Input | Key Switch Input | The Key Switch Input is a V_{PWR} level signal that indicates that the Key is inserted and turned to the ON/OFF position. In the ON position the ($KEYSW = V_{BAT}$) the IC is enabled and BATSW = HIGH (Relay 2 ON if programmed in the SPI). In the OFF position the IC is in Sleep mode, only when the PWREN bit in the SPI register is also low. |
| 38 | INJGND2 | Ground | Injector Driver 2 Ground | Ground connection for injector 2 low side driver. Must be tied to VPWR ground. |
| 39 | INJOUT2 | Output | Injector Driver 2 Output | Low side driver output for injector 2 driven by the SPI input or by parallel input INJIN2 |
| 40 | RGND1 | Ground | ROUT1 Power Ground | Ground connection for ROUT 1 low side driver. Must be tied to VPWR ground. |
| 41 | ROUT1 | Output | Relay Driver 1 Output | Low side relay driver output # 1 driven by the SPI input command or RIN1 logic input |
| 42 | INJGND1 | Ground | Injector Driver 1 Ground | Ground connection for injector 1 low side driver. Must be tied to VPWR ground. |
| 43 | INJOUT1 | Output | Injector Driver 1 Output | Low side driver output for injector 1 driven by the SPI input or by parallel input INJIN1 |
| 44 | ISO9141 | Input/Output | ISO9141 K-Line Bidirectional Serial Data Signal | ISO9141 pin is V_{PWR} level IN/OUT signal which is connected to an external ECU tester that uses the ISO9141 protocol. The output is open drain and the Input is a ratiometric V_{PWR} level threshold comparator. |
| 45 | IGNFB1 | Input | Feedback from Collector 1 | Voltage feedback from collector of ignition # 1 driver IGBT through 10:1 voltage divider (9R:1R) |
| 46 | IGNOUT1 | Output | Ignition Output 1 | Output to gate of IGBT or GPGD for ignition # 1 |
| 47 | IGNFB2 | Input | Feedback from Collector 2 | Voltage feedback from collector of ignition # 2 driver IGBT through 10:1 voltage divider (9R:1R) |
| 48 | IGNOUT2 | Output | Ignition Output 2 | Output to gate of IGBT or GPGD for ignition # 2 |

4 General Product Characteristics

4.1 Maximum Ratings

Table 3. MAXIMUM RATINGS

All voltages are with respect to ground, unless mentioned otherwise. Exceeding these ratings may cause malfunction or permanent device damage.

| Parameter | Symbol | Min. | Max. | Unit |
|---|--|--------------|--------------------|-----------------|
| ELECTRICAL RATINGS | | | | |
| V _{PWR} Supply Voltage | V _{PWR} | -0.3 | 45 | V _{DC} |
| V _{PP} Supply Voltage (If supplied externally and not using internal VPP regulator) • V _{PPREF} • V _{PPSENSE} | V _{PP_Ext} | -0.3 -0.3 | 45 10 | V _{DC} |
| V _{PROT} Regulator | V _{PROT} | -0.3 | V _{PWR} | V _{DC} |
| SPI Interface and Logic Input Voltage (V _{SI} , V _{SCLK} , V _{CSB} , V _{RIN1} , V _{RIN2} , V _{INJIN1} , V _{INJIN2} , V _{IGNIN1} , V _{IGNIN2} , V _{O2HIN} , V _{MTX}) | V _{IL} , V _{IH} | -0.3 | V _{CC} | V _{DC} |
| SPI Interface and Logic Output Voltage (V _{SO} , V _{BATSW} , V _{MRX} , V _{VRSOUT}) | V _{IL} , V _{IH} | -0.3 | V _{CC} | V _{DC} |
| All Low Side Drivers Drain Voltage (V _{INJOUT1} , V _{INJOUT2} , V _{ROUT1} , V _{ROUT2} , V _{LAMP} OUT, V _{TACH} OUT) | V _{OUTX} | -0.3 | V _{CLAMP} | V _{DC} |
| All Pre-drivers Output Voltage (V _{IGNOUT1} , V _{IGNOUT2} , V _{O2HOUT}) | V _{GDX} | -0.3 | 10 | V _{DC} |
| All Pre-driver Feedback Inputs Voltage (V _{IGNFB1} , V _{IGNFB2} , V _{O2HFB}) | V _{GDFB} | -1.5 | 60 | V _{DC} |
| All Pre-driver Current Sense Inputs Voltage (V _{IGNSENSN} , V _{IGNSENSP} , V _{O2HSENSN} , V _{O2HSENSP}) | V _{ISENS} | -0.3 | 1.0 | V _{DC} |
| KEYSW Input Voltage (V _{KEYSW}) | V _{KEYSW} | -18 | V _{PWR} | V _{DC} |
| RESETB Output Voltage (V _{RESETB}) | V _{RESETB} | -0.3 | V _{CC} | V _{DC} |
| ISO9141 Input/Output Voltage (V _{ISO9141}) | V _{ISO9141} | -18 | V _{PWR} | V _{DC} |
| Output Continuous Current (INJOUT1, INJOUT2) • T _{JUNCTION} = 150 °C | I _{OC_INJX} | – | 1.3 | A |
| Output Continuous Current (ROUT1) • T _{JUNCTION} = 150 °C | I _{OC_R1} | – | 2.0 | A |
| Output Continuous Current (ROUT2) • T _{JUNCTION} = 150 °C | I _{OC_R2} | – | 1.0 | A |
| Output Continuous Current (LAMP)OUT • T _{JUNCTION} = 150 °C | I _{OC_LAMP} | – | 1.0 | A |
| Output Continuous Current (TACH)OUT • T _{JUNCTION} = 150 °C | I _{OC_TACH} | – | 50 | mA |
| Maximum Voltage for VRSN and VRSP inputs to ground | V _{VRS_IN} | -0.5 | 6.0 | V _{DC} |
| Maximum Current for VRSN and VRSP inputs (internal diodes limit voltage) | I _{VRSX_IN} | – | 15 | mA |
| Output Clamp Energy (INJOUT1, INJOUT2, ROUT1)(Single Pulse) • T _{JUNCTION} = 150 °C, I _{OUT} = 1.0 A | E _{CLAMP_INJ_SP} E _{CLAMP_REL_SP} | – | 100 | mJ |

Table 3. MAXIMUM RATINGS

All voltages are with respect to ground, unless mentioned otherwise. Exceeding these ratings may cause malfunction or permanent device damage.

| Parameter | Symbol | Min. | Max. | Unit |
|--|---|-------------|--|------|
| ELECTRICAL RATINGS (CONTINUED) | | | | |
| Output Clamp Energy (INJOUT1, INJOUT2)(Continuous operation) • $T_{\text{JUNCTION}} = 125\text{ }^{\circ}\text{C}$, $I_{\text{OUT}} = 1.0\text{ A}$, (Max injector frequency is 70 Hz, Max duty cycle =90%) | $E_{\text{CLAMP_INJ_CP}}$ $E_{\text{CLAMP_REL_CP}}$ | – | 100 | mJ |
| Output Clamp Energy (LAMPOUT)(Single pulse) • $T_{\text{JUNCTION}} = 150\text{ }^{\circ}\text{C}$, $I_{\text{OUT}} = 0.5\text{ A}$ | $E_{\text{CLAMP_LAMP_SP}}$ | – | 35 | mJ |
| ESD Voltage ⁽²⁾ • Human Body Model (HBM) • VPWR pin (only) • Charge Device Model (CDM) (corner pins) • Charge Device Model (CDM) | V_{ESD1} V_{ESD2} V_{ESD3} | – – – | ± 2000 ± 1500 ± 750 ± 500 | V |

THERMAL RATINGS

| | | | | |
|---|--|-------------------|-------------------|--------------------|
| Operating Temperature (Automotive grade version) • Ambient • Junction • Case | T_{A} T_{J} T_{C} | -40 -40 -40 | 125 150 125 | $^{\circ}\text{C}$ |
| Storage Temperature | T_{STG} | -55 | 150 | $^{\circ}\text{C}$ |
| Power Dissipation ($T_{\text{A}} = 25\text{ }^{\circ}\text{C}$) | P_{D} | – | 3.0 | W |
| Peak Package Reflow Temperature During Reflow ^{(3), (4)} | T_{PPRT} | – | Note 4 | $^{\circ}\text{C}$ |

THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS

| | | | | |
|--|--|-----------|-----------|----------------------|
| Thermal Resistance • Junction-to-Ambient (LQFP-48-EP Package) (Single Layer Board) • Junction-to-Case (LQFP-48-EP Package) | $R_{\theta\text{JA}}$ $R_{\theta\text{JC}}$ | 29 2.4 | 29 2.4 | $^{\circ}\text{C/W}$ |
|--|--|-----------|-----------|----------------------|

Notes

- ESD testing is performed in accordance with the Human Body Model (HBM) ($C_{\text{ZAP}} = 100\text{ pF}$, $R_{\text{ZAP}} = 1500\text{ }\Omega$), and the Charge Device Model.
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescle's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxx enter 33xxx), and review parametrics.

4.2 Static Electrical Characteristics

Table 4. Power Input Static Electrical Characteristics

Characteristics noted under conditions of $6.0\text{ V} \leq V_{PWR} \leq 18\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_C \leq 125\text{ }^{\circ}\text{C}$, and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with $V_{PWR} = 14\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|----------------------|------|------|------|---------|
| POWER INPUT (VPWR) | | | | | |
| Supply Voltage (measured at VPWR pin) ⁽⁵⁾ | | | | | V |
| • Logic Stable Range | $V_{PWR(LS)}$ | 2.5 | – | 45 | |
| • Full Operational Range | $V_{PWR(FO)}$ | 4.5 | – | 36 | |
| • Full Parameter Specification Range | $V_{PWR(FP)}$ | 6.0 | – | 18 | |
| Supply Current | $I_{VPWR(ON)}$ | – | 10.0 | 14.0 | mA |
| • All Outputs Disabled (Normal Mode), excludes base current to the external pnp | | | | | |
| Sleep State Supply Current (Must have PWREN = 0 & KEYSW \leq 0.8 V for sleep state), | $I_{VPWR(SS)}$ | – | 10 | 20 | μ A |
| • $V_{PWR} = 18\text{ V}$ | | | | | |
| V_{PWR} Overvoltage Shutdown Threshold Voltage (OV Reset) ⁽⁶⁾ | $V_{PWR(OV)}$ | 37.5 | 39 | 42 | V |
| V_{PWR} Overvoltage Shutdown Hysteresis Voltage | $V_{PWR(OV-HYS)}$ | 0.5 | 1.5 | 3.0 | V |
| V_{CC} Power On Reset Voltage Threshold (POR Power On Reset), rising V_T | $V_{CC(POR)}$ | 3.9 | – | 4.9 | V |
| V_{CC} Undervoltage Shutdown Threshold Voltage (UV Reset) ⁽⁷⁾ , falling V_T | $V_{CC(UV)}$ | 2.9 | – | 3.9 | V |
| V_{CC} POR and Undervoltage Shutdown Hysteresis Voltage | $V_{CC(UV/POR-HYS)}$ | 100 | – | – | mV |
| V_{CC} POR and Undervoltage Non-overlap (POR-UV) | $V_{CC, NONOVERLAP}$ | 0.8 | 1.0 | 1.2 | V |
| VOLTAGE PRE-REGULATOR OUTPUT (VPPREF, VPPSENS) | | | | | |
| VPPREF Output Voltage | V_{PPREF} | 5.85 | 6.5 | 7.15 | V |
| VPPREF Output Current (includes external PNP current) | I_{VPPREF} | – | -5.0 | – | mA |
| VPPREF Current Limit | I_{VPPCL} | -5 | -15 | -20 | mA |
| Output Capacitance External (ceramic) | V_{OCE} | 2.2 | – | 25 | μ F |
| VPPSENS Input Current | $I_{VPPSENS}$ | – | – | 3 | mA |
| Line Regulation $I_{VCC} = 100\text{ mA}$, $I_{VPROT} = 50\text{ mA}$ $9.0\text{ V} < V_{PWR} < 18\text{ V}$ and Diodes Inc. FZT753TA PNP | REGLINE_VPP | – | 2.0 | 25 | mV |
| Dropout Voltage (Minimal Input/Output Voltage, tracks input below) $I_{VCC} = 100\text{ mA}$, $I_{VPROT} = 50\text{ mA}$ and Diodes Inc. FZT753TA PNP | $V_{DROPOUT_PP}$ | – | 1.05 | 1.4 | V |

Notes

- This parameter is guaranteed by design but is not production tested.
- Overvoltage thresholds minimum and maximum include hysteresis.
- Undervoltage thresholds minimum and maximum include hysteresis

Table 4. Power Input Static Electrical Characteristics

Characteristics noted under conditions of $6.0\text{ V} \leq V_{PWR} \leq 18\text{ V}$, $-40\text{ }^\circ\text{C} \leq T_C \leq 125\text{ }^\circ\text{C}$, and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with $V_{PWR} = 14\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|------------------------|---------------------|------|-----|---------------|
| VOLTAGE REGULATOR OUTPUTS (VCC, VPROT) | | | | | |
| VCC Output Voltage $0 \leq I_{VCC} \leq I_{VCC_C}$ | V_{CC} | 4.9 | 5.0 | 5.1 | V |
| VCC Output Current Continuous | I_{VCC_C} | – | – | 200 | mA |
| VPROT Output Voltage (tracks VCC) $I_{VCC} = 100\text{ mA}$, $I_{VPROT} = 50\text{ mA}$, $9.0\text{ V} < V_{PWR} < 18\text{ V}$ | $ I_{VCC} - V_{PROT} $ | – | – | 25 | mV |
| VPROT Output Current Continuous | I_{VPROT_C} | – | – | 100 | mA |
| VCC Output Current Limiting | I_{VCC_CL} | 200 ⁽¹¹⁾ | – | 500 | mA |
| VPROT Output Current Limiting | I_{VPROT_CL} | 110 | – | 260 | mA |
| Output Capacitance External (V_{CC} and V_{PROT}) without reverse protection diode | V_{OCE} | 2.2 | – | 47 | μF |
| Line Regulation (Both V_{CC} and V_{PROT}) $I_{VCC} = 100\text{ mA}$, $I_{PROT} = 50\text{ mA}$, $9.0\text{ V} < V_{PWR} < 18\text{ V}$ | REG_{LINE_VB} | – | 2.0 | 25 | mV |
| Load Regulation (Both V_{CC} and V_{PROT}) measured from 10% - 90% of I_{VCC_C} & I_{PROT_C} , $V_{PWR} = 13\text{ V}$ | REG_{LOAD_VB} | – | 20 | 35 | mV |
| Dropout Voltage (Both V_{CC} and V_{PROT}) (Minimal Input/Output Voltage at full load, tracks input below) | $V_{DROPOUT}$ | – | 1.05 | 1.4 | V |

ALL LOW SIDE DRIVERS (INJ1, INJ2, ROUT1, ROUT2, LAMPOUT, TACHOUT)

| | | | | | |
|---|-------------------|-----|-----|-----|------------------|
| Output Fault Detection Voltage Threshold ⁽⁸⁾ Outputs programmed OFF (Open Load) Outputs programmed ON (Short to Battery) | $V_{OUT(FLT-TH)}$ | 2.0 | 2.5 | 3.0 | V |
| Output OFF Open Load Detection Current (INJ1, INJ2, RELAY1, RELAY2 & LAMP) • $V_{DRAIN} = 18\text{ V}$, Outputs Programmed OFF | $I_{(OFF)OCO}$ | 40 | 75 | 115 | μA |
| Output OFF Open Load Detection Current TachOut | $I_{(OFF)TACH}$ | 10 | – | 30 | μA |
| Output Leakage Current • $V_{DRAIN} = 24\text{ V}$, Open Load Detection Disabled and Output commanded OFF | $I_{OUT(LKG)}$ | – | – | 20 | μA |
| Overtemperature Shutdown (OT) ⁽⁹⁾ | T_{LIM} | 155 | – | 185 | $^\circ\text{C}$ |
| Overtemperature Shutdown Hysteresis ⁽¹⁰⁾ | $T_{LIM(HYS)}$ | 5.0 | 10 | 15 | $^\circ\text{C}$ |
| Output Clamp Voltage • $I_D = 20\text{ mA}$ | V_{OC} | 48 | 53 | 60 | V |

INJOUT1, INJOUT2

| | | | | | |
|--|--|-------------|---------------|---------------|----------|
| Drain-to-Source ON Resistance • $I_{OUT} = 1.0\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$, $V_{PWR} = 13\text{ V}$ • $I_{OUT} = 1.0\text{ A}$, $T_J = 25\text{ }^\circ\text{C}$, $V_{PWR} = 13\text{ V}$ • $I_{OUT} = 1.0\text{ A}$, $T_J = -40\text{ }^\circ\text{C}$, $V_{PWR} = 13\text{ V}$ | $R_{DS(ON)_INJx}$ $R_{DS(ON)_INJx}$ $R_{DS(ON)_INJx}$ | – – – | – 0.4 – | 0.6 – – | Ω |
| Continuous Current (not to exceed) | $I_{OUT(CC)_INJx}$ | – | – | 1.3 | A |
| Output Self Limiting Current | $I_{OUT(LIM)_INJx}$ | 1.6 | – | 3.0 | A |

Notes

- These parameters are guaranteed by design. Production test equipment uses 1.0 MHz, 5.0 V SPI interface.
- This parameter is guaranteed by design, however it is not production tested.
- Programmable via SPI but variable with magnitude input frequency
- Guaranteed at $9.0\text{ V} \leq V_{PWR} \leq 18\text{ V}$

Table 4. Power Input Static Electrical Characteristics

Characteristics noted under conditions of $6.0\text{ V} \leq V_{PWR} \leq 18\text{ V}$, $-40\text{ }^\circ\text{C} \leq T_C \leq 125\text{ }^\circ\text{C}$, and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with $V_{PWR} = 14\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|------------|--------------|------------|---------------|
| ROUT1 | | | | | |
| Driver Drain-to-Source ON Resistance • $I_{OUT} = 700\text{ mA}$, $T_J = 150\text{ }^\circ\text{C}$, $V_{PWR} = 13\text{ V}$ | $R_{DS(ON)_R1}$ | – | 0.3 | 0.4 | Ω |
| Continuous Current (not to exceed) | $I_{OUT(CC)_R1}$ | – | – | 2.0 | A |
| Output Self-limiting Current (Has inrush current timer) | $I_{OUT(LIM)_R1}$ | 3.0 | – | 6.0 | A |
| ROUT2 | | | | | |
| Driver Drain-to-Source ON Resistance • $I_{OUT} = 350\text{ mA}$, $T_J = 150\text{ }^\circ\text{C}$, $V_{PWR} = 13\text{ V}$ | $R_{DS(ON)_R2}$ | – | – | 1.5 | Ω |
| Continuous Current (not to exceed) | $I_{OUT(CC)_R2}$ | – | – | 1.0 | A |
| Output Self-limiting Current | $I_{OUT(LIM)_R2}$ | 1.2 | – | 2.4 | A |
| LAMPOUT | | | | | |
| Driver Drain-to-Source ON Resistance • $I_{OUT} = 1.0\text{ A}$, $T_J = 150\text{ }^\circ\text{C}$, $V_{PWR} = 13\text{ V}$ | $R_{DS(ON)_LAMP}$ | – | – | 1.5 | Ω |
| Continuous Current | $I_{OUT(CC)_LAMP}$ | – | – | 1.0 | A |
| Output Self-limiting Current (Has inrush current timer) | $I_{OUT(LIM)_LAMP}$ | 1.2 | – | 2.4 | A |
| TACHOUT | | | | | |
| Driver Drain-to-Source ON Resistance • $I_{OUT} = 50\text{ mA}$, $T_J = 150\text{ }^\circ\text{C}$, $V_{PWR} = 13\text{ V}$ | $R_{DS(ON)_TACH}$ | – | – | 20 | Ω |
| Continuous Current (not to exceed) | $I_{OUT(CC)_TACH}$ | – | – | 50 | mA |
| Output Current Shutdown | $I_{OUT(SHUTDOWN)_TACH}$ | 60 | – | 110 | mA |
| ALL PRE-DRIVERS (IGNOUT1, IGNOUT2, AND O2HOUT) | | | | | |
| Pre-driver Output Voltage, $V_{PWR} = 13\text{ V}$ • $I_{GD} = 500\text{ }\mu\text{A}$ • $I_{GD} = -500\text{ }\mu\text{A}$ | $V_{GS(ON)}$ $V_{GS(OFF)}$ | 7.0 0.0 | 8.0 0.375 | 9.0 0.5 | V |
| IGNOUTx Output Source Current (IGNOUT1 and IGNOUT2 by default) • $1.0 \leq V_{GD} \leq 3.0$, $V_{PWR} = 13\text{ V}$ | $I_{IGN_GD_H}$ | 10 | – | – | mA |
| Output OFF Open Load Detection Current • $V_{DRAIN} = 18\text{ V}$, Outputs Programmed OFF | $I_{(OFF)OCO}$ | 40 | 75 | 115 | μA |
| GPGD Output Source Current (O2HOUT by default) at $1.0 \leq V_{GD} \leq 3.0$, $V_{PWR} = 13\text{ V}$ | $I_{GPGD_GD_H}$ | 10 | – | – | mA |
| Pre-driver short to battery fault threshold • $I_{GD} = 500\text{ }\mu\text{A}$ • $I_{GD} = -500\text{ }\mu\text{A}$ | $V_{IGNFB(FLT_TH)}$ $V_{GPGD(FLT_TH)}$ | 100 1.0 | 250 2.5 | 400 4.0 | mV V |
| Output Clamp Voltage | V_{CLAMP} | 48 | 53 | 60 | V |
| Overcurrent Voltage Threshold • $V_{O2HSENSN}$ to $V_{O2HSENSP}$ | $V_{SENS-TH}$ | 180 | 200 | 220 | mV |

Table 4. Power Input Static Electrical Characteristics

Characteristics noted under conditions of $6.0\text{ V} \leq V_{PWR} \leq 18\text{ V}$, $-40\text{ }^\circ\text{C} \leq T_C \leq 125\text{ }^\circ\text{C}$, and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with $V_{PWR} = 14\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|-------------------|-----|-----|-----|---------------|
| ALL PRE-DRIVERS (IGNOUT1, IGNOUT2, AND O2HOUT) (CONTINUED) | | | | | |
| Overcurrent Voltage Threshold | | | | | |
| • $V_{IGNSENSN}$ to $V_{IGNSENSP}$ (IGNIN1 or IGNIN2 = 1) | $V_{SENS-TH}$ | 180 | 200 | 220 | mV |
| • $V_{IGNSENSN}$ to $V_{IGNSENSP}$ (IGNIN1 and IGNIN2 = 1) | $V_{SENS-TH}$ | 360 | 400 | 440 | |
| Current Sense Input Offset Current (IGNSENSP,IGNSENSN, O2H) | $I_{SENS-OFFSET}$ | – | – | 15 | μA |
| Current Sense Input Bias Current | $I_{SENS-BIAS}$ | – | – | 15 | μA |

ISO-9141 TRANSCEIVER PARAMETERS (8.0 V < V_{PWR} < 18 V)

| | | | | | |
|--|-----------------|------------------------|-----|----------------------|----|
| Input Low Voltage at ISO I/O pin | V_{IL_ISO} | – | – | $0.3 \times V_{PWR}$ | V |
| Input High Voltage at ISO I/O pin | V_{IH_ISO} | $0.7 \times V_{PWR}$ | – | – | V |
| Input Hysteresis at ISO I/O pin | V_{HYST_ISO} | $0.15 \times V_{PWR}$ | – | – | V |
| Output Low-voltage at ISO I/O pin | V_{OL_ISO} | – | – | $0.2 \times V_{PWR}$ | V |
| Output High-voltage at ISO I/O pin | V_{OH_ISO} | $0.8 \times V_{PWR}^R$ | – | – | V |
| Output current limit at ISO I/O pin (MTX = 0) | I_{LIM_ISO} | 50 | 100 | 150 | mA |
| Load capacitance at ISO I/O pin ⁽¹²⁾ | C_{L_ISO} | 0.01 | 3.0 | 10 | nF |
| Output load current at ISO I/O pin (MTX = 0, RLOAD = 1.0 k Ω , $\pm 10\%$) | I_{ISO} | – | 12 | – | mA |

VRS CONDITIONER INPUT

| | | | | | |
|---|-------------------|-------|---|----------|---------------|
| Comparator Thresholds | V_{VRS_THRESH} | – | See Table variable via SPI or dynamically | | mV |
| Threshold Accuracy | | | | | |
| Steady State Condition ($\pm 20\%$ only valid for VRS DAC thresholds 110 mV and higher. All other thresholds guaranteed monotonic only.) | $ACCU_{THRESH}$ | – | – | ± 20 | % |
| Input Bias Current VRSP and VRSN (2.5 V common mode must be off) | $I_{BIASRSX}$ | -5.0 | | 5.0 | μA |
| VRS Positive Clamp Voltage at $I_{CLAMP} = 10\text{ mA}$ | V_{CLAMP_P} | 5.5 | – | 5.8 | V |
| VRS Negative Clamp Voltage at $I_{CLAMP} = 10\text{ mA}$ | V_{CLAMP_N} | -0.45 | – | -0.22 | V |

DIGITAL INTERFACE (MRX, MTX,CSB, SI, SCLK, SO, RINX,O2HIN, INJINX, IGNINX, BATSW, VRSOUT, RESETB)

| | | | | | |
|---|-----------------|---------------------|----|---------------------|---------------|
| Input Logic High-voltage Thresholds | V_{IH} | $0.7 \times V_{CC}$ | – | $V_{CC} + 0.3$ | V |
| Input Logic Low-voltage Thresholds | V_{IL} | $\text{GND} - 0.3$ | – | $0.2 \times V_{CC}$ | V |
| Input Logic Voltage Hysteresis | V_{HYS} | 500 | – | – | mV |
| Input Logic Capacitance | C_{IN} | – | – | 20 | pF |
| Sleep Mode Input Logic Current ⁽¹²⁾ | | | | | |
| • KEYSW = 0 V | I_{LOGIC_SS} | -10 | – | 10 | μA |
| Input Logic Pull-down Current ⁽¹²⁾ INJIN1, INJIN2, RIN1, RIN2, SI, SCLK, IGNIN1, IGNIN2, O2HIN | | | | | |
| • 0.8 V to 5.0 V | I_{LOGIC_PD} | 30 | 50 | 100 | μA |

Notes

12. This parameter is guaranteed by design, however it is not production tested.

Table 4. Power Input Static Electrical Characteristics

Characteristics noted under conditions of $6.0\text{ V} \leq V_{PWR} \leq 18\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_C \leq 125\text{ }^{\circ}\text{C}$, and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with $V_{PWR} = 14\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|-----------------------------------|----------------|-----|-----------|------------------|
| DIGITAL INTERFACE (MRX, MTX,CSB, SI, SCLK, SO, RINX,O2HIN, INJINX, IGNINX, BATSW, VRSOUT, RESETB) (CONTINUED) | | | | | |
| SO Tri-state Output (in Tri-state mode, CSB = 1) • 0 V to 5.0 V | I_{TRISO} | -10 | – | 10 | μA |
| CSB Input Current • CSB = V_{CC} | I_{CSB} | -10 | – | 10 | μA |
| Input Logic Pull-up Current - CSB and MTX • 0.0 to 4.2 V | I_{LOGIC_PU} | -20 | -40 | -90 | μA |
| CSB Leakage Current to V_{CC} • CSB = 5.0 V, KEYSW = 0.0 V | $I_{CSB(LKG)}$ | – | – | 10 | μA |
| SO, MRX High-state Output Voltage (CSB =0 for SO) • $I_{SO-HIGH} = -1.0\text{ mA}$ | V_{SO_HIGH} V_{MRX_HIGH} | $V_{CC} - 0.4$ | – | – | V |
| SO, MRX Low-state Output Voltage (CSB =0 for SO) • $I_{SO-LOW} = 1.0\text{ mA}$ | V_{SO_LOW} V_{MRX_LOW} | – | – | 0.4 | V |
| BATSW High-state Output Voltage • $I_{SO-HIGH} = -10\text{ mA}$ | V_{BATSW_HIGH} | $V_{CC} - 1.0$ | – | – | V |
| BATSW Low-state Output Voltage • $I_{SO-LOW} = 10\text{ mA}$ | V_{BATSW_LOW} | – | – | 1.0 | V |
| KEYSW High-state Input Voltage | V_{KEYSW_HIGH} | 4.5 | – | V_{PWR} | V |
| KEYSW Low-state Input Voltage | V_{KEYSW_LOW} | -0.3 | – | 2.5 | V |
| KEYSW Hysteresis | V_{KEYSW_HYS} | 100 | – | – | mV |
| VRS Low-state Output Voltage • $I_{VRS-LOW} = 1.0\text{ mA}$ | V_{VRSOUT_LOW} | – | – | 0.4 | V |
| VRS High-state Output Voltage • $I_{VRS-HIGH} = 1.0\text{ mA}$ | V_{VRSOUT_HIGH} | $V_{CC} - 0.4$ | – | 5.0 | V |
| RESET Low-state Output Voltage • $I_{RESET-LOW} = 1.0\text{ mA}$ | V_{RESET_LOW} | – | – | 0.4 | V |
| RESET High-state Leakage Current | $I_{RESET_LEAKAGE_HIGH}$ | 10 | – | 25 | μA |
| RESET Pull-down Resistor | $R_{RESET_PULDOWN}$ | 200 | – | 500 | $\text{k}\Omega$ |

4.3 Dynamic Electrical Characteristics

Table 5. Dynamic Electrical Characteristics ⁽¹⁴⁾

Characteristics noted under conditions of $6.0\text{ V} \leq V_{PWR} \leq 18\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_C \leq 125\text{ }^{\circ}\text{C}$, and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with $V_{PWR} = 14\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|----------------------------|---------------------|--------------------|--------------------|------------------------|
| POWER INPUT | | | | | |
| Required Low State Duration on V_{CC} for Power On Reset • $V_{CC} \leq 0.2\text{ V}$ | t_{RESET} | 1.0 | – | – | μs |
| Power on RESET pulse width | $t_{(POR)}$ | 100 | – | – | μs |
| WATCHDOG TIMER | | | | | |
| Maximum Time Value Watchdog can be loaded with (default time) | WDMAX | – | – | 10 | sec. |
| Minimum Time Value Watchdog can be loaded with | WD _{MIN} | 1.0 | – | – | ms |
| Reset Pulse Width when Watchdog times out | WD _{RESET} | 100 | – | – | μs |
| VRS CONDITIONING INPUT | | | | | |
| Output Blanking Time Programming Range (% of previous out pulse 0 to 15/32 in 1/32 steps, 15/32 = 46.9%) | OUTPUT _{BLANK} | 0 | – | 50 | % |
| Output Deglitch Filter Time (1/128 of the previous output pulse) | OUTPUT _{DEGLITCH} | – | 1.0 | – | % |
| Delay from CSB to Change in VRS Comparator Threshold ⁽¹³⁾ | DELAY _{THRESH} | – | – | 10 | μs |
| Delay from CSB to Change in VRS Output Blank Time ⁽¹³⁾ | DELAY _{OBT} | – | – | 10 | μs |
| ISO9141 TRANSCEIVER | | | | | |
| Typical ISO9141 Data Rate | ISO _{BR} | – | 10 | – | kbps |
| Turn OFF Delay MTX Input to ISO Output | t_{TXDF} | – | – | 2.0 | μs |
| Turn ON/OFF Delay ISO Input to MRX Output | t_{RXDF} , t_{RXDR} | – | – | 1.0 | μs |
| Rise and Fall Time MRX Output (measured from 10% to 90%) | t_{RXR} , t_{RXF} | – | – | 1.0 | μs |
| Maximum Rise and Fall Time MTX Input (measured from 10% to 90%) | t_{TXR} , t_{TXF} | – | – | 1.0 | μs |
| ALL LOW SIDE DRIVERS | | | | | |
| Output ON Current Limit Fault Filter Timer | t_{SC1} | 30 | 60 | 90 | μs |
| Output Retry Timer | t_{REF} | 7.0 | 10 | 13 | ms |
| Inrush Current Delay Timer | t_{INRUSH} | 7.0 ⁽¹³⁾ | 10 ⁽¹³⁾ | 13 ⁽¹³⁾ | ms |
| Output OFF Open-circuit Fault Filter Timer | $t_{(OFF)OC}$ | 100 | – | 400 | μs |
| Output Slew Rate, INJOUT1, INJOUT2, ROUT1, ROUT2, and LAMP • $R_{LOAD} = 500\ \Omega$, $V_{LOAD} = 14\text{ V}$ | $t_{SR(RISE)}$ | 1.0 | 5.0 | 10 | $\text{V}/\mu\text{s}$ |
| Output Slew Rate, INJOUT1, INJOUT2, ROUT1, ROUT2, and LAMP • $R_{LOAD} = 500\ \Omega$, $V_{LOAD} = 14\text{ V}$ | $t_{SR(FALL)}$ | 1.0 | 5.0 | 10 | $\text{V}/\mu\text{s}$ |
| Propagation Delay (Input Rising Edge OR CSB to Output Falling Edge) • Input at 50% V_{DD} to Output voltage 90% of V_{LOAD} (INJ1, INJ2, ROUT1, ROUT2, LAMP) | t_{PHL} | – | 1.0 | 5.0 | μs |
| Propagation Delay (Input Rising Edge OR CSB to Output Falling Edge) • Input at 50% V_{DD} to Output voltage 90% of V_{LOAD} (TACHOMETER) | t_{PHL} | – | 1.0 | 6.0 | μs |

Notes

13. Guaranteed by Design
14. internal oscillator of 4.0 MHz $\pm 10\%$ typical for $V_{PWR} = 13\text{ V}$, at room temp.

Table 5. Dynamic Electrical Characteristics ⁽¹⁴⁾

Characteristics noted under conditions of $6.0\text{ V} \leq V_{PWR} \leq 18\text{ V}$, $-40\text{ }^\circ\text{C} \leq T_C \leq 125\text{ }^\circ\text{C}$, and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with $V_{PWR} = 14\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|----------------|-----|-----|-----|------------------------|
| ALL LOW SIDE DRIVERS (CONTINUED) | | | | | |
| Propagation Delay (Input Falling Edge OR CSB to Output Rising Edge) • Input at 50% V_{DD} to Output voltage 10% of V_{LOAD} (INJ1, INJ2, ROUT1, ROUT2, LAMP) | t_{PLH} | – | 1.0 | 5.0 | μs |
| Propagation Delay (Input Falling Edge OR CSB to Output Rising Edge) • Input at 50% V_{DD} to Output voltage 10% of V_{LOAD} (TACHOMETER) | t_{PLH} | – | 1.0 | 6.0 | μs |
| Output Slew Rate, Tachout • $R_{LOAD} = 500\ \Omega$, $V_{LOAD} = 14\text{ V}$ | $t_{SR(FALL)}$ | 6.0 | – | 14 | $\text{V}/\mu\text{s}$ |

ALL GATE PRE-DRIVER (IGN1, IGN2, AND O2H)

| | | | | | |
|---|---------------|-----|-----|-----|---------------|
| Output OFF Open-circuit Fault Filter Timer | $t_{(OFF)OC}$ | 100 | – | 400 | μs |
| Overcurrent (short-circuit) Fault Filter Timer | t_{SC} | 30 | – | 90 | μs |
| Propagation Delay (Input Rising Edge OR CSB to Output Rising Edge) • Input at 50% V_{DD} to Output voltage 10% of $V_{GS(ON)}$ | t_{PLH} | – | 1.0 | 5.0 | μs |
| Propagation Delay (Input Falling Edge OR CSB to Output Falling Edge) • Input at 50% V_{DD} to Output voltage 90% of $V_{GS(ON)}$ | t_{PHL} | – | 1.0 | 5.0 | μs |

SPI DIGITAL INTERFACE TIMING ⁽¹⁵⁾

| | | | | | |
|--|----------------|-----|-----|-----|---------------|
| Falling Edge of CSB to Rising Edge of SCLK • Required Setup Time | t_{LEAD} | 100 | – | – | ns |
| Falling Edge of SCLK to Rising Edge of CSB • Required Setup Time | t_{LAG} | 50 | – | – | ns |
| SI to Rising Edge of SCLK • Required Setup Time | $t_{SI(SU)}$ | 16 | – | – | ns |
| Rising Edge of SCLK to SI • Required Hold Time | $t_{SI(HOLD)}$ | 20 | – | – | ns |
| SI, CSB, SCLK Signal Rise Time ⁽¹⁶⁾ | $t_{R(SI)}$ | – | 5.0 | – | ns |
| SI, CSB, SCLK Signal Fall Time ⁽¹⁶⁾ | $t_{F(SI)}$ | – | 5.0 | – | ns |
| Time from Falling Edge of CSB to SO Low-impedance ⁽¹⁷⁾ | $t_{SO(EN)}$ | – | – | 55 | ns |
| Time from Rising Edge of CSB to SO High-impedance | $t_{SO(DIS)}$ | – | – | 55 | ns |
| Time from Falling Edge of SCLK to SO Data Valid ⁽¹⁸⁾ | t_{VALID} | – | 25 | 55 | ns |
| Sequential Transfer Rate ⁽¹⁵⁾ • Time required between data transfers | t_{STR} | – | – | 1.0 | μs |

Notes

15. These parameters are guaranteed by design. Production test equipment uses 1.0 MHz, 5.0 V SPI interface.
16. Rise and Fall time of incoming SI, CSB, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
17. Time required for output states data to be terminated at SO pin.
18. Time required to obtain valid data out from SO following the fall of SCLK with 200 pF load.

4.4 Timing Diagrams

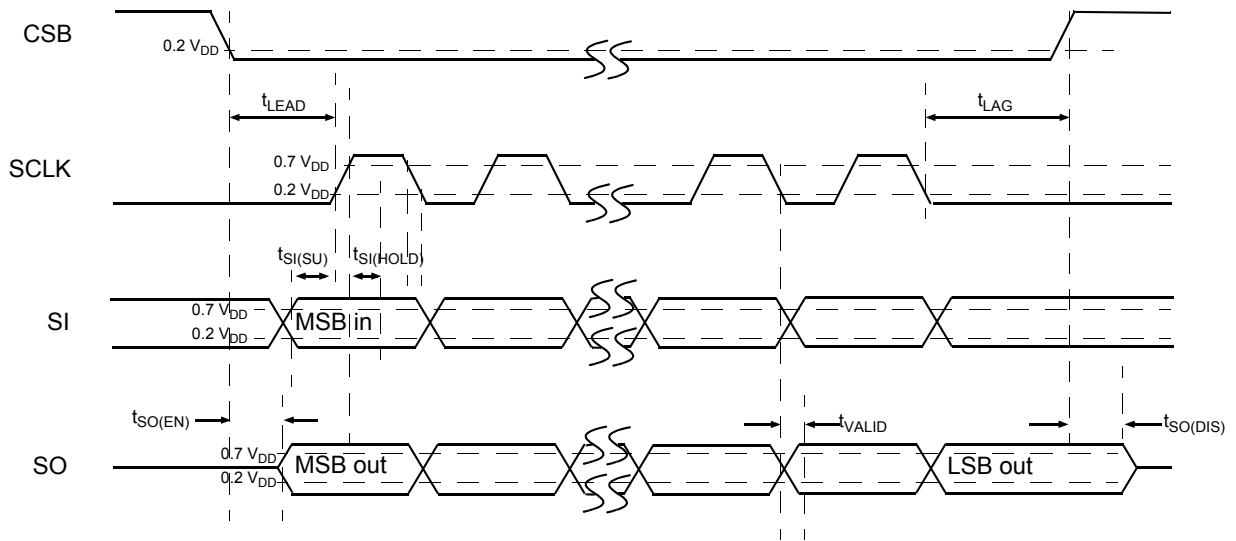


Figure 4. Timing Diagram

4.5 Typical Electrical Characteristics

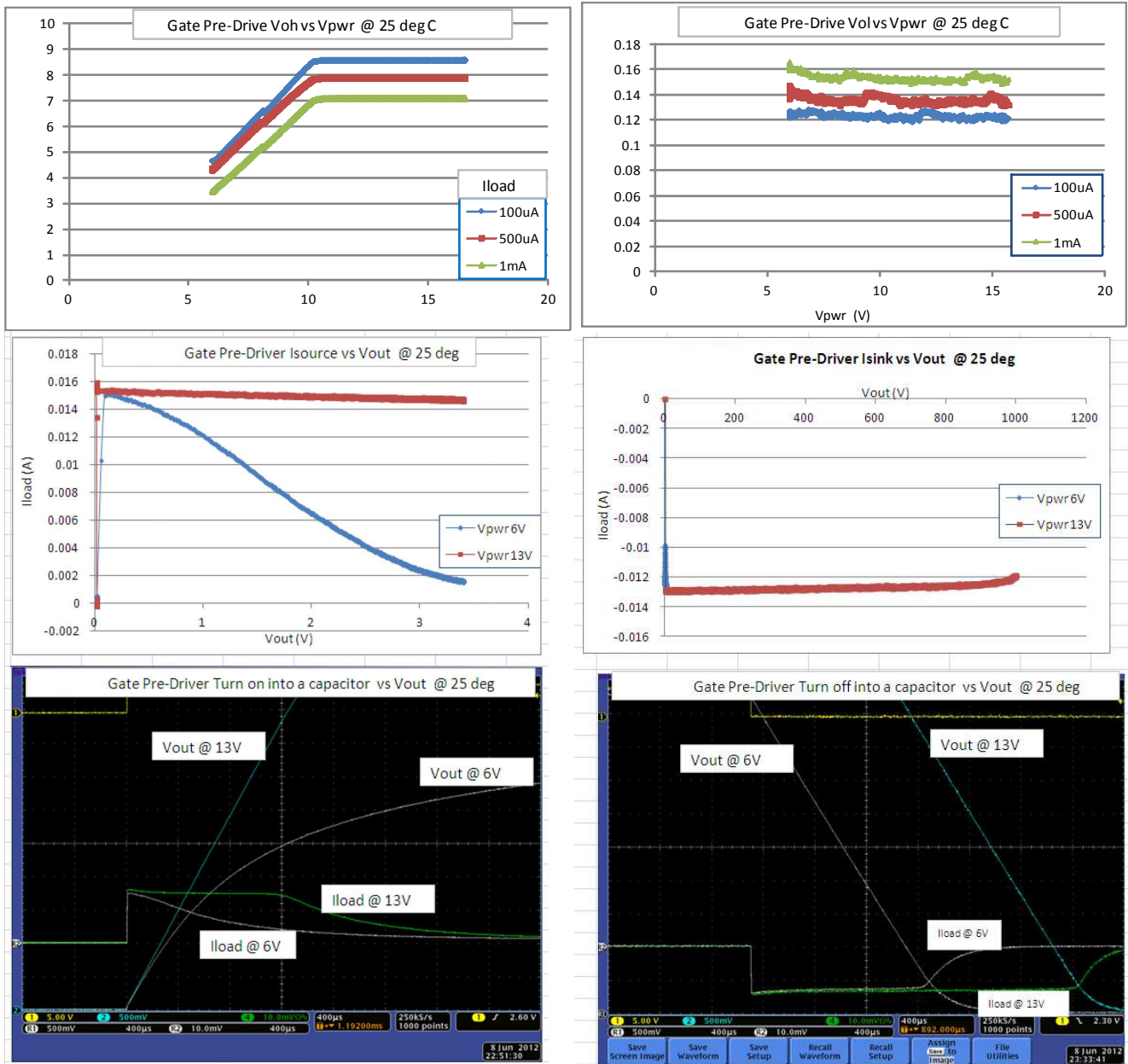


Figure 5. Typical Electrical Specifications

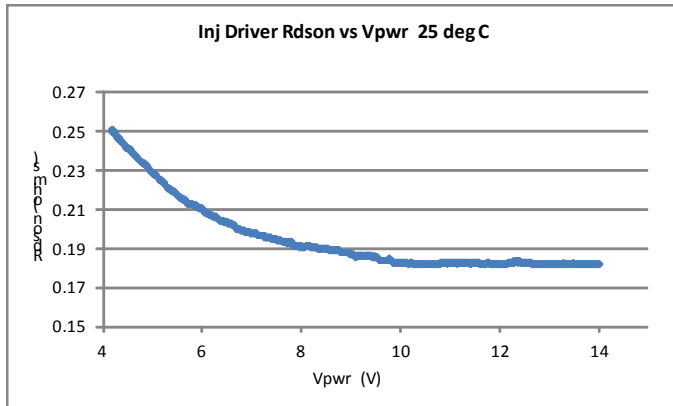
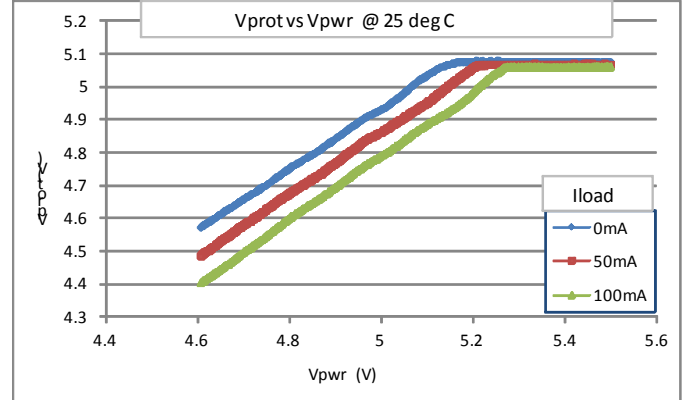
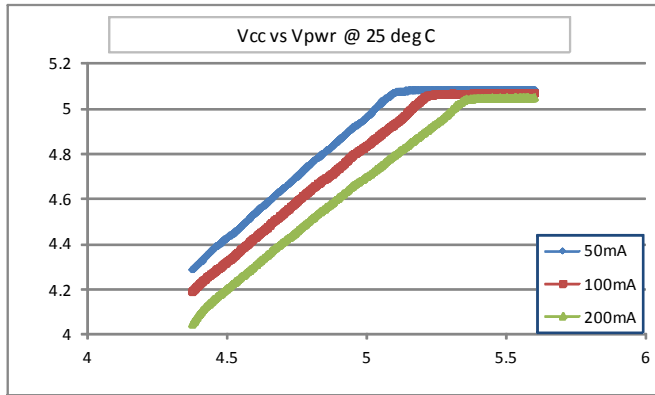


Figure 6. Typical Electrical Specifications (continued)

5 General IC Functional Description and Application Information

5.1 Functional Pin Description

5.1.1 VPWR Supply Input

The VPWR pin is the battery input to the 33814 IC. The VPWR pin requires external reverse battery and adequate transient voltage protection. All IC analog current and internal logic current is provided from the VPWR pin.

An overvoltage comparator monitors this pin and when an overvoltage condition is present all outputs and voltage regulators are shut off for protection. The VPWR pin should be bypassed to ground, as close to the IC as possible, with a 0.1 μF ceramic capacitor.

5.1.2 VPPREF Output

The VPPREF output pin is used to drive the base of an external regulator PNP pass transistor. The output of this V_{PP} regulator supplies the input voltage to the two internal 5.0 Volt regulators. The V_{PP} regulator is a low drop-out (LDO) regulator that provides a regulated output voltage when the input is greater than its specified voltage level, and follows the input voltage when it is below its specified voltage level. It is not recommended that this voltage be brought off of the module PC board, because it may not have adequate protection to prevent damage to the PNP pass transistor under short-to-ground or short-to-battery conditions.

5.1.3 VPPSENS Input

The VPPSENS pin is used to monitor the V_{PP} pre-regulator output voltage from the external pass transistor's collector, and to supply the input voltage to the V_{CC} and V_{PROT} regulators.

The VPPSENS pin should be bypassed to ground, as close to the IC as possible, with a 0.1 μF ceramic capacitor and a higher value electrolytic capacitor in parallel.

5.1.4 VCC Output (5.0 V Supply)

The V_{CC} regulator obtains its input voltage from the V_{PP} pre-regulator. The VCC output supplies 5.0 V power to the system MCU and other on-board peripherals.

A Power On Reset (POR) circuit monitors the VCC output voltage level. When the V_{CC} voltage exceeds the $V_{CC(POR)}$ threshold, the RESETB line is held low for an additional delay time, $t_{(POR)}$, and then brought to a logic one level.

An undervoltage (UV) circuit monitors the output of the V_{CC} regulator and when the voltage goes below the $V_{CC(UV)}$ threshold for more than the V_{CC} filter time, $t_{(VCC-UV)}$, the RESETB line is asserted to a logic zero state and remains there until the POR condition is met.

5.1.5 VPROT Output (5.0 V Protected Supply)

The V_{PROT} regulator obtains its input voltage from the V_{PP} pre-regulator and its reference voltage from the VCC output. V_{PROT} tracks V_{CC} and is protected against shorts to ground, shorts to battery, overcurrent and overtemperature. The VPROT output supplies 5.0 V power to any external sensors and other off-board peripherals. The V_{PROT} regulator on/off state can be controlled via a bit in the SPI Control Registers. The VPROT output should be protected against ESD by means of a 0.1 μF ceramic capacitor on the output and a higher value electrolytic capacitor in parallel.

5.1.6 GND

The GND pin provides the ground reference for the V_{PWR} , V_{PP} , V_{PROT} , and V_{CC} supplies. The GND pin is used as a return for both the power supplies as well as power ground for some of the lower current output drivers. The higher current output drivers have their own ground pins. All ground pins (INJGND1, INJGND2, RGND1, and RGND2) and the exposed pad must be directly connected to this pin and the negative battery terminal. There is no separate ground pin associated with the LAMPOUT driver, it shares a ground with ROUT2.

5.1.7 SCLK Input

The serial clock (SCLK) pin clocks the internal SPI shift register of the 33814. The SI data is latched into the input shift register on the rising edge of SCLK signal. The SO pin shifts status bits out on the falling edge of SCLK. The SO data is available for the MCU to read on the rising edge of SCLK. With CSB in a logic high state, signals on the SCLK and SI pins will be ignored and the SO pin will be in a high-impedance state. The SCLK signal consists of a 50% duty cycle with CMOS logic levels referenced to V_{CC} . All SPI transfers consist of exactly 16 SCLK pulses. If any more or less than 16 clock pulses are received within one frame of CSB going low and then high, a SPI error is reported in the SPI Status Register. The SPI error bit will also be set whenever an invalid SPI message is received, even though it may contain 16-bits.

5.1.8 CSB Input

The system MCU selects which slave is to receive SPI communication using separate chip select (CSB) pins. With the CSB in a logic low state, SPI words may be sent to the 33814 via the serial input (SI) pin, and status information is received by the MCU via the serial output (SO) pin. The falling edge of CSB enables the SO output and transfers status information into the SO buffer.

The rising edge of the CSB initiates the following operation:

1. Disables the SO driver (high-impedance)
2. Activates the received command word, allowing the 33814 to activate/deactivate output drivers.

To avoid any spurious data, it is essential that the high-to-low and low-to-high transitions of the CSB signal occur only when SCLK is in a logic low state. Internal to the 33814 device is an active pull-up to V_{CC} on CSB. In cases where voltage exists on CSB without the application of V_{CC} , no current will flow from CSB to the VCC pin. This input requires CMOS logic levels referenced to V_{CC} and has an internal active pull-up current source.

5.1.9 SI Input

The SI pin is used for serial instruction data input. SI information is latched into the input register on the rising edge of SCLK and the input data transitions on the falling edge of SCLK. A logic high state present on SI will program a one in the command word on the rising edge of the CSB signal. To program a complete word, 16 bits of information must be entered into the device. This input requires CMOS logic levels referenced to V_{CC} .

5.1.10 SO Output

The SO pin is the output from the SPI shift register. The SO pin remains high-impedance until the CSB pin transitions to a logic low state. All normal operating drivers are reported as zero, all faulted drivers are reported as one. The negative transition of CSB enables the SO driver.

The SI/SO shifting of the data follows a first-in-first-out protocol, with both input and output words transferring the most significant bit (MSB) first.

The serial output data is available to be latched by the MCU on the rising edge of SCLK. The SO data transitions on falling edge of the SCLK. This output provides CMOS logic levels referenced to V_{CC} .

5.1.11 KEYSW Input

KEYSW is the input from the vehicle ignition keyswitch. This signal is at V_{BAT} (12 V) when the key is inserted and turned to the ON position. When the key is in the OFF position and/or removed from the keyswitch, this input is pulled to ground by an internal pull-down resistor. When this signal is low, and the PWREN SPI Control register bit is also low, the 33814 is in the Sleep mode. If the PWREN SPI control register bit is logic one, when the KEYSW goes low, only the outputs are turned off (except ROUT2 if the Shut Down Disable bit is set). When the PWREN SPI Control register bit also goes to zero, the entire circuit enters Sleep mode. When KEYSW signal goes high, it wakes up the IC, turns on the V_{PP} regulator and a Power On Reset signal is generated. This pin is internally protected against a reverse battery condition by an internal diode.

The state of the KEYSW input is also available as a bit in the SPI Status Register.

5.1.12 PWREN SPI Control Register BIT

The PWREN signal is a bit in the SPI Control Register that, along with KEYSW, BATSW, and the ROUT2 output can provide the power start-up logic of the vehicle.

The purpose of the PWREN signal is allow the MCU to control the shutdown of power to itself when the user turns off the KEYSW. This may be necessary to allow the MCU the time required to perform its pre-shutdown routines.

When the MCU wants to shutdown the power supplies in the 33814, it must write a logic zero (0) to the PWREN bit in the SPI Control register. Only the state of the PWREN bit in the SPI Control register will control the shutdown of the 33814 power supplies.

5.1.13 BATSW Output

The BATSW output pin is a 5.0 V logic level output that by default is an indication of the state of the KEYSW input. When KEYSW is at V_{BAT} (12 V) level the BATSW output is a logic 1 (5.0 V), and when KEYSW is at ground (0 V) level, BATSW is at a logic 0. The BATSW output may be used to inform the MCU that the user is trying to shutdown the vehicle.

The BATSW output can also be used to control an LS driver, such as the Relay 2 driver, by connecting the BATSW output to the RIN2 input.

In certain packaged options of the 33814, the BATSW signal is not brought out to a pin. In this case, the BATSW signal can still be determined by the MCU by reading the state of BATSW bit in the SPI Status register. The MCU can then control the ROUT2 (Relay 2 output) by setting the "RIN2" bit in the SPI Control register.

If the BATSW signal is not needed by the MCU or to control the Relay 2 output, it can also be configured as a low current LED high side driver controlled through the SPI interface. As a high side driver, BATSW can also be PWM'd to allow an LED to be dimmed. A bit in the SPI Battery Switch Logic Output Configuration register called "HSD", controls whether the BATSW output will be a simple high side driver, or will be controlled by KEYSW as indicated above.

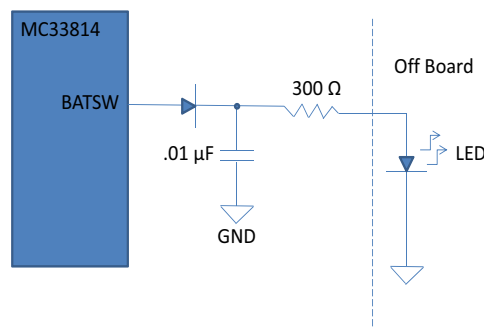


Figure 7. Recommended Circuit to Use BATSW as an LED Driver

If the BATSW output is used to control an LED, the LED cathode should be tied to ground and the LED anode should be connected to the BATSW pin through an external resistor. The value of the external resistor should be 340 ohms or greater. Care must be taken if the BATSW output is sent off-board due to the chance of shorts to the battery or shorts to ground, for which the output is not protected. At a minimum, this output should be protected by a diode, the current limit resistor, and an ESD capacitor (.01 μ F ceramic).

5.1.14 Using ROUT2 as a Power Relay

The ROUT2 (Relay 2 Output) can be used to drive a power relay. The RIN2 input or the RIN2 bit in the SPI Control register can be used to turn the ROUT2 output on or off as desired. The BATSW output can be connected to the RIN2 input to control the power relay, or the MCU can chose to control the RIN2 bit in the SPI Control register to actuate the power relay.

The ROUT2 output is unique in that it can be kept turned on even after KEYSW is turned off (as long as the PWREN bit is still set to a one) by setting the shut down disable (SDD) bit in the ROUT2 Configuration register.

5.1.15 ISO9141 Transceiver (MTX, MRX, ISO9141)

These three pins are used to provide an ISO9141, K-line communication link for the MCU to provide diagnostic support for the system. MRX is the 5.0 V logic level serial output line to the MCU. MTX is the 5.0 V logic level serial input to the IC from the MCU. The ISO9141 pin is a bi-directional line, consistent with the ISO9141 specification for signalling to and from the MCU. There is only one bit in the SPI Status register to indicate an overtemperature fault from the ISO9141 functional block. There are no Configuration or Control registers associated with this functional block.

5.1.16 Tachometer (TACHOUT)

The TACHOUT pin is a low side driver, that can used to drive a tachometer meter movement. TACHOUT can be programmed via the SPI to:

1. Output the same signal as VRSOUT divided by a 1 to 32 programmable divider,
2. Output a PWM signal with a frequency and duty cycle programmable via the SPI, or
3. Output one of 8 fixed frequencies as indicated in [Table 6](#).

If a tachometer is not required the TACHOUT output can also be used as a low current, SPI controlled, low side driver to drive a LED or other low current load. The SPI Configuration register for the Tachometer is used to determine which mode this output will be used in. The TACHOUT output handles overcurrent (OC) differently than the other low side drivers. When an overcurrent limit is reached the TACHOUT output does not enter a current limiting state but rather shuts the output off to protect the output device. The retry option works similarly to the other low side drivers.

In the LSD mode bit 4 of the SPI Configuration register controls the turn on or turn off of the Open Load detect current sink.

Table 6. TACHOUT SPI Configuration Register

| SPI Configuration Register 4 Bits 6,5 | TACHOUT Mode |
|---------------------------------------|--|
| 00 (default) | VRSOUT divided by 'N' where 'N' is defined by bits 0 thru 4 of SPI Configuration Register 4 (1 - 32) 00001 = 1 (default) . 11111 = 31 00000=32 |
| 01 | Oscillator Output |
| 10 | Low Side Driver (LSD) |
| 11 | Same as 10 above |

Table 7. TACHOUT SPI Configuration Register

| SPI Configuration Register Bits 2,1,0 | Oscillator Frequencies |
|---------------------------------------|-----------------------------------|
| 000 (default) | 10 Hz |
| 001 | 100 Hz |
| 010 | 1.0 kHz |
| 011 | 5.0 kHz |
| 100 | 10 kHz |
| 101 | 20 kHz |
| 110 | 40 kHz |
| 111 | 100 kHz (not recommended for use) |

Table 8. TACHOUT SPI CONFIGURATION REGISTER

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-------------------------|-------------------------------|--------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| Retry Enable | V _{RSOUT} /LSD | V _{RSOUT} /Osc. mode | OL Current Sink Enable | In-Rush Delay | Output Freq. 2 | Output/PWM Freq. 1 | Output/PWM Freq. 0 |
| (0) | (0) | (0) | (0) ÷ N ₁₆ | (0) ÷ N ₈ | (0) ÷ N ₄ | (0) ÷ N ₂ | (1) ÷ N ₁ |

5.1.17 INJIN1, INJIN2 Inputs

The INJIN1 and INJIN2 pins are the parallel inputs that control the injector outputs, INJOUT1 and INJOUT2 respectively. The INJIN1 and INJIN2 pins are logic level inputs with built-in pull-downs to ground to prevent accidental actuation of an injector if the connection to the pin is lost. As a default, INJIN1 and INJIN2 inputs are OR'd with the injector control bits in the SPI ON/OFF control word. This is to allow the INJOUT's to be controlled by either the INJIN's (parallel inputs) or via the SPI when either injector driver is being used for purposes other than injector drive.

5.1.18 INJOUT1, INJOUT2 Driver Outputs

These output pins are the injector driver outputs for the two injectors that the IC supports. If two injectors are not needed, one INJOUT can be used as a general purpose low side driver for relays, motors, lamps, gauges, etc. The injector driver outputs can be controlled by the parallel input (INJINx) or the appropriate bit in the SPI Injector Command register. The injector outputs can also be PWM'd via the SPI for use as variable speed motor drivers, LED/lamp dimming drivers, or as a fuel pump driver. Injector outputs are forced off during all RESET events.

5.1.19 RIN1, RIN2 Inputs

The RIN1 and RIN2 pins are the parallel inputs that control the relay outputs, ROUT1 and ROUT2 respectively. The RIN1 and RIN2 pins are 5.0 V logic level inputs with built-in pull-downs to ground to prevent accidental actuation of a relay if the connection to the pin is lost. As a default, RIN1 and RIN2 inputs are OR'd with the Relay control bits in the SPI ON/OFF control word. This is to allow the ROUT's to be controlled by either the RIN's (parallel inputs) or via the SPI when either relay driver is being used for purposes other than relay drive.

5.1.20 ROUT1, ROUT2 Driver Outputs

These are output pins for ROUT1 and ROUT2 low side drivers. These outputs have different current ratings and can be used to drive relays or other inductive loads. Each output is controlled via the SPI or via the RINx logic inputs. Each output has a pull-down current sink that can be enabled via the SPI to provide open load diagnostics. The open load detect current sink can be

disabled via the SPI to allow the outputs to be used as LED drivers. The ROUTx outputs can also be PWM'd via the SPI for use as variable speed motor drivers, LED/lamp dimming drivers, or as a fuel pump driver (ROUT1). All control and configuration for the ROUT's is via the SPI ROUT1 and ROUT2 ON/OFF word in the SPI Control register and the individual ROUT1 and ROUT2 words in the SPI Control register.

The ROUT2 relay output can be configured in SPI to drive a power relay controlled by the BATSW signal.

5.1.21 LAMPOUT Driver Output

The Lamp driver output, LAMPOUT is a low side driver capable of driving an incandescent lamp. The current limit contains a programmable delay to allow the driver to handle the inrush current of a cold lamp filament. A pull-down current sink is provided to allow the IC to detect when the bulb is burned out (open filament). The turn on and off of the LAMP is via the SPI ON/OFF Control register word and it also has the ability to be PWM'd for advanced diagnostic (dimming) purposes via the SPI Lamp Control register. The output can also be used to drive a LED if the open load detect current sink is commanded off via SPI, to prevent "ghosting". The LAMPOUT SPI Configuration Register contains the following bits.

Table 9. LAMPOUT SPI Configuration Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|-----|------------------------|---------------|-----|-------------|-------------|
| Retry Enable | x | x | OL Current Sink Enable | In-Rush Delay | x | PWM Freq. 1 | PWM Freq. 0 |
| (0) | (0) | (0) | (1) | (1) | (0) | (0) | (0) |

The Retry Enable bit, bit 7, when set will allow the output to turn on for a short period and off for a long period when an over current condition is present. The open load (OL) current sink disable allows the current sink to be turned off when using the driver as an LED driver to prevent ghosting, where the LEDS appears to be partially on due to the OL current sink. It can also be turned off to measure the output device leakage. The Inrush delay bit, when set (by default for the Lamp driver) waits an additional time before annunciating an overcurrent condition. This is done to allow for the inrush current of an incandescent lamp. The internal PWM duty cycles (D/C) are controlled by the lower 7 bits in the corresponding SPI Control Register. The external duty cycles are provided by the MCU on the input pin of the corresponding output driver. In PWM mode, for PWM periods and on times that are greater than the retry timer, retry works identical to non-PWM mode. For PWM periods and on times that are less than the retry timer, the PWM takes precedence and overrides the retry function.

| Bits 1, 0 | PWM Frequency | PWM D/C |
|-----------|---------------------|---------------------|
| 00 | None or on ext. pin | None or on ext. pin |
| 01 | 100 Hz | Internal |
| 10 | 1 KHz | Internal |
| 11 | On ext pin ÷ 100 | Internal |

5.1.22 VRSP, VRSN Inputs, VRSOUT Output

The 33814 contains a VRS input conditioning circuit that employs a differential input. VRSP and VRSN are the positive and negative inputs from the VRS (See [Figure 8](#)). Internal zener diode clamps to ground and V_{CC} limit the input voltage to within the safe operating range of the circuit. It is important to provide external 15 k current limiting resistors to prevent damage to the VRSP and VRSN inputs (See [Figure 8](#)). The VRS circuit conditions and digitizes the input from the crankshaft mounted toothed wheel to provide an angle clock and RPM data to the MCU. This circuit provides a comparator with multiple thresholds, which are programmed via the SPI to allow the VRS circuit to handle different sensors and the wide dynamic range of the VRS output at engine speeds from crank to running. The output of this circuit is provided on the VRSOUT pin, which is a 5.0 Volt logic level signal to the MCU. The comparator threshold values can also be controlled automatically based on the input signal amplitude. The output of the comparator contains a programmable one shot, noise blanking circuit. The time value of this blanking pulse can be selected via the SPI as a percentage of the last input high (or low) pulse. The VRSOUT output can also be divided and sent to the TACHOUT pin to drive a tachometer.

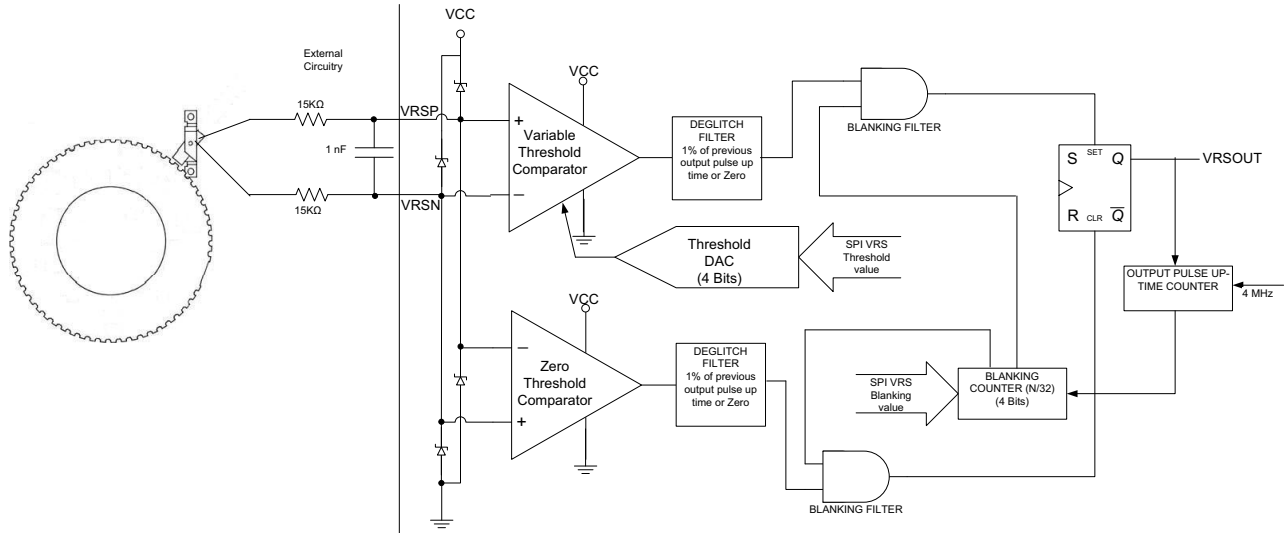


Figure 8. VRS Schematic

Table 10. SPI VRS Manual Configuration Register

| SPI VRS Manual Parameters Configuration Register Bits 7, 6, 5, 4 | Threshold Values (nominal) |
|---|---|
| 0000 | 0.01 - 28 mV (At 10 mV threshold, Tolerance not specified, and monotonicity not guaranteed) |
| 0001 | 0.01 - 36 mV (At 14 mV threshold, Tolerance not specified, and monotonicity not guaranteed) |
| 0010 | 3.0 - 38 mV (Tolerance not specified below 110 mV threshold. Only specified for monotonicity.) |
| 0011 | 5.0 - 50 mV (Tolerance not specified below 110 mV threshold. Only specified for monotonicity.) |
| 0100 | 21 - 55 mV (Tolerance not specified below 110 mV threshold. Only specified for monotonicity.) |
| 0101 (default) | 25 - 80 mV (Tolerance not specified below 110 mV threshold. Only specified for monotonicity.) |
| 0110 | 56 - 92 mV (Tolerance not specified below 110 mV threshold. Only specified for monotonicity.) |
| 0111 | 110 mV $\pm 20\%$ |
| 1000 | 150 mV $\pm 20\%$ |
| 1001 | 215 mV $\pm 20\%$ |
| 1010 | 300 mV $\pm 20\%$ |
| 1011 | 425 mV $\pm 20\%$ |
| 1100 | 600 mV $\pm 20\%$ |
| 1101 | 850 mV $\pm 20\%$ |
| 1110 | 1.210 V $\pm 20\%$ |
| 1111 | 1.715 V $\pm 20\%$ |

5.1.23 Controls for the VRSN and VRSP Inputs

The VRS can be connected to the 33814 in either a differential or single-ended fashion. The use of differential filtering capacitor, and grounded capacitors of at least 100 nF are also advisable. In some applications, a damping resistor of approximately 5.0 kOhm directly across the pickup coil is also useful to minimize high frequency ringing.

5.1.24 GND VRSN Bit

To use the VRS inputs in a single-ended configuration the “GND VRSN” bit in the SPI Configuration register must be set to indicate to the 33814 that this mode is being used. The VRS is then connected between the VRSP input and ground. The default for this bit is zero (0) indicating that the differential mode is selected.

5.1.25 2.5 Volt Reference Disconnect Bit

The disconnect 2.5 Volt reference bit in the SPI VRS configuration register is used to disconnect the internal 2.5 Volt reference signal from the VRSN and VRSP inputs, so that an external reference voltage can be employed. The default state of this bit is zero (0), indicating that the internal 2.5 Volt reference voltage is connected to the VRSN and VRSP inputs.

5.1.26 Selecting the Input Threshold and Blanking Time

Two different SPI registers are provided to control the VRS circuit values in the manual mode. The SPI VRS configuration register is used to set the “engine running” values for the threshold and blanking filter and the SPI VRS control register is used to provide the “engine cranking” threshold and blanking filter values. Once the engine is running, the MCU clears the SPI VRS control register and the 33814 will use the values found in the SPI VRS configuration register.

5.1.27 Input Comparator Threshold Values

The threshold voltage for the input comparator is produced by a 4-bit D/A converter. The control of the D/A output value is by means of the upper four bits of the SPI VRS configuration register or the upper four bits of the SPI VRS control register. When the contents of the SPI VRS control register contains all zeros, the binary value for the D/A threshold is taken from the value in the SPI VRS configuration register. When the contents of the SPI VRS control register is non-zero, then the value in the upper four bits of the SPI VRS control register is used to set the D/A output. The values outputted by this D/A, using either the SPI VRS control register or the SPI VRS Configuration register, are listed in [Table 10](#) in the threshold values table. The blanking one-shot time is also set via the lower 4 bits of the SPI VRS configuration register or the SPI VRS control register using the same condition, as described previously for the threshold D/A.

5.1.28 Blanking Time Definitions

The values for the one shot blanking, as a percentage of the last high output pulse period is shown in [Table 11](#).

Table 11. SPI VRS Manual Configuration Register

| SPI VRS Configuration/Control Register Bits 3,2,1,0 | Blanking Time in% (of last pulse high period) |
|---|---|
| 0000 (default) | 0.0 |
| 0001 | 3.12 |
| 0010 | 6.25 |
| 0011 | 9.37 |
| 0100 | 12.5 |
| 0101 | 15.62 |
| 0110 | 18.75 |
| 0111 | 21.87 |

Table 11. SPI VRS Manual Configuration Register

| SPI VRS Configuration/Control Register Bits 3,2,1,0 | Blanking Time in% (of last pulse high period) |
|---|---|
| 1000 | 25 |
| 1001 | 28.1 |
| 1010 | 31.3 |
| 1011 | 34.4 |
| 1100 | 37.5 |
| 1101 | 40.6 |
| 1110 | 43.8 |
| 1111 | 46.9 |

5.1.29 Manual and Automatic Modes

The SPI VRS miscellaneous configuration register has a bit to enable the automatic selection of the comparator threshold (bit 7). At this time, the operation of automatic mode remains TBD.

5.1.30 VRS Peak Detector

The VRS peak detector determines the magnitude of the positive peak of the VRS input signal and digitizes it. The value of the VRS peak voltage is reported in the VRS SPI status register bits 7, 6, 5, and 4. The MCU can read the value of peak voltage after the zero crossing time of the input pulse, and uses this information to set the threshold and blanking parameters for subsequent input pulses. Status bits reflect the last detected peak and only read 0000 after a POR or SPI reset command.

Table 12. Peak Detector Output in SPI VRS Status Register

| SPI VRS Status Register Bits 7,6,5,4 | Peak Values (nominal) |
|--------------------------------------|-----------------------|
| 0000 | 10 mV |
| 0001 | 14 mV |
| 0010 | 20 mV |
| 0011 | 28 mV |
| 0100 | 40 mV |
| 0101 | 56 mV |
| 0110 | 80 mV |
| 0111 | 110 mV |
| 1000 | 150 mV |
| 1001 | 2125 mV |
| 1010 | 300 mV |
| 1011 | 425 mV |
| 1100 | 600 mV |
| 1101 | 850 mV |
| 1110 | 1.210 V |
| 1111 | 1.715 V |

5.1.31 VRS Deglitching Filters

The VRS input circuit has additional filters on the rising and falling edges of the input waveforms to reduce the effect of short transitions that may occur during those noise sensitive times. The deglitching filters are approximately 1% of the last positive pulse period. The deglitch filters are enabled by setting the deglitch bit (bit 3) in the SPI VRS miscellaneous parameters configuration register. This bit is, by default, zero (0), meaning that the deglitch filters are disabled.

5.1.32 High/Low Reference Bit

The High/Low reference bit in the SPI VRS miscellaneous configuration register is used to change the use of the input high pulse timing to input low pulse timing, in cases where an elongated tooth wheel is being used rather than the missing tooth wheel. The default for this bit is zero (0), indicating the use of a crankshaft wheel with a missing tooth (or teeth).

5.1.33 Disable VRS bit

The disable VRS bit in the SPI VRS miscellaneous configuration register is used to disable the VRS input circuitry when there is no need for a VRS input conditioning circuit. This would be the case, for example, if the crankshaft wheel sensor was a hall effect device whose output could be directly input to the MCU. The default for this bit is zero (0) indicating that the VRS input conditioning circuitry is active.

5.1.34 Clamp Active Status bits

There are two clamp active status bits in the SPI VRS status register. One is for the low pulse clamp and the other is for the high pulse clamp. When either of these bits are a one (1), it indicates that the peak voltage for that part of the input waveform has exceeded the clamp voltage and is being clamped to the high or low voltage limit. These status bits can be used to indicate that the engine has attained the speed necessary to switch from “cranking” values for the threshold and blanking (in the SPI VRS control register) to the “running” values. (in the SPI VRS configuration register).

5.1.35 Pre-driver Operation

There are three identical pre-drivers in the 33814. Each pre-driver can be configured as either an ignition (IGBT) pre-driver or a general purpose gate driver (GPGD). By default, one pre-driver is configured as a GPGD (O2HOUT) and two pre-drivers are configured as ignition (IGNOUT1, IGNOUT2) pre-drivers.

A bit in each of the SPI Configuration registers, for each pre-driver, defines whether the pre-driver behaves as an ignition or a GPGD pre-driver.

It should be noted that there are only two current measurement circuits, ISGSENSP/N and O2SENSP/N. When all three pre-drivers are used as GPGD, then ISGSENSP/N is associated with the IGNOUT1 pre-driver only, and the O2SENSP/N is associated with the O2OUT pre-driver. The IGNOUT2 pre-driver will not have an associated current sense circuit and will rely on Short to Battery (drain voltage sense) protection only. When all three pre-drivers are used as ignition pre-drivers, then IGNOUT1 and IGNOUT2 will share the ISGSENSP/N current measurement circuit, and IGNOUT3 (O2HOUT) will have its own current sense circuit, O2SENSP/N.

5.1.36 O2HIN Input

The O2HIN pin is the parallel input that controls the O2HOUT pre-driver output. The O2HIN pin is a 5.0 V logic level input with a built-in pull-down to ground to prevent accidental actuation of the pre-driver output if the connection to the pin is lost. As a default, the O2HIN input is ORed with the O2HOUT control bit in the SPI ON/OFF control word. This is to allow the O2HOUT to be controlled by either the O2HIN (parallel input) or via the SPI.

5.1.37 O2HOUT Pre-driver Output with Drain Feedback Input O2HFB

The O2HOUT output is a pre-driver output that controls the gate of a MOSFET to drive a heater on an O2 (Lamda) sensor. The pre-driver is capable of driving most power MOSFETs. The O2HOUT output and associated drain feedback pin O2HFB provide short to battery, overcurrent protection for the external driver MOSFET. More accurate current control can be provided by placing a current sense resistor between the O2SENSP and O2SENSN pins.

Output-off open circuit (OL) and output-on overcurrent (OC) faults are detected and annunciated via the SPI.

5.1.38 IGNIN1 and IGNIN2 Inputs

The IGNIN1 and IGNIN2 pins are the parallel inputs that control the IGNOUT1 and IGNOUT2 pre-driver outputs, respectively. The IGNIN1 and IGNIN2 pins are 5.0 V logic level inputs with built-in pull-downs to ground to prevent accidental actuation of a pre-driver output if the connection to the pin is lost. As a default, IGNIN1 and IGNIN2 inputs are ORed with the IGNOUT1 and IGNOUT2 control bits in the SPI ON/OFF control word. This is to allow the IGNOUTs to be controlled by either the IGNINs (parallel inputs) or via the SPI.

5.1.39 IGNOUT1 and IGNOUT2 Pre-driver Outputs, with Feedback IGNFB1 and IGNFB2, and Current Sense Inputs

The IGNOUT1 and IGNOUT2 outputs are pre-driver outputs that drive an IGBT that controls the ignition coil current to produce a spark. The IGNOUTx outputs and their associated feedback pins IGNFBx provide short to battery and one shared current sense resistor provides overcurrent protection for the external driver transistors. When used as an IGBT driver, a 10:1 voltage divider (9R:1R) must be used on the feedback pins to prevent the 400 Volt flyback from damaging the IC.

If two Ignition pre-drivers are not required, they can be reconfigured, via the SPI, as general purpose gate drivers (GPGDs) used to drive ordinary MOSFETs.

More accurate current control can be provided by placing a current sense resistor between the IGNSENSP and IGNSNSN pins. When both pre-drivers are used as ignition (IGBT) pre-drivers, the both pre-drivers can share one current sense resistor. The input controls will determine the value of the current sense threshold voltage across the current sense resistor. When either one of the inputs is ON, the threshold voltage will be $V_{\text{SENS-TH}}$, but when both inputs are ON simultaneously, the threshold will be raised to $2V_{\text{SENS-TH}}$ to compensate for both pre-drivers being ON.

When one pre-driver is used as an ignition pre-driver and the other pre-driver is used as a GPGD, the current sense circuit is connected ONLY to the ignition driver channel. When both pre-drivers are designated as GPGD pre-drivers, only pre-driver #1 will have use of the current sense circuit, the other pre-driver, #2, will only have short to battery protection via the drain sense voltage comparator.

5.1.40 RESETB

The RESETB pin is a 5.0 volt logic, low level output that is used to reset the MCU. The RESETB pin is an open drain output. Without power on the 33814 circuit, the RESETB pin is held low by an internal pull-down resistor. In a typical application, the RESETB pin must be pulled up externally by a pull-up resistor to VCC. When power is applied to the circuit and the voltage on the VCC pin reaches the lower voltage threshold, the RESETB pin will remain at a low level (open drain FET turned on) for a period of time equal to the time value WD_{RESET} . After this time period, the RESETB pin will go high and stay high until a reset pulse is generated due to any of the following events:

1. A watchdog timer timeout event occurs,
2. An undervoltage event on VCC occurs, or
3. An overvoltage event on VPWR occurs.

A Power On Reset (POR) is always provided upon power ON (i.e. anytime the IC goes from sleep state to active state).

5.1.41 Disabling the Watchdog Timer

Since a watchdog reset occurs, by default 10 seconds after the POR, if the MCU needs to be programmed in-circuit, a means of disabling the watchdog must be provided to avoid interrupting the MCU programming procedure. This disable mechanism can be a jumper between the RESETB pin of the 33814 and the MCU's Reset input pin, or via an isolation resistor placed between the RESETB pin on the 33814 and the MCU's reset input pin that allows the MCU's reset pin to be pulled high independently of the 33814 RESETB. The watchdog can also be disabled via a bit in the SPI WD configuration register.

5.1.42 Internal Reset

There is a bit in the SPI control register that is labelled "Reset". When this bit is set to a one (1) by the MCU, it will instruct the 33814 to perform an internal reset. This reset will NOT toggle the RESETB output pin, but will cause all internal registers to be initialized back to their default values, including clearing the reset bit in the SPI control register.

5.2 MCU SPI Interface Description

The 33814 device directly interfaces to a 5.0 V micro controller unit (MCU) using a 16-bit serial peripheral interface (SPI) protocol. SPI serial clock frequencies up to 8.0 MHz may be used when programming and reading output status information (production tested at 1.0 MHz). [Figure 9](#) illustrates the SPI configuration between an MCU and one 33814.

Data is sent to the 33814 device through the SI input pin. As data is being clocked into the SI pin, other data is being clocked out of the device by the SO output pin. The response data received by the MCU during SPI communication depends on the previous SPI message sent to the device. The SPI can be used to read or write data to the configuration and control registers and to read or write the data contained in the status registers.

The MCU is only allowed to read or clear bits (write zeros) in the status register unless the Power ON Self-test (POST) enable bit in the control register is set. When the POST enable bit is set the MCU can read and write zeros or ones to the status register.

Note that the MCU must clear the POST enable bit before operation is resumed or the status register will not be updated with fault indications.

5.2.1 SPI Integrity Check

One SPI word is reserved as a SPI check message. When bits 12 through 15 are all zero, then the SPI will echo the remaining 12-bit SPI word sent and will flip bits 12 through 14, bit 15 will remain a 0. This allows the MCU to poll the SPI and compare the received message to confirm the integrity of the SPI communication channel to the 33814. There is a SPI error bit in the SPI status register that indicates if an incorrect SPI message has been received. The SPI error bit in the SPI status register is set whenever any SPI message error is detected.

Important A SCLK pulse count strategy has been implemented to ensure integrity of SPI communications. Only SPI messages consisting of 16 SCLK pulses will be acknowledged. SPI messages consisting of other than 16 SCLK pulses will be ignored by the device and reported as a SPI error. Invalid SPI messages, that contain invalid commands or addresses will also be flagged as a SPI error.

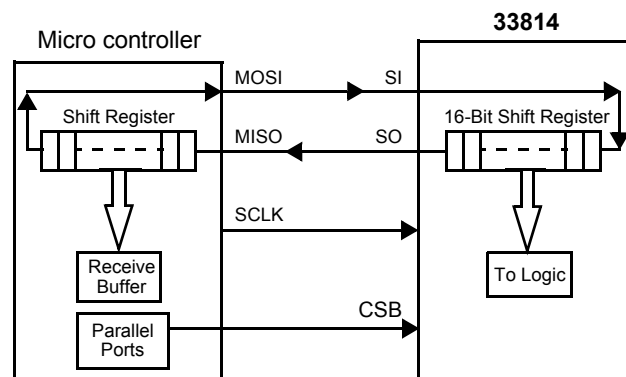


Figure 9. SPI Interface with Microprocessor

Two or more 33814 devices may be used in a module system. Multiple ICs may be SPI configured in parallel only. [Figure 10](#) demonstrates the configuration.

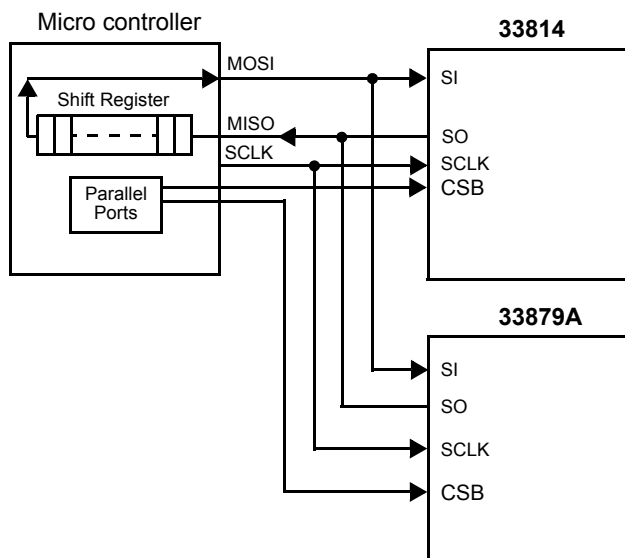


Figure 10. SPI Parallel Interface (Only) with Microprocessor

5.3 Functional Device Operation

5.3.1 Power Supply

The 33814 is designed to operate from V_{PWR_MIN} to V_{PWR_MAX} on the VPWR pin. The VPWR pin supplies power to all internal regulators, and analog and logic circuit blocks.

5.3.1.1 V_{PP} Pre-regulator

The V_{PP} pre-regulator supplies the input voltage to the V_{CC} and V_{PROT} regulators. It uses an external PNP transistor as a pass element. This allows the user to choose the PNP's size and package considerations to meet the system requirements. The amount of power that the external PNP transistor will have to dissipate depends on the maximum voltage the system can be expected to run at and the maximum expected current drawn from the V_{CC} and V_{PROT} regulators. The VPPSENS pin is used to feedback the value of the V_{PP} voltage for regulation. Since the V_{PP} regulator is not intended to supply off-the-board loads, there is no short to ground or short to battery protection on the output of the external PNP.

5.3.1.2 V_{CC} Regulator

The V_{CC} regulator output is used for supplying 5.0 Volts to the MCU, and for setting communication threshold levels via the internal SPI SO driver. The V_{CC} regulator contains an internal pass transistor which is protected against overcurrent.

5.3.1.3 V_{PROT} Regulator

The protected output V_{PROT} is a tracking regulator that uses the V_{CC} output as a reference. Since it is expected that the V_{PROT} regulator will supply 5.0 Volts to external sensors in the vehicle, it is well protected against shorts to battery, shorts to ground and overcurrent. The V_{PROT} supply is enabled at power-on but can be disabled via the SPI control register.

5.3.2 Power ON Reset (POR)

Applying V_{PWR} and bringing KEYSW high (VBAT) will generate a Power On Reset (POR) and place the device in the Normal operating state. The Power On Reset circuit incorporates a timer to prevent high frequency transients from causing an erroneous POR.

Upon enabling the device (KEYSW High), outputs will be activated based on the initial state of the control register or parallel input. All three supplies, V_{PP} , V_{CC} , and V_{PROT} , are enabled when KEYSW is brought high.

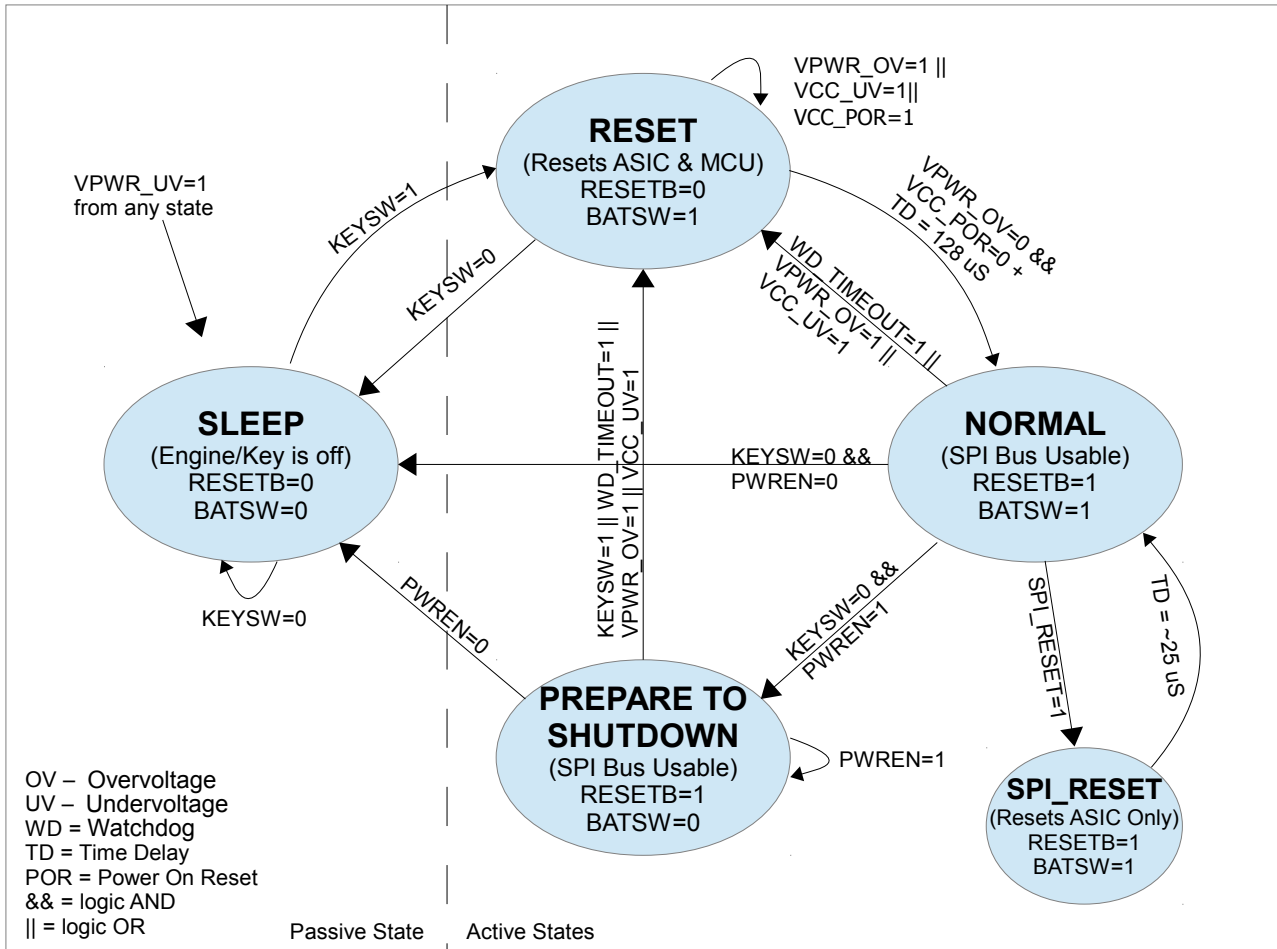


Figure 11. 33814 Functional State Diagram

Table 13. Operational States

| KEYSW Input | PWREN SPI Bit Input | BATSWB Output | All Supplies | STATE |
|-------------|---------------------|---------------|--------------|---------------------|
| L | L | L | OFF | Sleep |
| H | L | H | ON | NORMAL |
| H | H | H | ON | NORMAL |
| L | H | L | ON | Prepare to shutdown |

5.3.3 SLEEP State

Sleep State is entered when the V_{BAT} level signal is removed from the KEYSW pin and the PWREN SPI bit is a logic low. In Sleep state all outputs and current sources and sinks are off and the device consumes less than $I_{VPWR(SS)}$ μA . Applying a V_{BAT} level to the KEYSW pin will force the device to exit the Sleep state and generates a POR.

5.3.4 NORMAL State

The default NORMAL state is entered when power is applied to the VPWR and the KEYSW pin.

Note that the device is designed to have V_{PWR} present before KEYSW is brought high. It is acceptable to bring VPWR and KEYSW high simultaneously, however it is not recommended to bring KEYSW high while VPWR is low.

SPI register settings from Power-ON Reset (POR) are as follows:

- All outputs turned off.
- Off State open load detection enabled (LSD)
- Default values in the SPI Configuration, Control and Status registers.

5.3.5 Power On Self-test (POST)

At power on, after a POR, it may be desired to go through an initial Power On Self-test routine to ensure that the SPI is working correctly and the status registers in the 33814 are viable. After a POR, all the registers in the 33814 contain their “default” values, as indicated in the SPI register tables later in this document. The watchdog is also set to its default timeout value of 10 seconds, so any POST routine must be accomplished within this time frame or a WD reset may occur. To perform a POST routine, the MCU should first send a SPI message to set the POST enable bit in the SPI control register 1, bit 6. Once this bit is set, the status registers are disconnected from the analog and logic portions of the 33814, and are connected only to the SPI circuitry. The POST can then write various data patterns to the status registers and verify that none of the bits are “stuck” or otherwise unworking. Note that bits in the status register labelled “x” are not implemented and when testing these bits may result in erroneous data. After testing all the status registers and confirming that they are viable, the status registers can be set back to their default values by clearing the POST Enable bit back to 0. The POST enable bit allows the MCU to write ones (1s) to the Status registers.

Normally, the status register can only be cleared to zeros by the MCU and written ones by the 33814 internal logic. This was designed to prevent the MCU from missing any reported fault bits, and for the 33814, to prevent system status errors that could result from the MCU erroneously writing a one (1) to a fault bit.

Once the POST enable bit is set back to a zero (0) by the MCU, the status register returns to the condition where the 33814 can only write ones(1s) to it and the MCU can only write zeros (0s) to it.

Again, it is important to note that any POST routine should be designed to take less than 10 seconds to avoid a watchdog reset from occurring and truncating the POST routine because the WD reset will clear the POST Enable bit as well.

The 33814 IC has two modes of operation, Normal mode, and Sleep mode.

5.3.6 Watchdog (WD)

5.3.6.1 Watchdog Normal Operation

The watchdog is a programmable timer that is used to monitor the operation of the MCU. When the MCU is executing code properly, its program code should contain instructions to periodically send a SPI message to the watchdog SPI control register to refresh the watchdog. The watchdog timer, once refreshed, will reload the time interval value stored in the SPI watchdog configuration register and begin counting time again. Under normal operating conditions this sequence will continue until the MCU shuts down, typically, when the KEYSW is turned off.

5.3.6.2 Watchdog Fault Operation

In the event that something goes wrong during the MCU program execution, such as an unexpected breakpoint or other program hang-up such as the execution of a HALT instruction, the watchdog may not be refreshed. When the WD time interval value programmed in the SPI Configuration register elapses, the watchdog will issue a RESETB pulse. This RESETB pulse will cause the MCU to restart its program and correct operation should be restored.

After any RESETB (power-on or other), the watchdog SPI configuration register will contain the default value for the refresh time, 10 seconds. The watchdog is also enabled by default.

The MCU, in its initialization (start-up) code, can choose to change this default value and/or disable the watchdog by sending a SPI command to write new information in the watchdog SPI configuration register.

5.3.6.3 Watchdog SPI Configuration Register

There are seven bits in the watchdog SPI configuration register which define the time value that is loaded into the watchdog timer. Bits 3, 2, 1, 0 are a Binary coded decimal (BCD) value from 1 to 10. (11 to 16 are mapped to 10 and 0 is mapped to 1) The remaining three bits, 6, 5, and 4 are the time multiplier values. There are three time multiplier values so only one bit, 6, 5, or 4 may be set at one time. Setting more than one bit will result in the highest multiplier value getting precedence.

Bit 7 is the watchdog enable(1) or disable(0) bit.

The time multipliers are as follows:

Bit 6 = x1 seconds (s)

Bit 5 = x 100 milliseconds (ms)

Bit 4 = x 10 milliseconds (ms)

The register in [Table 14](#) shows the watchdog enabled and the time value of 10 seconds. Using this technique, time values from 1.0 ms. to 10 seconds can be programmed into the watchdog.

Table 14. Watchdog SPI Configuration Register

| Enable/ Disable | x1 sec. | x100 ms. | x10 ms. | 8 | 4 | 2 | 1 |
|--------------------|---------|----------|---------|---|---|---|---|
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |

5.3.6.4 Watchdog SPI Control Register

The watchdog relies on Bit 7 of the watchdog SPI control register being written as a one (1) to refresh the watchdog timer. (i.e. reload the time value from the watchdog SPI configuration register) The watchdog SPI control register can also be loaded with a time value to temporarily set a different value in the watchdog timer for the next cycle.

Table 15. Watchdog SPI Control Register

| Refresh | x1 sec. | x100 ms. | x10 ms. | 8 | 4 | 2 | 1 |
|---------|---------|----------|---------|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

When Bits 6 thru 0 in the watchdog SPI control register are zero, the value stored in the watchdog SPI configuration register will be loaded into the watchdog timer. If there is a temporary time value written into the watchdog SPI control register then that value will be loaded into the watchdog. Since the watchdog SPI control register is automatically cleared to zero when the watchdog timer is loaded, the next watchdog timer load will be from the value stored in the watchdog SPI configuration register, unless a new temporary time value is again written to the watchdog SPI Control Register.

Example:

To enable and set the watchdog for a timeout value of 200 ms, the MCU will write the following byte into the watchdog SPI configuration register:

Table 16.

| Enable/ Disable | x1 sec. | x100 ms. | x10 ms. | 8 | 4 | 2 | 1 |
|--------------------|---------|----------|---------|---|---|---|---|
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

In the main loop of the MCU's program there will be a call to a routine to write the following byte into the watchdog SPI Control Register to refresh the watchdog periodically (must be < 200 ms).

Table 17.

| WD Refresh | x1 sec. | x100 ms. | x10 ms. | 8 | 4 | 2 | 1 |
|------------|---------|----------|---------|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

5.3.7 Low Side Drivers (LSD)

The six open drain low side drivers (LSDs) are designed to control various automotive loads such as injectors, fuel pumps, solenoids, lamps, and relays, etc. Each driver includes off-state open load detection, on-state short to ground detection, short-circuit to battery protection, overcurrent protection, overtemperature protection, and diagnostic fault reporting via the SPI. The LSDs are individually controlled through the parallel input pins or/and via the SPI. All outputs except ROUT2 are disabled when the KEYSW input pin is brought low regardless of the state of the input pins. All outputs, including ROUT2 are disabled when the RESETB pin is low.

5.3.7.1 LSD Input Logic Control

The LSDs (and the pre-drivers) are controlled individually using a combination of the external pin input (if one exists) and/or a SPI On/Off Control bit. The logic can be made to turn the outputs on or off by means of a logical combination of the external pin ORed with the SPI Control On/Off Bit or a logical combination of the external pin ANDed with the SPI Control On/Off Bit. A separate OR/AND select bit is found in the SPI configuration registers to accomplish this selection.

5.3.7.2 Pulse Width Modulation Mode

Besides just turning the outputs ON or OFF, the outputs can be Pulse Width Modulated (PWM'd) to control the outputs with a variable 0 to 100% duty cycle at a selection of different frequencies. There are two built-in PWM frequencies (100 Hz and 1.0 kHz) and the external input pin can also be used as either an external PWM frequency input (divided by 100) or a total PWM (frequency and duty cycle) input. Two bits (Bits 1, 0) in the SPI configuration register control which mode of input control is selected.

The internal PWM duty cycles (D/C) are controlled by the lower 7 bits in the corresponding SPI control register. The duty cycle for the internal PWM is in 1% increments and is specified in the SPI control register as a 7 bit binary word which provides 128 different binary combinations. The binary values of 0000000 to 1100100 represent 0% to 100% and the binary values 1100100 to 1111111 (100 to 127) all map to 100%.

The external PWM duty cycles (D/C) are provided by the MCU on the input pin of the corresponding output driver.

Table 18.

| Bits 1, 0 | PWM Frequency | PWM D/C |
|-----------|---------------------|---------------------|
| 00 | None or on ext. pin | None or on ext. pin |
| 01 | 100 Hz | Internal |
| 10 | 1.0 kHz | Internal |
| 11 | On ext pin ÷ 100 | Internal |

5.3.7.3 LSD Output Protection

Output protection consists of a dual strategy which utilizes overcurrent and/or overtemperature sensing to detect a fault and then automatically control the output to protect the output device from damage.

5.3.7.4 Overcurrent (OC) Protection

The first protection scheme works by sensing an overcurrent condition by monitoring the voltage on the individual output device drain.

When the SPI configuration retry enable bit is set to a one (1), the default state, during an overcurrent event the device enters current limit and will remain in current limit for a fixed time period. At the end of this time period the output device will turn off and wait a delay time roughly 100 times greater than the on time. The output will try to turn on again after this off time. If the short is still present, the process will start again. This on/off cycling will continue until the output is commanded off or the overtemperature (OT) on the output device is reached.

If the SPI configuration register retry enable bit is set to a zero (0), this on/off cycling will not occur and the output will turn off if the overcurrent threshold is reached. The output will not turn on again until the output is commanded off and then on again.

The Inrush Delay bit, in the SPI Configuration Register for each output, when set to a one(1), will prevent the overcurrent fault bit from being set and the overcurrent protection from shutting off the output for t_{INRUSH} time rather than t_{SC} .

Table 19. Inrush Delay Bit

| Inrush Delay Bit | Timer Value |
|------------------|---------------------|
| 0 | t_{SC} |
| 1 | t_{INRUSH} |

5.3.7.5 Temperature Limit (OT) Protection

The second protection scheme works by sensing the local temperature of the individual output device. During an overcurrent event, the device enters current limit and will remain in current limit until the output driver maximum temperature limit is exceeded (OT). At this point, the device will shutdown automatically, regardless of the input state. The output will try to turn on again only when the junction temperature falls below the maximum temperature minus the T_{LIM} hysteresis temperature value and the input state is commanding the output to be on. The T_{LIM} hysteresis value is specified in the static parameter table.

The temperature limit (T_{LIM}) protection is independent of the overcurrent protection and is not controlled by the SPI. T_{LIM} is always enabled and is always a retry operation.

Outputs may be used in parallel to drive higher current loads provided the turn-off energy of the load does not exceed the energy rating of a single output driver.

5.3.7.6 Output Driver Diagnostics.

Overcurrent (OC), temperature limit (OT) exceeded, short to ground (SG), and open load (OL) conditions are reported through the status register for each driver (no SG for the tachometer). Only open load and overcurrent are reported for pre-drivers. There is also a bit in the SPI status register to indicate when any of the LSDs or pre-drivers are reporting a fault and when a particular output has any of the four possible fault conditions present. This makes it easy for the MCU to poll for fault conditions by looking for a single bit in one register to detect the presence of any fault in the circuit.

5.3.7.7 Open Load Pull-down Current Enable/Disable Bit

An open load condition is detected by the voltage level on the drain of the MOSFET in the off state. Internal to the device is a pull-down current sink. This current sink may be disabled by clearing the appropriate bit in the in the LSD configuration register. When the current sink is disabled, the off-state open load fault status bit will be forced to a logic 0.

5.3.7.8 Open Load and Short to Battery Strategy

The injectors, lamps, relays, and tachometer low side outputs are capable of detecting an open load in the off state and short to battery condition in the on state. All faults are reported through the SPI status register communication. For open load detection, a current source is placed between the MOSFET drain pin and ground of the IC. An open load fault is reported when the drain voltage is less than the listed threshold. Open load fault detect threshold is set internally to the listed threshold and may not be programmed. A shorted load fault is reported when the drain pin voltage is greater than the programmed short threshold voltage when the device is in the on state.

The open load and short to battery fault threshold voltage is fixed and cannot be modified via the SPI.

5.3.7.9 Short to Ground Strategy

The Injectors, Lamps, and Relays (but not the Tachometer) low side driver outputs are capable of detecting a short to ground by measuring the current flow in the output device and comparing it to a known current value. If a short to ground is detected it is annunciated via a bit in the appropriate SPI status register.

5.3.8 SPI REGISTER DEFINITIONS

There are three basic SPI register types:

Configuration Registers - used to set the operating modes and parameters for the 33814 functional blocks. Each output can be configured by setting the individual bits in the configuration register for that output according to the descriptions in the previous functional descriptions for each particular output.

Control Registers - used to turn outputs on and off and set the PWM duty cycle for outputs that are used as PWM outputs. Also used to set the temporary operating parameters for the watchdog timer and the VRS circuit.

Status Registers - used to annunciate faults and other values that the MCU may need to act upon. Each output and functional block has a status register associated with it and the individual fault bits for each of the faults monitored are contained in these registers. An "Any Fault" bit, bit 7, is the OR of all the individual fault bits in the register and indicates that one or more of the fault bits is set. There is a system-wide "Any Fault" bit in the power supply and Any Fault Status register 13, (Bit 7) whose state is the OR of all the other "Any Fault" bits in the other status registers. The MCU can monitor this system-wide Any Fault bit to discover if any of the outputs has a fault condition present. Once the MCU detects the system-wide Any Fault bit =1, then it must interrogate the all the other status registers to determine the actual fault(s) that are present.

Once a fault bit in any status register is set, by the 33814 circuit, it can only be cleared by the MCU or by any of the reset actions including a software reset.

Non-fault bits in the status register can be set and cleared by the 33814 circuit. All existing bits in the status register, bits not marked as "x" can only be cleared by the MCU when the POST bit is zero (0). When the POST bit is one (1), the MCU can read or write any existing bit in the status register. Non-existing bits, marked with an "x" in the table cannot be changed from the default zero (0) value.

5.3.8.1 Existing and Non-existing Bits in the SPI Registers

Entries in the following SPI Registers marked with an "x" are non-existent bits. They are set to zero (0) by default and cannot be changed by reading or writing to them. They should be ignored when testing registers during POST.

System On/Off Indicators

One of the registers in the status register contains the On/Off status indication of the six LSDs and three pre-driver outputs. (The TACHOUT output is the only output not annunciated in this register). The output is considered to be On (1) whenever all of the following conditions are true:

1. The output is commanded on via the Input pin or/and SPI bit, subject to the OR/AND logic condition selected.
2. There are no overcurrent (OC), short to battery (SB), or overtemperature (OT) faults present.
3. If PWM is enabled, the PWM control is set to a value greater than 0%.
4. There is no reset condition present. (OV, UV, WD, SW)
5. The 33814 is in the Normal state. (i.e. KEYSW=1)

Note: For ROUT2, the 33814 can be in either the Normal state or the Pre-shutdown state if the shutdown disable (SDD) bit is set and PWREN=1.

If all of the five conditions above are true, the System On/Off bit for that output will be on (1).

If any of the five conditions above are false, the System On/Off bit for that output will be off (0).

5.3.8.2 Model Code and Revision Number

One status register is reserved for reporting the model code and revision of the 33814 circuits. The model code for the 33814 is 001. The revision code is the current version number for the circuit. This register is read-only.

5.3.9 SPI Command Summary

The SPI commands are defined as 16 bits with 4 address control bits and 12 command data bits. There are 7 separate commands that are used to set the operational parameters of device. The operational parameters are stored internally in 8-bit registers. Write commands write the data contained in the present SPI word whereas read commands have to wait until the next SPI command is sent to read the data requested.

[Table 17](#) defines the commands and default state of the internal registers at POR. SPI commands may be sent to the device at any time while the device is in the Normal state.

Messages sent are acted upon on the rising edge of the CSB input.

Bit value returned equals bit value sent for this command

Table 20. SPI Command Messages

| Command | hex | Control Address Bits | | | | Data Bits | | | | | | | | | | | |
|------------------------------|-----|----------------------|----|----|----|-------------------------------------|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPI Check | 0 | 0 | 0 | 0 | 0 | X* | X* | X* | X* | X* | X* | X* | X* | X* | X* | X* | X* |
| Read Configuration Register | 1 | 0 | 0 | 0 | 1 | <0000> Internal Register Address | | | | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |
| Write Configuration Register | 2 | 0 | 0 | 1 | 0 | <0000> Internal Register Address | | | | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |
| Read Status Register | 3 | 0 | 0 | 1 | 1 | <0000> Internal Register Address | | | | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |
| Write Status Register | 4 | 0 | 1 | 0 | 0 | <0000> Internal Register Address | | | | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |
| Read Control Register | 5 | 0 | 1 | 0 | 1 | <0000> Internal Register Address | | | | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |
| Write Control Register | 6 | 0 | 1 | 1 | 0 | <0000> Internal Register Address | | | | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |
| SPI Check Response | 7 | 0 | 1 | 1 | 1 | X* | X* | X* | X* | X* | X* | X* | X* | X* | X* | X* | X* |

5.3.9.1 SPI Commands

There are seven SPI commands that can be issued by the MCU to:

- Do a SPI Check verification
- Read the contents of the SPI configuration registers
- Write the contents of the SPI configuration registers
- Read the contents of the SPI status registers
- Write the contents of the SPI status registers
- Read the contents of the SPI control registers
- Write the contents of the SPI control registers

5.3.9.2 SPI Registers

The SPI interface consists of three blocks of four, 8-bit read/write registers.

There are three types of SPI registers:

- **Configuration Registers** - These registers allow the MCU to configure the various parameters and options for the various functional blocks.
- **Control Registers** - These registers are used to command the outputs on and off and set the PWM duty cycle values.
- **Status Registers** - These registers report back faults and other conditions of the various functional blocks.

The following acronyms are use in the SPI table:

- OC = overcurrent, could be short to battery (SB)
- OV = overvoltage

- OT = overtemperature
- OL = open load
- SG = short to ground
- PWM = pulse width modulation
- DC = duty cycle

The following conventions are used in the SPI register tables:

- All **default selections** are in **BOLD** fonts
- Non-default selections are in normal font
- The first selection listed is the **default selection**
- The binary values shown, (0 or 1) are the **default values** after a reset has occurred.

Table 21. SPI Configuration Registers

| Reg # | Hex | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-----|-----------------------------|-------------------------------|---------------------------------------|---|---|---|--|--|--|
| 0 | 0 | Injector 1 Driver | Retry Enable (0) | x (0) | x (0) | OL Current Sink Enable (1) | In-Rush Delay (0) | OR/AND (0) | PWM Freq. 1 (0) | PWM Freq. 0 (0) |
| 1 | 1 | Injector 2 Driver | Retry Enable (0) | x (0) | x (0) | OL Current Sink Enable (1) | In-Rush Delay (0) | OR/AND (0) | PWM Freq. 1 (0) | PWM Freq. 0 (0) |
| 2 | 2 | Relay 1 Driver | Retry Enable (0) | x (0) | x (0) | OL Current Sink Enable (1) | In-Rush Delay (1) | OR/AND (0) | PWM Freq. 1 (0) | PWM Freq. 0 (0) |
| 3 | 3 | Relay 2 Driver | Retry Enable (0) | Shutdown DisableSD D (0) | x (0) | OL Current Sink Enable (1) | In-Rush Delay (0) | OR/AND (0) | PWM Freq. 1 (0) | PWM Freq. 0 (0) |
| 4 | 4 | Tachometer Driver | Retry Enable (0) | Vrsout/LSD (0) | Vrsout/ Osc. mode (0) | OL Current Sink Enable (0) ÷ N₁₆ | In-Rush Delay (0) ÷ N₉ | Output Freq. 2 (0) ÷ N₄ | Output/PWM Freq. 1 (0) ÷ N₂ | Output/PWM Freq. 0 (1) ÷ N₁ |
| 5 | 5 | Lamp Driver | Retry Enable (0) | x (0) | x (0) | OL Current Sink Enable (1) | In-Rush Delay (1) | x (0) | PWM Freq. 1 (0) | PWM Freq. 0 (0) |
| 6 | 6 | Battery Switch Logic Output | HSD Mode (0) | X (0) | x (0) | x (0) | x (0) | x (0) | PWM Freq. 1 (0) | PWM Freq. 0 (0) |
| 7 | 7 | O2 Heater Pre-Driver | IGN/GPGD Select (0) | Retry Enable (0) | x (0) | OL Current Sink (1) | x (0) | OR/AND (0) | PWM Freq. 1 (0) | PWM Freq. 0 (0) |
| 8 | 8 | Ignition 1 Pre-Driver | IGN/GPGD Select (1) | Retry Enable (0) | x (0) | OL Current Sink (0) | x (0) | OR/AND (0) | PWM Freq. 1 (0) | PWM Freq. 0 (0) |

Table 21. SPI Configuration Registers

| Reg # | Hex | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-----|------------------------------|------------------------|-------------------------|--------------------------|-------------------------|----------------------|----------------------|----------------------|-------------------------|
| 9 | 9 | Ignition 2 Pre-Driver | IGN/GPGD Select (1) | Retry Enable (0) | x (0) | OL Current Sink (0) | x (0) | OR/AND (0) | PWM Freq. 1 (0) | PWM Freq. 0 (0) |
| 10 | A | Watchdog Parameters | Enable/Disable (1) | Load Time x1 sec (1) | Load Time x100 ms (0) | Load Time x10 ms (0) | Load Time 8 (1) | Load Time 4 (0) | Load Time 2 (1) | Load Time (0) |
| 11 | B | VRS Manual Parameters | Threshold 3 (0) | Threshold 2 (1) | Threshold 1 (0) | Threshold 0 (1) | Filter Time 3 (0) | Filter Time 2 (0) | Filter Time 1 (1) | Filter Time 0 (1) |
| 12 | C | VRS Automatic Parameters | mantiss 8 (0) | mantiss 4 (0) | mantiss 2 (1) | mantiss 1 (0) | exponent 8 (0) | exponent 4 (0) | exponent 2 (0) | exponent 1 (1) |
| 13 | D | VRS Miscellaneous Parameters | Man./Auto (0)(0) | Disable VRS (0) | x (0) | High/Low Ref (0) | De-glitch (0) | Gnd VRSN (0) | Inv Inputs (0) | Disable 2.5 V CM (0) |

Table 22. SPI Control Registers

| Reg # | Hex | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-----|----------------------|------------------------|------------------------------|---------------|------------------------|---------------|------------------------|-----------------------|----------------------------|
| 0 | 0 | Main OFF/ON Control | INJ1 (0/1) | INJ2 (0/1) | REL1 (0/1) | REL2 (0/1) | LAMP (0/1) | IGN1 (0/1) | IGN2 (0/1) | O2H (0/1) |
| 1 | 1 | Other OFF/ON Control | Pwren OFF/ON (0) | POST Enable OFF/ON (0) | X (0) | VProt ON/OFF (1) | X (0) | Batsw OFF/ON (0) | Tach OFF/ON (1) | RESET internal only (0) |
| 2 | 2 | Injector 1 Driver | X (0) | PWM6 (0) | PWM5 (0) | PWM4 (0) | PWM3 (0) | PWM2 (0) | PWM1 (0) | PWM0 (0) |
| 3 | 3 | Injector 2 Driver | X (0) | PWM6 (0) | PWM5 (0) | PWM4 (0) | PWM3 (0) | PWM2 (0) | PWM1 (0) | PWM0 (0) |
| 4 | 4 | Relay 1 Driver | X (0) | PWM6 (0) | PWM5 (0) | PWM4 (0) | PWM3 (0) | PWM2 (0) | PWM1 (0) | PWM0 (0) |
| 5 | 5 | Relay 2 Driver | X (0) | PWM6 (0) | PWM5 (0) | PWM4 (0) | PWM3 (0) | PWM2 (0) | PWM1 (0) | PWM0 (0) |
| 6 | 6 | Tachometer Driver | X (0) | PWM6 (0) | PWM5 (0) | PWM4 (0) | PWM3 (0) | PWM2 (0) | PWM1 (0) | PWM0 (0) |
| 7 | 7 | Lamp Driver | X (0) | PWM6 (0) | PWM5 (0) | PWM4 (0) | PWM3 (0) | PWM2 (0) | PWM1 (0) | PWM0 (0) |
| 8 | 8 | Batsw | X (0) | PWM6 (0) | PWM5 (0) | PWM4 (0) | PWM3 (0) | PWM2 (0) | PWM1 (0) | PWM0 (0) |
| 9 | 9 | O2 Heater Pre-Driver | X (0) | PWM6 (0) | PWM5 (0) | PWM4 (0) | PWM3 (0) | PWM2 (0) | PWM1 (0) | PWM0 (0) |

Table 22. SPI Control Registers

| Reg # | Hex | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-----|-----------------------|-----------------------|----------------------------|-----------------------------|----------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| 10 | A | Ignition 1 Pre-Driver | X (0) | PWM6 (0) | PWM5 (0) | PWM4 (0) | PWM3 (0) | PWM2 (0) | PWM1 (0) | PWM0 (0) |
| 11 | B | Ignition 2 Pre-Driver | X (0) | PWM6 (0) | PWM5 (0) | PWM4 (0) | PWM3 (0) | PWM2 (0) | PWM1 (0) | PWM0 (0) |
| 12 | C | Watchdog | WDRFSH (0) | Load Time x1 sec (0) | Load Time x100 ms (0) | Load Time x10 ms (0) | Load Time 8 (0) | Load Time 4 (0) | Load Time 2 (0) | Load Time 1 (0) |
| 13 | D | VRS Conditioner | Threshold 3 (0) | Threshold 2 (0) | Threshold 1 (0) | Threshold 0 (0) | Filter Time 3 (0) | Filter Time 2 (0) | Filter Time 1 (0) | Filter Time 0 (0) |

Table 23. SPI Status Registers

| Reg # | Hex | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-----|------------------------------|--------------------|-------------------|-------------------|-------------------|------------------------|-----------------------------|-----------------------|------------------------|
| 0 | 0 | Injector 1 Driver Faults | Faults (0) | x (0) | x (0) | x (0) | Open Load OL (0) | Over - current OC (0) | Overtemp OT (0) | Short Gnd SG (0) |
| 1 | 1 | Injector 2 Driver Faults | Faults (0) | x (0) | x (0) | x (0) | Open Load OL (0) | Overcurrent t OC (0) | Overtemp OT (0) | Short Gnd SG (0) |
| 2 | 2 | Relay 1 Driver Faults | Faults (0) | x (0) | x (0) | x (0) | Open Load OL (0) | Overcurrent t OC (0) | Overtemp OT (0) | Short Gnd SG (0) |
| 3 | 3 | Relay 2 Driver Faults | Faults (0) | x (0) | x (0) | x (0) | Open Load OL (0) | Overcurrent t OC (0) | Overtemp OT (0) | Short Gnd SG (0) |
| 4 | 4 | Tachometer Driver Faults | Faults (0) | x (0) | x (0) | x (0) | Open Load OL (0) | Overcurrent t OC (0) | Overtemp OT (0) | x (0) |
| 5 | 5 | Lamp Driver Faults | Faults (0) | x (0) | x (0) | x (0) | Open Load OL (0) | Overcurrent t OC (0) | Overtemp OT (0) | Short Gnd SG (0) |
| 7 | 7 | O2 Heater Pre-Driver Faults | Faults (0) | x (0) | x (0) | x (0) | Open Load OL (0) | Overcurrent t OC (0) | x (0) | x (0) |
| 8 | 8 | Ignition 1 Pre-driver Faults | Faults (0) | x (0) | x (0) | x (0) | Open Load OL (0) | Overcurrent t OC (0) | x (0) | x (0) |
| 9 | 9 | Ignition 2 Pre-driver Faults | Faults (0) | x (0) | x (0) | x (0) | Open Load OL (0) | Overcurrent t OC (0) | x (0) | x (0) |
| 10 | A | Watchdog State | Enable/ Disable | WD timer bit 6 | WD timer bit 5 | WD timer bit 4 | WD timer bit 3 | WD timer bit 2 | WD timer bit 1 | WD timer bit 0 |

Table 23. SPI Status Registers

| | | | | | | | | | | |
|----|---|--|--------------------------|-----------------------|-----------------------|-----------------------|-----------------------|---|--|--|
| 11 | B | VRS Conditioner and ISO9141 Faults | Peak 8 (0) | Peak 4 (0) | Peak 2 (0) | Peak 1 (0) | x (0) | Clamp-active VRSP (0) | Clamp-active VRSN (0) | ISO Overtemp OT (0) |
| 13 | D | Power Supply and Any System Faults | Any System Faults (0) | Keysw (1/0) | Pwren (0/1) | Batsw (0/1) | SPI Error (0/1) | V _{PROT} Short to Battery (0/1) | V _{PROT} Overtemp OT (0/1) | V _{PROT} Short to Ground (0/1) |
| 14 | E | System On/Off Indicators | INJ1 Off/On (0) | INJ2 Off/On (0) | REL1 Off/On (0) | REL2 Off/On (0) | LAMP Off/On (0) | IGN1 Off/On (0) | IGN2 Off/On (0) | O2H Off/On (0) |
| 15 | F | Model Code/ Revision Number* *Read Only except for POST Enable | Model Code 2 (0) | Model Code 1 (0) | Model Code 0 (1) | Rev # (0) | Rev # (0) | Rev # (0) | Rev # (0) | Rev # (0) |

6 Typical Applications

6.0.1 Output OFF Open Load Fault

An Output OFF Open Load Fault is the detection and reporting of an *open* load when the corresponding output is disabled (input bit programmed to a logic low state). The Output OFF Open Load Fault is detected by comparing the drain-to-source voltage of the specific MOSFET output to an internally generated reference. Each output has one dedicated comparator for this purpose. Each output has an internal pull-down current source or resistor. The pull-down current sources are enabled on power-up and must be enabled for Open Load Detect to function. In cases where the Open Load Detect current is disabled, the status bit will always respond with logic 0. The device will only shut down the pull-down current in Sleep mode or when disabled via the SPI. During output switching, especially with capacitive loads, a false Output OFF Open Load Fault may be triggered. To prevent this false fault from being reported, an internal fault filter of 100 to 450 μ s is incorporated. The duration for which a false fault may be reported is a function of the load impedance, $R_{DS(ON)}$, C_{OUT} of the MOSFET, as well as the supply voltage, V_{PWR} . The rising edge of CSB triggers the built-in fault delay timer. The timer must time out before the fault comparator is enabled to detect a faulted threshold. Once the condition causing the Open Load Fault is removed, the device resumes normal operation. The Open Load Fault, however, will be latched in the output SO Response register for the MCU to read.

6.0.2 Low Voltage Operation

Low voltage condition ($6.5\text{ V} < V_{PWR} < 9.0\text{ V}$) will operate per the command word, however parameter tables may be out of specification and status reported on SO pin is not guaranteed.

6.0.3 Low Side Injector Driver Voltage Clamp

Each Injector output of the 33814 incorporates an internal voltage clamp to provide fast turn-OFF and transient protection. Each clamp independently limits the drain-to-source voltage to V_{CL} . The total energy clamped (E_J) can be calculated by multiplying the current area under the current curve (I_A) times the clamp voltage (V_{CL}) (see [Figure 12](#)).

Characterization of the output clamps, using a repetitive pulse method at 1.0 A, indicates the maximum energy to be 100 mJ at 125 °C junction temperature per output.

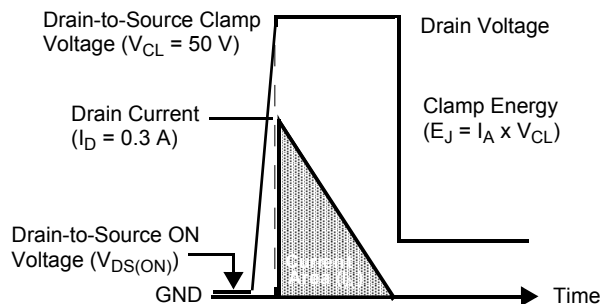


Figure 12. Output Voltage Clamping

6.0.4 Reverse Battery Protection

The 33814 device requires external reverse battery protection on the VPWR pin.

All outputs consist of a power MOSFET with an integral substrate diode. During a reverse battery condition, current will flow through the load via the substrate diode. Under this condition load devices will turn on. If load reverse battery protection is desired, a diode must be placed in series with the load.

7 Packaging

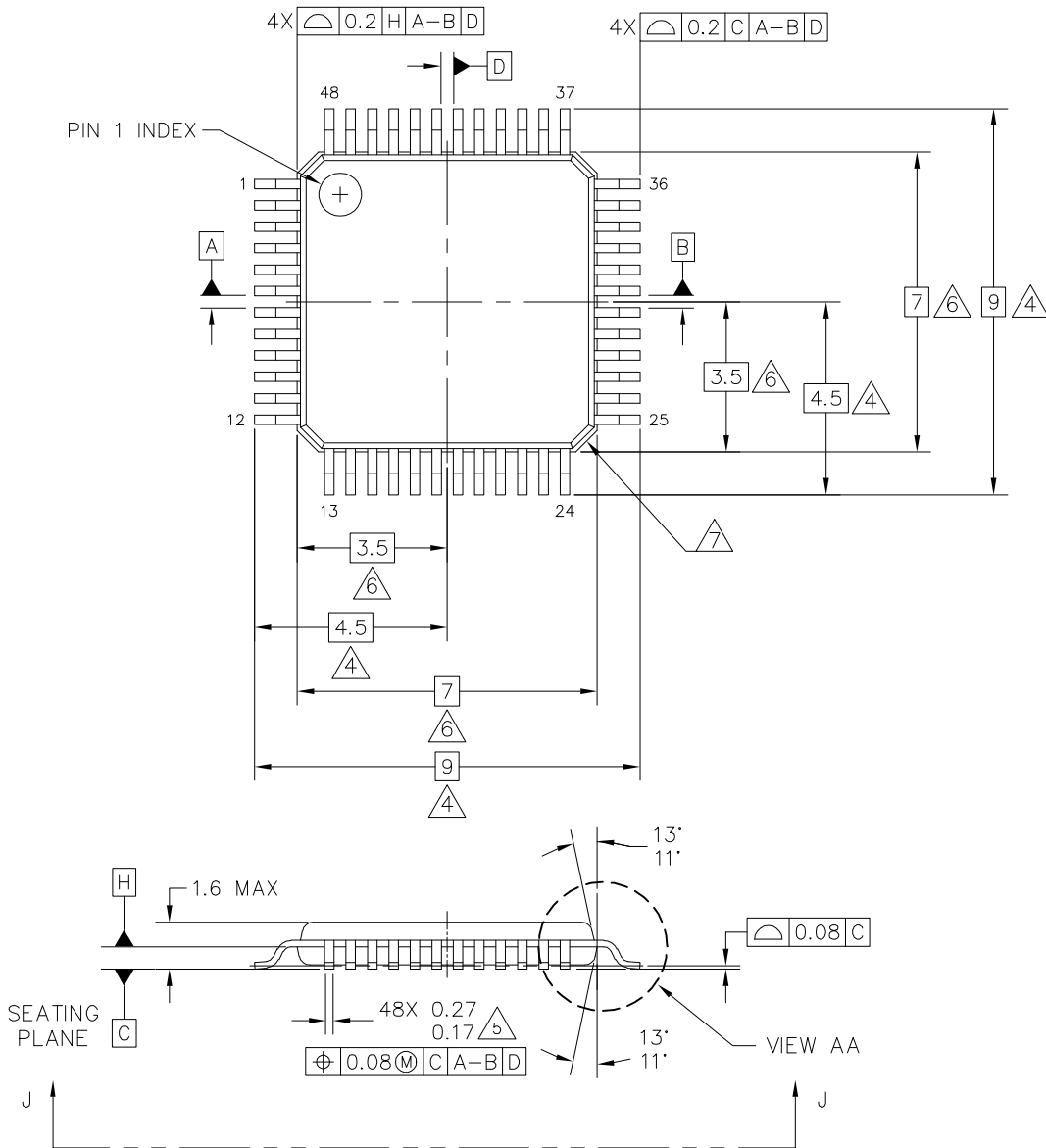
7.1 Package Mechanical Dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.freescale.com and perform a keyword search for the drawing's document number.

Table 24. 98A Reference Documents

| Package | Suffix | Package Outline Drawing Number |
|----------------|--------|--------------------------------|
| 48-Pin LQFP-EP | AE | 98ASA00173D |

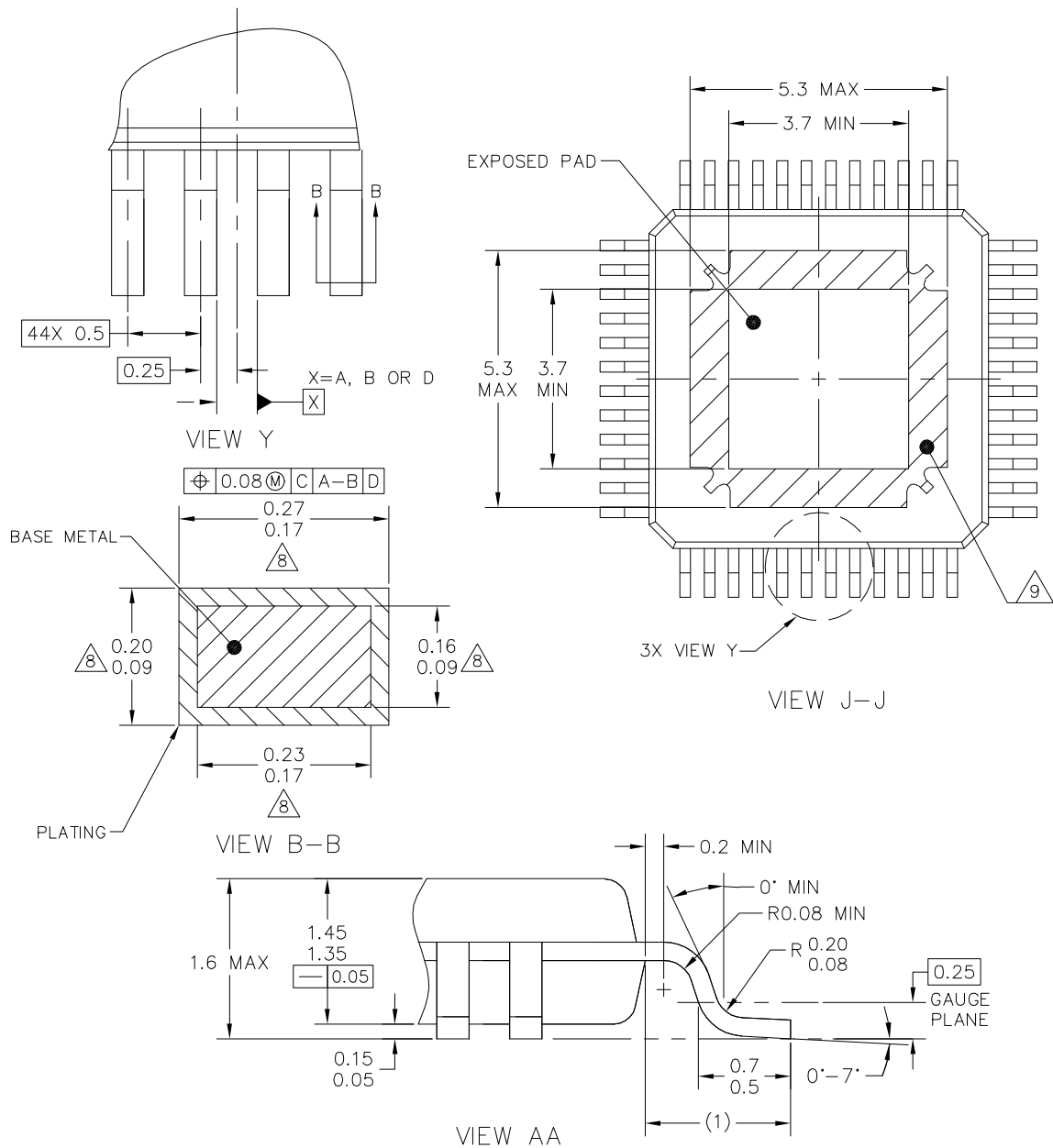
Dimensions shown are provided for reference ONLY
(For Layout and Design, refer to the Package Outline Drawing listed in the 98A Reference Documents table)



| | | | |
|--|----------------------------|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE | |
| TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.5X4.5 EXPOSED PAD | DOCUMENT NO: 98ASA00173D | REV: A | |
| | CASE NUMBER: 2003-02 | 30 JUN 2011 | |
| | STANDARD: JEDEC MS-026 BBC | | |

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48-PIN LQFP-EP
98ASA00173D
ISSUE A

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







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| | | CASE NUMBER: 2003-02 | 30 JUN 2011 |
| | | STANDARD: JEDEC MS-026 BBC | |

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48-PIN LQFP-EP
98ASA00173D
ISSUE A

MC33814

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4.  DIMENSION TO BE DETERMINED AT SEATING PLANE C.
5.  THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.
6.  THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7.  EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8.  THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1MM AND 0.25MM FROM THE LEAD TIP.
9.  HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

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AE SUFFIX
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8 Revision History

| REVISION | DATE | DESCRIPTION OF CHANGES |
|----------|---------|--|
| 1.0 | 8/2012 | <ul style="list-style-type: none"> Initial release Removed Freescale Confidential Proprietary on page 1 |
| 2.0 | 4/2013 | <ul style="list-style-type: none"> Confirmed that all known edits requested for version 1.0 are present. Changed "VRS Low-state Output Voltage" to "VRS High-state Output Voltage" and "IVRS-LOW" to "IVRS-HIGH" for V_{VRSOUT_HIGH} in Table 4. Changed "Voltage to Current" for $I_{RESET_LEAKAGE_HIGH}$ in Table 4 Added units to the ROUT2 section of Table 4 Corrected spelling of "ISO9141" in section 5.1.15 Changed VPP Supply Voltage (If supplied externally and not using internal VPP regulator) to reflect two separate limits Changed VPROT Output Voltage (tracks VCC) Max limit. Changed Typ and Max limit on Load Regulation (Both VCC and VPROT) measured from 10% - 90% of IVCC_C & IPROT_C, VPWR = 13 V Changed Min limit on VRS Negative Clamp Voltage at ICLAMP = 10 mA Changed Note 12 Updated Table 10 and Table 12 Added lower limit note for VCC Output Current Limiting Updated Output Clamp Energy (INJOUT1, INJOUT2, ROUT1)(Single Pulse), Output Clamp Energy (INJOUT1, INJOUT2)(Continuous operation), and added Output Clamp Energy (LAMPOUT)(Single pulse) Added ESD Voltage ⁽²⁾ Added clarification to 5.1.21, "LAMPOUT Driver Output" Corrected RESET Pull-down Resistor min and max |
| 3.0 | 5/2013 | <ul style="list-style-type: none"> Added symbol to Output OFF Open Load Detection Current TachOut Added Output load current at ISO I/O pin (MTX = 0, RLOAD = 1.0 kΩ, ±10%) |
| 4.0 | 5/30/13 | <ul style="list-style-type: none"> Changed part number from PC33814AE to MC33814AE in Table 1, Orderable Part Variations |



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