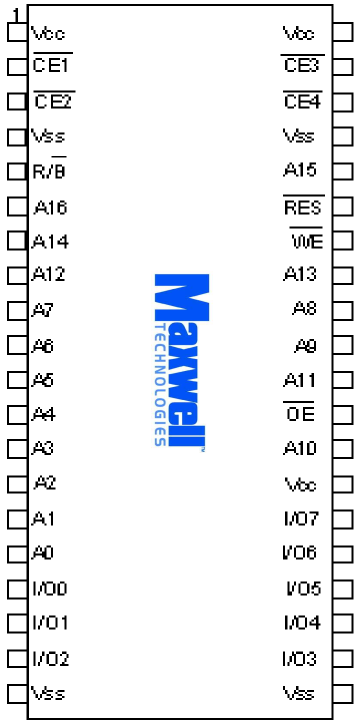
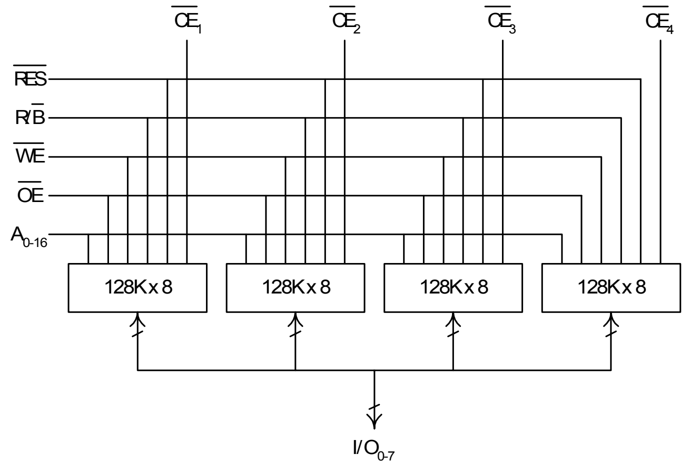
79LV0408

Low Voltage 4 Megabit (512k x 8-bit) EEPROM





Logic Diagram

Features:

- Four 128k x 8-bit EEPROMs MCM
- RAD-PAK® radiation-hardened against natural space radiation
- Total dose hardness:
  - \> 100 krad (Si), depending upon space mission
- Excellent Single Event Effects
  - SEL > 84 MeV/mg/cm²
  - SEU >26.6 MeV/mg/cm² (read mode)
  - SEU = 11.4 MeV/mg/cm² (write mode)
- Package:
- - 40 pin RAD-PAK® flat pack
- - 40 pin X-Ray Pak™ flat pack
- - 40 pin Rad-Tolerant flat pack
- High speed:
  - -200 and 250 ns access times available
- Data Polling and Ready/Busy signal
- Software data protection
- Write protection by RES pin
- High endurance
  - 10,000 erase/write (in Page Mode),
  - 10 year data retention
- Page write mode: 1 to 128 byte page
- Low power dissipation
  - 88 mW/MHz active mode
  - 440 μW standby mode

Description:

Maxwell Technologies' 79LV0408 multi-chip module (MCM) memory features a greater than 100 krad (Si) total dose tolerance, depending upon space mission. Using Maxwell Technologies' patented radiation-hardened RAD-PAK® MCM packaging technology, the 79LV0408 is the first radiation-hardened 4 Megabit MCM EEPROM for space applications. The 79LV0408 uses four 1 Megabit high-speed CMOS die to yield a 4 Megabit product. The 79LV0408 is capable of in-system electrical Byte and Page programmability. It has a 128 bytes Page Programming function to make its erase and write operations faster. It also features Data Polling and a Ready/Busy signal to indicate the completion of erase and programming operations. In the 79LV0408, hardware data protection is provided with the RES pin, in addition to noise protection on the WE signal. Software data protection is implemented using the JEDEC optional standard algorithm.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, the RAD-PAK® package provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Maxwell Technologies self-defined Class K.

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Table 1. 79LV0408 Pin Description

Pin	Symbol	Description
16-9, 32-31, 28, 30, 8, 33, 7, 36, 6	A0 to A16	Address Input
17-19, 22-26	I/O0 to I/O7	Data Input/Output
29	$\overline{OE}$	Output Enable
2, 3, 39, 38	$\overline{CE1\text{-}4}$	Chip Enable 1 through 4
34	$\overline{WE}$	Write Enable
1, 27, 40	VCC	Power Supply
4, 20, 21, 37	VSS	Ground
5	RDY/$\overline{BUSY}$	Ready/Busy
35	$\overline{RES}$	Reset

Table 2. 79LV0408 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	-0.6	7.0	V
Input Voltage	V_{IN}	-0.5[1]	7.0	V
Package Weight	RP		23	Grams
	RT		10	
Thermal Resistance (RP Package)	Tjc		7.3	˚C/W
Operating Temperature Range	T_{OPR}	-55	125	˚C
Storage Temperature Range	T_{STG}	-65	150	˚C

1. V_{IN} min = -3.0V for pulse width $\leq$50ns.

Table 3. 79LV0408 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input Voltage $\overline{RES}$_PIN	V_{IL} V_{IH} V_H	-0.3[1] 2.2 V_{CC}-0.5	0.8 V_{CC} +0.3 V_{CC} +1	V V V
Case Operating Temperature	T_C	-55	125	˚C

1. V_{IL} min = -1.0V for pulse width $\leq$ 50 ns

Table 4. 79LV0408 Capacitance[1]

(T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance: V_{IN} = 0 V [1]	C_{IN}			pf
$\overline{WE}$		--	24	
$\overline{CE}_{1-4}$		--	6	
$\overline{OE}$		--	24	
A_{0-16}		--	24	
Output Capacitance: V_{OUT} = 0 V [1]	C_{OUT}		48	pF

1. Guaranteed by design.

Table 5. Delta Parameters

Parameter	Condition
I_{CC1}	± 10% of value in Table 6
I_{CC2}	± 10% of value in Table 6
I_{CC3}	± 10% of value in Table 6
I_{CC4}	± 10% of value in Table 6

Table 6. 79LV0408 DC Electrical Characteristics

(V_{cc} = 3.3V ±10%, T_A = -55 to +125°C)

Parameter	Test Condition	Symbol	Subgroups	Min	Max	Units
Input Leakage Current	V_{CC} = 3.6V, V_{IN} = 3.6V[1]	I_{IL}	1, 2, 3			μA
	$\overline{CE}_{1-4}$			--	2 [1]	
	$\overline{OE}$, $\overline{WE}$			--	8	
	A_{0-16}			--	8	
Output Leakage Current	V_{CC} = 3.6V, V_{OUT} = 3.6V/0.4V	I_{LO}	1, 2, 3	--	8	μA
Standby V_{CC} Current	$\overline{CE}$ = V_{CC}	I_{CC1}		--	80	μA
	$\overline{CE}$ = V_{IH}	I_{CC2}		--	4	mA
Operating V_{CC} Current[2]	I_{OUT} = 0mA, Duty = 100%, Cycle = 1μs at V_{CC} = 3.6V	I_{CC3}	1, 2, 3	--	15	mA
	I_{OUT} = 0mA, Duty = 100%, Cycle = 150ns at V_{CC} = 3.6V	I_{CC4}	1, 2, 3	--	50	
Input Voltage		V_{IL}	1, 2, 3	--	0.8	V
		V_{IH}		2.2	--	
$\overline{RES}$_PIN		V_H		V_{CC} -0.5	--	
Output Voltage	I_{OL} = 2.1 mA	V_{OL}	1, 2, 3	--	0.4	V
	I_{OH} = -0.4 mA	V_{OH}		2.4	--	

1. I_{LI} on RES = 100 uA max.
2. Only on CE\ Active.

Table 7. 79LV0408 AC Electrical Characteristics for Read Operations[1]

(V_{cc} = 3.3V ±10%, T_A = -55 to +125°C)

Parameter	Symbol	Subgroups	Min	Max	Unit
Address Access Time $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} -200 -250	t_{ACC}	9, 10, 11	 -- --	 200 250	ns
Chip Enable Access Time $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} -200 -250	t_{CE}	9, 10, 11	 0 0	 200 250	ns
Output Enable Access Time $\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH} -200 -250	t_{OE}	9, 10, 11	 0 0	 110 120	ns
Output Hold to Address Change $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} -200 -250	t_{OH}	9, 10, 11	 0 0-	 -- --	ns
Output Disable to High-Z[2] $\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH} -200 -250	t_{DF}	9, 10, 11	 0 0	 60 60	ns
$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} -200 -250	t_{DFR}	9, 10, 11	 0 0	 300 350	
$\overline{RES}$ to Output Delay $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} [3] -200 -250	t_{RR}	9, 10, 11	 -- --	 520 550	ns

1. Test conditions: Input pulse levels - 0.4V to 2.4V; input rise and fall times < 20ns; output load - 1 TTL gate + 100pF (including scope and jig); reference levels for measuring timing - 0.8V/1.8V.
2. t_{DF} and t_{DFR} are defined as the time at which the output becomes an open circuit and data is no longer driven.
3. Guaranteed by design.

Table 8. 79LV0408 AC Electrical Characteristics for Write Operations

(V_{cc} = 3.3V ±10%, T_A = -55 to +125°C)

Parameter	Symbol	Subgroups	Min[1]	Max	Unit
Address Setup Time -200 -250	t_{AS}	9, 10, 11	 0 0	 -- --	ns

Table 8. 79LV0408 AC Electrical Characteristics for Write Operations

(V_{cc} = 3.3V ±10%, T_A = -55 to +125°C)

Parameter	Symbol	Subgroups	Min[1]	Max	Unit
Chip Enable to Write Setup Time ($\overline{WE}$ Controlled) -200 -250	t_{CS}	9, 10, 11	 0 0	 -- --	ns
Write Pulse Width$\overline{CE}$ Controlled -200 -250 $\overline{WE}$ Controlled -200 -250	 t_{CW} t_{WP}	9, 10, 11	 200 250 200 250	 -- -- -- --	ns
Address Hold Time -200 -250	t_{AH}	9, 10, 11	 125 150	 -- --	ns
Data Setup Time -200 -250	t_{DS}	9, 10, 11	 100 100	 -- --	ns
Data Hold Time -200 -250	t_{DH}	9, 10, 11	 10 10	 -- --	ns
Chip Enable Hold Time ($\overline{WE}$ Controlled) -200 -250	t_{CH}	9, 10, 11	 0 0	 -- --	ns
Write Enable to Write Setup Time ($\overline{CE}$ Controlled) -200 -250	t_{WS}	9, 10, 11	 0 0	 -- --	ns
Write Enable Hold Time ($\overline{CE}$ Controlled) -200 -250	t_{WH}	9, 10, 11	 0 0	 -- --	ns
Output Enable to Write Setup Time -200 -250	t_{OES}	9, 10, 11	 0 0	 -- --	ns
Output Enable Hold Time -200 -250	t_{OEH}	9, 10, 11	 0 0	 -- --	ns
Write Cycle Time[2] -200 -250	t_{WC}	9, 10, 11	 -- --	 15 15	ms
Data Latch Time -200 -250	t_{DL}	9, 10, 11	 700 750	 -- --	ns
Byte Load Window -200 -250	t_{BL}	9, 10, 11	 100 100	 -- --	μs

Table 8. 79LV0408 AC Electrical Characteristics for Write Operations

(V_{cc} = 3.3V ±10%, T_A = -55 to +125°C)

Parameter	Symbol	Subgroups	Min[1]	Max	Unit
Byte Load Cycle -200 -250	t_{BLC}	9, 10, 11	 1 1	 -- --	μs
Time to Device Busy -200 -250	t_{DB}	9, 10, 11	 150 150	 -- --	ns
Write Start Time[3] -200 -250	t_{DW}	9, 10, 11	 150 150	 -- --	ns
$\overline{RES}$ to Write Setup Time -200 -250	t_{RP}	9, 10, 11	 100 100	 -- --	μs
V_{CC} to $\overline{RES}$ Setup Time[4] -200 -250	t_{RES}	9, 10, 11	 1 1	 -- --	μs

1. Use this divice in a longer cycle than this value.
2. t_{WC} must be longer than this value unless polling techniques or RDY/BUSY are used. This device automatically completes the internal write operation within this value.
3. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/BUSY are used.
4. Guaranteed by design.

Table 9. 79LV0408 Mode Selection [1, 2]

Parameter	$\overline{CE}$ [3]	$\overline{OE}$	$\overline{WE}$	I/O	$\overline{RES}$	RDY/$\overline{BUSY}$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	V_H	High-Z
Standby	V_{IH}	X	X	High-Z	X	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_H	High-Z --> V_{OL}
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z	V_H	High-Z
Write Inhibit	X	X	V_{IH}	--	X	--
	X	V_{IL}	X	--	X	--
Data Polling	V_{IL}	V_{IL}	V_{IH}	Data Out (I/O7)	V_H	V_{OL}
Program	X	X	X	High-Z	V_{IL}	High-Z

1. X = Don't care.
2. Refer to the recommended DC operating conditions.
3. For $\overline{CE}_{1-4}$ only one $\overline{CE}$ can be used ("on") at a time.

FIGURE 1. READ TIMING WAVEFORM

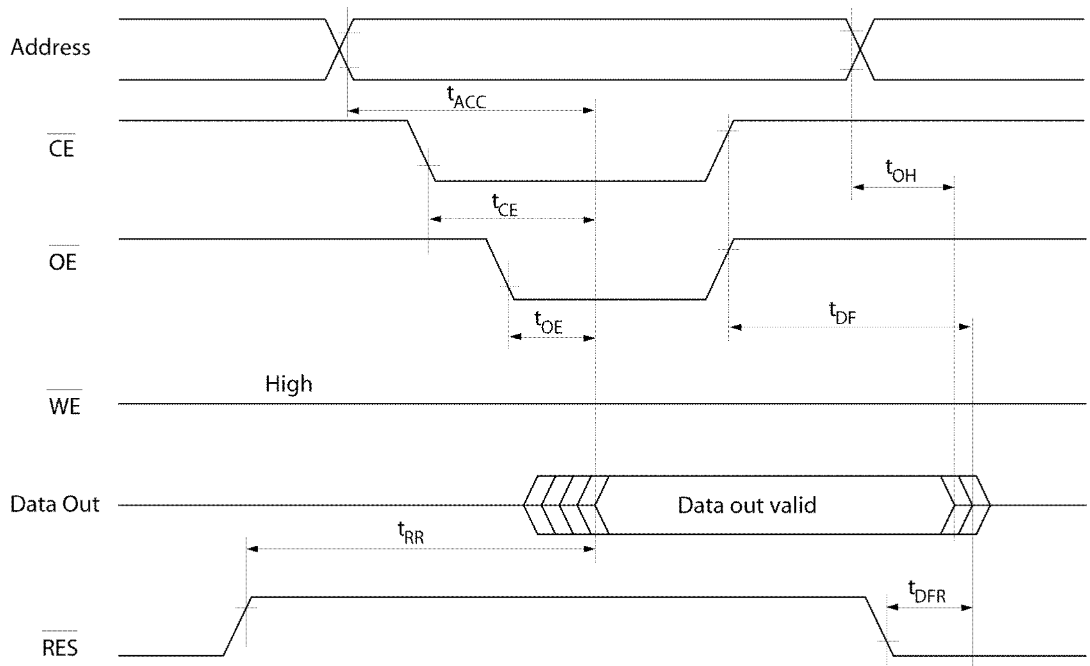


FIGURE 2. BYTE WRITE TIMING WAVEFORM(1) ($\overline{WE}$ CONTROLLED)

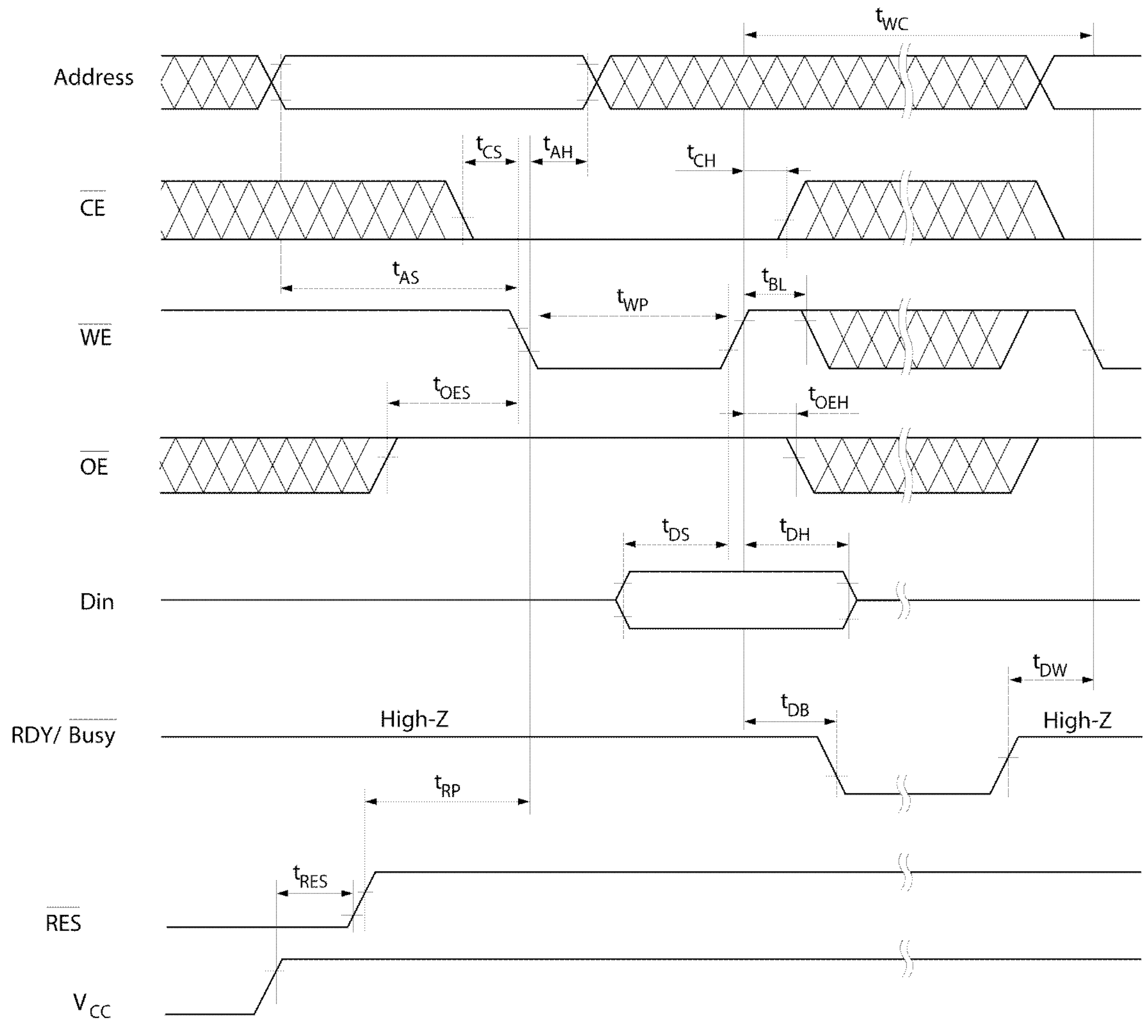


FIGURE 3. BYTE WRITE TIMING WAVEFORM (2) ($\overline{CE}$ CONTROLLED)

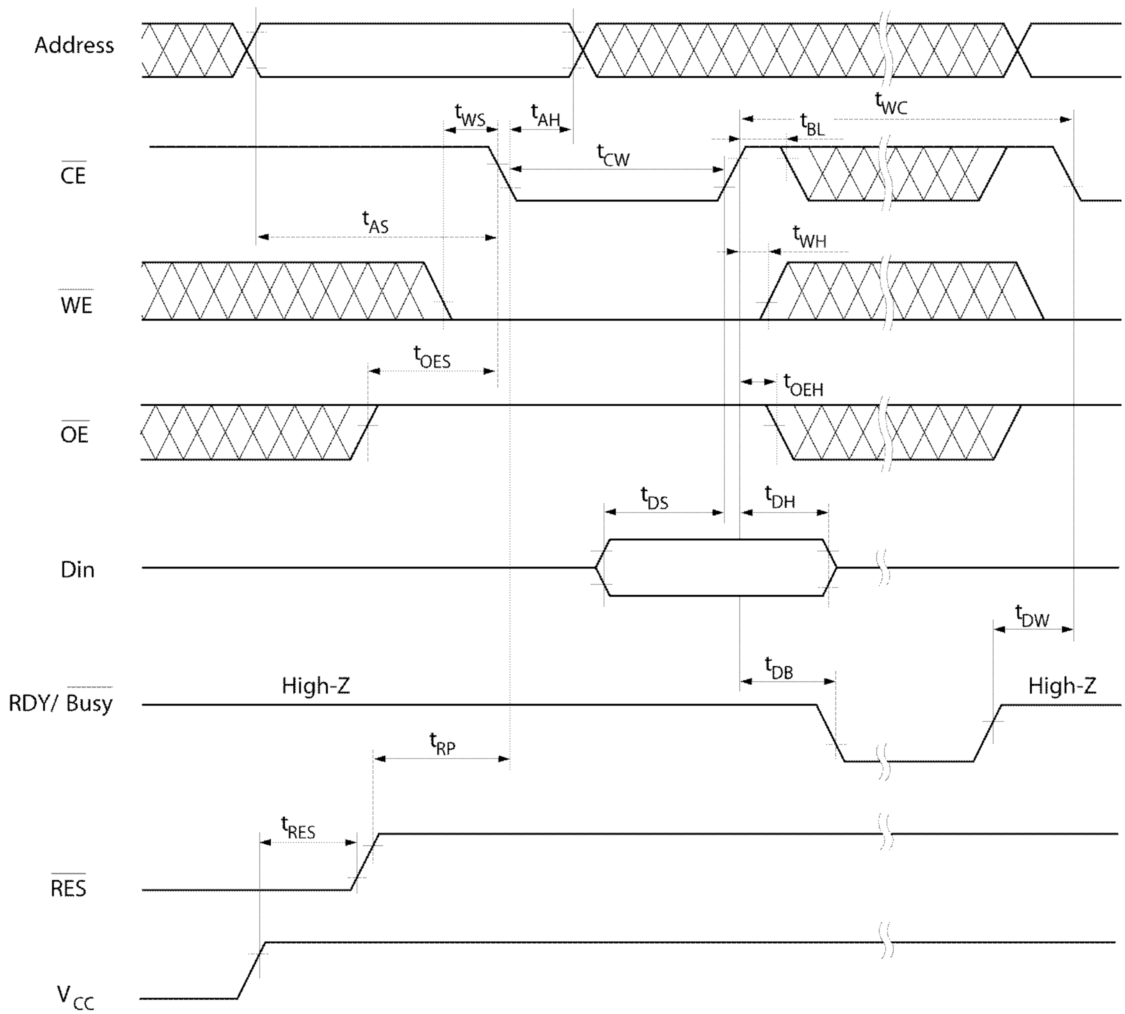


FIGURE 4. PAGE WRITE TIMING WAVEFORM(1) ($\overline{WE}$ CONTROLLED)

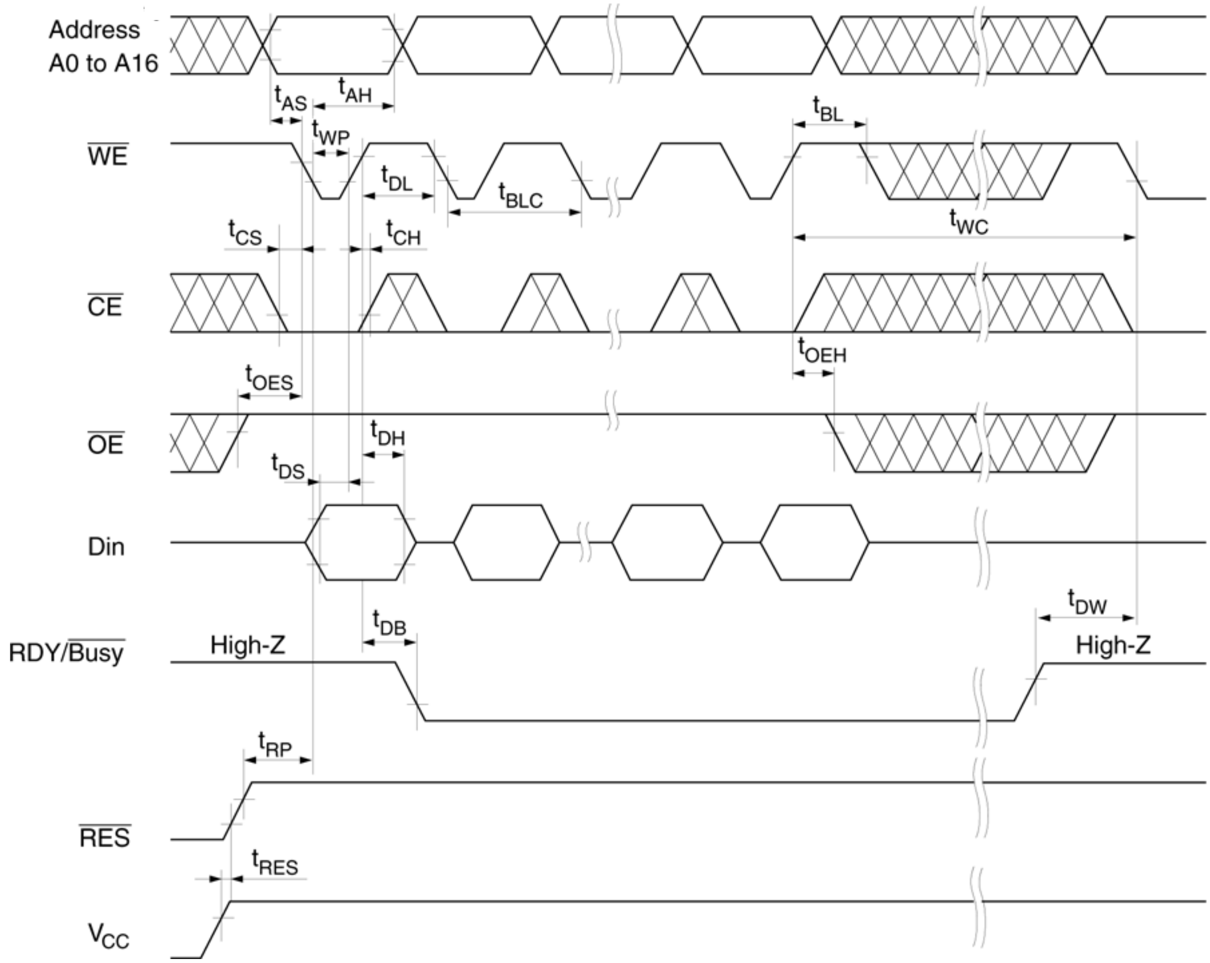


FIGURE 5. PAGE WRITE TIMING WAVEFORM(2) ($\overline{CE}$ CONTROLLED)

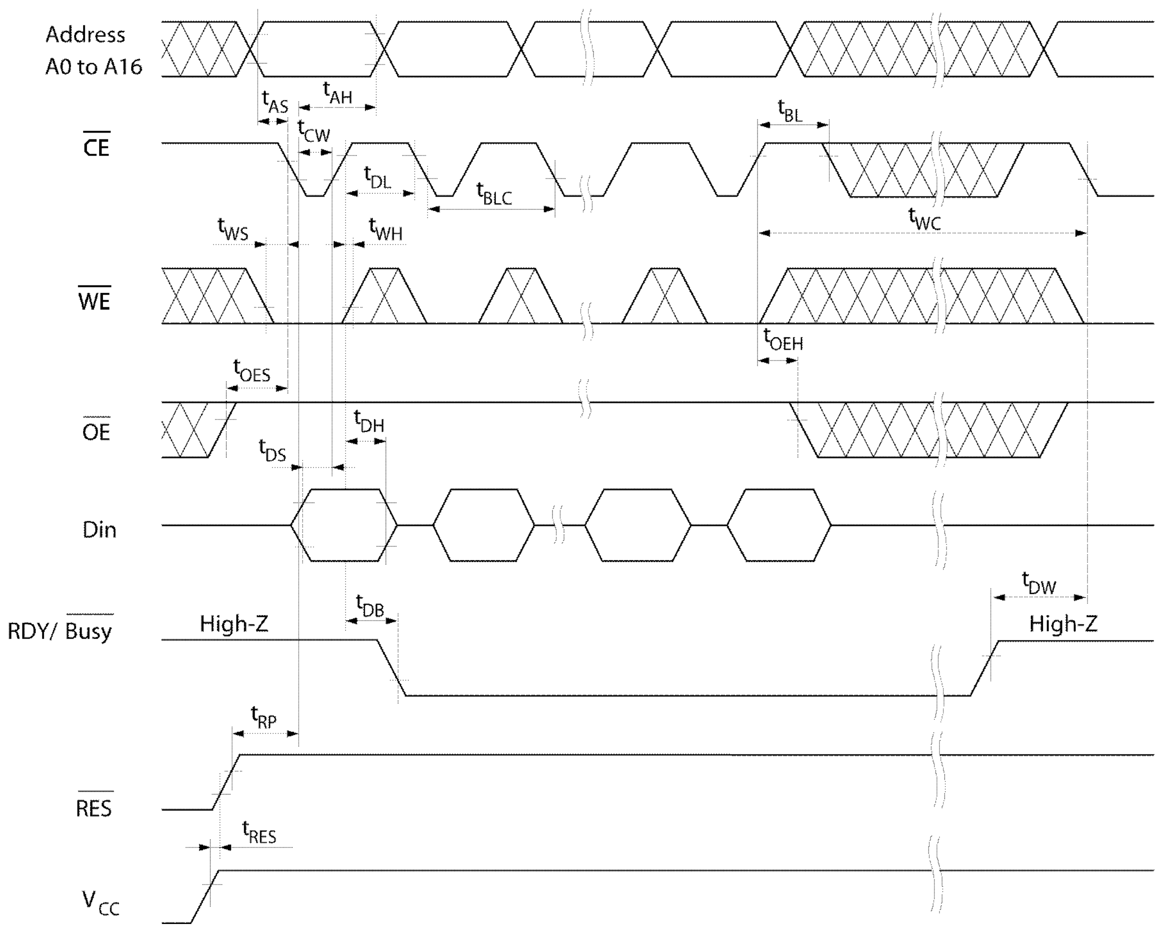


FIGURE 6. $\overline{DATA}$ POLLING TIMING WAVEFORM

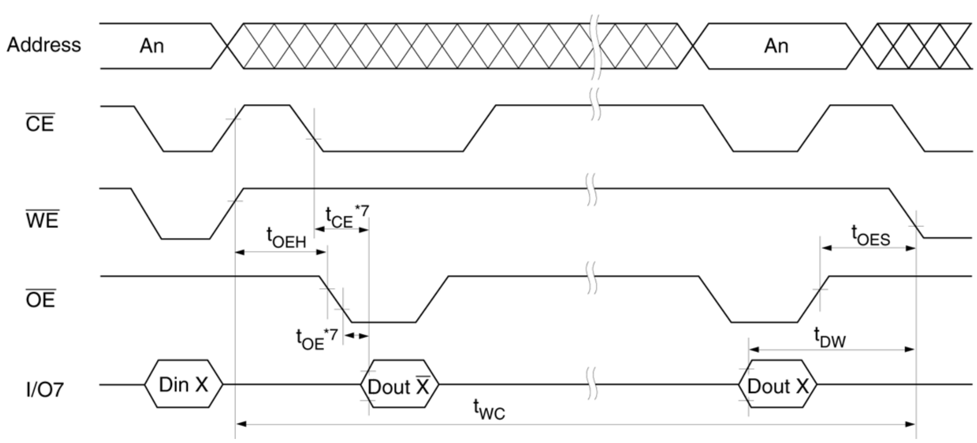


FIGURE 7. SOFTWARE DATA PROTECTION TIMING WAVEFORM(1) (IN PROTECTION MODE)

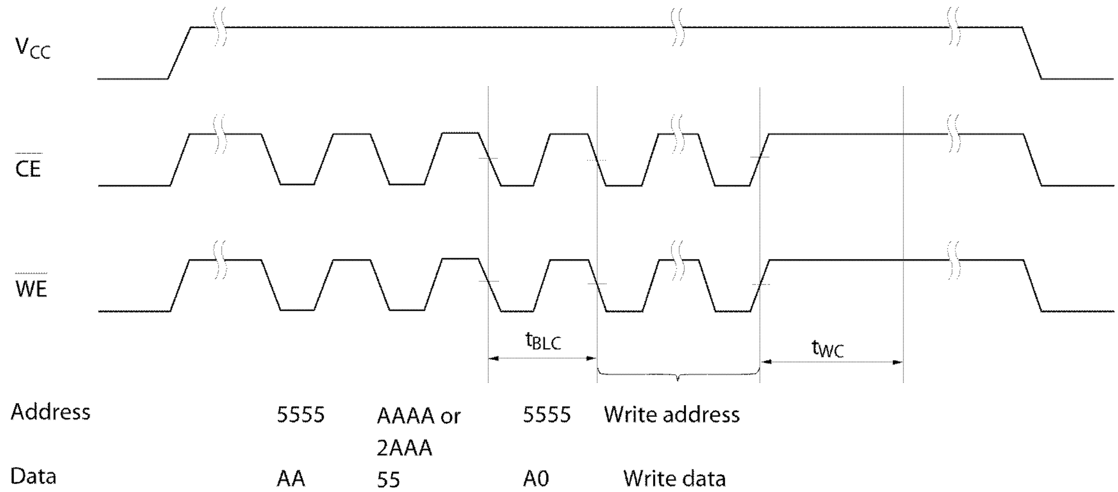
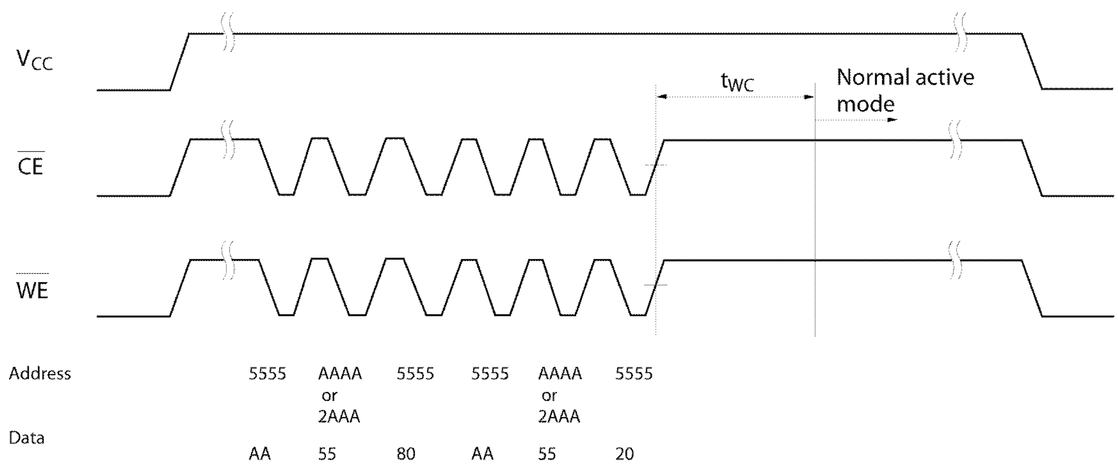


FIGURE 8. SOFTWARE DATA PROTECTION TIMING WAVEFORM(2) (IN NON-PROTECTION MODE)



Toggle Bit Waveform

EEPROM APPLICATION NOTES

This application note describes the programming procedures for each EEPROM module (four in each MCM) and details of various techniques to preserve data protection.

Automatic Page Write

Page-mode write feature allows from 1 to 128 bytes of data to be written into the EEPROM in a single write cycle, and allows the undefined data within 128 bytes to be written corresponding to the undefined address (A0 to A6). Loading the first byte of data, the data load window opens 30 µs for the second byte. In the same manner each additional byte of data can be loaded within 30 µs. In case $\overline{CE}$ and $\overline{WE}$ are kept high for 100 µs after data input, the EEPROM enters erase and write mode automatically and only the input data are written into the EEPROM.

$\overline{WE}$ $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

$\overline{Data}$ Polling

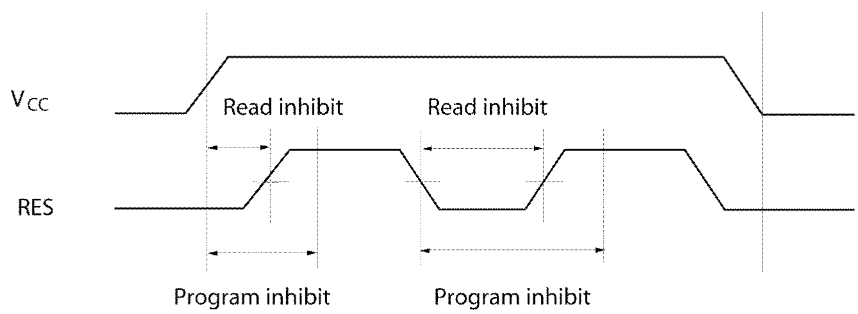
$\overline{Data}$ Polling function allows the status of the EEPROM to be determined. If the EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded output is from I/O 7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{Busy}$ Signal

RDY/$\overline{Busy}$ signal also allows a comparison operation to determine the status of the EEPROM. The RDY/$\overline{Busy}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the-end of a write cycle, the RDY/Busy signal changes state to high impedance.

$\overline{RES}$ Signal

When $\overline{RES}$ is LOW, the EEPROM cannot be read and programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be kept high during read and programming because it doesn't provide a latch function.

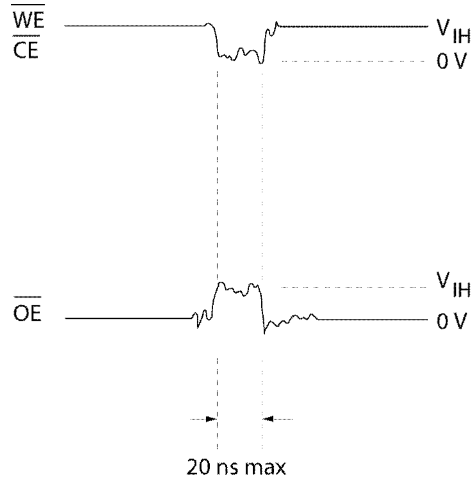


Data Protection

To protect the data during operation and power on/off, the EEPROM has the internal functions described below.

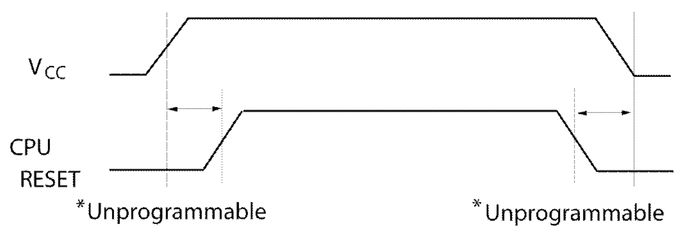
1. Data Protection against Noise of Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the EEPROM has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20ns on the control pins.

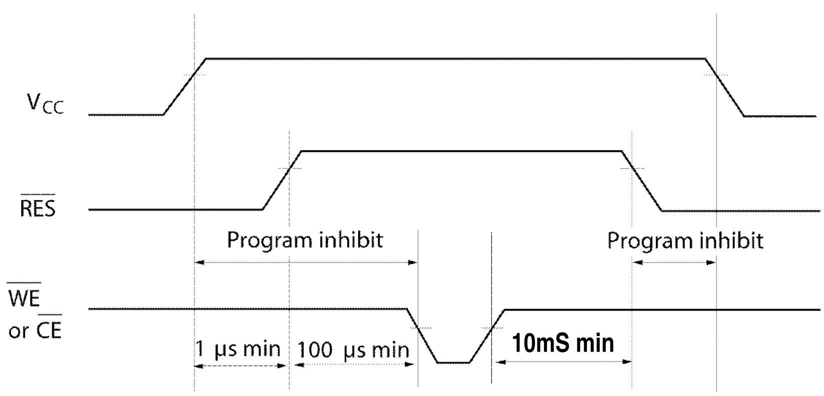


2. Data Protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits, such as CPUs, may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in unprogrammable state during V_{CC} on/off by using a CPU reset signal to $\overline{RES}$ pin.



$\overline{RES}$ should be kept at V_{SS} level when V_{CC} is turned on or off. The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.



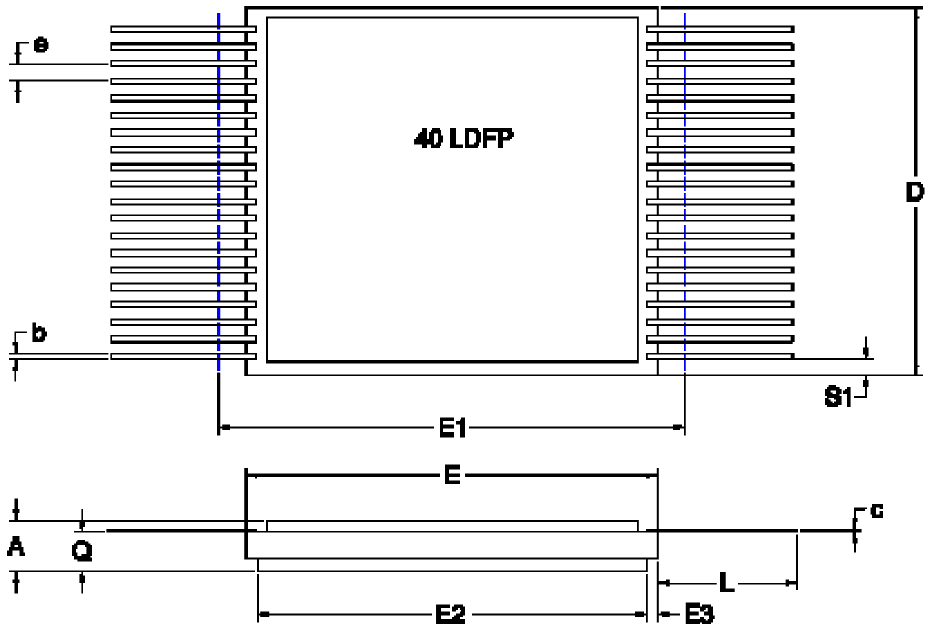
3. Software Data Protection

The software data protection function is to prevent unintentional programming caused by noise generated by external circuits. In software data protection mode, 3 bytes of data must be input before write data as follows. These bytes can switch the non-protection mode to the protection mode.

Address	Data	
5555	AA	
↓	↓	
AAAA or 2AAA	55	
↓	↓	
5555	A0	
↓	↓	
Write address	Write data }	Normal data input

Software data protection mode can be canceled by inputting the following 6 bytes. Then, the EEPROM turns to the non-protection mode and can write data normally. However, when the data is input in the canceling cycle, the data cannot be written.

Address	Data
5555	AA
↓	↓
AAAA or 2AAA	55
↓	↓
5555	80
↓	↓
5555	AA
↓	↓
AAAA or 2AAA	55
↓	↓
5555	20

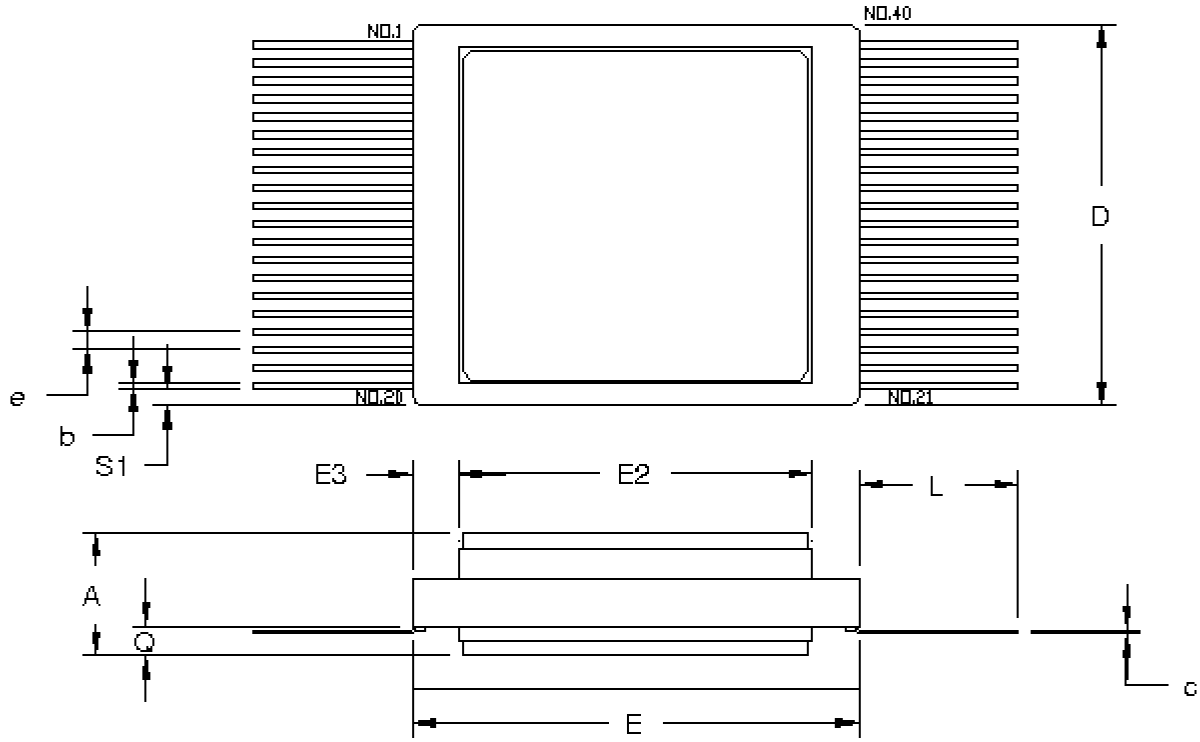


40 Pin Rad-Pak® Package Dimensions

Symbol	Dimension		
	Min	Nom	Max
A	0.248	0.274	0.300
b	0.013	0.015	0.022
c	0.006	0.008	0.010
D	--	0.850	0.860
E	0.985	0.995	1.005
E1	--	--	1.025
E2	0.890	0.895	--
E3	0.000	0.050	--
e	0.040 BSC		
L	0.380	0.390	0.400
Q	0.214	0.245	0.270
S1	0.005	0.038	--
N	40		

F40-01

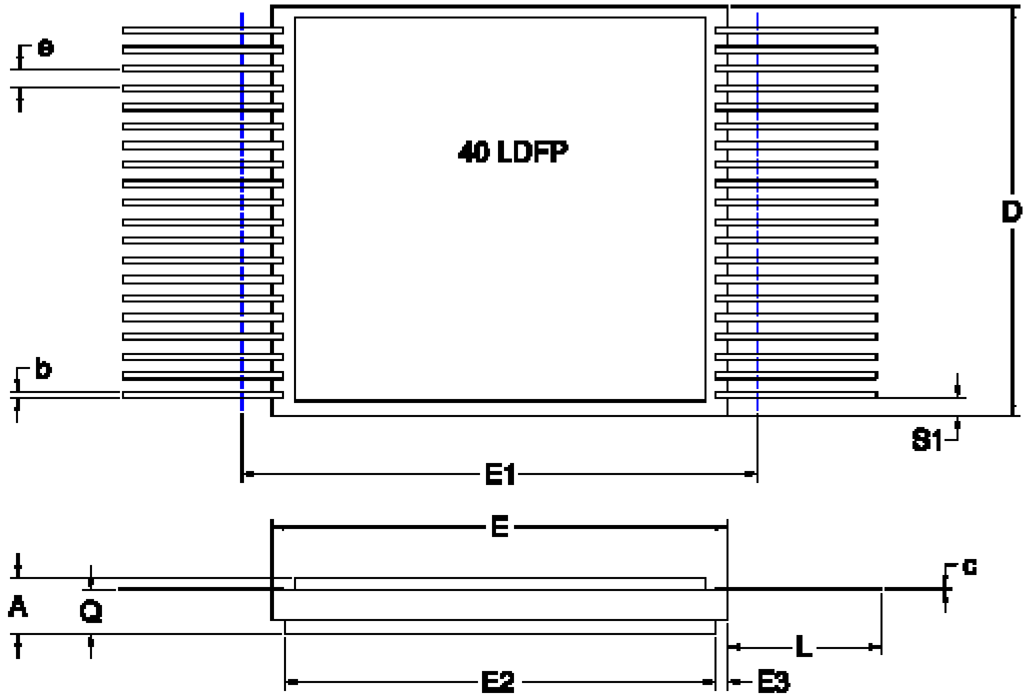
Note: All dimensions in inches



40 Pin X-Ray-Pak™ Flat Package Dimensions

Symbol	Dimension		
	Min	Nom	Max
A	0.248	0.274	0.300
b	0.013	0.015	0.022
c	0.006	0.008	0.010
D	0.840	0.850	0.860
E	0.985	0.995	1.005
E2	--	0.785	--
E3	--	0.105	--
e	0.040 BSC		
L	0.340	0.350	0.400
Q	0.050	0.065	0.075
S1	--	0.035	--
N	40		

NOTE: All Dimensions in Inches



40 Pin Rad-Tolerant Flat Package Dimensions

Symbol	Dimension		
	Min	Nom	Max
A	0.202	0.224	0.246
b	0.013	0.015	0.022
c	0.006	0.008	0.010
D	--	0.850	0.860
E	0.985	0.995	1.005
E1	--	--	1.025
E2	0.890	0.895	--
E3	0.000	0.050	--
e	0.040 BSC		
L	0.380	0.390	0.400
Q	0.190	0.212	0.236
S1	0.005	0.038	--
N	40		

NOTE: All Dimensions in Inches

Important Notice:

These data sheets are created using the chip manufacturers published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

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Product Ordering Options

Model Number

79LV0408 XX F X -XX

	Feature	Option Details
-XX	Access Time	20 = 200 ns 25 = 250 ns
X	Screening Flow	Multi Chip Module (MCM)[1] K = Maxwell Self-Defined Class K H = Maxwell Self-Defined Class H I = Engineering (testing @-55°C, +25°C and +125°C) E = Engineering (testing @ +25°C
F	Package	F = Flat Pack
XX	Radiation Feature	RP = RAD-PAK® package RT1 = Guaranteed to 10 krad at die level RT2 = Guaranteed to 25 krad at die level RT4 = Guaranteed to 40 krad at die level XP = X-Ray Pak
79LV0408	Base Product Nomenclature	4 Megabit (512k x 8-bit) EEPROM MCM

1) Products are manufactured and screened to Maxwell Technologies self-defined Class H and Class K flows.