SONY

CXD2463R

Timing Controller for CCD Camera

Description

The CXD2463R generates the sync signals for timing control and back end signal processing in a CCD camera system using a 510H or 760H black-and-white CCD image sensor.

Features

- Built-in sync signal generation function
- Built-in electronic iris (electronic shutter) function
- Supports low-speed limiter for electronic iris
- Supports external synchronization (Line-Lock, VReset + HPLL)
- Supports automatic external sync discrimination
- Window pulse output for backlight compensation
- Built-in V driver

Applications

- Surveillance camera
- Door phone camera

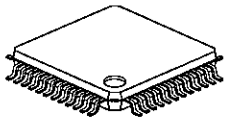
Structure

Silicon gate CMOS IC

Applicable CCD Image Sensors

- Type 1/2, 760H black-and-white CCD (EIA/CCIR)
- Type 1/3, 510/760H black-and-white CCD (EIA/CCIR)
- Type 1/4, 510/760H black-and-white CCD (EIA/CCIR)

48 pin LQFP (Plastic)



Absolute Maximum Ratings

• Supply voltage	V_{DD}, AV_{DD}	V_{SS} – 0.5 to V_{SS} + 7.0	V
• Supply voltage	V_{SS}	VL – 0.5 to VL + 26.0	V
• Supply voltage	VH	VL – 0.5 to VL + 26.0	V
• Supply voltage	VM	VL – 0.5 to VL + 26.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

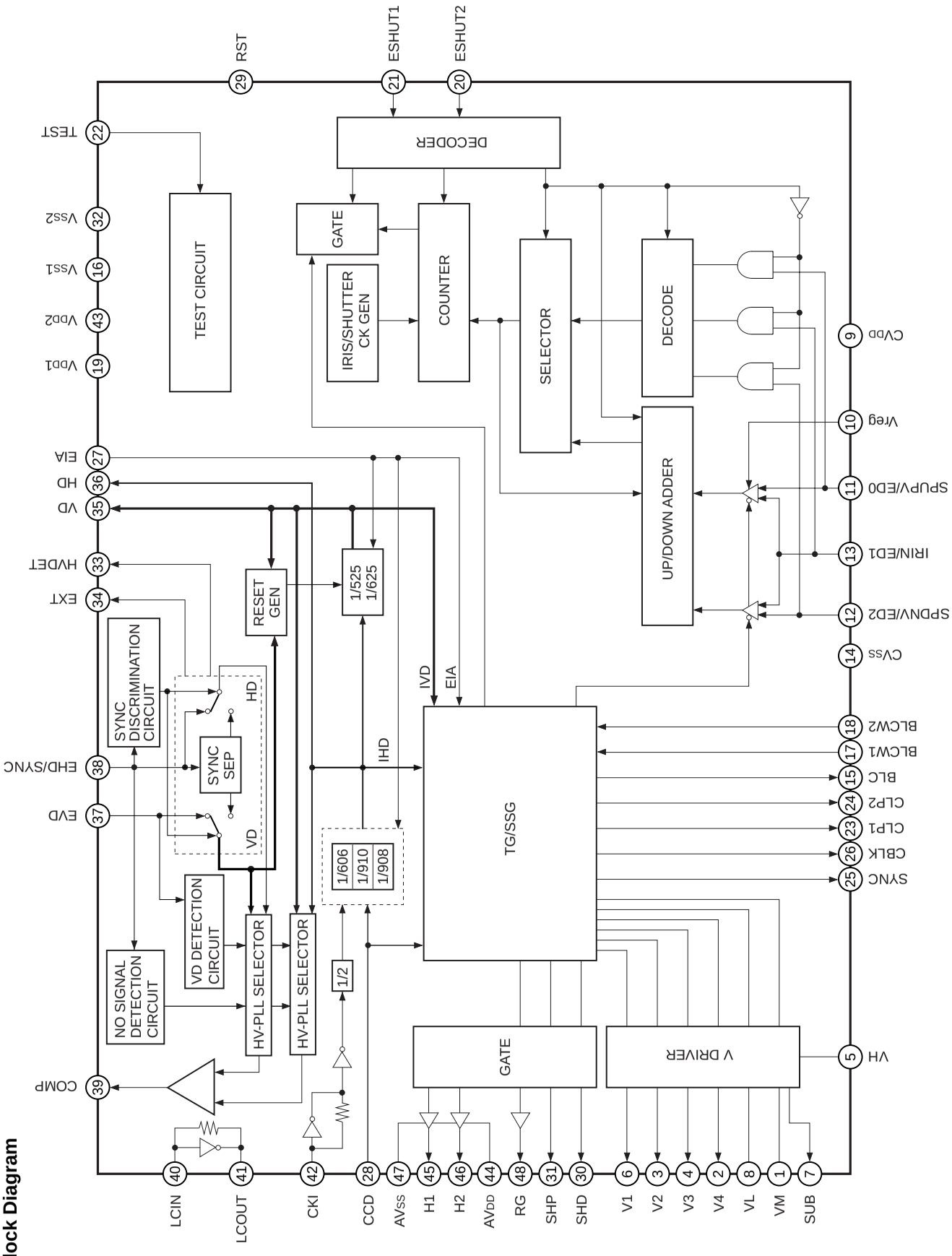
• Supply voltage 1	V_{DD}, AV_{DD}	4.75 to 5.25	V
• Supply voltage 3	VH	14.55 to 15.45	V
• Supply voltage 4	VL	–9.0 to –8.0	V
• Supply voltage 5	VM	0	V
• Operating temperature	Topr	–20 to +75	°C

Base oscillation

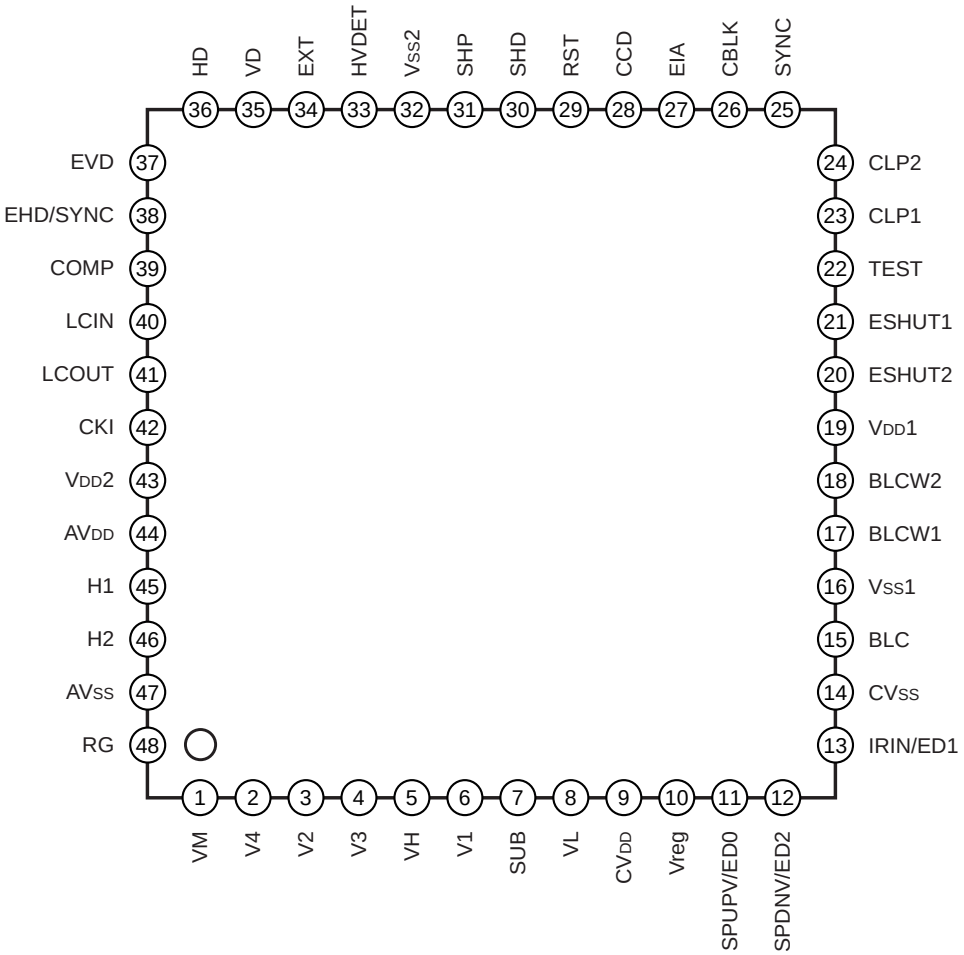
- 1212f_H (EIA: 19.0699MHz)
  (CCIR: 18.9375MHz)
- 1820f_H (EIA: 28.6364MHz)
- 1816f_H (CCIR: 28.375MHz)

E98930F1Z

Block Diagram



Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	I/O	Description
1	VM	—	Power supply (GND for V driver)
2	V4	O	Pulse output for CCD vertical register drive
3	V2	O	Pulse output for CCD vertical register drive
4	V3	O	Pulse output for CCD vertical register drive
5	VH	—	Power supply (positive power supply for V driver)
6	V1	O	Pulse output for CCD vertical register drive
7	SUB	O	CCD discharge pulse output
8	VL	—	Power supply (negative power supply for V driver)
9	CV_{DD}	—	Power supply (for comparator)
10	Vreg	—	Bias current supply for comparator
11	SPUPV/ED0	I	Shutter speed up reference voltage/shutter speed setting
12	SPDNV/ED2	I	Shutter speed down reference voltage/shutter speed setting
13	IRIN/ED1	I	Iris signal input/shutter speed setting
14	CV_{SS}	—	GND (for comparator)

Pin No.	Symbol	I/O	Description
15	BLC	O	Window pulse output for backlight compensation
16	$V_{SS}1$	—	GND
17	BLCW1	I	Window select 1 for backlight compensation (with pull-down resistor)
18	BLCW2	I	Window select 2 for backlight compensation (with pull-down resistor)
19	$V_{DD}1$	—	Power supply
20	ESHUT2	I	Sub pulse control (with pull-down resistor)
21	ESHUT1	I	Sub pulse control (with pull-down resistor)
22	TEST	I	Fixed low (with pull-down resistor)
23	CLP1	O	Clamp pulse output
24	CLP2	O	Clamp pulse output
25	SYNC	O	Composite sync output
26	CBLK	O	Composite blanking output
27	EIA	I	Low: EIA, High: CCIR (with pull-down resistor)
28	CCD	I	Low: 510H, High: 760H (with pull-down resistor)
29	RST	I	Reset (low reset). Always input reset pulse after power-on.
30	SHD	O	Data sample-and-hold pulse
31	SHP	O	Precharge level sample-and-hold pulse
32	$V_{SS}2$	—	GND
33	HVDET	O	Horizontal PLL/Vertical PLL discrimination signal High: Vertical PLL, Low: Horizontal PLL
34	EXT	O	External sync/internal sync discrimination signal High: External sync, Low: Internal sync
35	VD	O	Vertical drive output
36	HD	O	Horizontal drive output
37	EVD	I	Vertical drive signal input (with pull-up resistor)
38	EHD/SYNC	I	Horizontal drive signal input/Composite sync input (with pull-up resistor)
39	COMP	O	Comparator output
40	LCIN	I	Inverter input for oscillation
41	LCOUT	O	Inverter output for oscillation
42	CKI	I	2MCK input
43	$V_{DD}2$	—	Power supply
44	AV_{DD}	—	Power supply (for H1, H2, and RG)
45	H1	O	H1 clock output for CCD horizontal register drive
46	H2	O	H2 clock output for CCD horizontal register drive
47	AV_{SS}	—	GND (for H1, H2, and RG)
48	RG	O	Reset gate pulse output

Electrical Characteristics

1) DC Characteristics

(V_{DD} = 5V ± 0.25V, Topr = –20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.75	5.0	5.25	V
Input voltage 1 (For input pins not listed below)	$V_{IH}1$		0.7V_{DD}			V
	$V_{IL}1$				0.3V_{DD}	V
Input voltage 2 (Pin 29)	$V_{IH}2$		0.8V_{DD}			V
	$V_{IL}2$				0.2V_{DD}	V
Input voltage 3 (Pins 11 and 12 in electronic iris mode)	$V_{IN}3$		2.0		V_{DD}	V
Input voltage 4 (Pin 13 in electronic iris mode)	$V_{IN}4$		V_{SS}		V_{DD}	V
Output voltage 1 (Pins 15, 23, 24, 25, 26, 33, 34, 35 and 36)	$V_{OH}1$	I_{OH} = –4.0mA	V_{DD} – 0.8			V
	$V_{OL}1$	I_{OL} = 8.0mA			0.4	V
Output voltage 2 (Pins 30, 31 and 48)	$V_{OH}2$	I_{OH} = –6.9mA	V_{DD} – 0.8			V
	$V_{OL}2$	I_{OL} = 3.0mA			0.4	V
Output voltage 3 (Pins 45 and 46)	$V_{OH}3$	I_{OH} = –17.4mA	V_{DD} – 0.8			V
	$V_{OL}3$	I_{OL} = 12.0mA			0.4	V
Output voltage 4 (Pin 39)	$V_{OH}4$	I_{OH} = –6.0mA	V_{DD} – 0.8			V
	$V_{OL}4$	I_{OL} = 4.0mA			0.4	V
Output voltage 5 (Pins 2, 3, 4 and 6)	$V_{OH}5$	I_{OH} = –5.0mA	V_M – 0.25			V
	$V_{OL}5$	I_{OL} = 10.0mA			V_L + 0.25	V
Output voltage 6 (Pins 4 and 6 (SG))	$V_{OH}6$	I_{OH} = –7.2mA	V_H – 0.25			V
	$V_{OL}6$	I_{OL} = 5.0mA			V_M + 0.25	V
Output voltage 7 (Pin 7)	$V_{OH}7$	I_{OH} = –4.0mA	V_H – 0.25			V
	$V_{OL}7$	I_{OL} = 5.4mA			V_L + 0.25	V
Feedback resistor 1 (Pin 42)	$R_{FE}1$	V_{IN} = V_{DD} or V_{SS}	250k	1M	2.5M	Ω
Feedback resistor 2 (Resistor between Pins 40 and 41)	$R_{FE}2$	V_{IN} = V_{DD} or V_{SS}	250k	1M	2.5M	Ω
Pull-up resistor	R_{PU}	V_{IL} = 0V	20k	50k	125k	Ω
Pull-down resistor	R_{RD}	V_{IH} = V_{DD}	20k	50k	125k	Ω
Current consumption	I_{VM}	AV_{DD} = 5V CV_{DD} = 5V $V_{DD}1$ = 5V $V_{DD}2$ = 5V		24		mA
	I_{VL}	V_L = –8.5V		1.9		mA
	I_{VH}	V_H = 15V		0.8		mA

* The typical power consumption is 148mW with the ICX054BL load (in the normal operating state).

2) Input/Output Capacitance (V_{DD} = V_I = 0V, f_M = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_{IN}			9	pF
Output pin capacitance	C_{OUT}			11	pF
I/O pin capacitance	$C_{I/O}$			11	pF

3) Comparator Characteristics (V_{DD} = 5V ± 0.25V, Topr = –20 to +75°C)

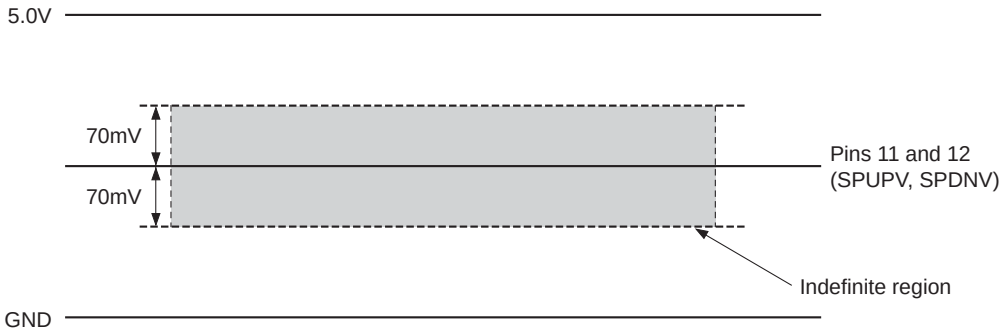
Item	Symbol	Min.	Typ.	Max.	Unit
Indefinite region	Vf			±70	mV

Note 1) Input offset voltage and indefinite region

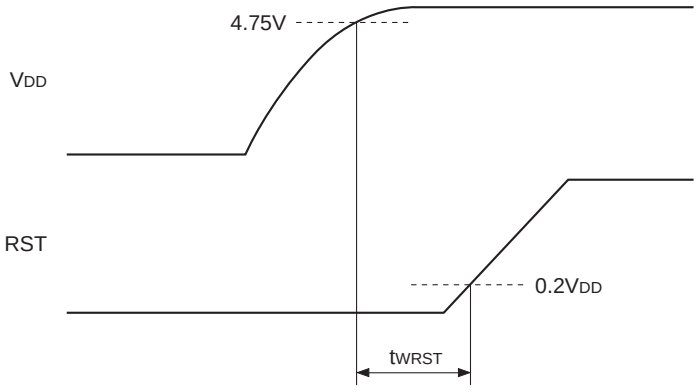
The input offset voltage and indefinite region (region in which the comparator output is not set to high or low) shown in the figure below exist in the built-in comparator in this IC, so be careful when designing the external circuit.

Note 2) Pins 11 and 12 in electronic iris mode

Make sure of Pin 11 (SPUPV) < Pin 12 (SPDNV).



4) Power-on Reset Condition



(Within the recommended operating condition)

Item	Symbol	Min.	Typ.	Max.	Unit
Power-on reset period	t_{WRST}	35			ns

1. Electronic Iris/Electronic Shutter Function

The electronic iris or electronic shutter can be selected by setting the following pins to different combinations of high and low.

ESHUT1 Pin 21	ESHUT2 Pin 20	Operating Mode
L	L	Electronic iris without limiter
H	L	Electronic iris with limiter EIA: 1/100 (s), CCIR: 1/120 (s)
L	H	Electronic shutter mode
H	H	Sub pulse stopped

1) Electronic Iris Mode

Symbol	Pin No.	Function
IRIN/ED1	13	Iris signal input
SPDNV/ED2	12	Shutter speed down reference voltage
SPUPV/ED0	11	Shutter speed up reference voltage

2) Electronic Shutter Mode

Symbol	Pin No.	Mode							
SPUPV/ED0	11	H	L	H	L	H	L	H	L
IRIN/ED1	13	H	H	L	L	H	H	L	L
SPDNV/ED2	12	H	H	H	H	L	L	L	L
Shutter speed		EIA: 1/100 CCIR: 1/120	1/250	1/500	1/1000	1/2000	1/5000	1/10000	1/100000

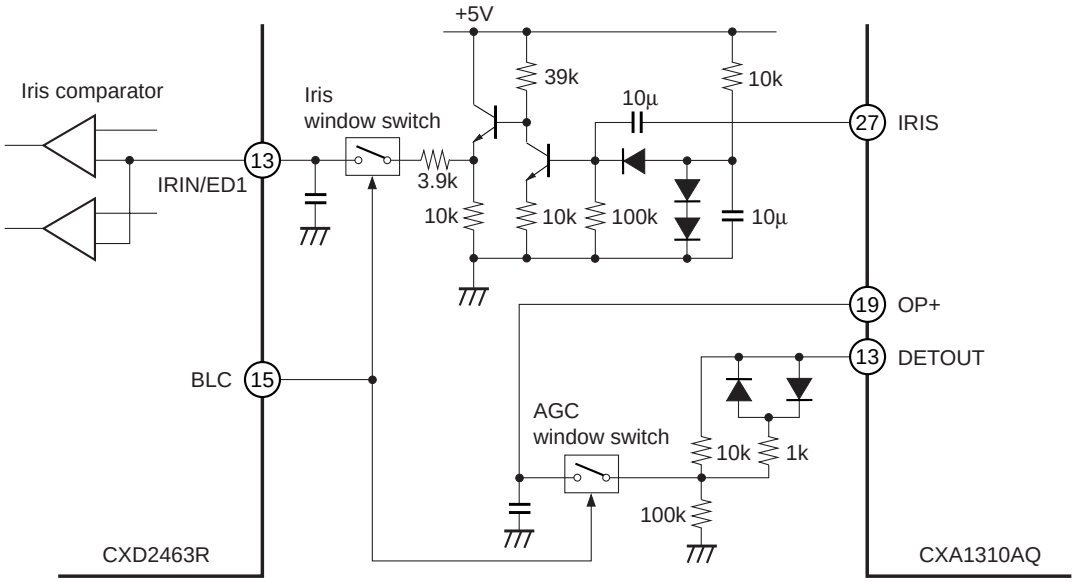
2. Backlighting Correction Function

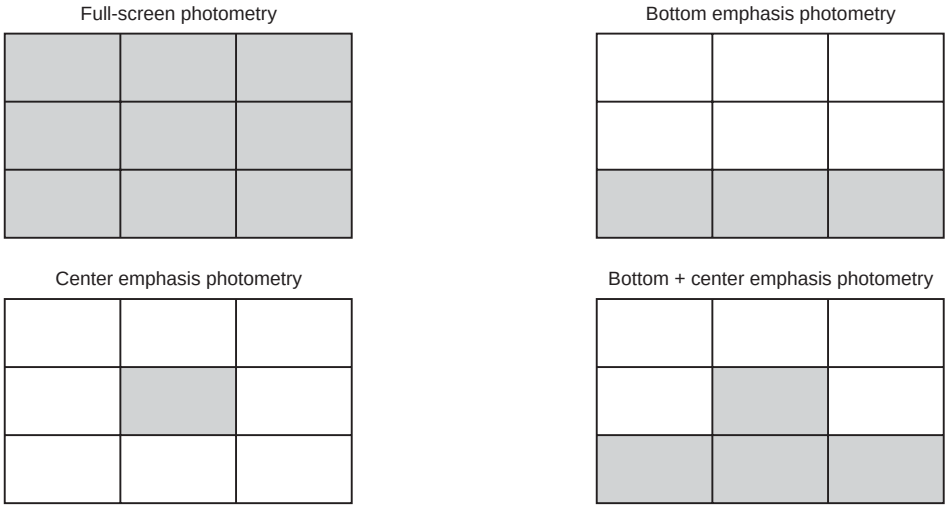
The CXD2463R has a function to output the window pulse for backlight compensation.
The backlight compensation pulse is output from BLC (Pin 15) in the following range according to the high/low combination of BLCW1 (Pin 17) and BLCW2 (Pin 18).

Window Type for Different Pin Combinations

Window type	BLCW1 (Pin 17)	BLCW2 (Pin 18)
Full-screen photometry	L	L
Bottom emphasis photometry	H	L
Center emphasis photometry	L	H
Bottom + center emphasis photometry	H	H

Example of Basic Circuit Configuration

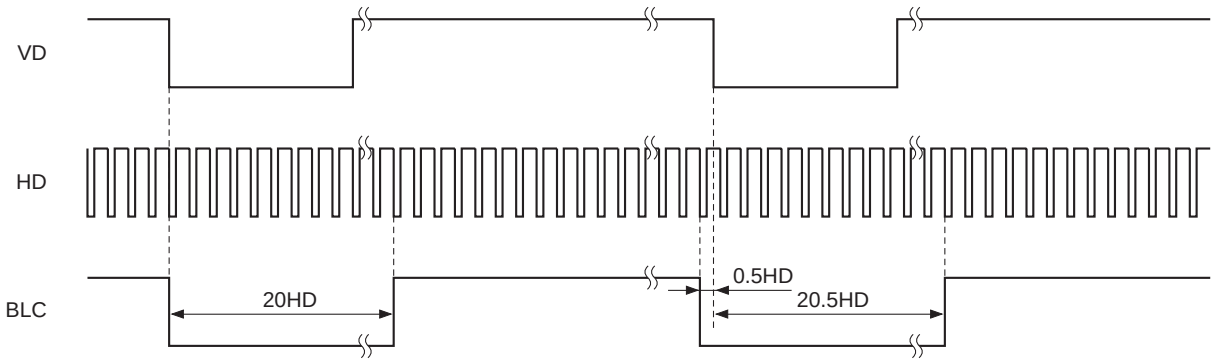




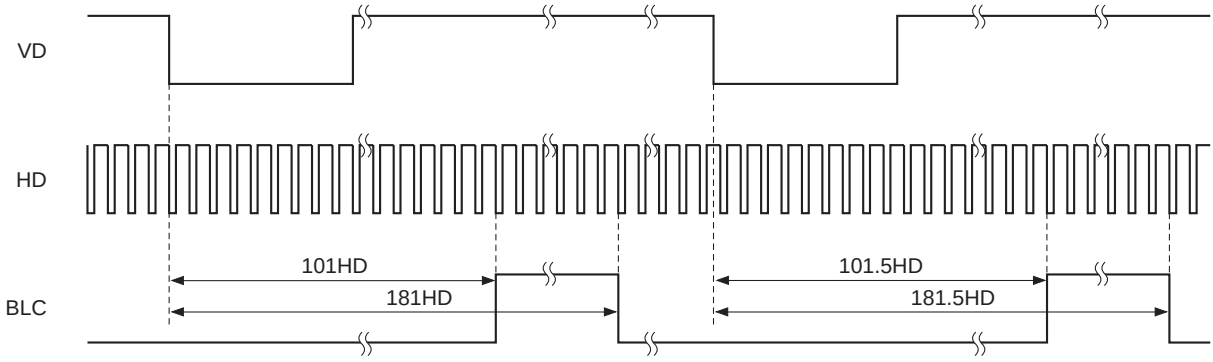
1) Window Pulse Timing Charts

• EIA Mode/Vertical Direction Timing

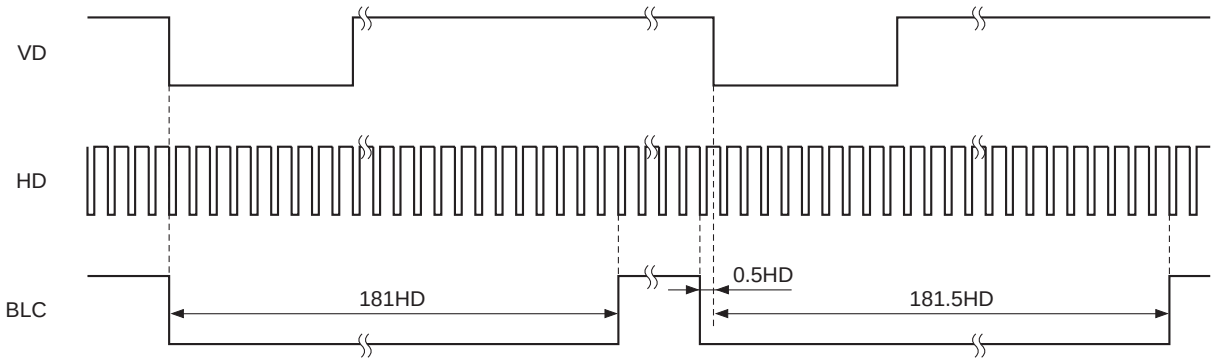
(1) Full-screen photometry



(2) Center emphasis photometry

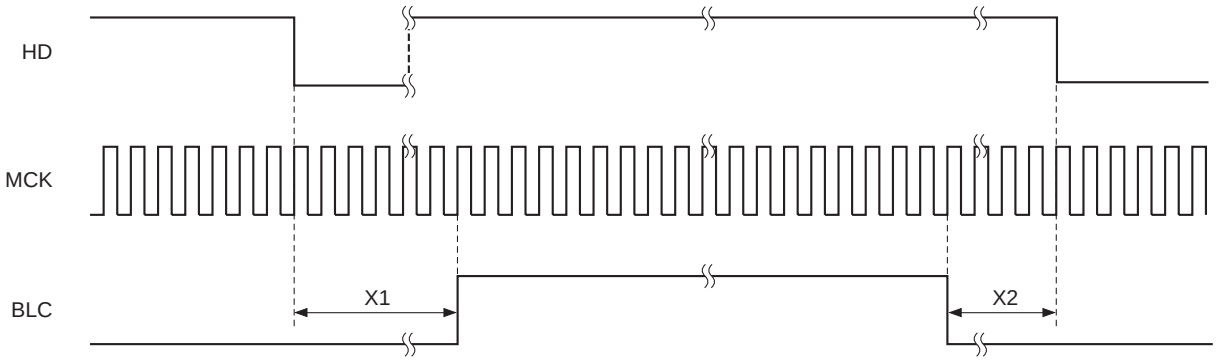


(3) Bottom emphasis photometry



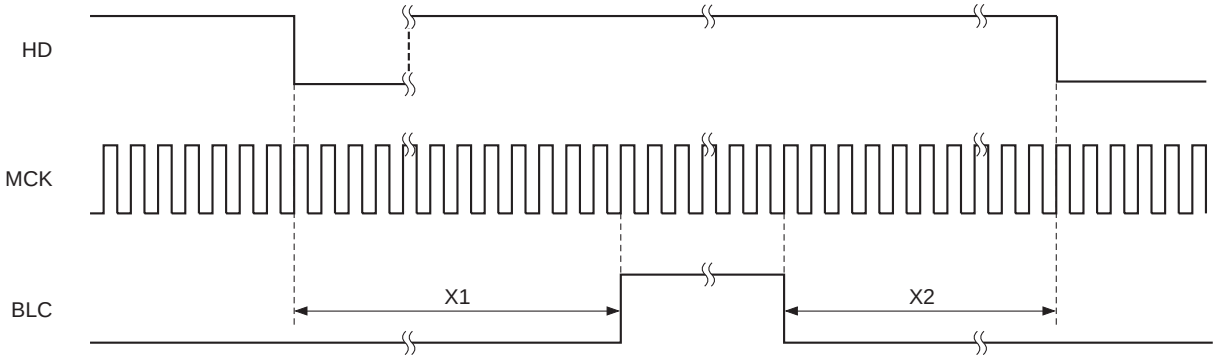
• EIA Mode/Horizontal Direction Timing

(1) Bottom emphasis photometry and full-screen photometry



X1	510H	104MCK
	760H	154MCK
X2	510H	3MCK
	760H	22MCK

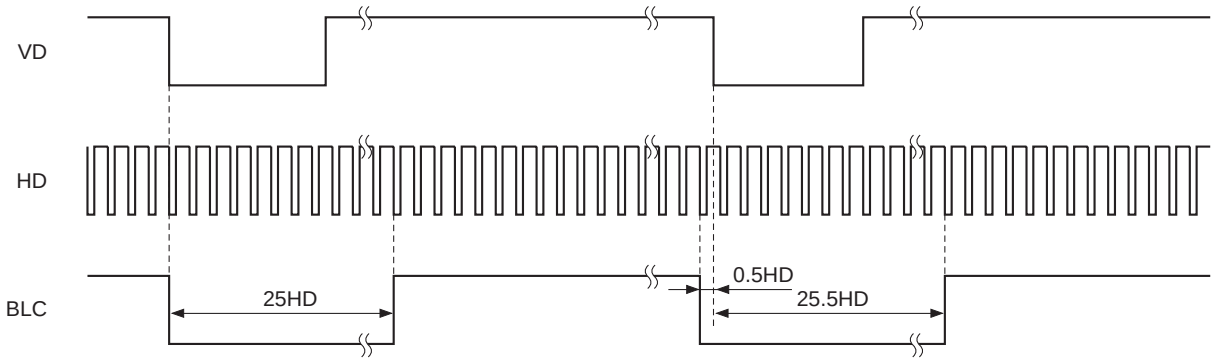
(2) Center emphasis photometry



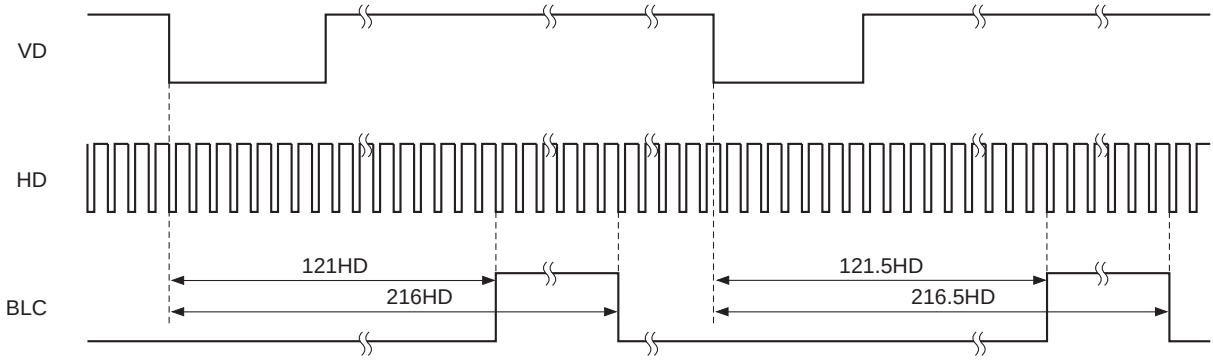
X1	510H	272MCK
	760H	407MCK
X2	510H	167MCK
	760H	252MCK

• CCIR Mode/Vertical Direction Timing

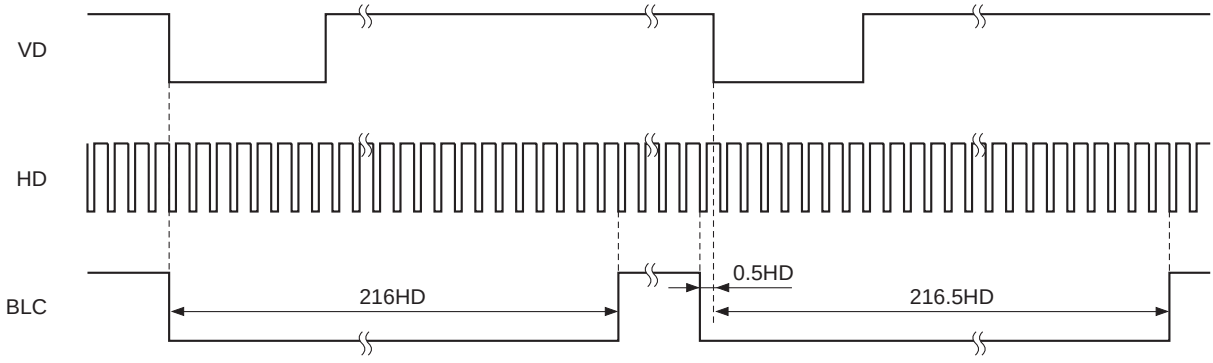
(1) Full-screen photometry



(2) Center emphasis photometry

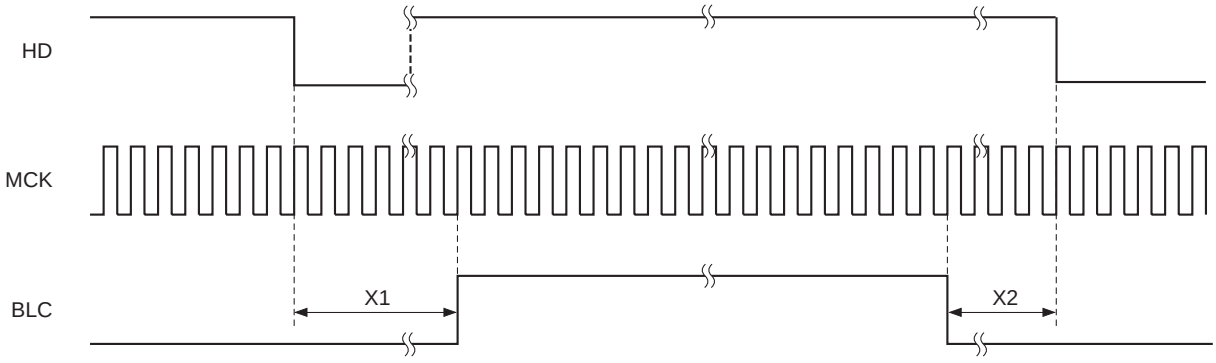


(3) Bottom emphasis photometry



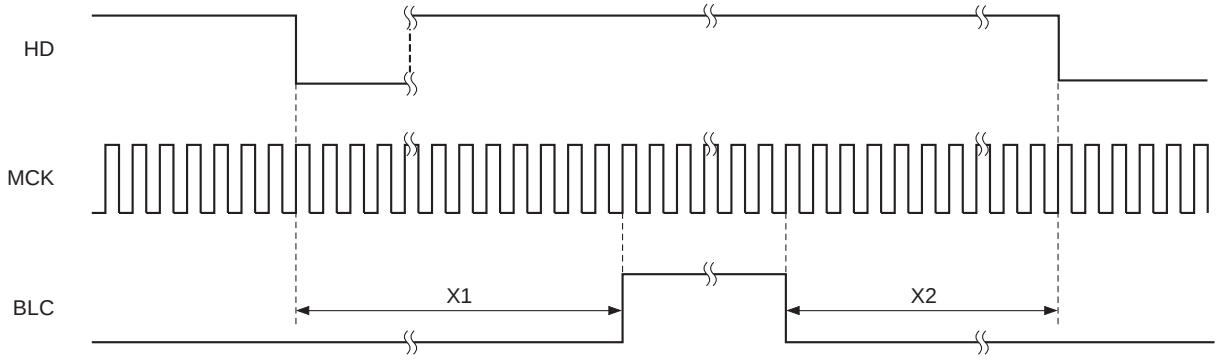
• CCIR Mode/Horizontal Direction Timing

(1) Bottom emphasis photometry and full-screen photometry



X1	510H	114MCK
	760H	169MCK
X2	510H	3MCK
	760H	22MCK

(2) Center emphasis photometry



X1	510H	279MCK
	760H	416MCK
X2	510H	164MCK
	760H	246MCK

3. External Sync Function

The CXD2463R supports the three modes of Line-Lock, VReset + HPLL (VD and HD inputs), and VReset + HPLL (Sync input) as the external sync functions. Each mode is automatically switched according to the combination of signals input to EHD/SYNC (Pin 38) and EVD (Pin 37).

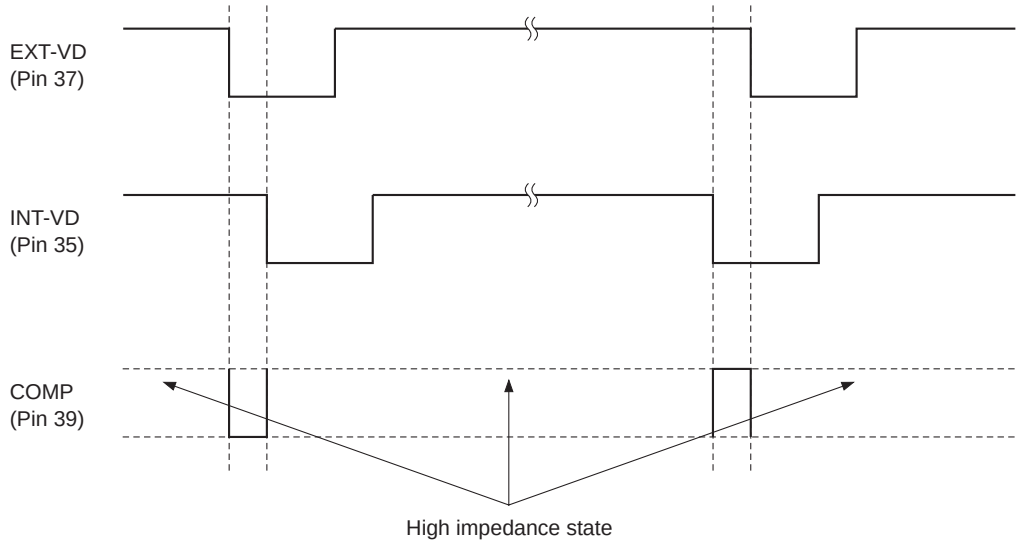
1) Automatic External Sync Discrimination

I/O	Symbol	Pin No.	EHD/SYNC and EVD pins signal input state and HVDET and EXT pins discrimination results				
I	EHD/SYNC	38	HD	No signal	HD	SYNC	No signal
I	EVD	37	No signal	VD	VD	HD after SYNC separation	No signal
O	HVDET	33	L	H	L	L	L
O	EXT	34	L	H	H	H	L
Mode			INT	LL	VReset + HPLL	VReset + HPLL	INT

• If unspecified signals are input for the external signals given above, there may be recognition errors.

2) LL (Line-Lock) Mode

When the V sync clock is externally input to EVD (Pin 37), the result of comparing the falling edge of the clock and the falling edge of the internal VD is output from COMP (Pin 39). The output polarity is compatible with the active filter.

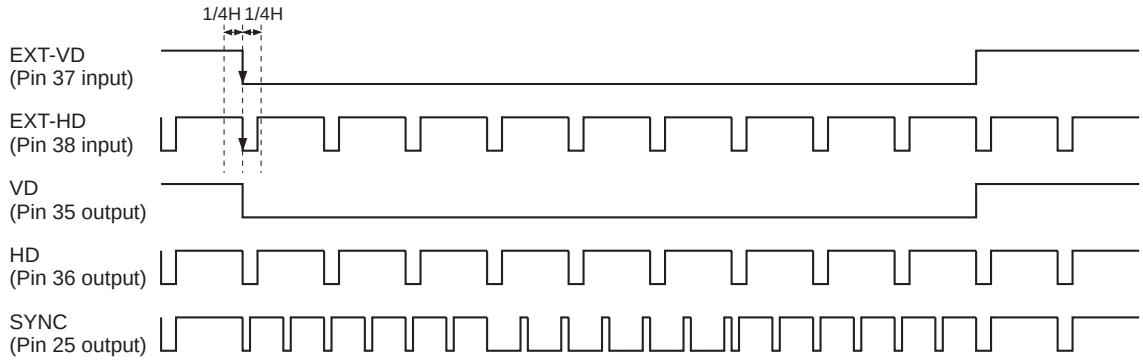


3) VReset + HPLL (VD and HD Inputs) Mode

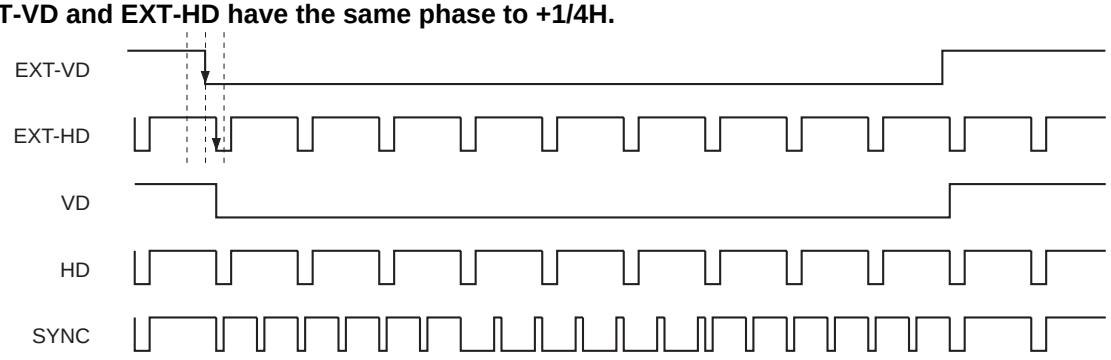
When the HD cycle clock is externally input to EHD/SYNC (Pin 38) and the V cycle clock is externally input to the EVD (Pin 37), the CXD2463R sync signal is output as shown below based on the phase difference between these signals.
Similar to Line-Lock mode, the result of comparing the phase of the falling edges of the HD cycle clock input to Pin 38 and the CXD2463R internal HD is output from COMP (Pin 39). The PLL is applied using this signal. Similar to Line-Lock mode, the polarity of the COMP (Pin 39) output is compatible with the active filter. The phase of the HD falling edge can be shifted up to ±1/4H with respect to the falling edge of the master VD (EXT-VD).

• EIA/ODD

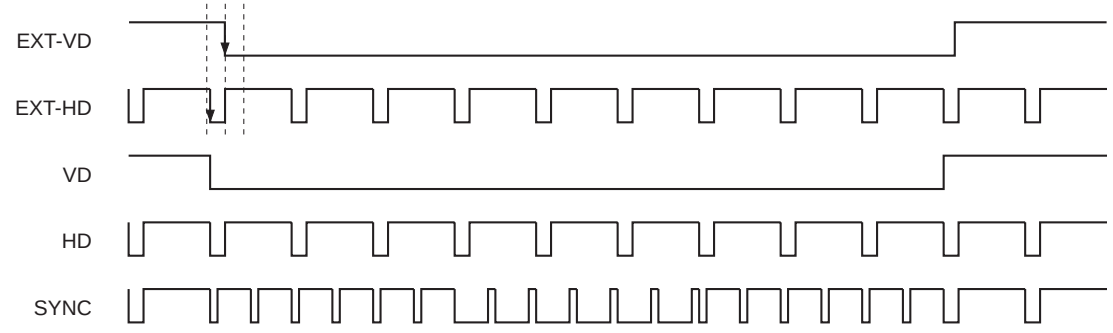
(1) EXT-VD and EXT-HD have the same phase.



(2) EXT-VD and EXT-HD have the same phase to +1/4H.

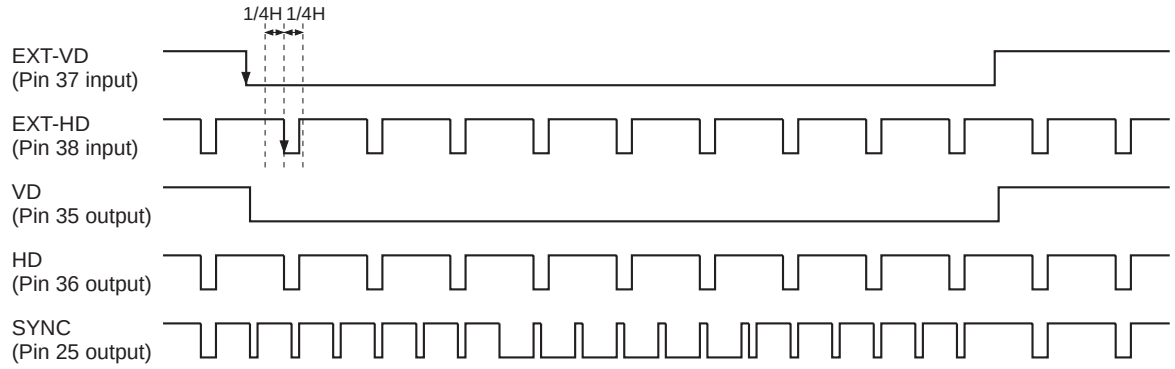


(3) EXT-VD and EXT-HD have the –1/4H to the same phase.

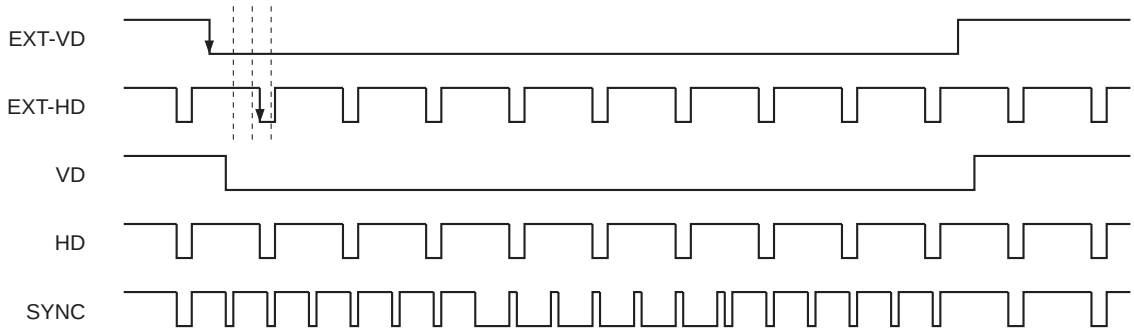


• EIA/EVEN

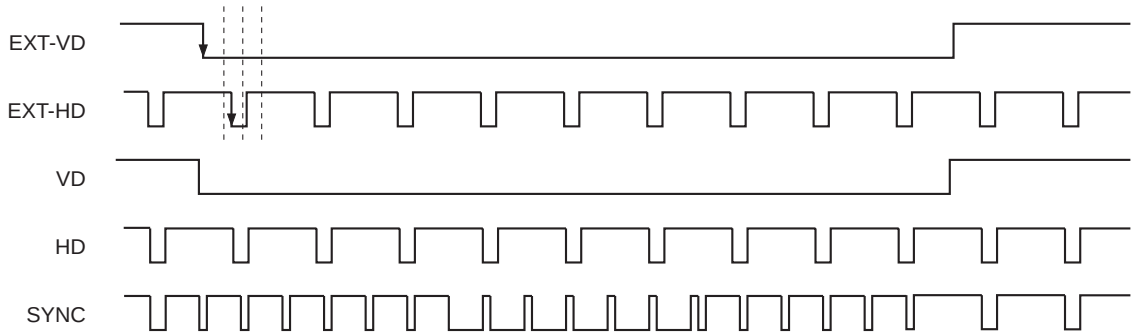
(1) EXT-VD and EXT-HD have the same phase.



(2) EXT-VD and EXT-HD have the same phase to +1/4H.

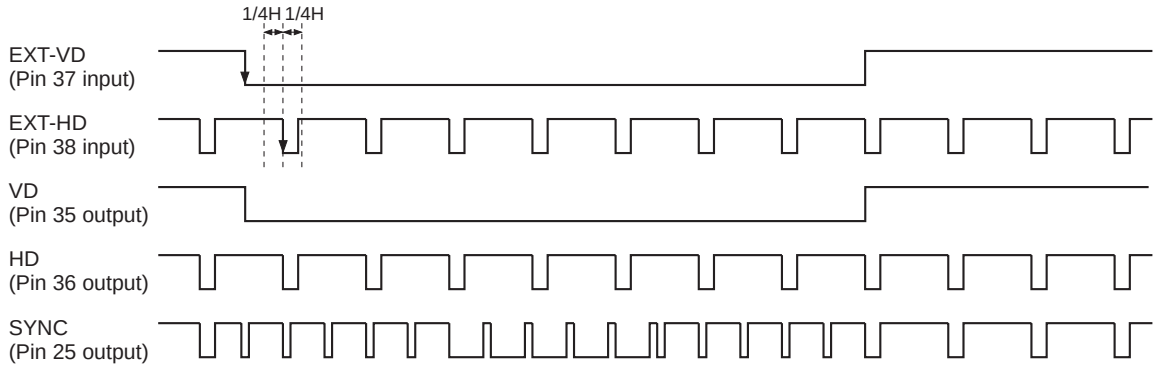


(3) EXT-VD and EXT-HD have the same phase to –1/4H.

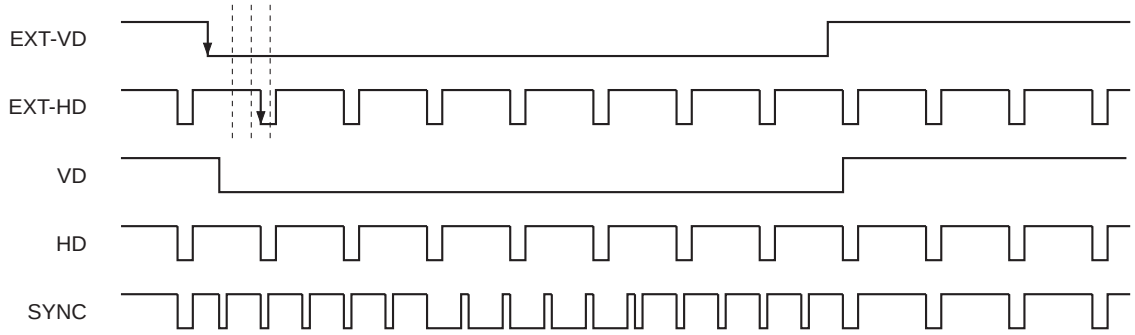


• CCIR/ODD

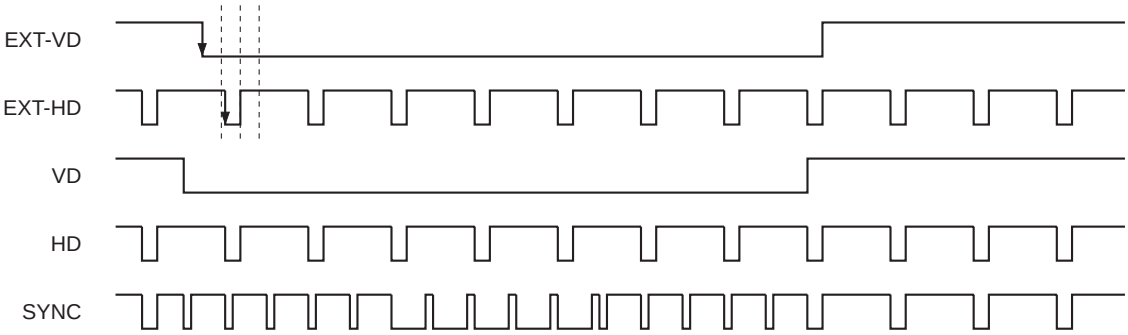
(1) EXT-VD and EXT-HD have the same phase.



(2) EXT-VD and EXT-HD have the same phase to +1/4H.

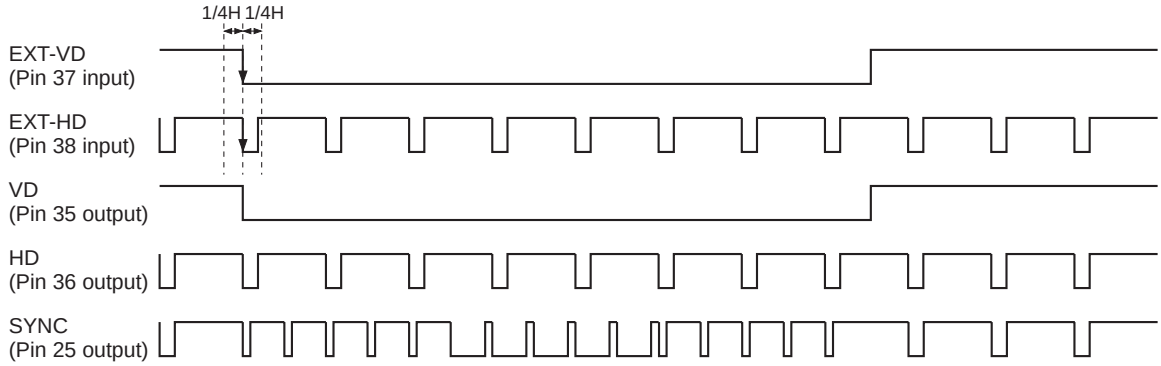


(3) EXT-VD and EXT-HD have the same phase to –1/4H.

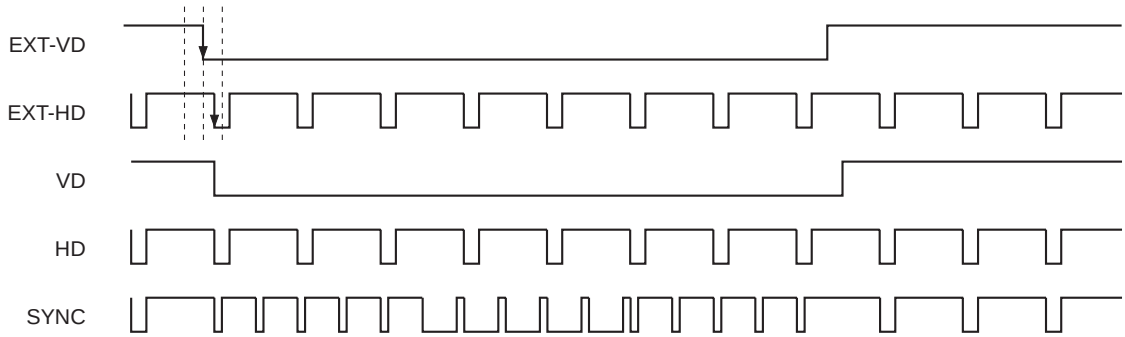


• CCIR/EVEN

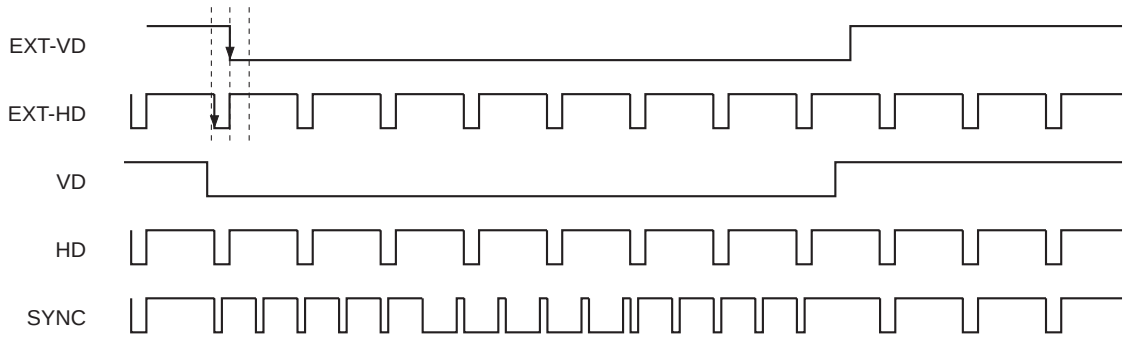
(1) EXT-VD and EXT-HD have the same phase.



(2) EXT-VD and EXT-HD have the same phase to +1/4H.



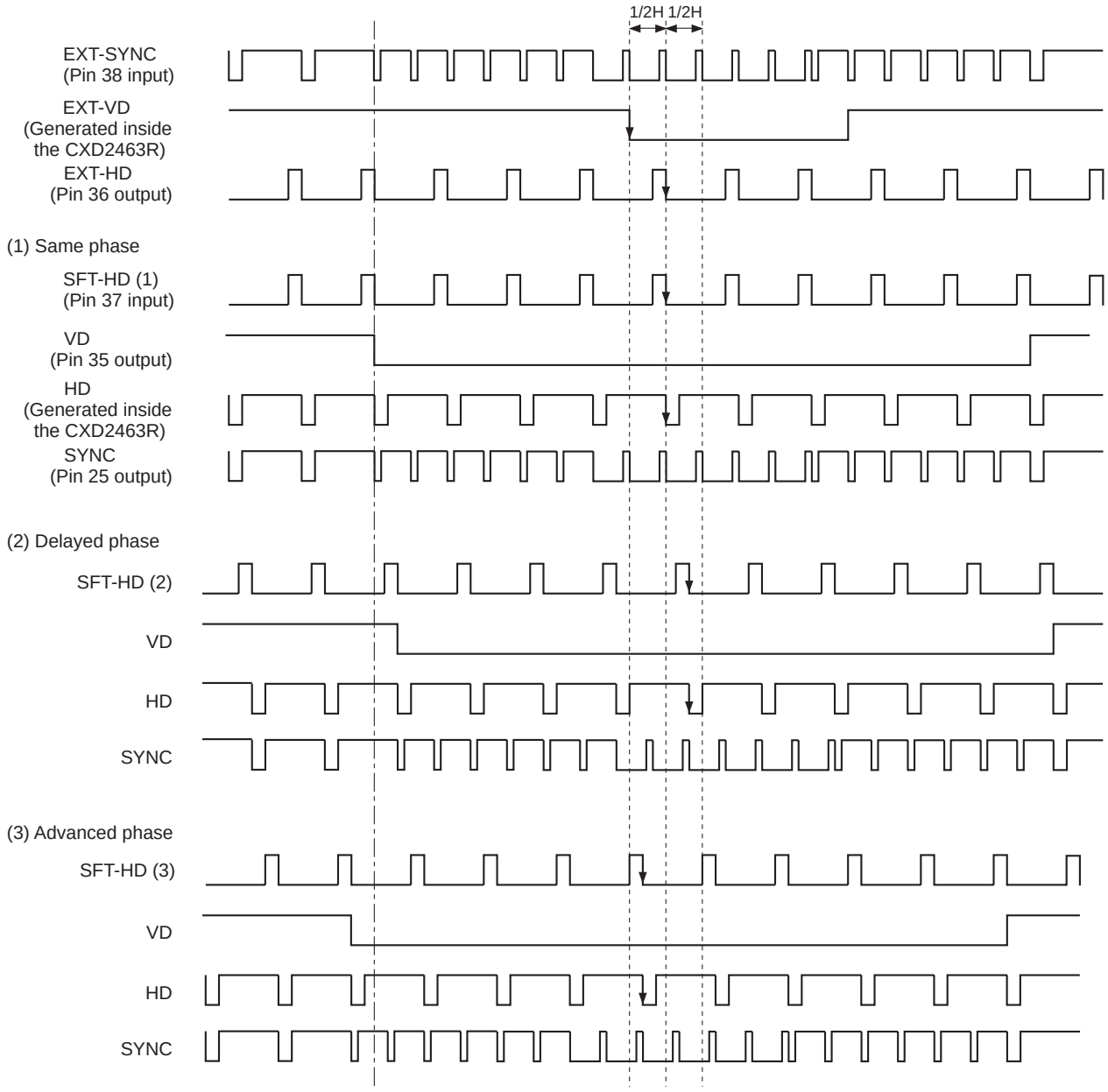
(3) EXT-VD and EXT-HD have the same phase to –1/4H.



4) VReset + HPLL (SYNC Input) Mode

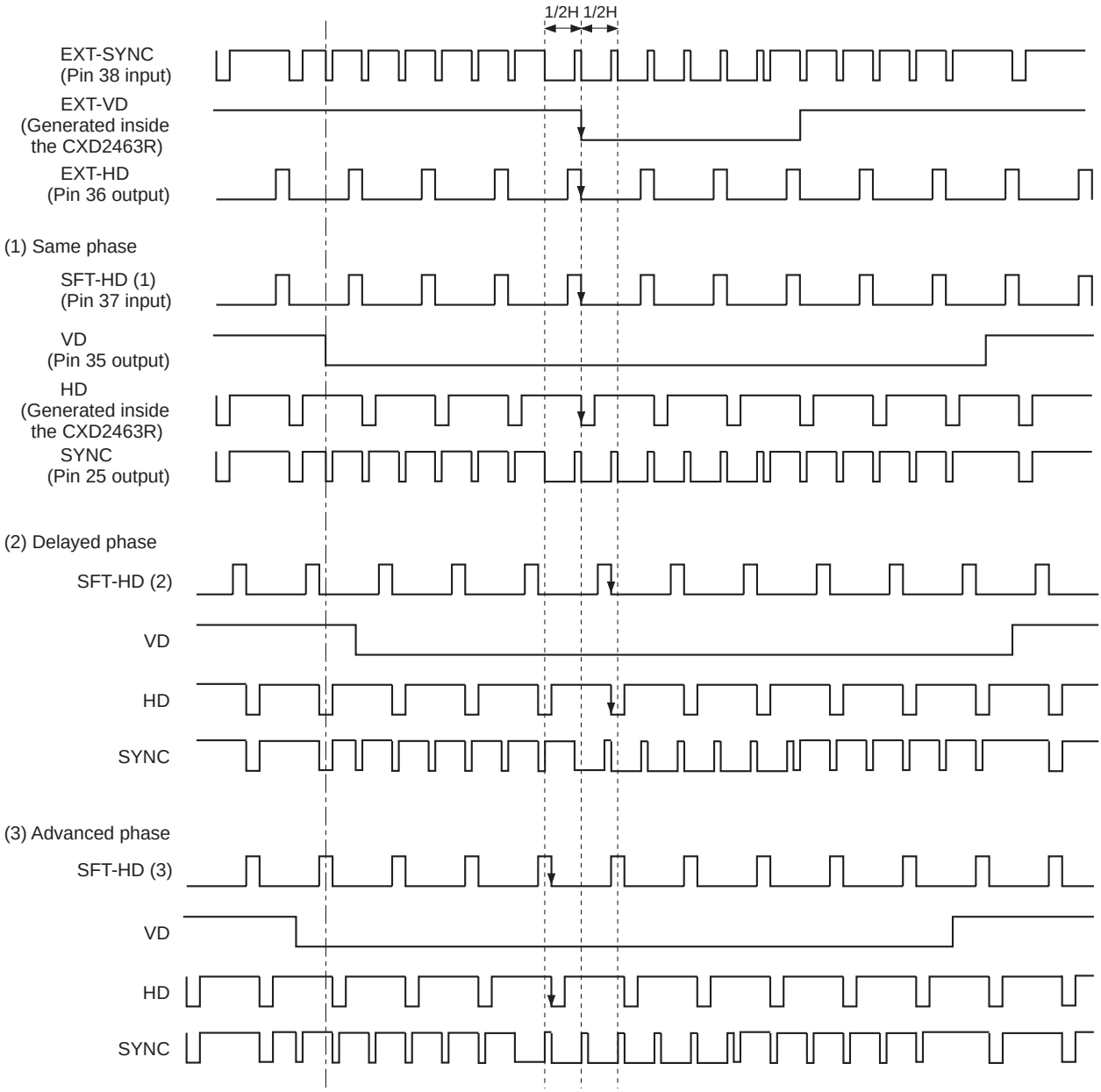
When the specified sync signal is externally input to EHD/SYNC (Pin 38), the EXT-HD separated from this sync signal is output from HD (Pin 36). This signal is input through the shifter to EVD (Pin 37). At this time, the CXD2463R sync signal is output as shown below based on the amount by which EXT-HD is shifted. (The phase can be shifted up to ±1/2H with respect to the falling edge of EXT-HD.)
COMP (Pin 39) outputs the result of comparing the phase of the falling edge of the shifted EXT-HD (signal input to Pin 37) and the falling edge of the CXD2463R internal HD. The polarity is compatible with the active filter.

• EIA/ODD

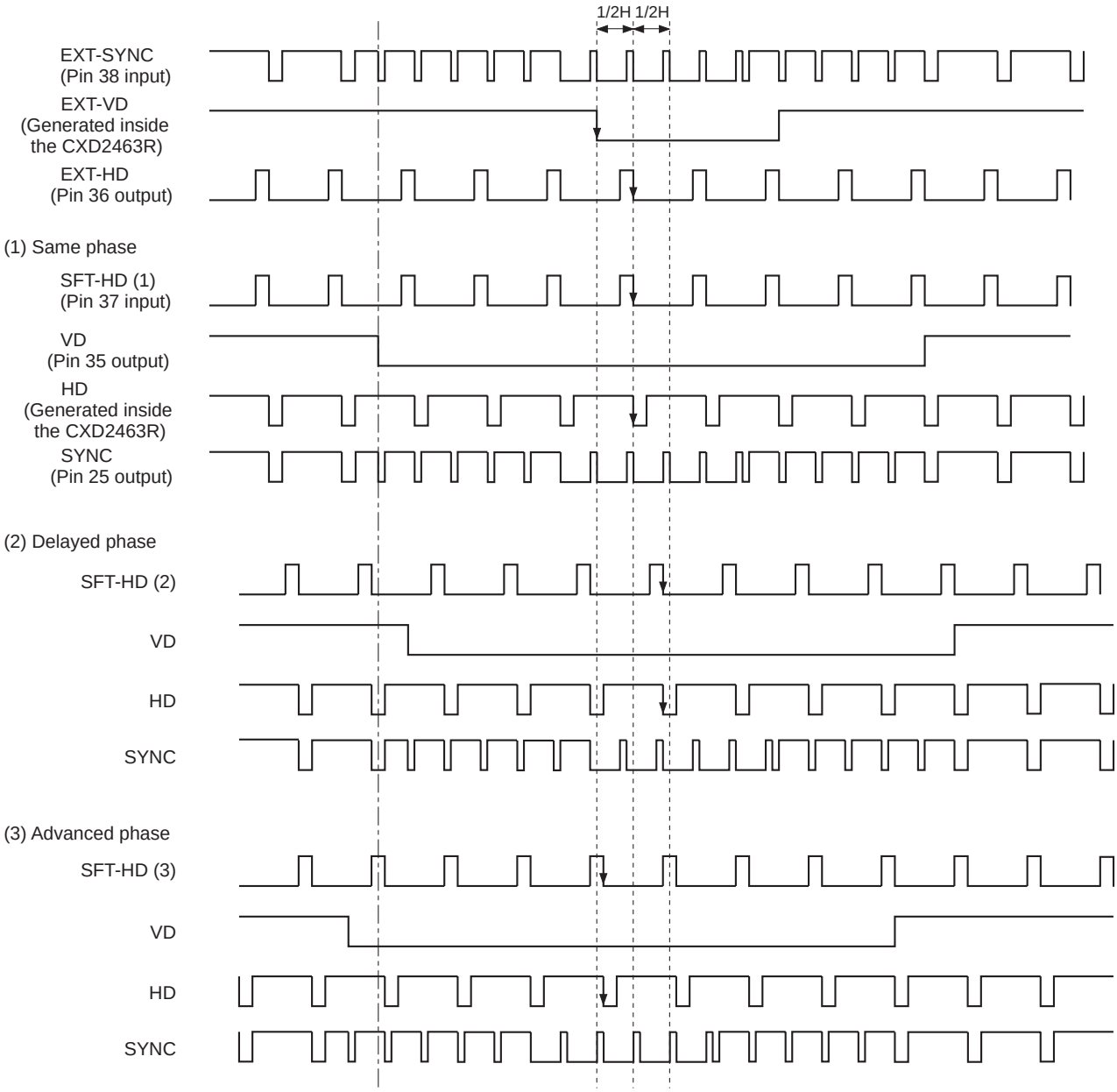


* SFT-HD (1) to (3) are the signals after shifting EXT-HD.

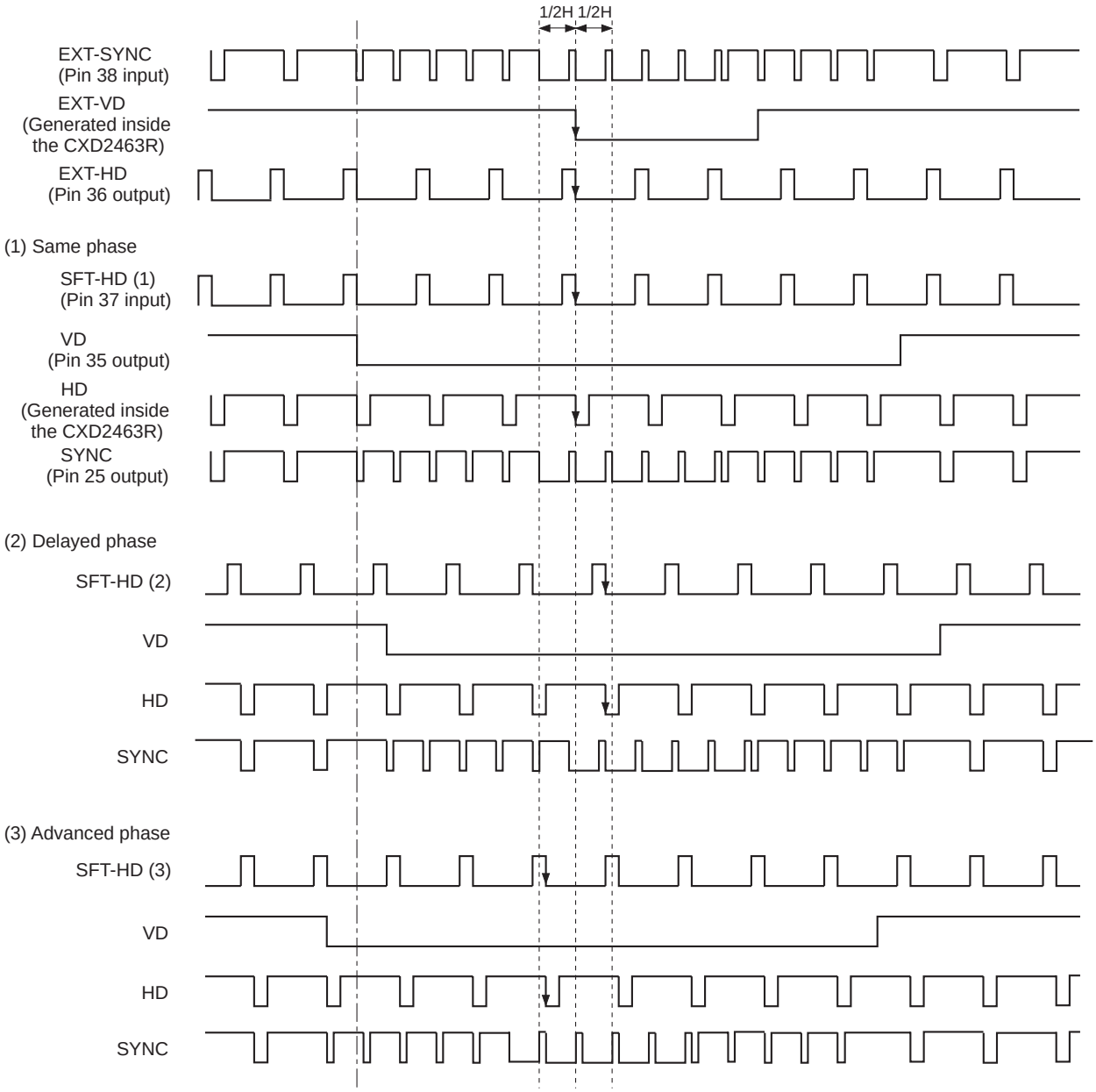
• EIA/EVEN


1/2H 1/2H
EXT-SYNC
(Pin 38 input)
EXT-VD
(Generated inside
the CXD2463R)
EXT-HD
(Pin 36 output)
(1) Same phase
SFT-HD (1)
(Pin 37 input)
VD
(Pin 35 output)
HD
(Generated inside
the CXD2463R)
SYNC
(Pin 25 output)
(2) Delayed phase
SFT-HD (2)
VD
HD
SYNC
(3) Advanced phase
SFT-HD (3)
VD
HD
SYNC

• CCIR/ODD

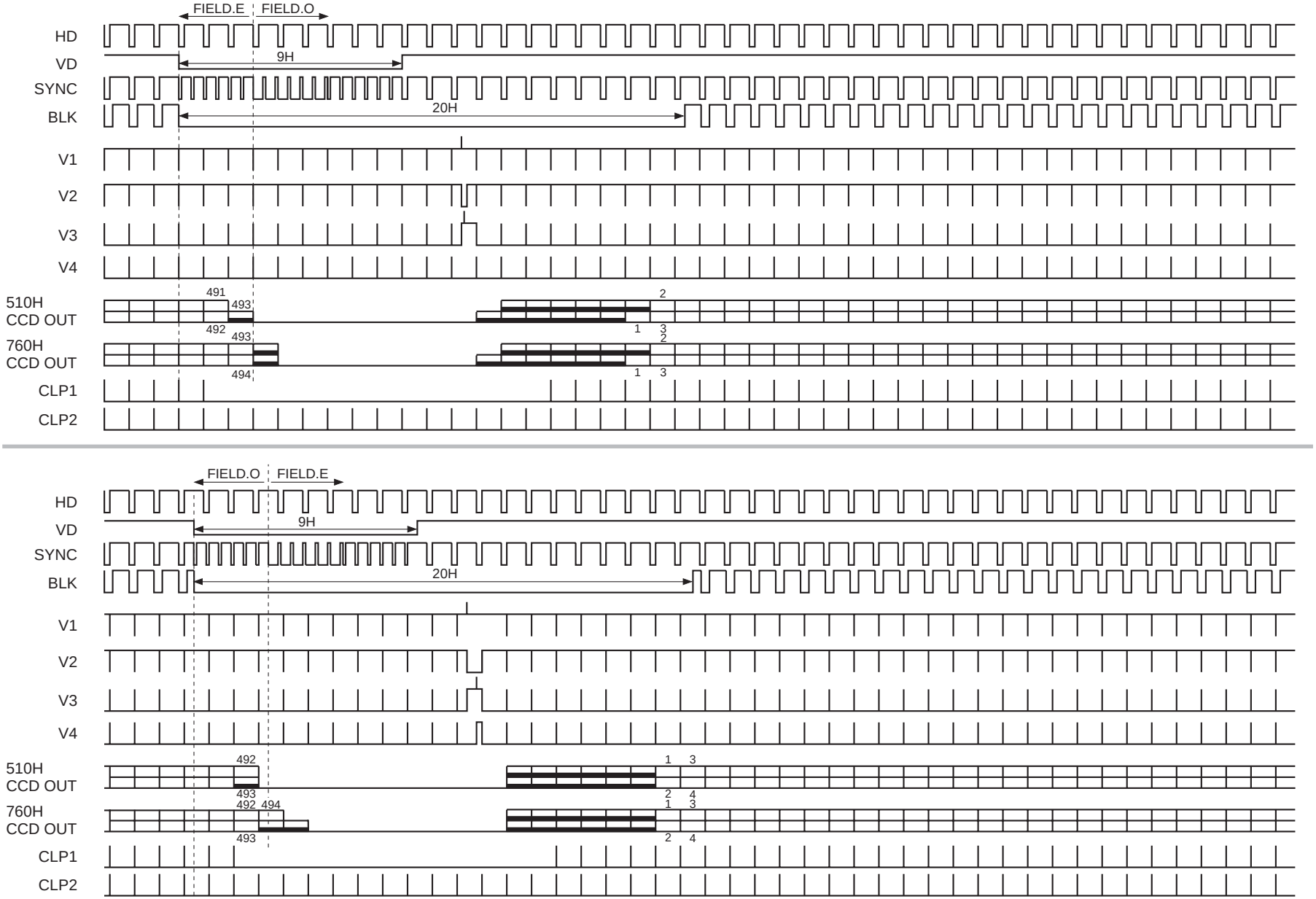

1/2H 1/2H
EXT-SYNC
(Pin 38 input)
EXT-VD
(Generated inside
the CXD2463R)
EXT-HD
(Pin 36 output)
(1) Same phase
SFT-HD (1)
(Pin 37 input)
VD
(Pin 35 output)
HD
(Generated inside
the CXD2463R)
SYNC
(Pin 25 output)
(2) Delayed phase
SFT-HD (2)
VD
HD
SYNC
(3) Advanced phase
SFT-HD (3)
VD
HD
SYNC

• CCIR/EVEN


1/2H 1/2H
EXT-SYNC
(Pin 38 input)
EXT-VD
(Generated inside
the CXD2463R)
EXT-HD
(Pin 36 output)
(1) Same phase
SFT-HD (1)
(Pin 37 input)
VD
(Pin 35 output)
HD
(Generated inside
the CXD2463R)
SYNC
(Pin 25 output)
(2) Delayed phase
SFT-HD (2)
VD
HD
SYNC
(3) Advanced phase
SFT-HD (3)
VD
HD
SYNC

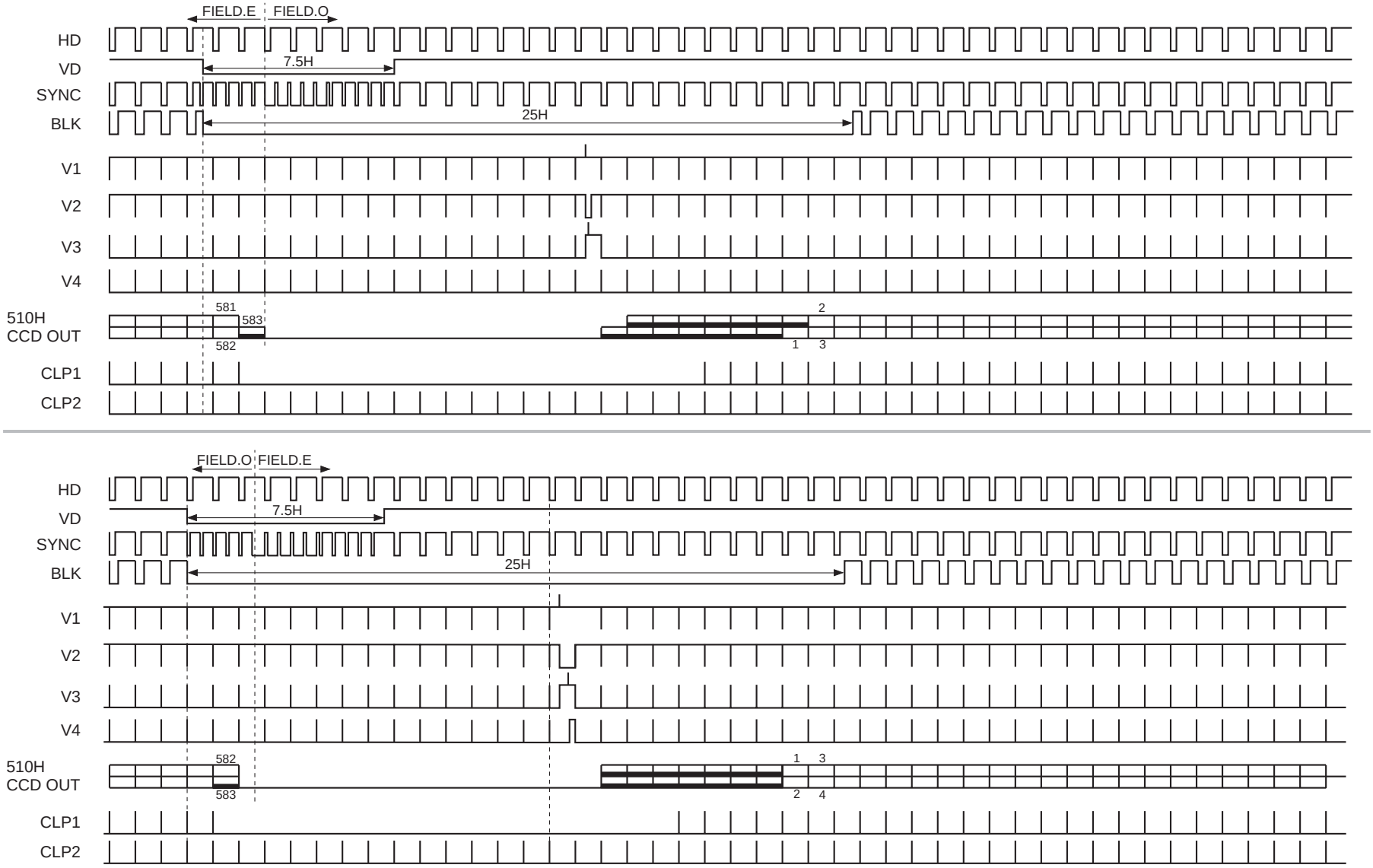
Timing Generator + Sync Generator Block Timing Chart

Vertical Direction EIA (during 510H/760H CCD drive)



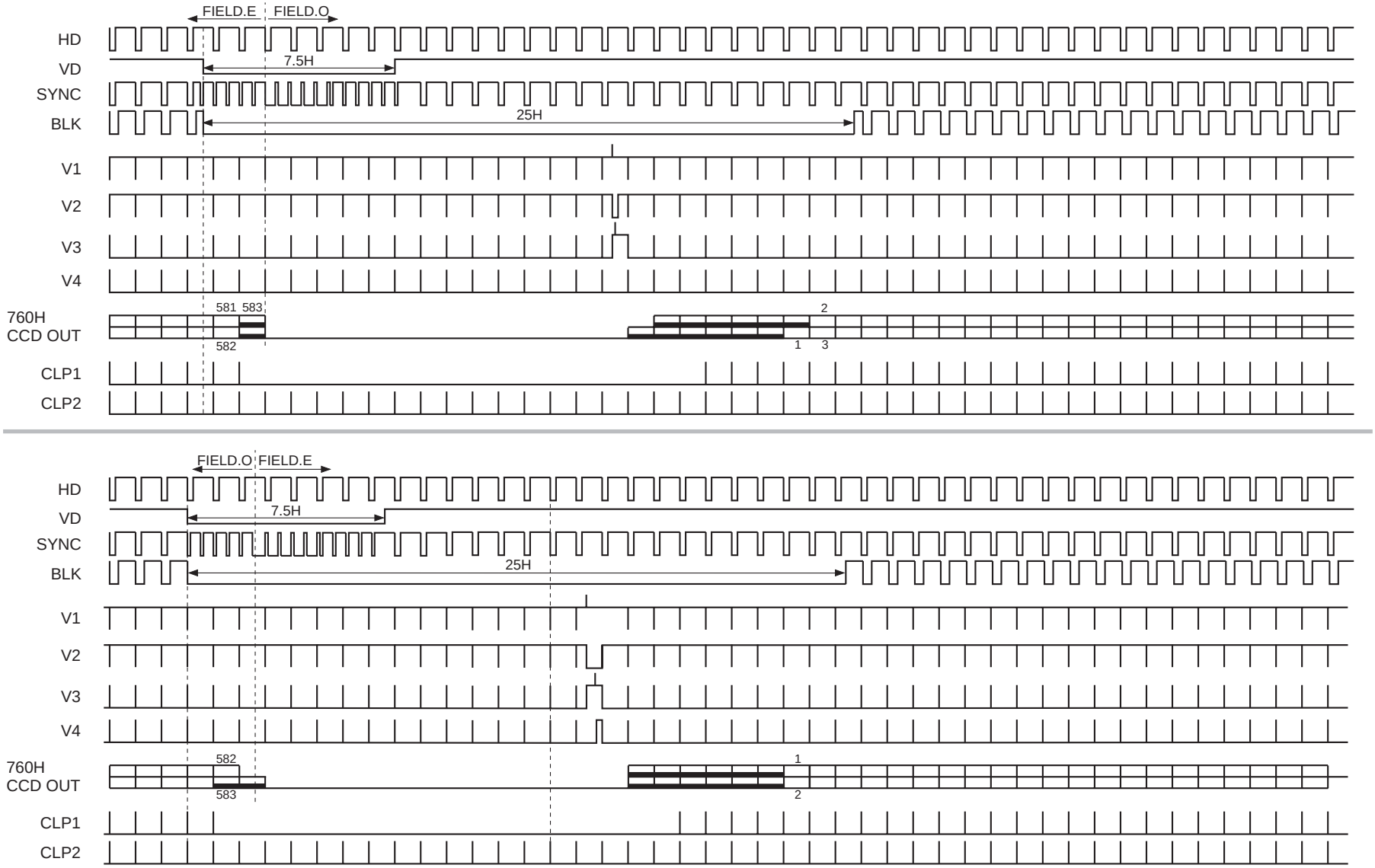
Timing Generator + Sync Generator Block Timing Chart

Vertical Direction CCIR (during 510H CCD drive)



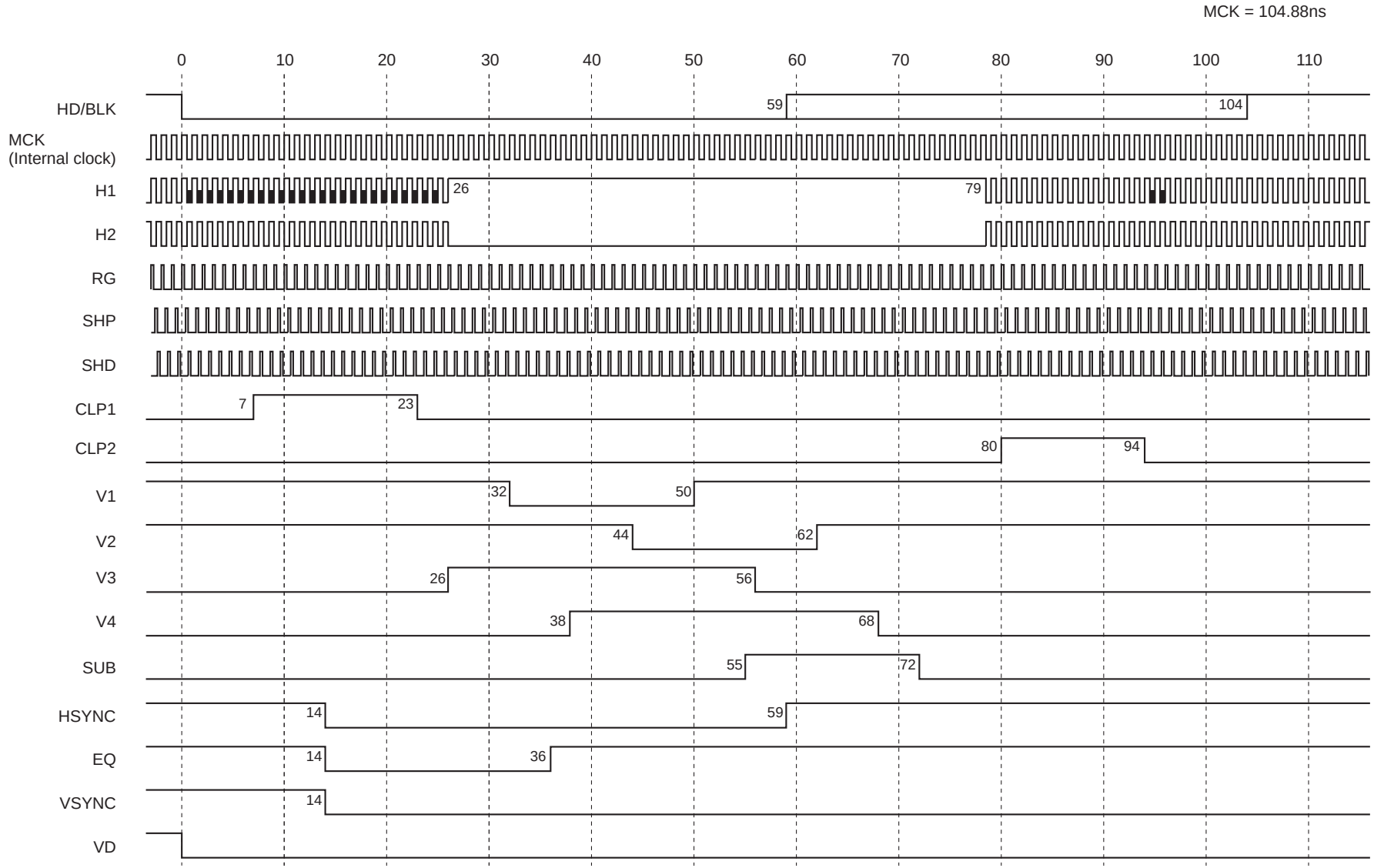
Timing Generator + Sync Generator Block Timing Chart

Vertical Direction CCIR (during 760H CCD drive)



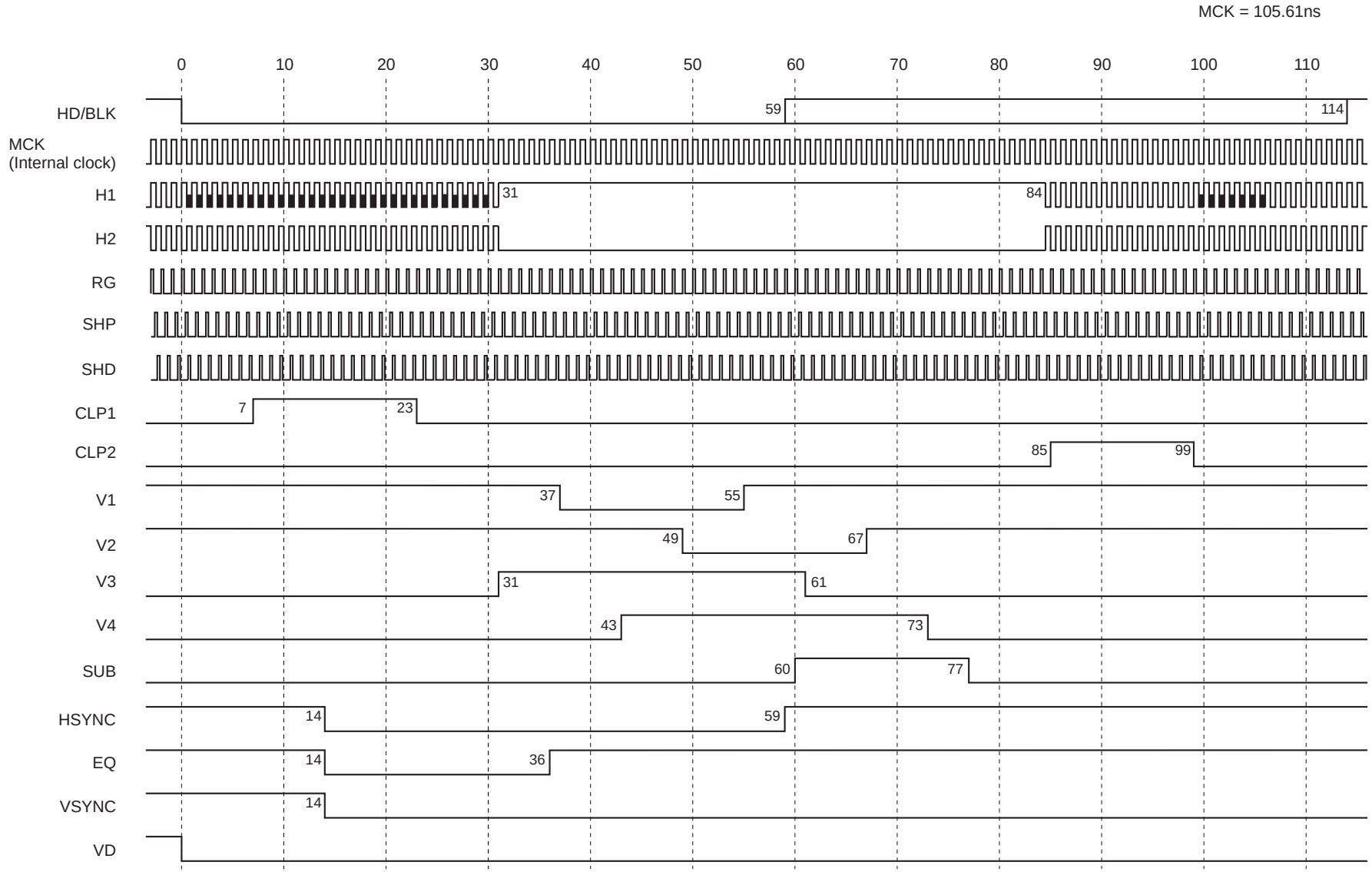
Timing Generator + Sync Generator Block Timing Chart

Horizontal Direction EIA (during 510H CCD drive)



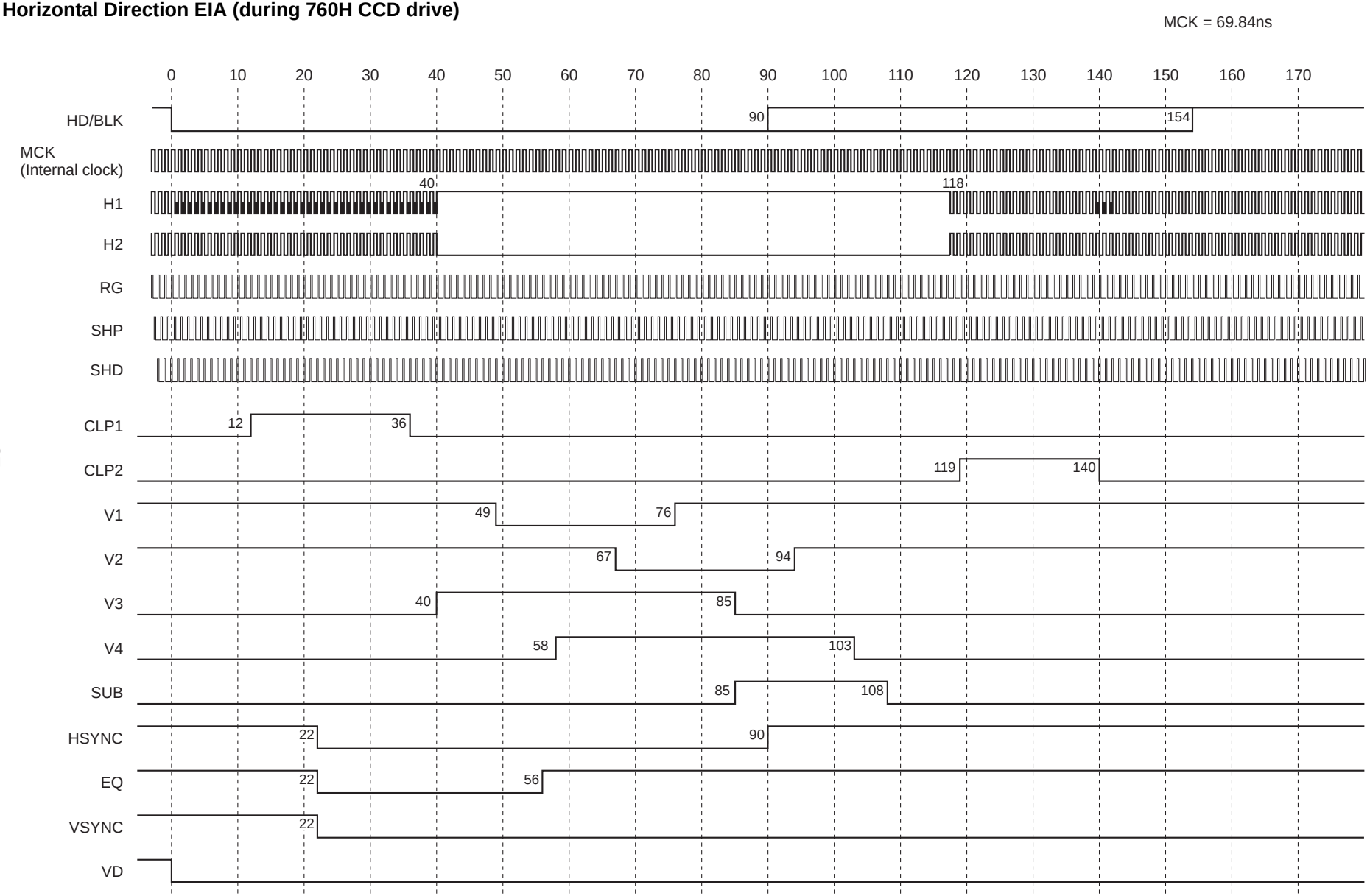
Timing Generator + Sync Generator Block Timing Chart

Horizontal Direction CCIR (during 510H CCD drive)



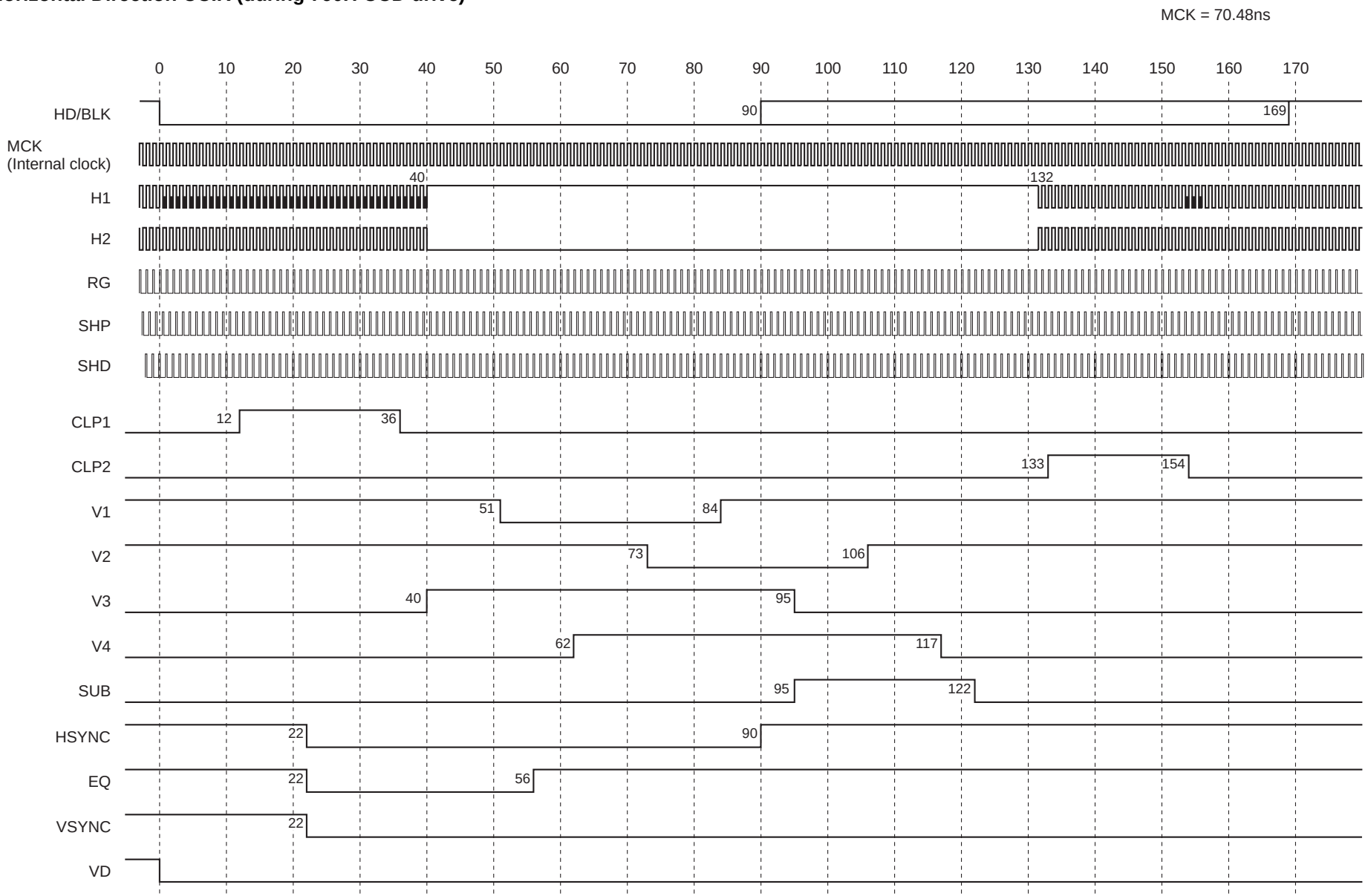
Timing Generator + Sync Generator Block Timing Chart

Horizontal Direction EIA (during 760H CCD drive)



Timing Generator + Sync Generator Block Timing Chart

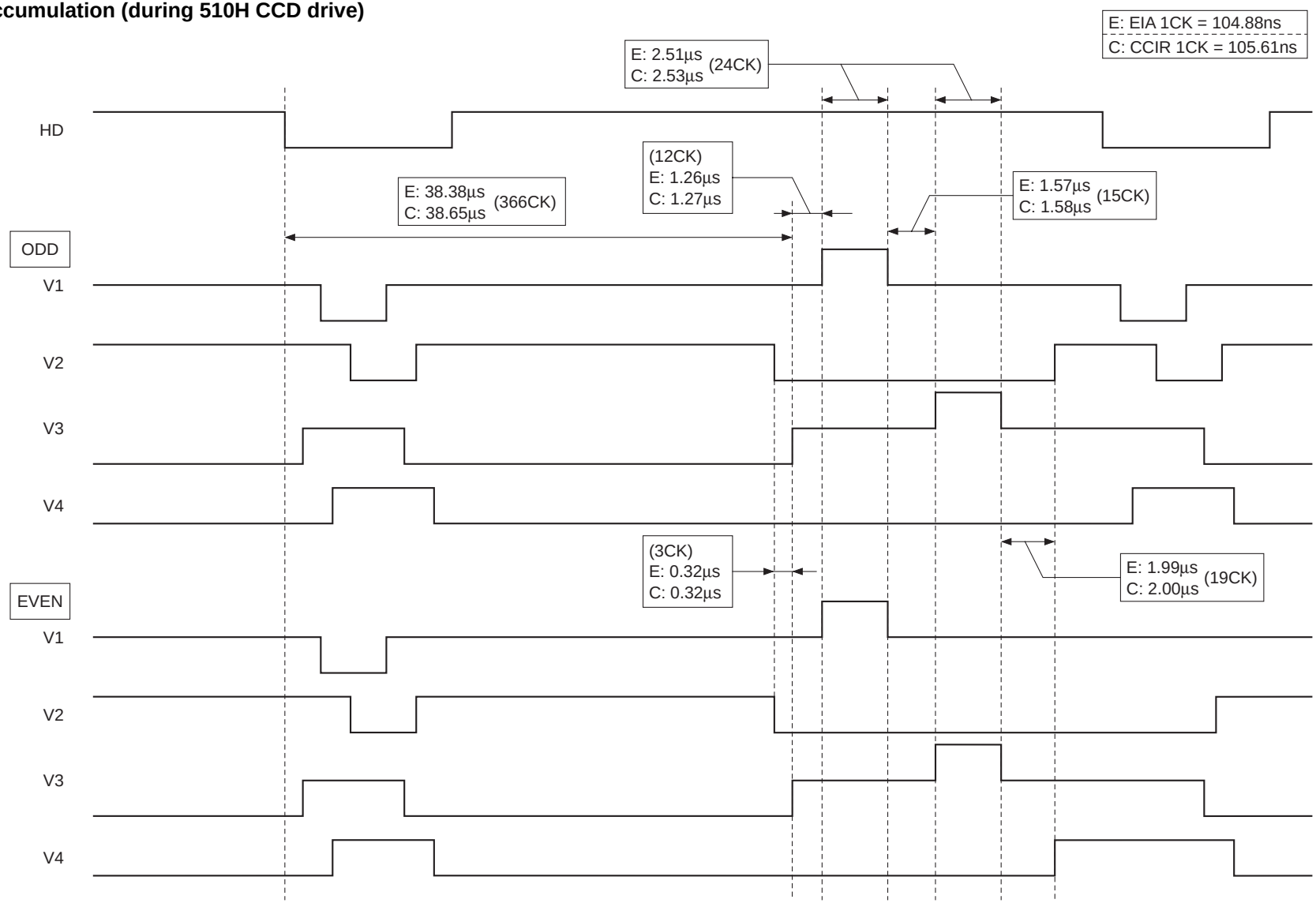
Horizontal Direction CCIR (during 760H CCD drive)



Timing Generator + Sync Generator Block Timing Chart

Charge Readout Timing

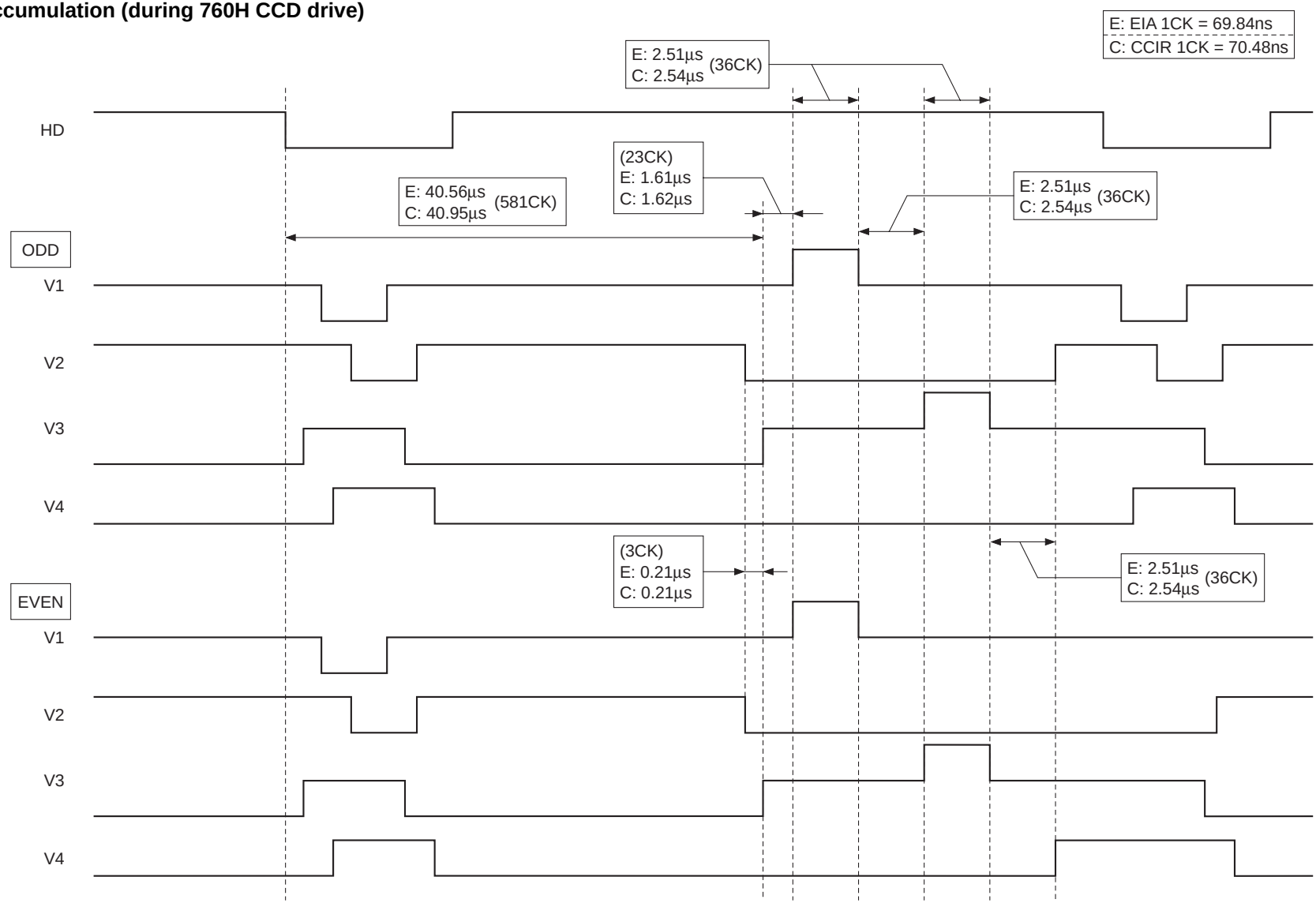
Field Accumulation (during 510H CCD drive)



Timing Generator + Sync Generator Block Timing Chart

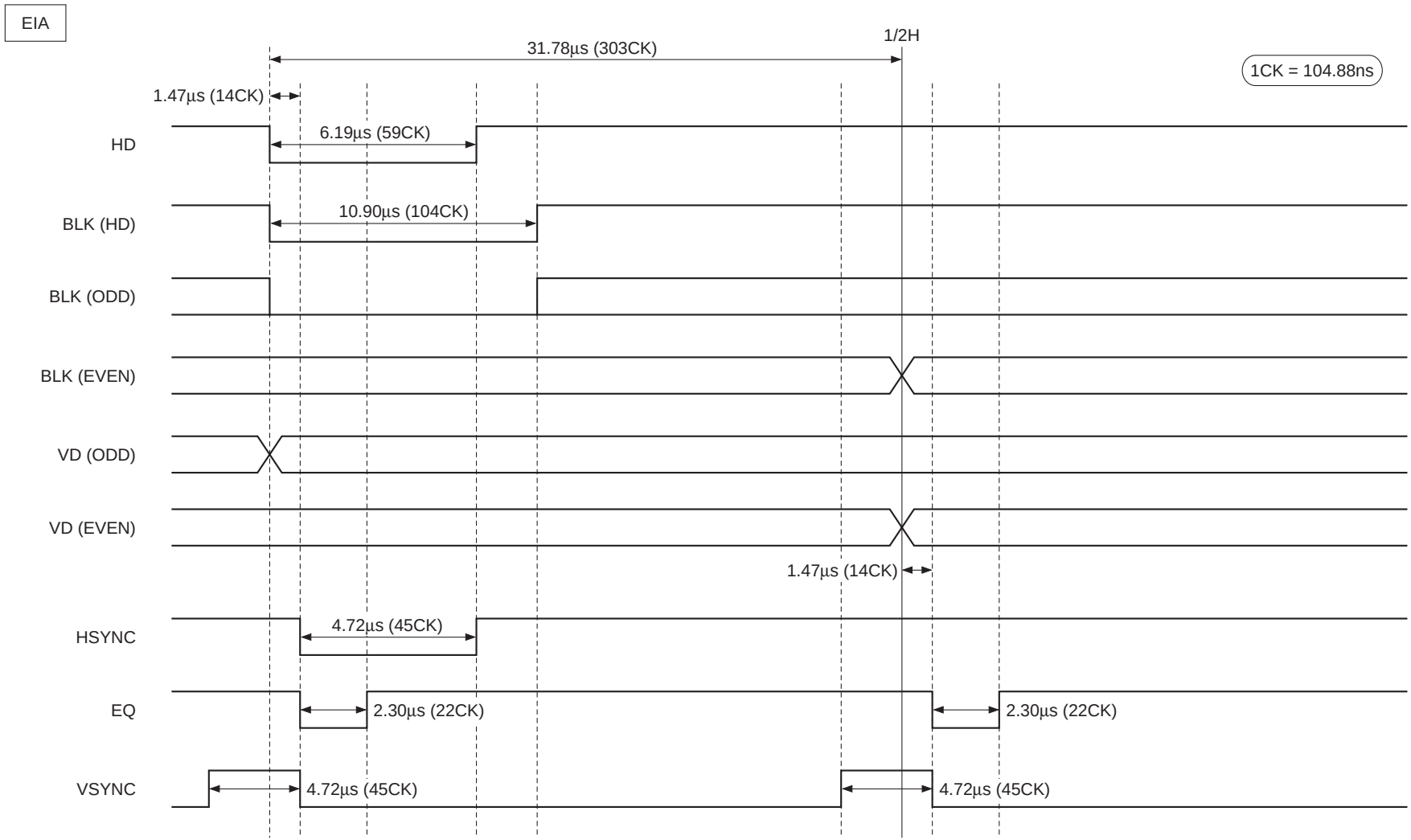
Charge Readout Timing

Field Accumulation (during 760H CCD drive)



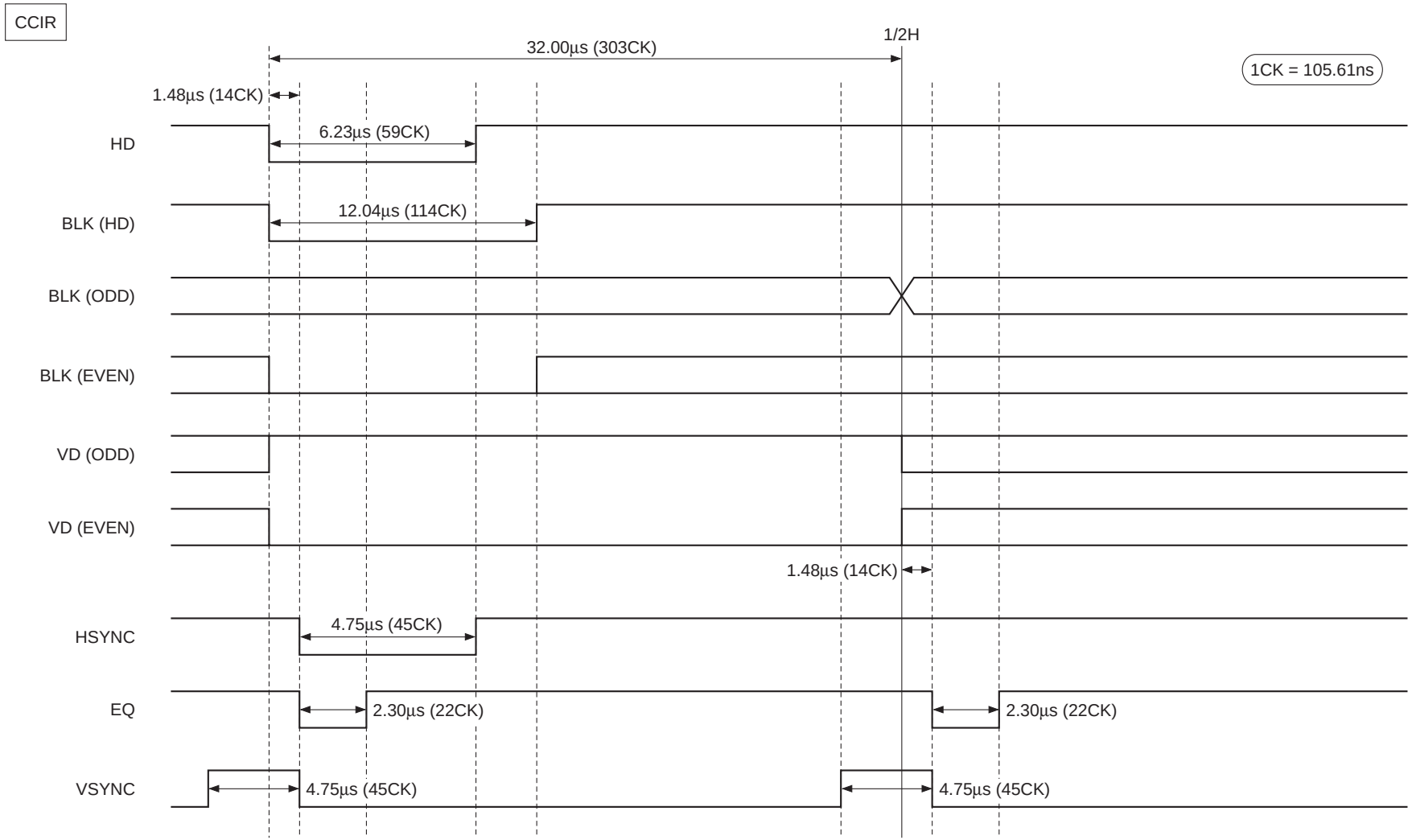
Timing Generator + Sync Generator Block Timing Chart

Effective Horizontal Period (during 510H CCD drive)



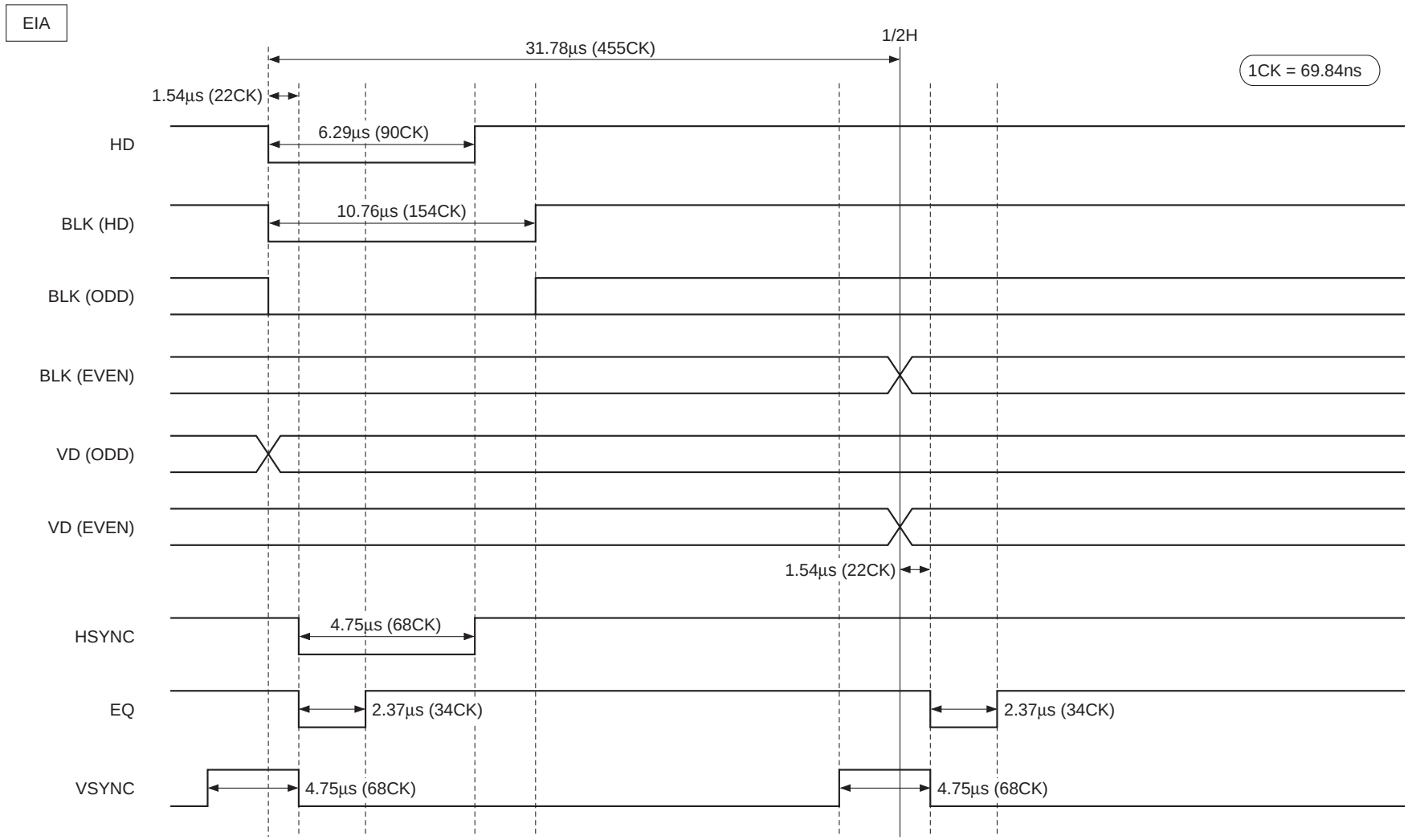
Timing Generator + Sync Generator Block Timing Chart

Effective Horizontal Period (during 510H CCD drive)



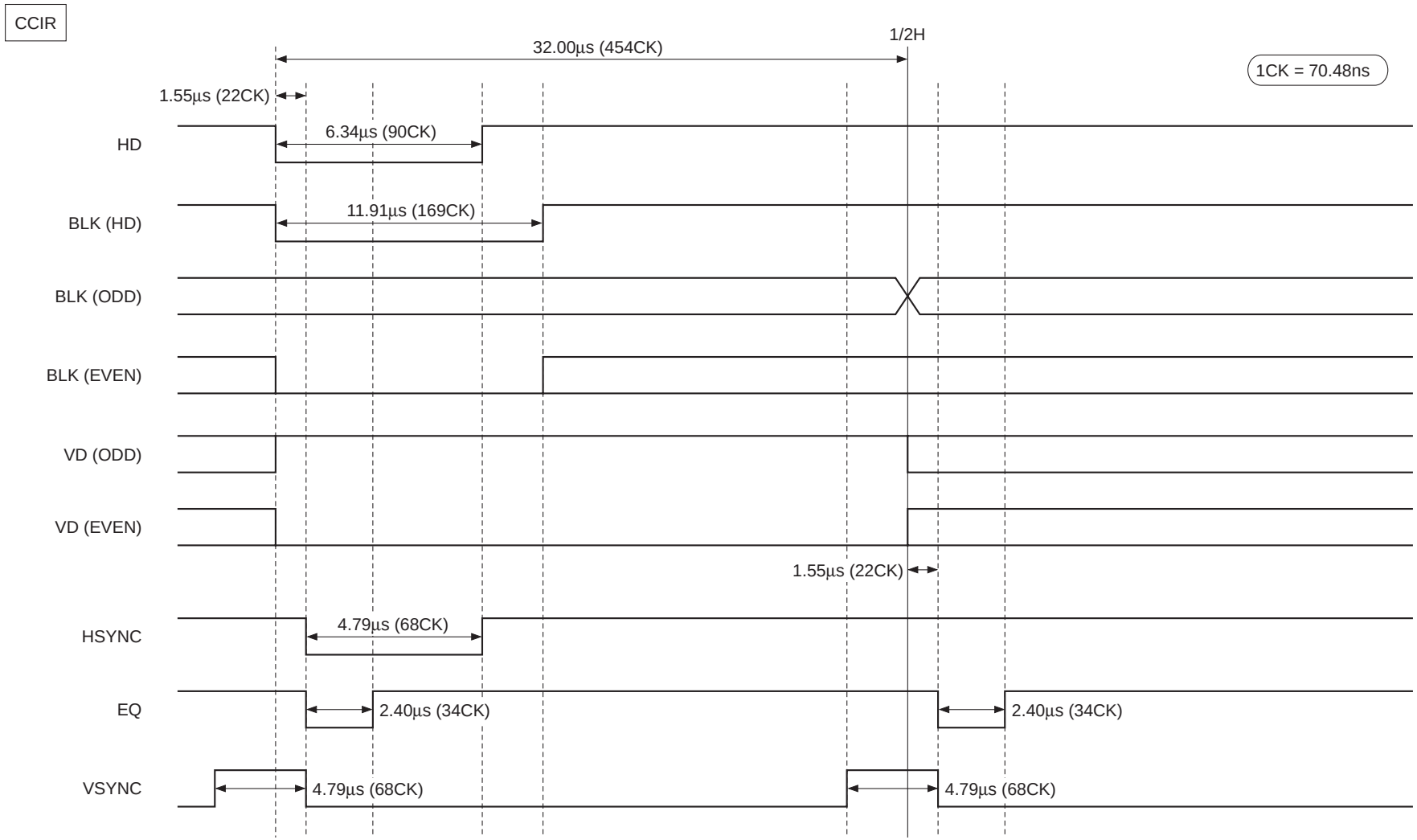
Timing Generator + Sync Generator Block Timing Chart

Effective Horizontal Period (during 760H CCD drive)

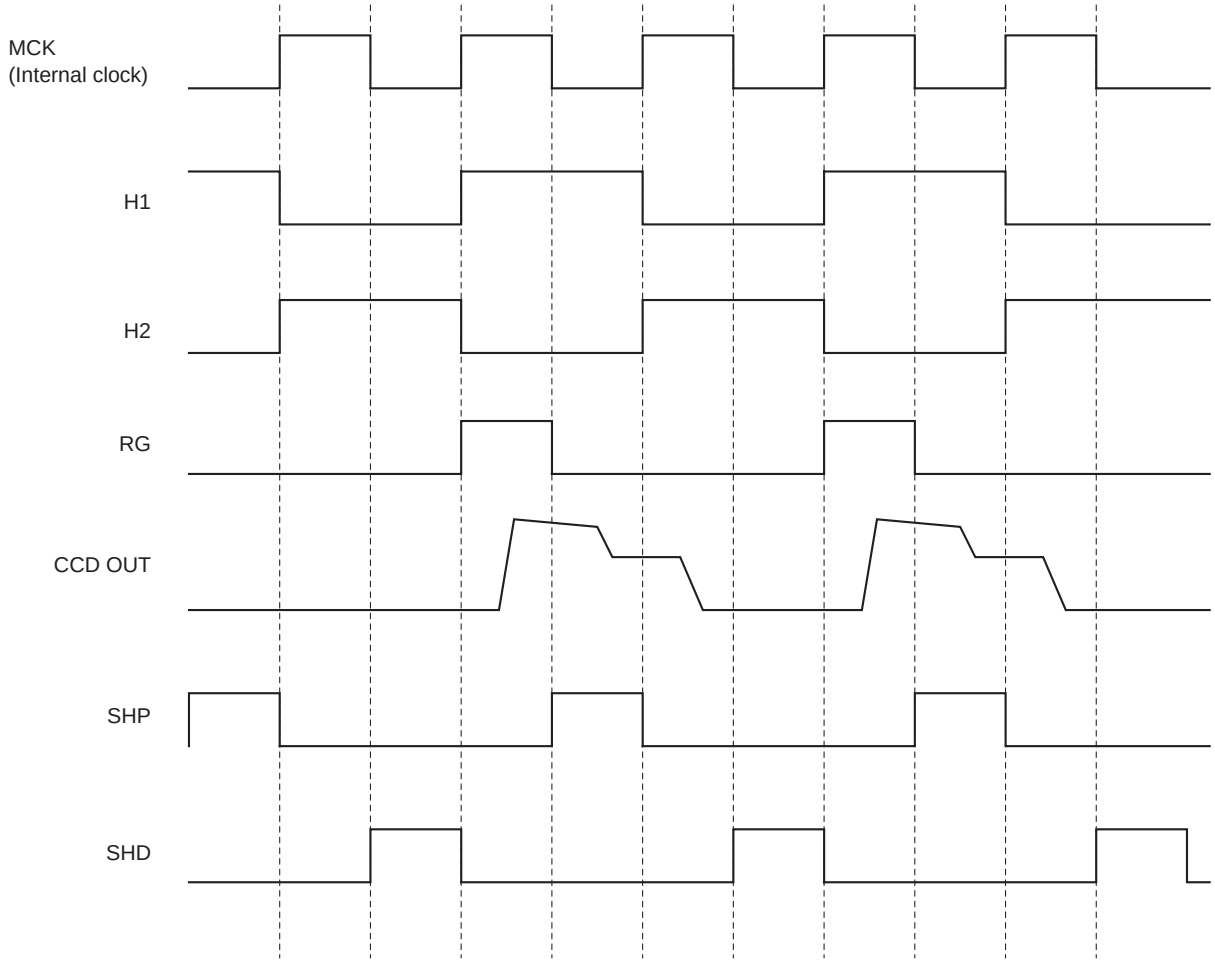


Timing Generator + Sync Generator Block Timing Chart

Effective Horizontal Period (during 760H CCD drive)

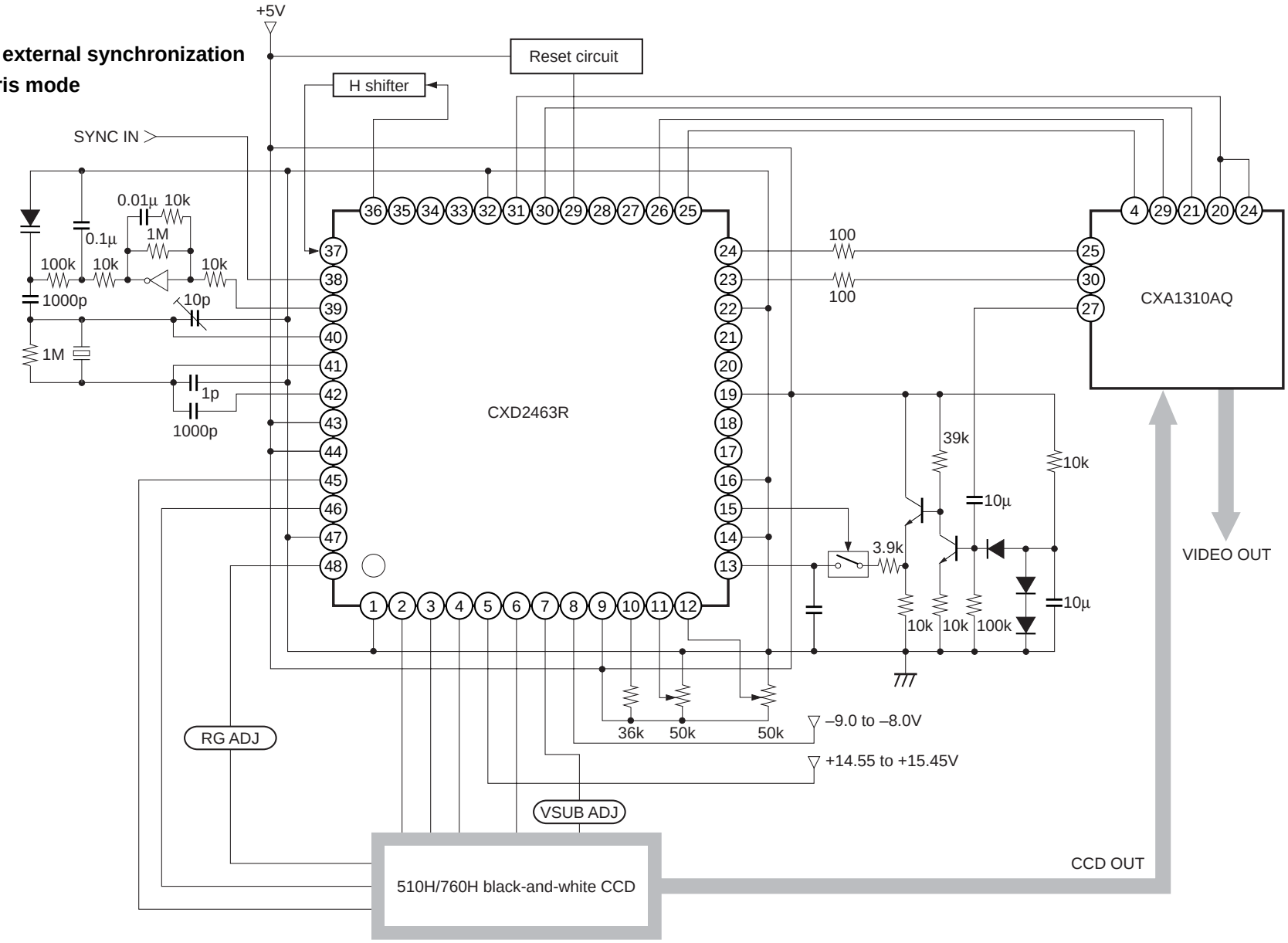


High-Speed Phase Timing Chart for the Timing Generator Block



Application Circuit

- **SYNC input external synchronization**
- **Electronic iris mode**

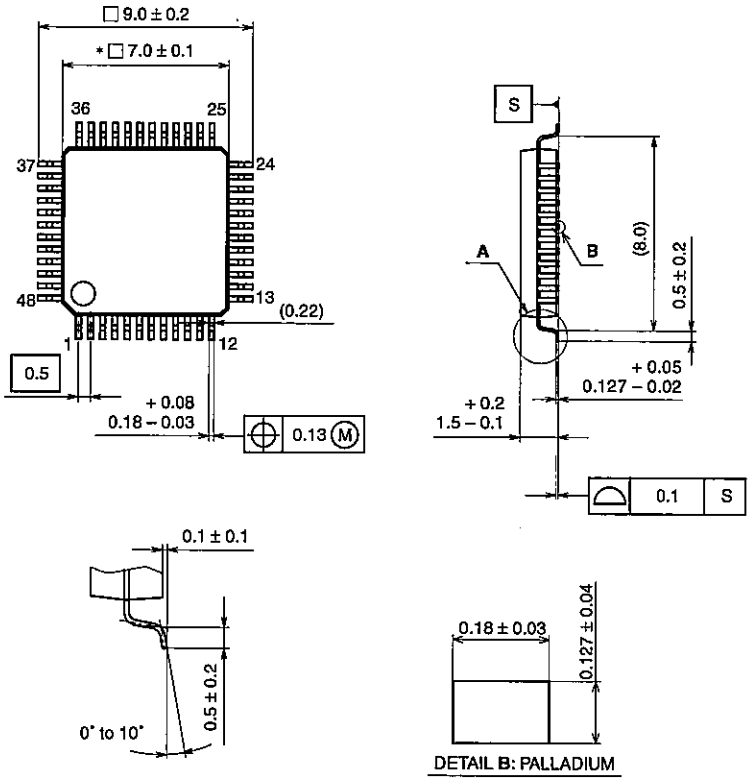


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

SCK Kagoshima Ass'y

48PIN LQFP (PLASTIC)



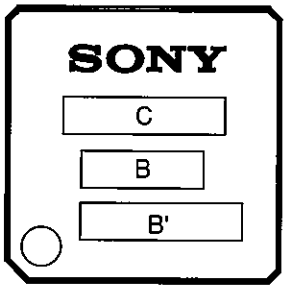
NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	P-LQFP48-7x7-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g

Marking



C:D2463R

B: Lot No. (Max. 3)

□□□

製造週 (Week manufactured)

製造年 (西暦下1桁)
(Year manufactured)

B': Lot No. (Max. 4)

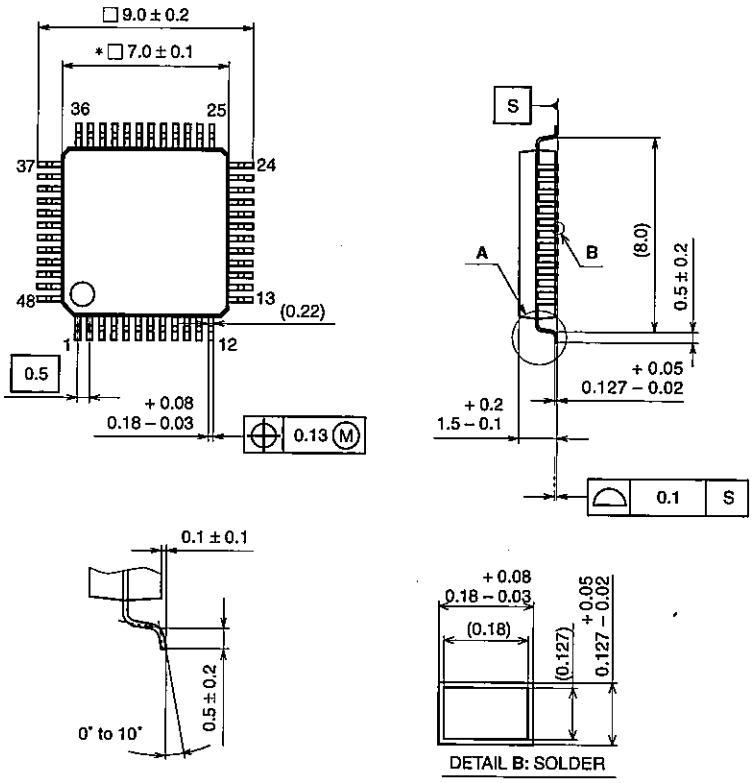
□□□□

管理記号 (Control No.)

Package Outline Unit: mm

SDT Ass'y

48PIN LQFP (PLASTIC)



DETAIL A

DETAIL B: SOLDER

NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	P-LQFP48-7x7-0.5
JEDEC CODE	————

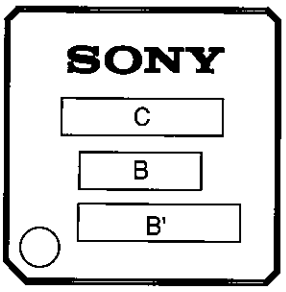
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm

Marking



C:D2463R

B: Lot No. (Max. 3)

□□□

製造週 (Week manufactured)

製造年 (西暦下1桁)
(Year manufactured)

B': Lot No. (Max. 4)

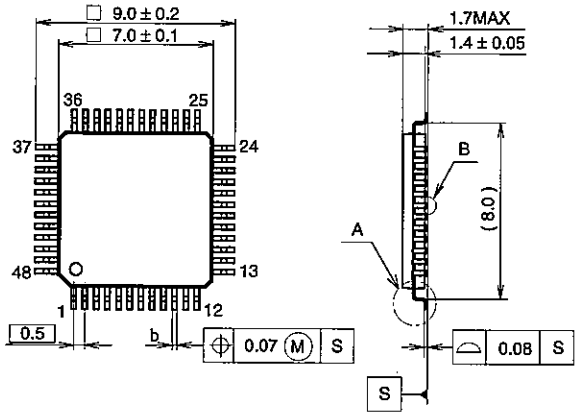
□□□□

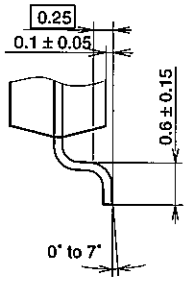
管理記号 (Control No.)

Package Outline Unit: mm

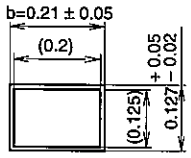
Amkor Ass'y

48PIN LQFP (PLASTIC)





DETAIL A



DETAIL B

SONY CODE	LQFP-48P-L282
EIAJ CODE	P-LQFP48-7X7-0.5
JEDEC CODE	———

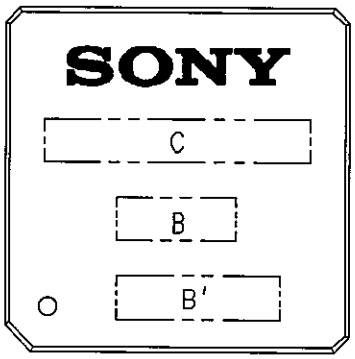
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18μm

Marking



MARKING C: D2463R

注1) C部は製品名(Max7文字)を配置する。
(7文字を超える場合は製品名省略標示規定に従う。)
2) B, B' 部はロット番号(Max7文字)を配置する。
(但し B部Max3文字, B' 部Max4文字とする。)

< INSTRUCTIONS >
1) TYPE NO. (MAX 7 CHARACTERS) IN SECTION C.
(FOR MORE THAN 7 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
2) LOT NO. (MAX 7 CHARACTERS) IN SECTION B, B'.
(B: 3 CHARACTERS , B': 4 CHARACTERS.)