SONY

Intelligent Panel Controller Pro for Standard Frame System

CXD4732R

1. Description

The CXD4732R performs picture quality enhancement signal processing for post-scaling full-HD and WXGA progressive scan signals. This IC can achieve high-end picture quality easily, and provides even further added value in end products.

The CXD4732R has high-performance MC-3DNR functions, Super resolution functions, dynamic contrast functions, and color representation improvement functions.

The device is provided a 128-pin LQFP package. Neither external DRAM nor any special firmware is required.

(Applications: LCD TV, Panel Module)

2. Features

- ◆ High performance video processing
  - ◆ 3D noise reduction combined with motion compensation(MC-3DNR)
  - ◆ MPEG-NR, especially effective for mosquito noise, block noise
  - ◆ Gradation creation
  - ◆ Super Resolution
  - ◆ Screen division contrast enhancement
  - ◆ Chromaticity diagram based color conversion
  - ◆ 2D Sharpness
  - ◆ Basic user controls : static contrast, color saturation, brightness
  - ◆ Digital Gamma Function with two selectable 12bit GBR independent LUT
  - ◆ Dither Function for 8bit panel system
- ◆ IC Interface
  - ◆ LVDS receiver and transmitter which support single/dual links 8bit GBR or 10bit GBR
  - ◆ Tolerates Spread Spectrum clock at the LVDS input
  - ◆ SSCG (Spread Spectrum Clock Generator) for LVDS Tx clock
  - ◆ Support display resolutions WXGA(1366x768p) or Full-HD(1920x1080p)
  - ◆ Support I2C Slave Interface for external host CPU (100kHz~400kHz)
  - ◆ Support I2C Master Interface for stand-alone startup with 64kbit or 128kbit external EEPROM (optional)

E12108

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3. Package

QFP 128pin (0.5mm pin pitch, body size 20mm × 14mm)

4. Structure

Silicon gate CMOS IC

5. Block Diagram

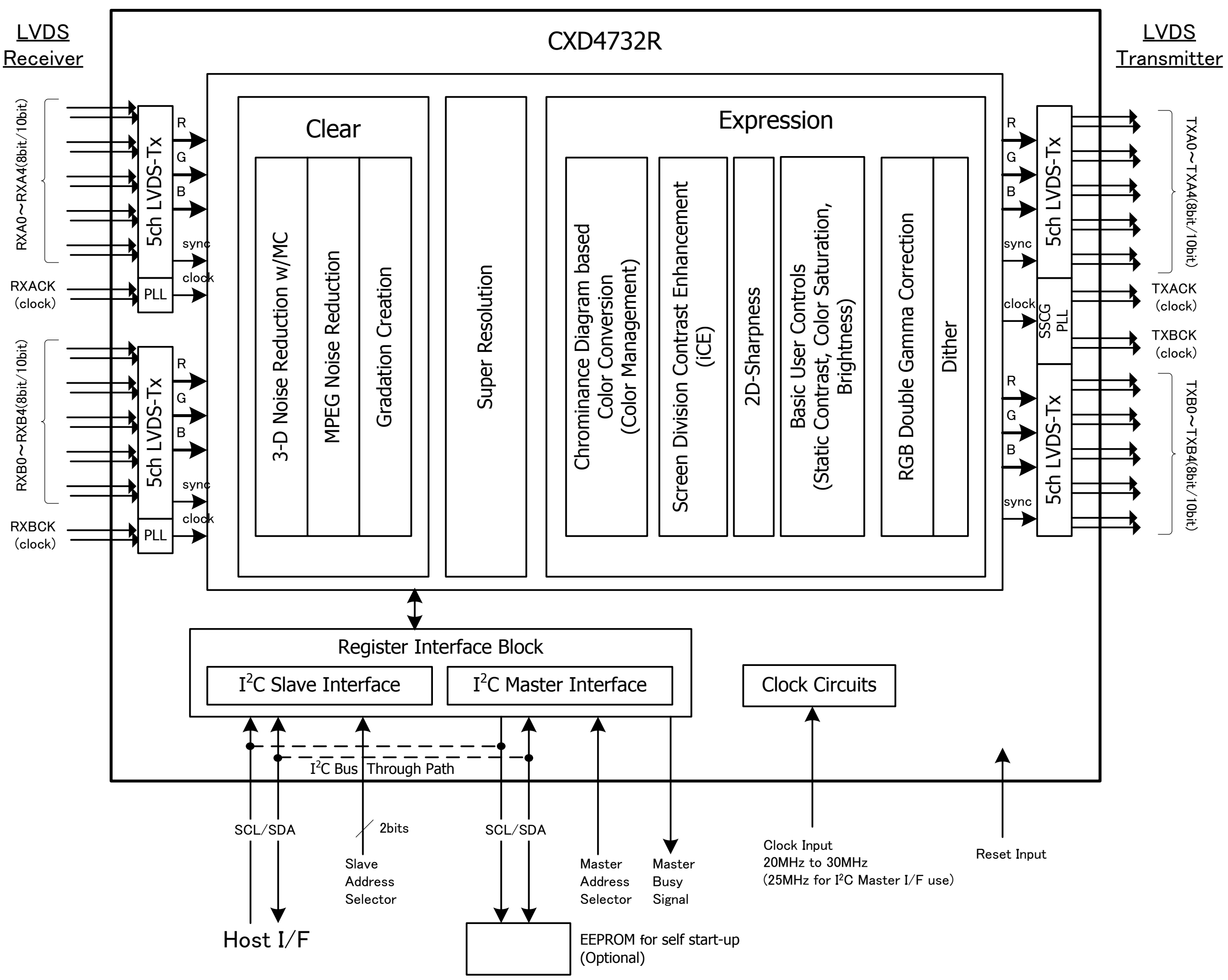
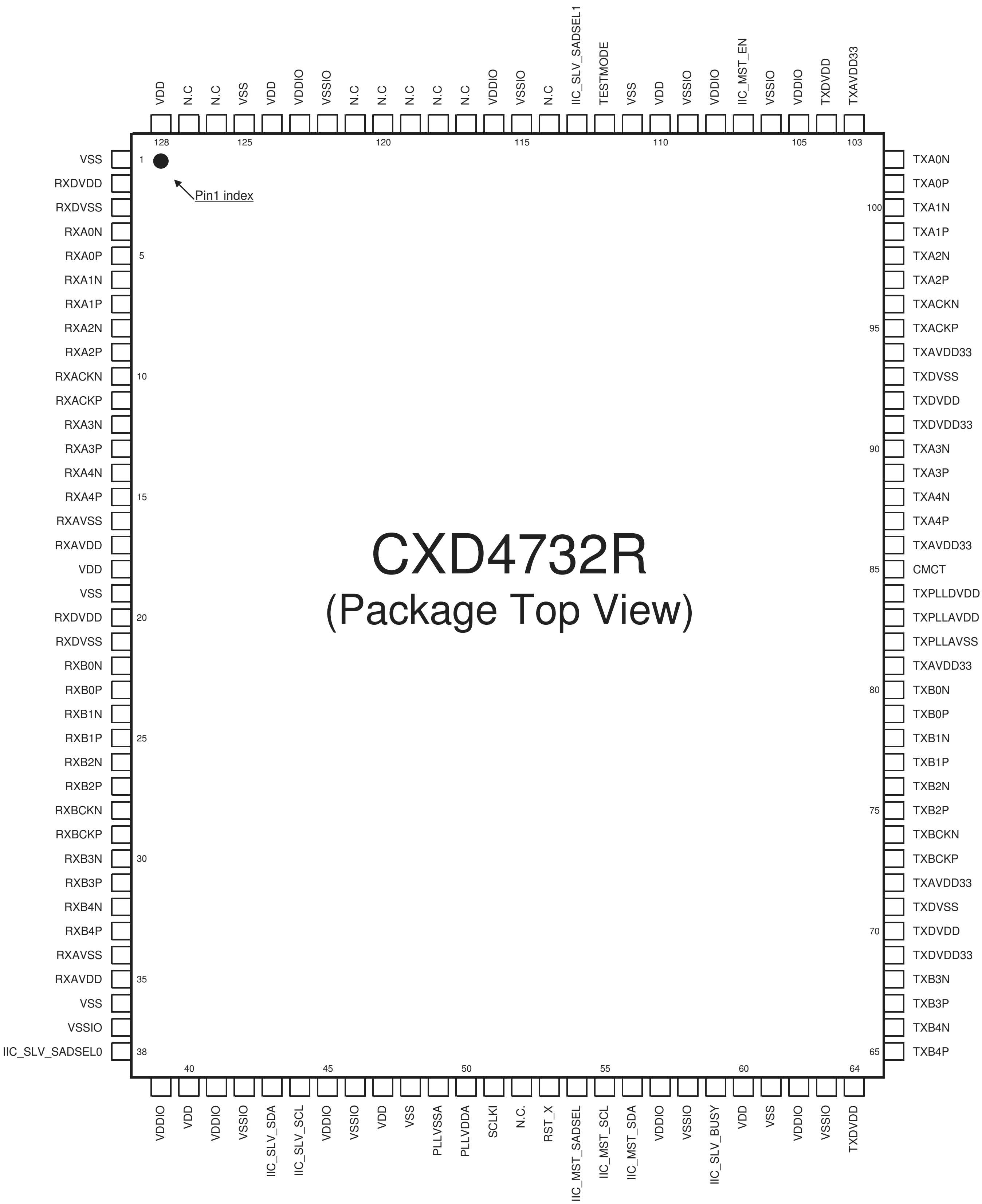


Figure 5.1 CXD4732R Block Diagram

6. Pin Configuration



Note) Exposed Pad must be connected to GND and soldered to PCB.

Figure 6.1 CXD4732R Pin Configuration

7. Pin Description

Pin #	Pin Name	Type	Pin Descriptions	Condition at Hard Reset	Note
4	RXA0N	LVDS IN	LVDS receiver data input, Link A, Channel 0 (-)		(1)
5	RXA0P	LVDS IN	LVDS receiver data input, Link A, Channel 0 (+)		(1)
6	RXA1N	LVDS IN	LVDS receiver data input, Link A, Channel 1 (-)		(1)
7	RXA1P	LVDS IN	LVDS receiver data input, Link A, Channel 1 (+)		(1)
8	RXA2N	LVDS IN	LVDS receiver data input, Link A, Channel 2 (-)		(1)
9	RXA2P	LVDS IN	LVDS receiver data input, Link A, Channel 2 (+)		(1)
10	RXACKN	LVDS IN	LVDS receiver clock input for Link A (-)		(1)
11	RXACKP	LVDS IN	LVDS receiver clock input for Link A (+)		(1)
12	RXA3N	LVDS IN	LVDS receiver data input, Link A, Channel 3 (-)		(1)
13	RXA3P	LVDS IN	LVDS receiver data input, Link A, Channel 3 (+)		(1)
14	RXA4N	LVDS IN	LVDS receiver data input, Link A, Channel 4 (-) In 8bit input mode, this pin is disabled.		(1)
15	RXA4P	LVDS IN	LVDS receiver data input, Link A, Channel 4 (+) In 8bit input mode, this pin is disabled.		(1)
22	RXB0N	LVDS IN	LVDS receiver data input, Link B, Channel 0 (-)		(1)
23	RXB0P	LVDS IN	LVDS receiver data input, Link B, Channel 0 (+)		(1)
24	RXB1N	LVDS IN	LVDS receiver data input, Link B, Channel 1 (-)		(1)
25	RXB1P	LVDS IN	LVDS receiver data input, Link B, Channel 1 (+)		(1)
26	RXB2N	LVDS IN	LVDS receiver data input, Link B, Channel 2 (-)		(1)
27	RXB2P	LVDS IN	LVDS receiver data input, Link B, Channel 2 (+)		(1)
28	RXBCKN	LVDS IN	LVDS receiver clock input for Link B (-)		(1)
29	RXBCKP	LVDS IN	LVDS receiver clock input for Link B (+)		(1)
30	RXB3N	LVDS IN	LVDS receiver data input, Link B, Channel 3 (-)		(1)
31	RXB3P	LVDS IN	LVDS receiver data input, Link B, Channel 3 (+)		(1)
32	RXB4N	LVDS IN	LVDS receiver data input, Link B, Channel 4 (-) In 8bit input mode, this pin is disabled.		(1)
33	RXB4P	LVDS IN	LVDS receiver data input, Link B, Channel 4 (+) In 8bit input mode, this pin is disabled.		(1)
102	TXA0N	LVDS OUT	LVDS transmitter data output, Link A, Channel 0 (-)	Uncertain value (high or low)	(2)
101	TXA0P	LVDS OUT	LVDS transmitter data output, Link A, Channel 0 (+)	Uncertain value (high or low)	(2)
100	TXA1N	LVDS OUT	LVDS transmitter data output, Link A, Channel 1 (-)	Uncertain value (high or low)	(2)
99	TXA1P	LVDS OUT	LVDS transmitter data output, Link A, Channel 1 (+)	Uncertain value (high or low)	(2)
98	TXA2N	LVDS OUT	LVDS transmitter data output, Link A, Channel 2 (-)	Uncertain value (high or low)	(2)
97	TXA2P	LVDS OUT	LVDS transmitter data output, Link A, Channel 2 (+)	Uncertain value (high or low)	(2)

Pin #	Pin Name	Type	Pin Descriptions	Condition at Hard Reset	Note
96	TXACKN	LVDS OUT	LVDS transmitter clock output for Link A (-)	Uncertain value (high or low)	(2)
95	TXACKP	LVDS OUT	LVDS transmitter clock output for Link A (+)	Uncertain value (high or low)	(2)
90	TXA3N	LVDS OUT	LVDS transmitter data output, Link A, Channel 3 (-)	Uncertain value (high or low)	(2)
89	TXA3P	LVDS OUT	LVDS transmitter data output, Link A, Channel 3 (+)	Uncertain value (high or low)	(2)
88	TXA4N	LVDS OUT	LVDS transmitter data output, Link A, Channel 4 (-) In 8bit output mode, this pin is disabled.	Uncertain value (high or low)	(2)
87	TXA4P	LVDS OUT	LVDS transmitter data output, Link A, Channel 4 (+) In 8bit output mode, this pin is disabled.	Uncertain value (high or low)	(2)
80	TXB0N	LVDS OUT	LVDS transmitter data output, Link B, Channel 0 (-)	Uncertain value (high or low)	(2)
79	TXB0P	LVDS OUT	LVDS transmitter data output, Link B, Channel 0 (+)	Uncertain value (high or low)	(2)
78	TXB1N	LVDS OUT	LVDS transmitter data output, Link B, Channel 1 (-)	Uncertain value (high or low)	(2)
77	TXB1P	LVDS OUT	LVDS transmitter data output, Link B, Channel 1 (+)	Uncertain value (high or low)	(2)
76	TXB2N	LVDS OUT	LVDS transmitter data output, Link B, Channel 2 (-)	Uncertain value (high or low)	(2)
75	TXB2P	LVDS OUT	LVDS transmitter data output, Link B, Channel 2 (+)	Uncertain value (high or low)	(2)
74	TXBCKN	LVDS OUT	LVDS transmitter clock output for Link B (-)	Uncertain value (high or low)	(2)
73	TXBCKP	LVDS OUT	LVDS transmitter clock output for Link B (+)	Uncertain value (high or low)	(2)
68	TXB3N	LVDS OUT	LVDS transmitter data output, Link B, Channel 3 (-)	Uncertain value (high or low)	(2)
67	TXB3P	LVDS OUT	LVDS transmitter data output, Link B, Channel 3 (+)	Uncertain value (high or low)	(2)
66	TXB4N	LVDS OUT	LVDS transmitter data output, Link B, Channel 4 (-) In 8bit output mode, this pin is disabled.	Uncertain value (high or low)	(2)
65	TXB4P	LVDS OUT	LVDS transmitter data output, Link B, Channel 4 (+) In 8bit output mode, this pin is disabled.	Uncertain value (high or low)	(2)
51	SCLKI	3.3V IN	System clock input.		
52	N.C.	3.3V OUT	Do not Connect this terminal.		
53	RST_X	3.3V IN	System Reset input. This signal is active low.		(3)
38	IIC_SLV_SADSEL0	3.3V IN	I^2C address selector bit 0 for I^2C slave interface		
113	IIC_SLV_SADSEL1	3.3V IN	I^2C address selector bit 1 for I^2C slave interface		
43	IIC_SLV_SDA	Open Drain	I^2C data signal for I^2C slave interface		(4)
44	IIC_SLV_SCL	Open Drain	I^2C clock signal for I^2C slave interface		(4)
54	IIC_MST_SADSEL	3.3V IN	I^2C address selector for I^2C master interface		
55	IIC_MST_SCL	Open Drain	I^2C data signal for I^2C master interface. If external EEPROM is not used (IIC_MST_EN = Low), connect this pin to the GND.		(4)
56	IIC_MST_SDA	Open Drain	I^2C clock signal for I^2C master interface. If external EEPROM is not used (IIC_MST_EN = Low), connect this pin to the GND.		(4)

Pin #	Pin Name	Type	Pin Descriptions	Condition at Hard Reset	Note
59	IIC_SLV_BUSY	3.3V OUT	I^2C slave interface busy signal output. High: busy	Low	(5)
107	IIC_MST_EN	3.3V IN	I^2C master interface enable, High: enable, Low: disable		
112	TESTMODE	3.3V IN	**Always Connect this terminal to digital ground (VSSIO).**		
114	N.C		Do not Connect this terminal.		
117					
118					
119					
120					
121					
126					
127					
17	RXAVDD	3.3V POWER	Analog power (3.3V) for LVDS receiver		
35					
16	RXAVSS	GND	Ground for LVDS receiver		
34					
2	RXDVDD	1.2V POWER	Digital power (1.2V) for LVDS receiver		
20					
3	RXDVSS	GND	Ground for LVDS receiver		
21					
72	TXAVDD33	3.3V POWER	Analog power (3.3V) for LVDS transmitter		
81					
86					
94					
103					
83	TXPLLAVDD	1.2V POWER	PLL analog power (1.2V) for LVDS transmitter		
82	TXPLLAVSS	GND	PLL ground for LVDS transmitter		
84	TXPLLDVDD	1.2V POWER	PLL digital power (1.2V) for LVDS transmitter		
85	CMCT	Analog IN	Connect external Capacitance (>0.1uF) to this terminal and GND		
64	TXDVDD	1.2V POWER	Digital power (1.2V) for LVDS transmitter		
70					
92					
104					
69	TXDVDD33	3.3V POWER	Digital power (3.3V) for LVDS transmitter		
91					

Pin #	Pin Name	Type	Pin Descriptions	Condition at Hard Reset	Note
71	TXDVSS	GND	Ground for LVDS transmitter		
93					
50	PLLVDDA	1.2V POWER	PLL analog power (1.2V) for core circuits		
49	PLLVSSA	Analog IN	See the **12. Example Application Circuit.** Do not connect this terminal to PCB GND.		
18	VDD	1.2V POWER	Digital power (1.2V) for core circuit		
40					
47					
60					
110					
124					
128					
1	VSS	GND	Ground for core circuit		
19					
36					
48					
61					
111					
125					
39	VDDIO	3.3V POWER	Digital power (3.3V) for I/O		
41					
45					
57					
62					
105					
108					
116					
123					
37	VSSIO	GND	Ground for I/O		
42					
46					
58					
63					
106					
109					
115					
122					

Pin #	Pin Name	Type	Pin Descriptions	Condition at Hard Reset	Note
-	Exposed Pad	GND	Ground for LVDS transmitter		(6)

Note)

(1) Unused pins must be fixed to high (3.3V) or OPEN for LVDS Rx.
(2) Unused pins must be OPEN for LVDS Tx.
(3) Active low reset is required after turn on.
(4) External pull-up registers are required.
(5) At the releasing RST_X, if the terminal “IIC_MST_EN” is high, this terminal “IIC_SLV_BUSY” becomes high till an I^2C Master Reading Operation is completed.
(6) Exposed Pad must be connected to GND and soldered to PCB.

8. Electrical Characteristics

8.1. Absolute Maximum Ratings

Item		Symbol	Min.	Max.	Unit
Power Supply Voltage	Digital I/O	VDDIO	-0.5	+4.6	V
	LVDS Rx, Tx I/O	RXAVDD, TXAVDD33, TXDVDD33	-0.5	+4.6	V
	Core Logic	VDD	-0.5	+1.6	V
	LVDS Rx, Tx Logic	RXDVDD, TXDVDD	-0.5	+1.6	V
	PLL	PLLVDDA, TXPLLAVDD, TXPLLDVDD	-0.5	+1.6	V
Operating Junction Temperature		Tj	-10	+115	℃

8.2. Recommended Operating Conditions

Item		Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	3.3V Digital I/O	VDDIO	3.0	3.3	3.6	V
	I^2C Bus DC supply voltage for output pull-up termination	$V_{I2C\text{-}BUS}$	3.0	3.3	5.0	V
	LVDS Rx, Tx I/O	RXAVDD, TXAVDD33, TXDVDD33	3.0	3.3	3.6	V
	Core Logic	VDD	1.1	1.2	1.3	V
	LVDS Rx Logic	RXDVDD	1.1	1.2	1.3	V
	LVDS Tx Logic	TXDVDD	*1)1.1	1.2	1.3	V
	PLL	PLLVDDA, TXPLLAVDD, TXPLLDVDD	1.1	1.2	1.3	V
Operating Ambient Temperature		Ta	0		75	℃

***1) If you use SSCG （*LVTX_SSEN* =1 ）, this value is 1.15V.**

8.3. DC characteristics

8.3.1. Digital In/Out Terminal

(VDDIO = 3.3V+/-0.3V)

Item	Symbol	Applicable pins / Condition	Min.	Typ.	Max.	Unit
Digital Input High Voltage	V_{IH}	*1), 2)	2		3.6	V
Digital Input High Voltage(I^2C pin)	V_{IH-I2C}	*3)	0.7* $V_{I2C-BUS}$	$V_{I2C-BUS}$	$V_{I2C-BUS}$	V
Digital Input Low Voltage	V_{IL}	*1), 2)	-0.3		0.8	V
Digital Input Low Voltage(I^2C pin)	V_{IL-I2C}	*3)	-0.3		0.3* $V_{I2C-BUS}$	
Digital Output High Voltage	V_{OH}	*4)	2.4			V
Digital Output High Voltage(I^2C pin)	V_{OH-I2C}	*3)	Output is not driven high by CXD4732R			
Digital Output Low Voltage	V_{OL}	*4)			0.4	V
Digital Output Low Voltage(I^2C pin)	V_{OL-I2C}	*3)			0.4	V
Operating current for 1.2V VDD	$I_{OP\_1.2}$	*5),LVDS Clock = 74.25MHz, Full-HD		700	800	mA
Operating current for 3.3V VDD	$I_{OP\_3.3}$	*6),LVDS Clock = 74.25MHz, Full-HD		200	220	mA

*1) SCLKI
*2) IIC_MST_EN, IIC_MST_SADSEL, IIC_SLV_SADSEL0, IIC_SLV_SADSEL1, RST_X
*3) IIC_MST_SDA, IIC_MST_SCL, IIC_SLV_SDA, IIC_SLV_SCL
*4) IIC_MST_SCL, IIC_SLV_BUSY
*5) 1.2V VDD includes RXDVDD, TXPLLAVDD, TXPLLDVDD, TXDVDD, PLLVDDA, VDD
*6) 3.3V VDD includes RXAVDD, TXAVDD33, TXDVDD33, VDDIO

8.3.2. LVDS Receiver

(RXAVDD = 3.3V+/-0.3V, RXDVDD = 1.2V+/-0.1V)

Item	Symbol	Applicable pins / Condition	Min.	Typ.	Max.	Unit
Differential Input High Threshold	V_{RXTH}	*1), *2) V_{CM} = 1.2V			100	mV
Differential Input Low Threshold	V_{RXTL}	*1), *2) V_{CM} = 1.2V	-100			mV
Input Voltage Range	V_{RXIN}	*1)	0		2.4	V

*1) RXB0N, RXB0P, RXB1N, RXB1P, RXB2N, RXB2P, RXBCKN, RXBCKP, RXB3N, RXB3P, RXB4N, RXB4P, RXA0N, RXA0P, RXA1N, RXA1P, RXA2N, RXA2P, RXACKN, RXACKP, RXA3N, RXA3P, RXA4N, RXA4P
*2) V_{CM} : LVDS Common Voltage

8.3.3. LVDS Transmitter

(TXAVDD33 = TXDVDD33 = 3.3V+/-0.3V, TXDVDD = 1.2V+/-0.1V)

Item	Symbol	Applicable pins / Condition	Min.	Typ.	Max.	Unit
Differential Output Voltage	V_{TXOD}	*1), *2) R_L = 100Ω, I_{LVDS} = 3.5mA,	280	350	420	mV
		*1), *2) R_L = 100Ω, I_{LVDS} = 2.5mA,	200	250	300	mV
Offset Voltage	V_{TXOS}	*1), *2) R_L = 100Ω	1.125	1.25	1.375	V

*1) TXA4P, TXA4N, TXA3P, TXA3N, TXACKP, TXACKN, TXA2P, TXA2N, TXA1P, TXA1N, TXA0P, TXA0N, TXB4P, TXB4N, TXB3P, TXB3N, TXBCKP, TXBCKN, TXB2P, TXB2N, TXB1P, TXB1N, TXB0P, TXB0N
*2) R_L: Load Condition, I_{LVDS}: LVDS Driver Current on LVDS Tx Bus

8.4. AC characteristics

8.4.1. System Clock and Reset Input

(VDDIO = 3.3V+/-0.3V)

Item	Symbol	Applicable pins / Condition	Min.	Typ.	Max.	Unit
System Clock Frequency	$1/T_{SYSCLK}$	SCLKI *1)	20	25	30	MHz
Duty Cycle		SCLKI	40	50	60	%
Reset Low Period	T_{RST}	RST_X	250			ns

*1) It is desirable to set frequency to 25MHz if the I²C master interface is enabled.

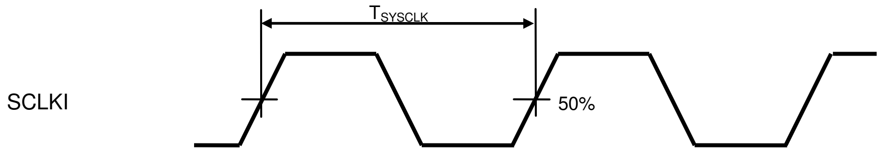


Figure 8.4.1.1 System Clock SCLKI Timing Definition

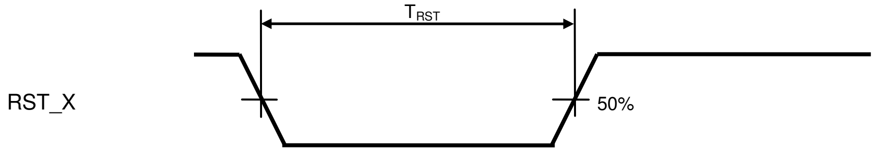


Figure 8.4.1.2 System Reset Input Waveform

8.4.2 I²C Slave Interface

(VDDIO = 3.3V+/-0.3V)

Item	Symbol	Applicable pins / Condition	Min.	Typ.	Max.	Unit
Input Clock Frequency	$1/T_{SLC}$	IIC_SLV_SCL			400	kHz
Clock Pulse Width High	T_{SLCHL}	IIC_SLV_SCL	600			ns
Clock Pulse Width Low	T_{SLCLL}	IIC_SLV_SCL	1300			ns
Data In Set Up Time	T_{SLDIS}	IIC_SLV_SDA	100			ns
Slave Data In Hold Time	T_{SLDIH}	IIC_SLV_SDA	0			ns
Start Condition Hold Time	T_{SLSTH}	IIC_SLV_SDA	600			ns
Stop Condition Set Up Time	T_{SLSPS}	IIC_SLV_SDA	600			ns
Time between Stop and Next Start	T_{SLSSH}	IIC_SLV_SDA	1300			ns
Data Out Hold Time	T_{SLDOH}	IIC_SLV_SDA	0		900	ns

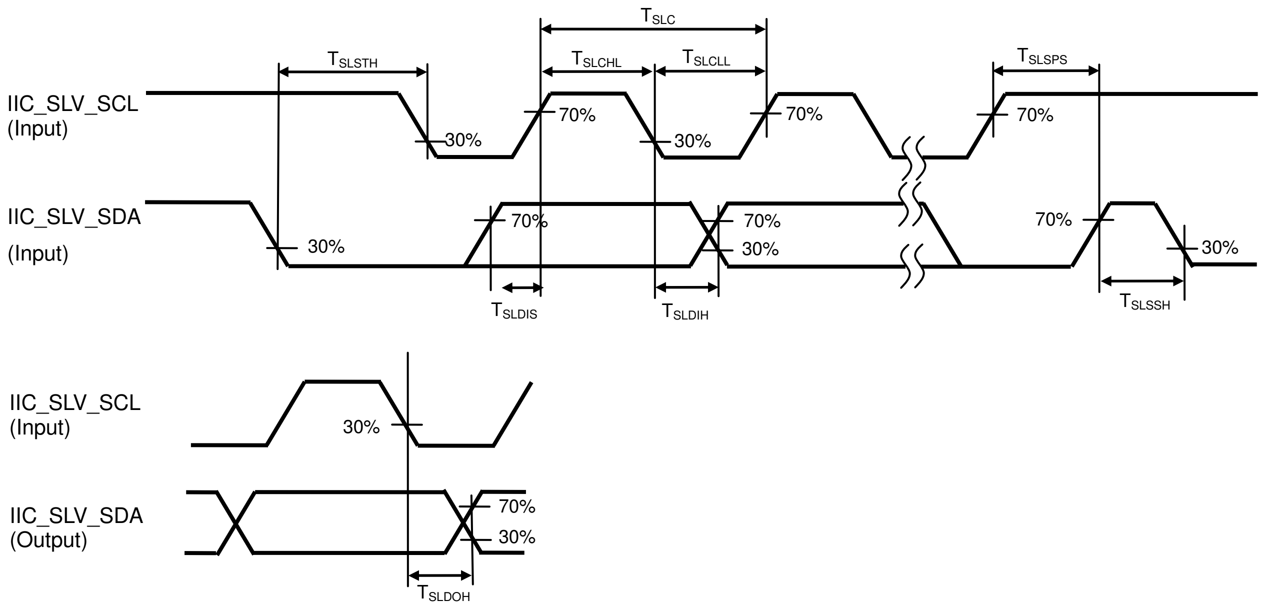


Figure 8.4.2 I²C Slave Interface Timing Definition

8.4.3. I²C Master Interface

(VDDIO = 3.3V+/-0.3V)

Item	Symbol	Applicable pins / Condition	Min.	Typ.	Max.	Unit
Output Clock Frequency	$1/T_{MAC}$	IIC_MST_SCL, *1)		391		kHz
Clock Pulse Width High	T_{MACHL}	IIC_MST_SCL	600			ns
Clock Pulse Width Low	T_{MACLL}	IIC_MST_SCL	1300			ns
Data Out Set Up Time	T_{MADOS}	IIC_MST_SDA	100			ns
Data Out Hold Time	T_{MADOH}	IIC_MST_SDA	0		900	ns
Start Condition Hold Time	T_{MASTH}	IIC_MST_SDA	600			ns
Stop Condition Set Up Time	T_{MASPS}	IIC_MST_SDA	600			ns
Time between Stop and Next Start	T_{MASSH}	IIC_MST_SDA	1300			ns
Data In Set Up Time	T_{MADIS}	IIC_MST_SDA	100			ns

*1) System Clock Frequency (SCLKI) = 25MHz.

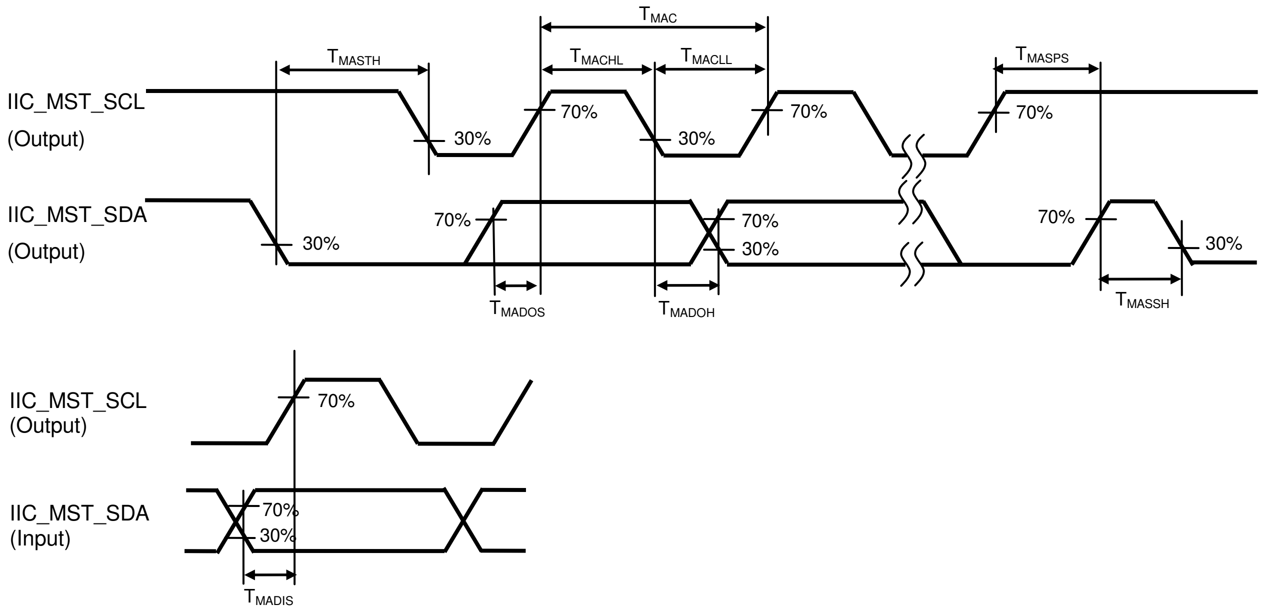


Figure 8.4.3 I²C Master Interface Timing Definition

8.4.4. LVDS Receiver

(RXAVDD = 3.3V+/-0.3V, RXDVDD = 1.2V+/-0.1V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Receiver Clock Period	T_{RCP}	*1)	14.70		11.77	ns
Input Data Position for Bit 1	T_{RIP1}	*2)	$- T_{RSKM}$	0	$+ T_{RSKM}$	ns
Input Data Position for Bit 0	T_{RIP0}	*2)	$(1/7)\ T_{RCP} - T_{RSKM}$	$(1/7)\ T_{RCP}$	$(1/7)\ T_{RCP} + T_{RSKM}$	ns
Input Data Position for Bit 6	T_{RIP6}	*2)	$(2/7)\ T_{RCP} - T_{RSKM}$	$(2/7)\ T_{RCP}$	$(2/7)\ T_{RCP} + T_{RSKM}$	ns
Input Data Position for Bit 5	T_{RIP5}	*2)	$(3/7)\ T_{RCP} - T_{RSKM}$	$(3/7)\ T_{RCP}$	$(3/7)\ T_{RCP} + T_{RSKM}$	ns
Input Data Position for Bit 4	T_{RIP4}	*2)	$(4/7)\ T_{RCP} - T_{RSKM}$	$(4/7)\ T_{RCP}$	$(4/7)\ T_{RCP} + T_{RSKM}$	ns
Input Data Position for Bit 3	T_{RIP3}	*2)	$(5/7)\ T_{RCP} - T_{RSKM}$	$(5/7)\ T_{RCP}$	$(5/7)\ T_{RCP} + T_{RSKM}$	ns
Input Data Position for Bit 2	T_{RIP2}	*2)	$(6/7)\ T_{RCP} - T_{RSKM}$	$(6/7)\ T_{RCP}$	$(6/7)\ T_{RCP} + T_{RSKM}$	ns
Receiver Skew Margin	T_{RSKM}	*2)	-0.35		0.35	ns

*1) RXBCKN, RXBCKP, RXACKN, RXACKP
*2) RXB0N, RXB0P, RXB1N, RXB1P, RXB2N, RXB2P, RXB3N, RXB3P, RXB4N, RXB4P, RXA0N, RXA0P, RXA1N, RXA1P, RXA2N, RXA2P, RXA3N, RXA3P, RXA4N, RXA4P

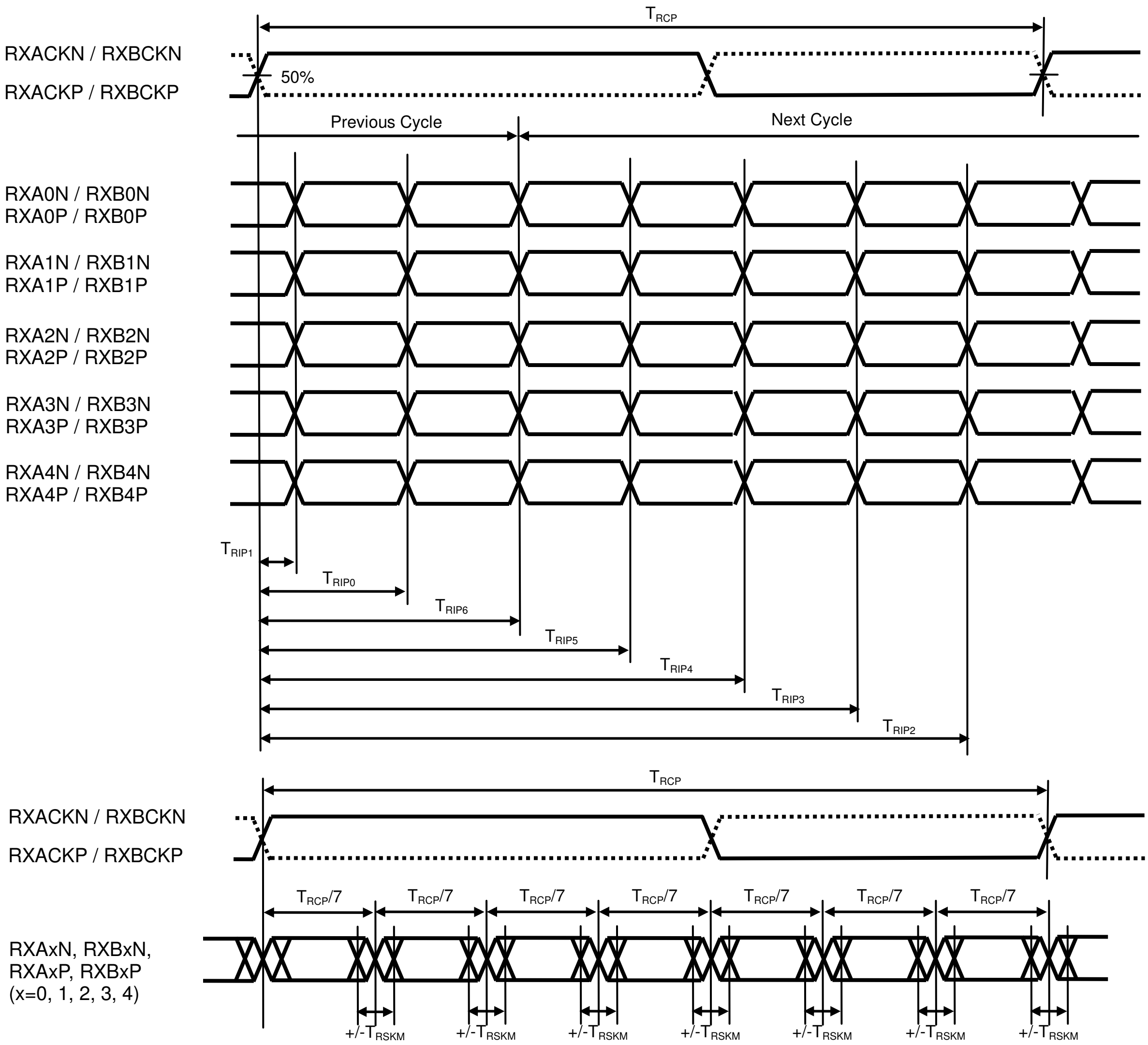


Figure 8.4.4 LVDS Receiver Timing Definition

8.4.5. LVDS Transmitter

(TXAVDD33 = TXDVDD33 = 3.3V+/-0.3V, TXDVDD = 1.2V+/-0.1V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmitter Clock Period	T_{TCP}	*1)	14.70		11.77	ns
Input Data Position for Bit 1	T_{TOP1}	*2)	$- T_{RSK}$	0	$+ T_{RSK}$	ns
Input Data Position for Bit 0	T_{TOP0}	*2)	$(1/7)\ T_{RCP} - T_{RSK}$	$(1/7)\ T_{RCP}$	$(1/7)\ T_{RCP} + T_{RSK}$	ns
Input Data Position for Bit 6	T_{TOP6}	*2)	$(2/7)\ T_{RCP} - T_{RSK}$	$(2/7)\ T_{RCP}$	$(2/7)\ T_{RCP} + T_{RSK}$	ns
Input Data Position for Bit 5	T_{TOP5}	*2)	$(3/7)\ T_{RCP} - T_{RSK}$	$(3/7)\ T_{RCP}$	$(3/7)\ T_{RCP} + T_{RSK}$	ns
Input Data Position for Bit 4	T_{TOP4}	*2)	$(4/7)\ T_{RCP} - T_{RSK}$	$(4/7)\ T_{RCP}$	$(4/7)\ T_{RCP} + T_{RSK}$	ns
Input Data Position for Bit 3	T_{TOP3}	*2)	$(5/7)\ T_{RCP} - T_{RSK}$	$(5/7)\ T_{RCP}$	$(5/7)\ T_{RCP} + T_{RSK}$	ns
Input Data Position for Bit 2	T_{TOP2}	*2)	$(6/7)\ T_{RCP} - T_{RSK}$	$(6/7)\ T_{RCP}$	$(6/7)\ T_{RCP} + T_{RSK}$	ns
Transmitter Skew	T_{TSK}	*2)	-0.35		0.35	ns

*1) TXACKP, TXACKN, TXBCKP, TXBCKN
*2) TXA4P, TXA4N, TXA3P, TXA3N, TXA2P, TXA2N, TXA1P, TXA1N, TXA0P, TXA0N, TXB4P, TXB4N, TXB3P, TXB3N, TXB2P, TXB2N, TXB1P, TXB1N, TXB0P, TXB0N

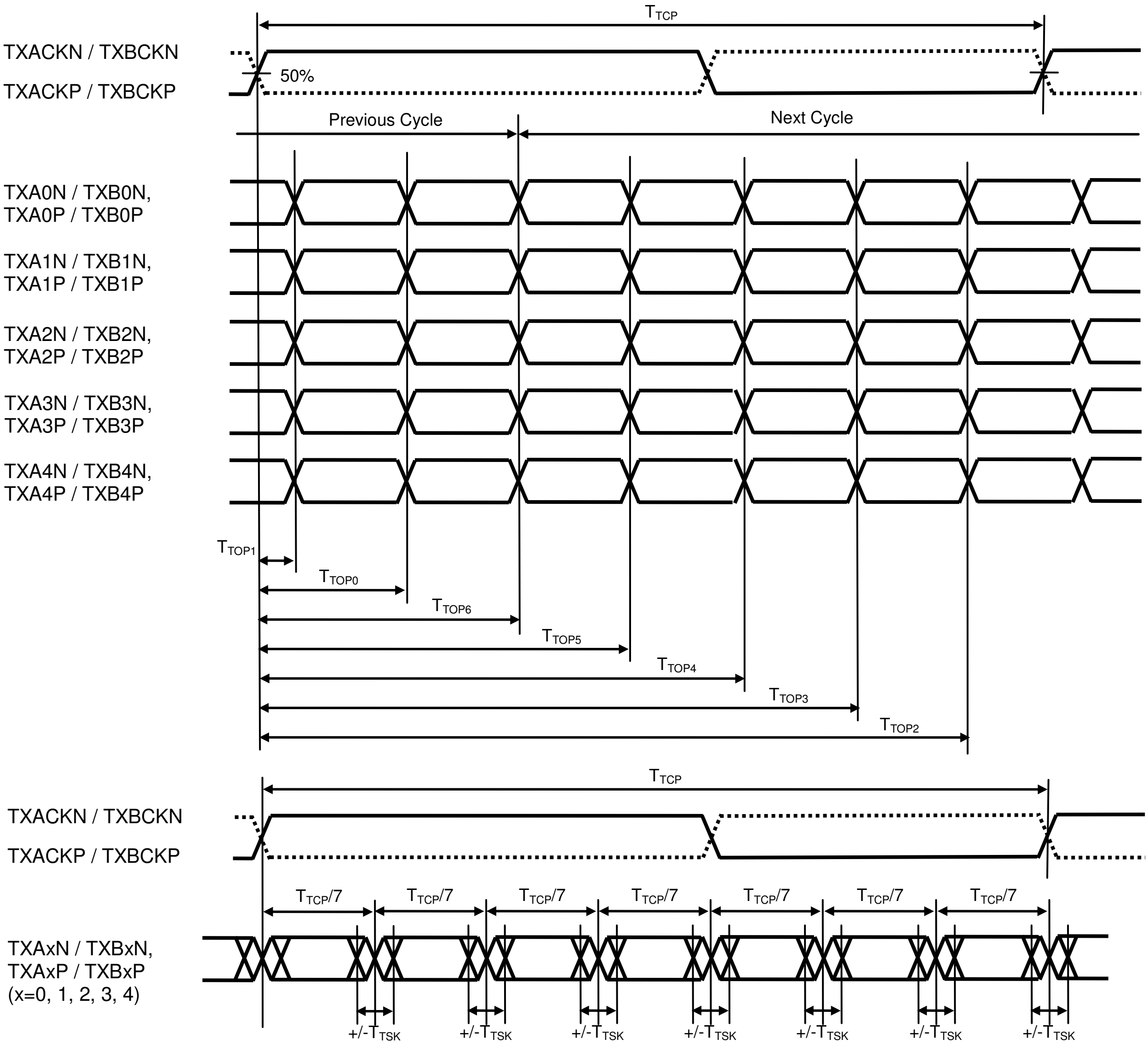


Figure 8.4.5 LVDS Transmitter Timing Definition

9. Description of Functions

9.1. LVDS Receiver

The CXD4732R has two links of LVDS Receiver for 8bit/10bit video input. The external termination registers (100 Ω) are needed for each differential pair. Place them near each pin.

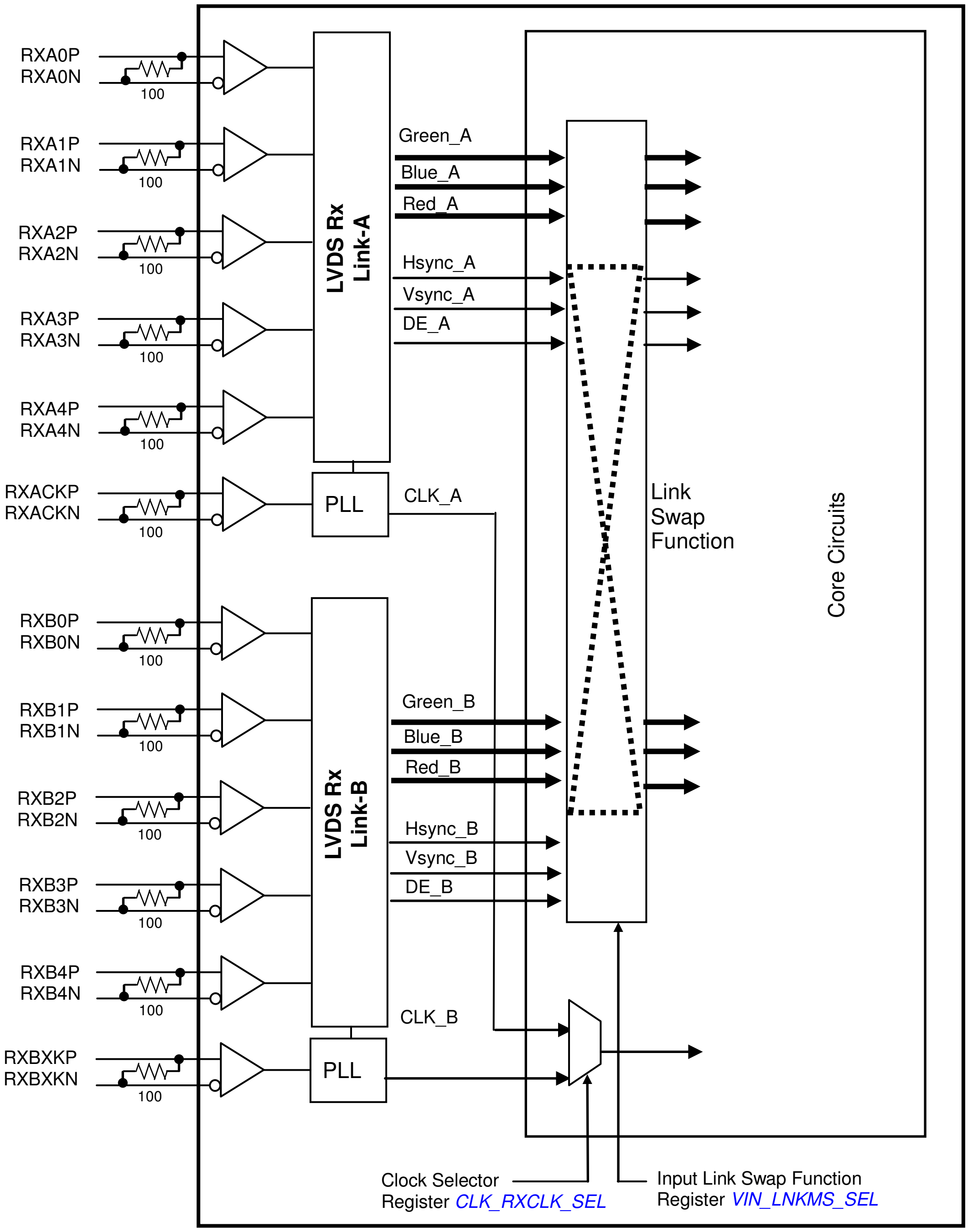


Figure 9.1 LVDS Receiver Block Diagram

9.1.1. Picture Size

This LSI supports two video formats as follows. That mode is applied to both LVDS Rx and Tx. To change the mode, refer to Application note.

Mode	Active Video Size	Number of Link
WXGA	1366 × 768	Single Link (default link is Link-A)
FHD	1920 × 1080	Dual Link (default master link is Link-A, slave link is Link-B) Master Link: pixel 1, 3, 5, 7, …, 1919 Slave Link: pixel 2, 4, 6, 8, …, 1920

9.1.2. Link Swap Function, Master/Slave Link

LVDS Rx link swap function can replace Link-B with Link-A. For single link (WXGA), choose Link-A or B by this function. If Link-B is used, change the link by the *VIN_LNKMS_SEL*. For dual link (FHD), 1st link (1, 3, 5, …, 1919) is Master link, and 2nd link (2, 4, 6, …, 1920) is Slave link. Master/Slave link can be swapped by this function.

9.1.3. Video Clock Selector

One of LVDS Rx links is selected for the internal video clock as shown in **Figure 9.1**. For single link, select to active link. For dual link, choose from the Link A or B. To select the clock, use the *CLK_RXCLK_SEL*.

9.1.4. 8-bit /10-bit Input Mode Selector

This LSI supports both 8-bit and 10-bit inputs. In 8-bit mode, Channel 4 of each link is disabled. The LVDS bit assignment is shown in chapter “9.1.7 LVDS Data Format”. This setting is applied to both Link A and B. To change this mode, see application note.

9.1.5. Support Frequency Range

Mode	Item		Symbol	Min.	Typ. 50Hz System	Typ. 60Hz System	Max.	Unit
WXGA / Single Link Input	LVDS Rx Clock Frequency		1/Tc_wxga	68	82.86		85	MHz
	Frame Rate		Fv_wxga	-	50	60	-	Hz
	Vertical Section	Vertical Total	Tv_wxga	785	838		950	Th_wxga
		Vertical Active	Tvact_wxga	768				Th_wxga
		Blanking Total	Tvblank_wxga	20	70		182	Th_wxga
	Horizontal Section	Horizontal Total	Th_wxga	1450	1978	1648	2050	Tc_wxga
		Horizontal Active	Thact_wxga	1366				Tc_wxga
		Blanking Total	Thblank_wxga	84	612	282	684	Tc_wxga
FHD / Dual Link Input	LVDS Rx Clock Frequency		1/Tc_fhd	68	74.25		80	MHz
	Frame Rate		Fv_fhd	-	50	60	-	Hz
	Vertical Section	Vertical Total	Tv_fhd	1100	1125		1200	Th_fhd
		Vertical Active	Tvact_fhd	1080				Th_fhd
		Blanking Total	Tvblank_fhd	20	45		120	Th_fhd
	Horizontal Section	Horizontal Total	Th_fhd	2150 / 2	2640 / 2	2200 / 2	2690 / 2	Tc_fhd
		Horizontal Active	Thact_fhd	1920 / 2				Tc_fhd
		Blanking Total	Thblank_fhd	230 / 2	720 / 2	280 / 2	770 / 2	Tc_fhd

9.1.6. Video Sync Mode

This LSI supports the following two video sync modes.

9.1.6.1. Sync through Mode

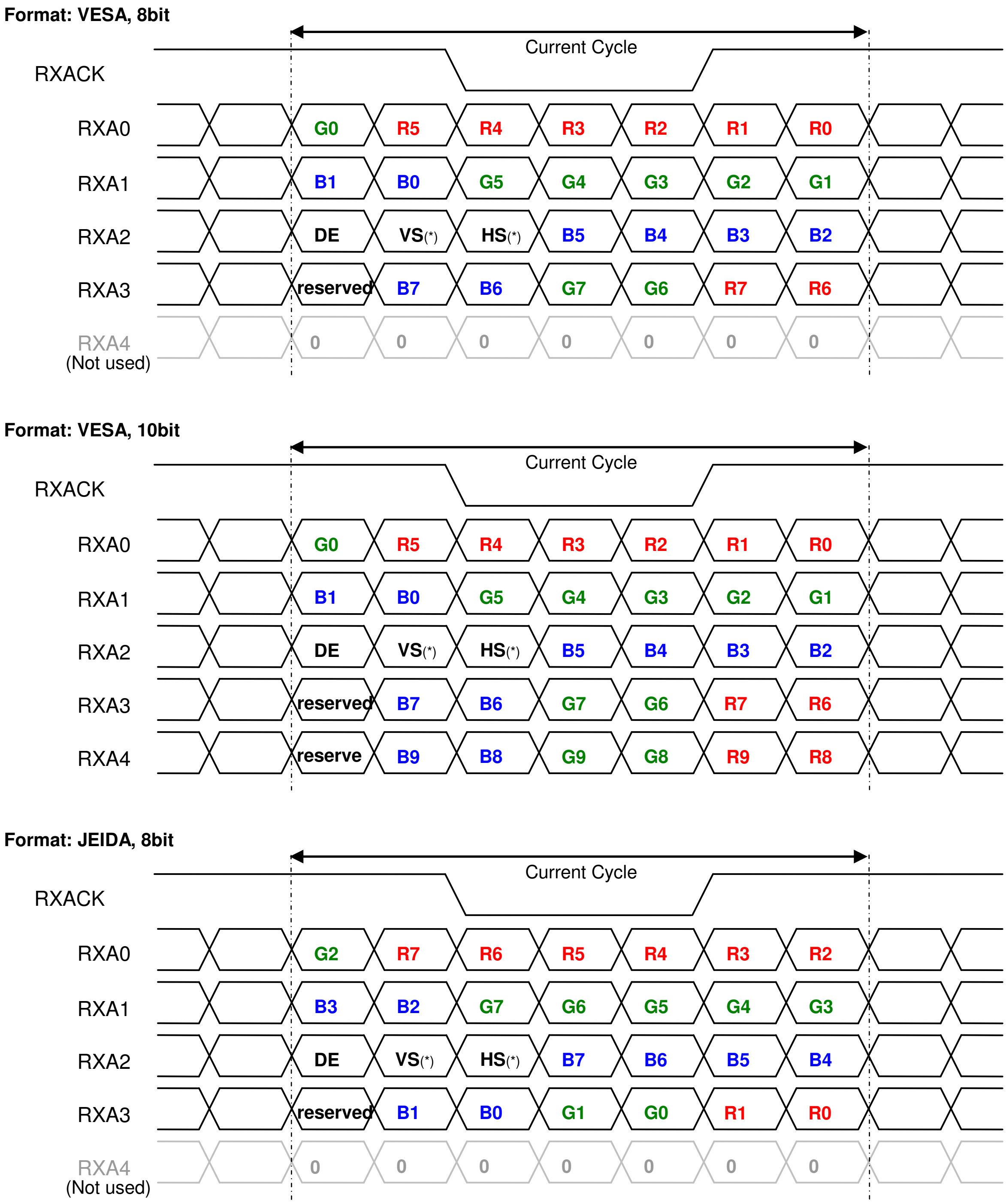
If input video signal is associated with V-Sync, H-Sync and DataEnable, this LSI works on the Sync through mode. In this mode, this LSI operates with V-Sync, H-Sync and DataEnable and outputs them with processed video signals. This mode is set by *SYNC_MODE* =1h, *VIN_SYNC1* =13h, *VIN_SYNC2* =13h, *VIN_SYNC3* =13h and *VOT_SYNC1* =1h.

9.1.6.2. Sync through Mode

If there is neither V-Sync nor H-Sync in input video signal, but the input signal is associated with DataEnable (DE), this LSI operates on the DE-only mode. In this mode, only DE is used for video sync. V-Sync and H-Sync are disregarded and there is neither V-Sync output nor H-Sync output from this LSI. This mode is set by *SYNC_MODE* =0h, *VIN_SYNC1* =14h, *VIN_SYNC2* =14h, *VIN_SYNC3* =14h and *VOT_SYNC1* =0h.

9.1.7. LVDS Data Format

This LSI supports two modes, VESA and JEIDA. Bit assignment is shown in the **Figure 9.1.7**. To change this format, see Application note. Selected format is applied to both Link A and B, and LVDS Rx and Tx.



Format: JEIDA, 10bit

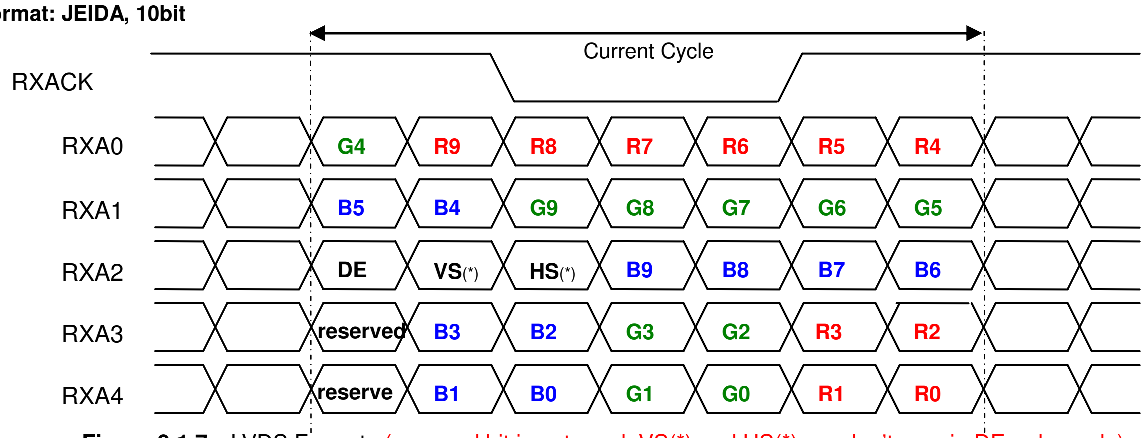


Figure 9.1.7 LVDS Formats (reserved bit is not used, VS(*) and HS(*) are don't care in DE-only mode)

9.1.8. [Important] Restrictions for VS,HS,DE

Input signal VS,HS,DE must be satisfied following three restrictions.

① Logical cycles of VS,HS,DE both Link-A and Link-B must be synchronized. (see Figure 9.1.8)

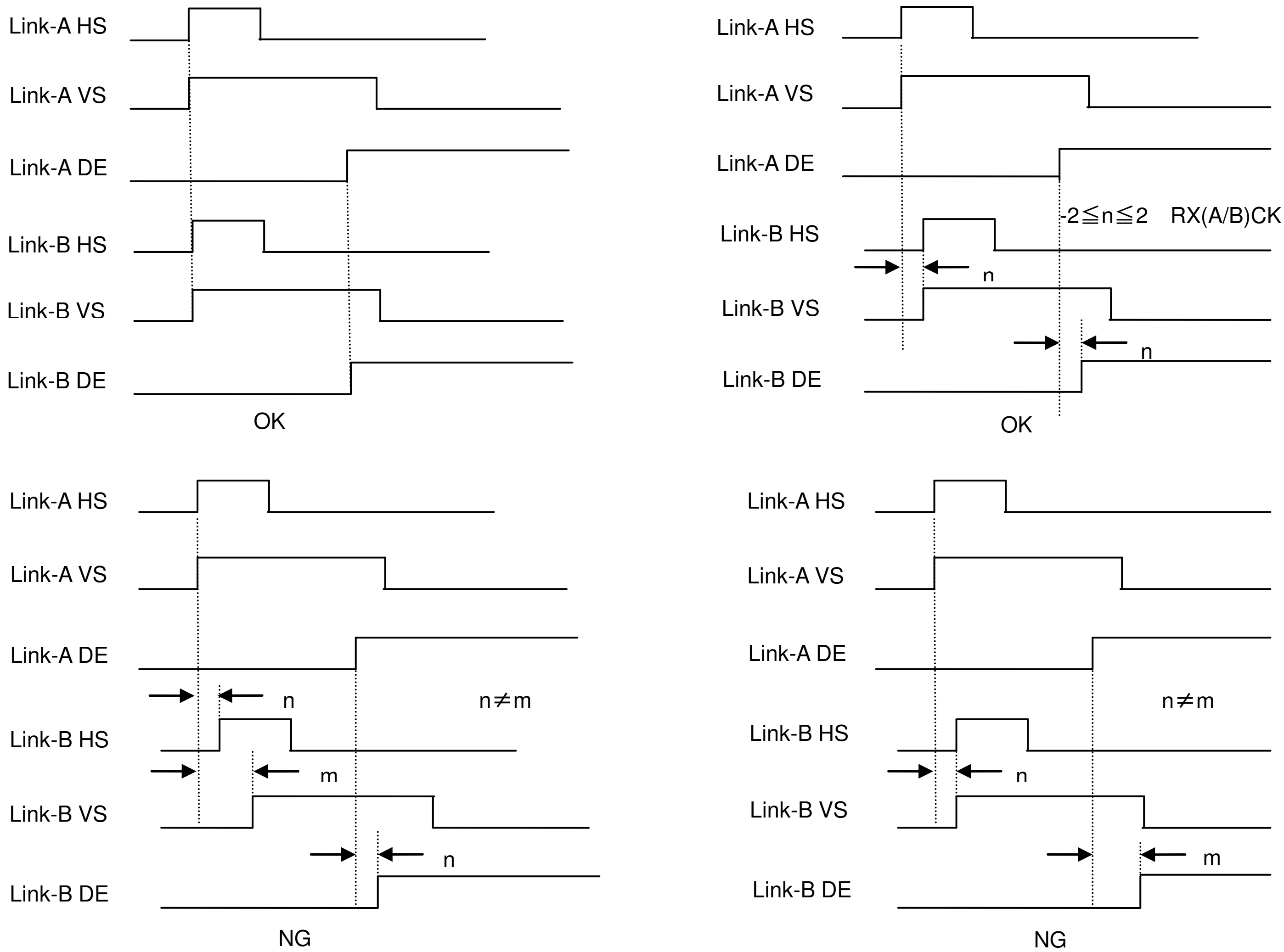
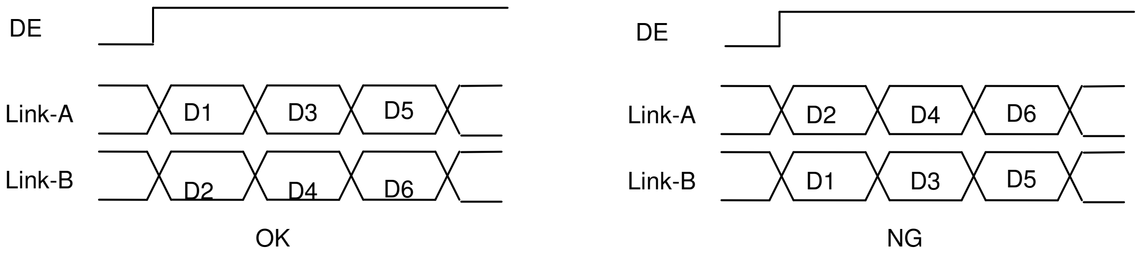


Figure 9.1.8 LVDS input Restriction 1

②First data must be started from Master link.　(see Figure 9.1.9)

Master link : Link-A



Master link : Link-B

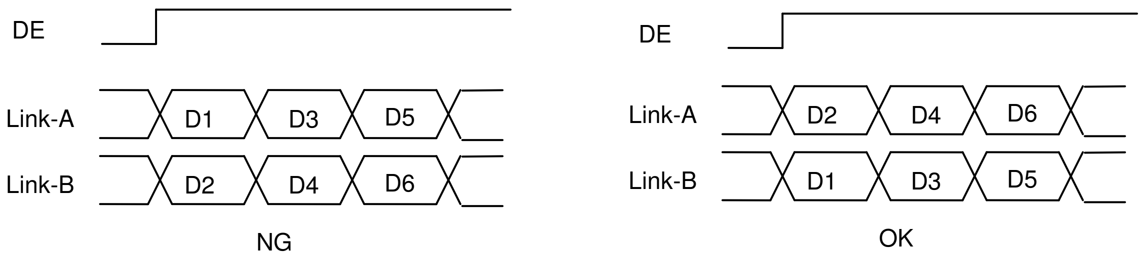


Figure 9.1.9　LVDS input Restriction 2

③DE must be 0 when VS and HS are rising. (see Figure 9.1.10)　(Except DE-only Mode)

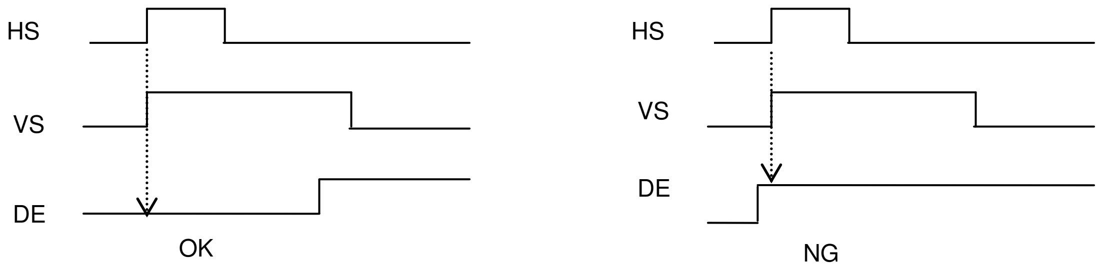


Figure 9.1.10　LVDS input Restriction 3

9.2. LVDS Transmitter

This LSI has also two links of LVDS Transmitter for 8bit/10bit video output.

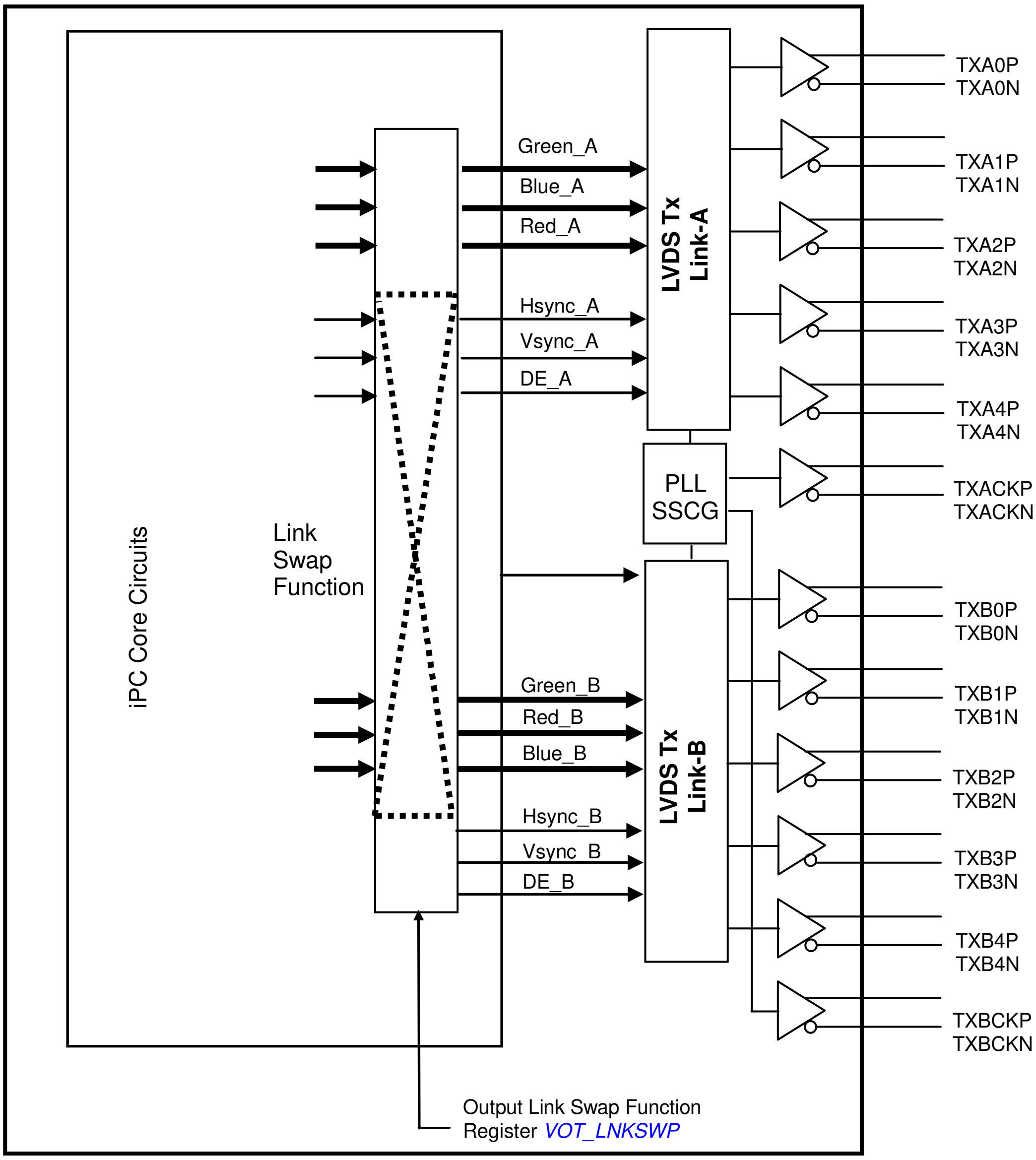


Figure 9.2 LVDS Transmitter Block Diagram

9.2.1. Link Swap Function

As shown **Figure 9.2**, LVDS Tx link swap function can replace Link-B with Link-A. For single link (WXGA), choose Link-A or B by this function. For dual link (FHD), 1st link (1, 3, 5… 1919) and 2nd link (2, 4, 6… 1920) can be swapped by this function. The *VOT_LNKSWP* is used to control this function. The LVDS Tx link swap function operates independently from the LVDS Rx link swap function.

9.2.2. 8-bit / 10-bit Output Mode Selector

This LSI supports both 8-bit and 10-bit outputs. In 8-bit mode, Channel 4 of each link is disabled. The LVDS bit assignment is shown in chapter "9.1.7 LVDS Data Format". This setting is applied to both Link-A and B. To change this mode, see application note. This function works independently from LVDS Rx.

9.2.3. LVDS Tx Output Differential Voltage Adjusting

LVDS Tx differential voltage is selectable from 250mV or 350mV. This is selected by register *LVTX_SWING*.

9.2.4. LVDS Tx Output Disable

The registers *LVTX_ENA* for LVDS Tx Link-A, *LVTX_ENB* for LVDS Tx Link-B are used to disable the LVDS Tx all signals which include both clock and data. If those signals are disabled, the differential voltages of each pair for all clock and data are set at common voltage. The initial value of this registers are "0" (it is disabled at reset).

9.2.5. Spread-spectrum Clock Generator (SSCG) for LVDS Tx

This LSI includes the SSCG to reduce EMI. It supports Center Spreading as shown in **Figure 9.2.5.1**. To enable this SSCG function, set to *LVTX_SSEN*.

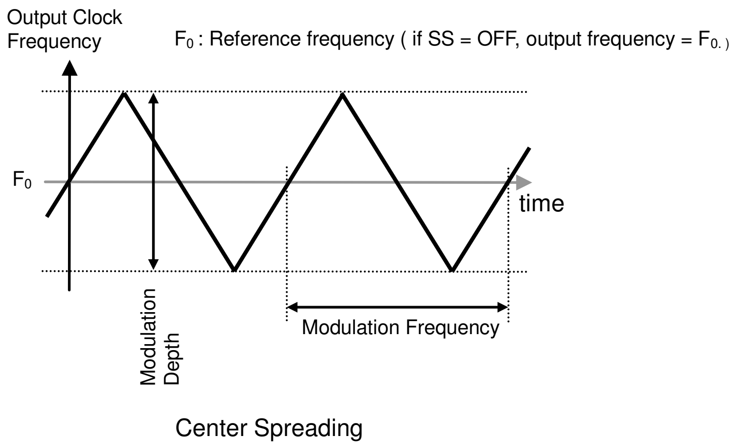


Figure 9.2.5.1 SSCG Modulation Frequency and Depth

The modulation frequency is calculated by the expression of reference frequency / N. N is selected from 4 conditions by setting *LVTX_FRSEL*. For example, at the Reference frequency = 74.25MHz and N = 512, then Modulation Frequency = 145 kHz.

LVTX_FRSEL	N
00h	N/A
01h	512
02h	640
03h	1024

Modulation depth is selected from 8 conditions by setting *LVTX_SSEL* and *LVTX_SRSEL*.

LVTX_SSEL	*LVTX_SRSEL*	**Modulation Depth (Center Spreading)**
00h	00h	±0.625 %
00h	01h	±1.25 %
00h	02h	N/A
00h	03h	N/A
01h	00h	N/A
01h	01h	N/A
01h	02h	N/A
01h	03h	N/A

Note) This SSCG uses the LVDS Rx clock for source clock. In case of the internal SSCG is enabled, non-SS clock is required for the LVDS Rx clock. If the LVDS Rx clock is SSC (Spread-spectrum Clock), internal SSCG must be disabled.

9.2.6. Spread-spectrum Clock Tracking Capability of LVDS Rx

Internal SSCG is OFF and the LVDS Rx clock is SSC, the tracking range of that SSC is shown the following table (Note: these values are only for reference).

Tracking Frequency Range	Tracking Depth Range
70~150kHz	（Tracking Frequency Range * Tracking Depth Range(%)） ≦±150kHz ・%

9.3. Color Management

The Color Management function can tune the color reproduction for user's liking.

9.3.1. Color Control Algorithm

The color area which a user wants to adjust is selectable from nine color area independently. The colors are Green, Pale Orange1, Red, Blue, Yellow, Magenta, Cyan, Pink, and White when *COM_MODE* =0h. When *COM_MODE* =1h, the colors are Green, Pale Orange1, Pale Orange2 (fix area), Red, Blue, Yellow, Magenta, Cyan and White.

The **Figure 9.3.1.1** shows the concept of the Color Management. This function changes a normalized chromaticity (x, y) only in that color area to an arbitrary chromaticity by setting the direction (dx, dy) and quantity of movement (gain). Maximum chromaticity ranges of each nine color area are fixed and those color area are not overlapped each other. This is to keep color consecutiveness between different color areas after a color changes.

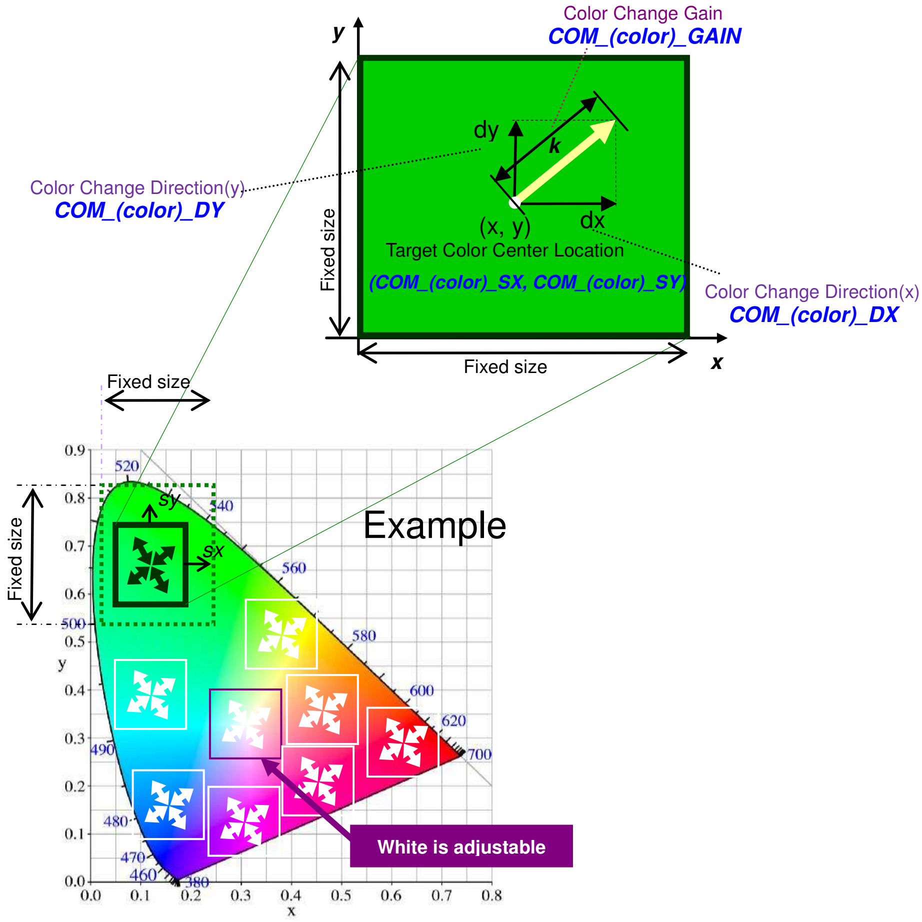


Figure 9.3.1.1 Color Management

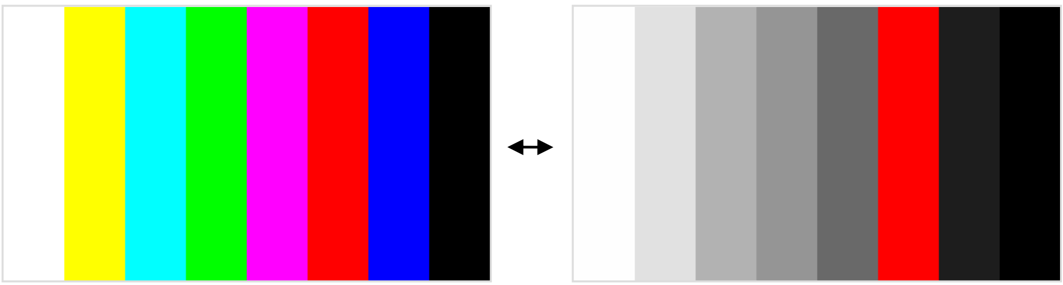
The **Table 9.3.1** shows the Registers to control colors in this function, there is only 45 parameters.

Color	**Target Color Coordinates(-8~+7)**		**Color Change Direction (-8~+7) and Gain (0~31)**		
	sx	sy	dx	dy	gain (x & y)
White	*COM_W_SX*	*COM_W_SY*	*COM_W_DX*	*COM_W_DY*	*COM_W_GAIN*
Green	*COM_G_SX*	*COM_G_SY*	*COM_G_DX*	*COM_G_DY*	*COM_G_GAIN*
Pale Orange1	*COM_PO_SX*	*COM_PO_SY*	*COM_PO_DX*	*COM_PO_DY*	*COM_PO_GAIN*
Red	*COM_R_SX*	*COM_R_SY*	*COM_R_DX*	*COM_R_DY*	*COM_R_GAIN*
Blue	*COM_B_SX*	*COM_B_SY*	*COM_B_DX*	*COM_B_DY*	*COM_B_GAIN*
Yellow	*COM_Y_SX*	*COM_Y_SY*	*COM_Y_DX*	*COM_Y_DY*	*COM_Y_GAIN*
Magenta	*COM_M_SX*	*COM_M_SY*	*COM_M_DX*	*COM_M_DY*	*COM_M_GAIN*
Cyan	*COM_C_SX*	*COM_C_SY*	*COM_C_DX*	*COM_C_DY*	*COM_C_GAIN*
Pink (COM_MODE=0)	*COM_P_SX*	*COM_P_SY*	*COM_P_DX*	*COM_P_DY*	*COM_P_GAIN*
Pale Orange2 (COM_MODE=1)	-	-	*COM_P_DX*	*COM_P_DY*	*COM_P_GAIN*

Table 9.3.1 Color Management registers (Page 00h for all registers. See the register map for details)

9.3.2. Gray Out Function

The Gray Out function can drop a color ingredient except a selected color to confirm a chosen color area. The *COM_GO_EN* is used to enable/disable this function. A color is selected by the *COM_GON_COL*.



Normal Mode

Gray Out Enable (example: red is selected)

Figure 9.3.2 Gray Out Function

9.4. Intelligent Contrast Enhancer（iCE）

The iCE function improves contrast feeling depending on picture content adaptively.

The iCE function measures histogram of brightness signals for every frame, and a characteristic of a picture is extracted. The contrast gain result is calculated for every frame. The contrast gain level can be adjusted by the *ICE_A*, *ICE_B*, and *ICE_C*. *ICE_A* and *ICE_B* decide compensation quantity of gain compensation characteristic A, B determined by histogram of a brightness signal for the whole picture. *ICE_C* decides quantity of gain compensation determined by calculating histogram of a partial brightness signal for a picture

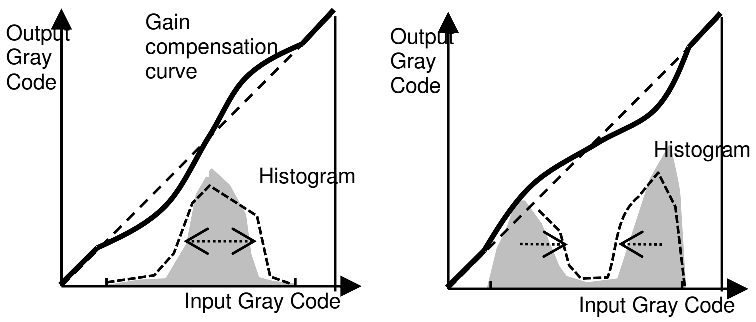
9.4.1 Brightness Contrast Gain Control

ICE_A **: iCE A function gain**

When the brightness histogram of all the pictures concentrates on a center or sides as shown in **Figure 9.4.1.1 (a)** and **(b)**, iCE adjusts contrast with gain compensation curve where compensation quantity turns over with the center gray level. The *ICE_A* adjusts quantity of gain compensation for the histogram. If the *ICE_A* value is high, the quantity of gain compensation increases.

For example, when brightness of all the pictures concentrates on a center level and contrast lacks generally as shown in **Figure 9.4.1.1 (a)**, iCE expands brightness distribution to the level shown in the dashed line.

When brightness of all the pictures concentrates to the sides (black and white) as shown in **Figure 9.4.1.1 (b)**,iCE also expands brightness distribution to the level shown in dashed line.



(a) (b)

Figure 9.4.1.1 iCE example histogram, case A

ICE_B **: iCE B function gain**

When the brightness histogram of all the pictures concentrates on a black or white such as **Figure 9.4.1.2 (a)** and **(b)**, iCE adjusts contrast with gain compensation curve which connects a white level from a black level smoothly. The *ICE_B* adjusts quantity of gain compensation for such histogram. If the *ICE_B* value is high, the quantity of gain compensation increases. For example, when brightness of all the pictures concentrates to high level and contrast lacks on white as shown in **Figure 9.4.1.2 (a)**, iCE expands brightness distribution to low gray level shown in the dashed line. When brightness of all the pictures concentrates to low level and contrast lacks on black as shown in **Figure 9.4.1.2 (b)**, iCE expands brightness distribution to high gray level shown in the dashed line. Therefore, average brightness level (APL or

DC level) of a picture is adjusted by this function automatically.

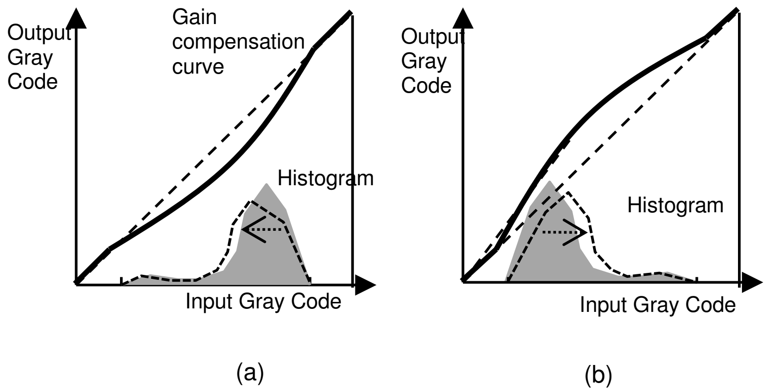


Figure 9.4.1.2 iCE example histogram, case B

ICE_C : iCE C function gain

ICE_C controls the signal gain to improve the contrast to react accordingly to the histogram condition of a brightness signal on the each part of the picture. The characteristics of the *ICE_C* gain compensation is faithful to the histogram of a brightness signal which is shown in **Figure 9.4.1.3**.

Same as *ICE_A*/*ICE_B*, the user can adjust how much compensate when checking the result of this control on the real picture to set the register setting.

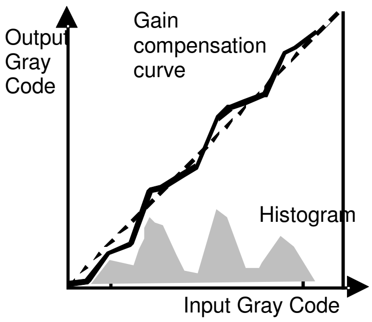


Figure 9.4.1.3 iCE example histogram for type C

9.4.2 Color Contrast Gain Control

ICE_COLOR_GAIN_A : iCE Color gain compensation（DC gain）

This register sets the levels of chroma signal values to match the brightness signal values. When brightness signal contrast is enhanced, the balance between brightness signal and chroma signal may be unbalanced. Especially, when the brightness signal distribution after enhancing the contrast by *ICE_B* setting would be closer to the black level, the average level of luminance (APL) is increased. It makes the picture to be whiter as close as being lacking of chroma signal value.

The setting of the *ICE_COLOR_GAIN_A* is made as shown in **Figure 9.4.1.2 (b)**. The better setting would be available only by user's eyes checking at the effects after changing the value *ICE_B*. When setting “0” to this register, the function can be set to “Off”.

ICE_COLOR_GAIN_B **iCE Color gain compensation（Differential gain）**

Same as *ICE_COLOR_GAIN_A*, the *ICE_COLOR_GAIN_B* can adjust the signal balance between brightness and chroma. Especially this register is effective to improve balance in case of histogram which is shown for **Figure 9.4.1.1 (a)**. In other words this register is effective in a case without much change in average level of brightness (APL).The setting of the *ICE_COLOR_GAIN_B* would be made as shown in **Figure 9.4.1.1 (a)**. Same as *ICE_COLOR_GAIN_A*, the better setting would be available only by user's eyes checking at the effects after changing the value *ICE_A*. When setting “0” to this register, the function can be set to “Off”.

ICE_SCENE_CHDET **iCE Scene change detect sense**

The iCE function measures histogram of a brightness signal for every frame, and contrast gain is calculated by using this result for every frame. When the gain control speed is fast, brightness level change of a picture can be seen, and the picture seems unnatural. Therefore a gain control circuit has a time constant so that gain change speed becomes slow. In case of “scene change”, brightness histogram of a picture changes greatly and quantity of gain compensation changes greatly. Then, an image just after scene change becomes unnatural by the influence of time constant. The iCE can detect “scene change” by calculating quantity of change in the histogram, iCE makes time constant fast. The *ICE_SCENE_CHDET* controls threshold of brightness histogram change quantity to detect scene change. When this register is set to low, scene change detection sensitivity is high.

ICE_COLOR_GAIN_LMT **iCE Color Gain Compensation Limiter**

The *ICE_COLOR_GAIN_LMT* limits quantity of color gain compensation set with the *ICE_COLOR_GAIN_A*, *ICE_COLOR_GAIN_B*. A color gain does not become too large with this register because it is difficult to decide quantity of color gain compensation corresponding to quantity of brightness gain compensation theoretically. The limiter value is shown in the Table 9.4.1.

Table 9.4.1 *ICE_COLOR_GAIN_LMT* register definition

ICE_COLOR_GAIN_LMT	Limiter Level (dB)	*ICE_COLOR_GAIN_LMT*	Limiter Level (dB)
0	0.0	4	3.5
1	0.5	5	6.0
2	1.0	6	8.0
3	2.0	7	9.0

9.4.3. Black level Control

ICE_A_BLACKLEV1 **iCE_A Black level compensation knee down point**

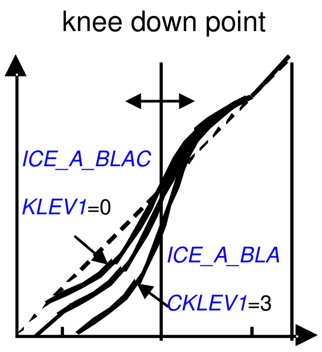


Figure 9.4.3.1

When *ICE_A* works, if the value of *ICE_A_BLACKLEV1* is increased, minus gain versus linear go up. *ICE_A_BLACKLEV1* controls knee down point as shown Figure 9.4.3.1.

ICE_A_BLACKLEV2 iCE_A Black level compensation level

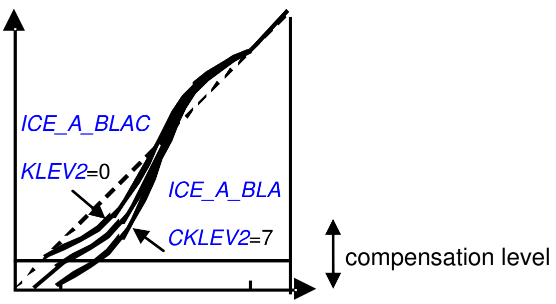


Figure 9.4.3.2

When *ICE_A* works, if the value of *ICE_A_BLACKLEV2* is increased, minus gain versus linear go up. *ICE_A_BLACKLEV2* controls minus gain level as shown Figure 9.4.3.2.

9.5. 2D-Sharpness

This LSI includes two sharpness functions; Y sharpness (Frequency ingredient emphasis of a brightness signal) and CTI (Chrominance Transient Improvement).

The Y sharpness function can improve sharpness independently (show **Figure 9.5.1**) by using a filter of the optimum band-pass, high-pass type for a vertical, horizontal and diagonal of Y signal. Horizontal is 11-tap filter and it has 5 kinds of coefficient. Vertical is 5-tap filter with 4-line memory and it has 2 kinds of coefficient. Those characteristics are changed by the registers of *YHSHP_HBAND*, *YHSHP_VBAND*, *YVSHP_HBAND* and *YVSHP_VBAND*. The emphasis level can adjust it to ±2 times by using each register *YHSHP* for horizontal, *YVSHP* for vertical, and *YTSHP* for diagonal. The emphasis waveform can be adjusted as shown in **Figure. 9.5.2**. The *YSHP_WB* is used for it.

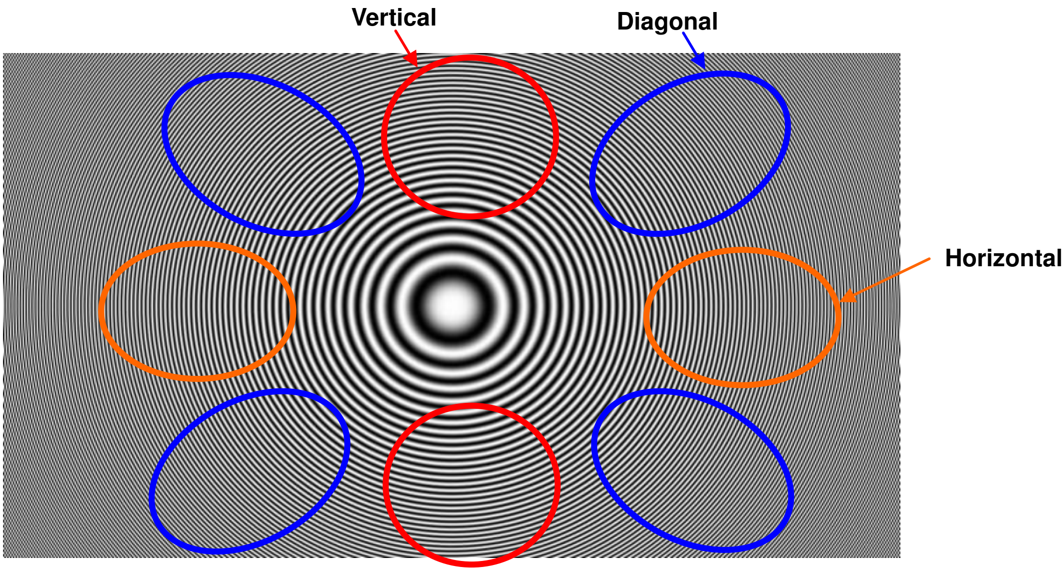


Figure 9.5.1 Y sharpness control area

This function has coring; it can control noise increase more than it for a picture with many noises. Coring level is changed to four phases with register *YSHP_CORE*.

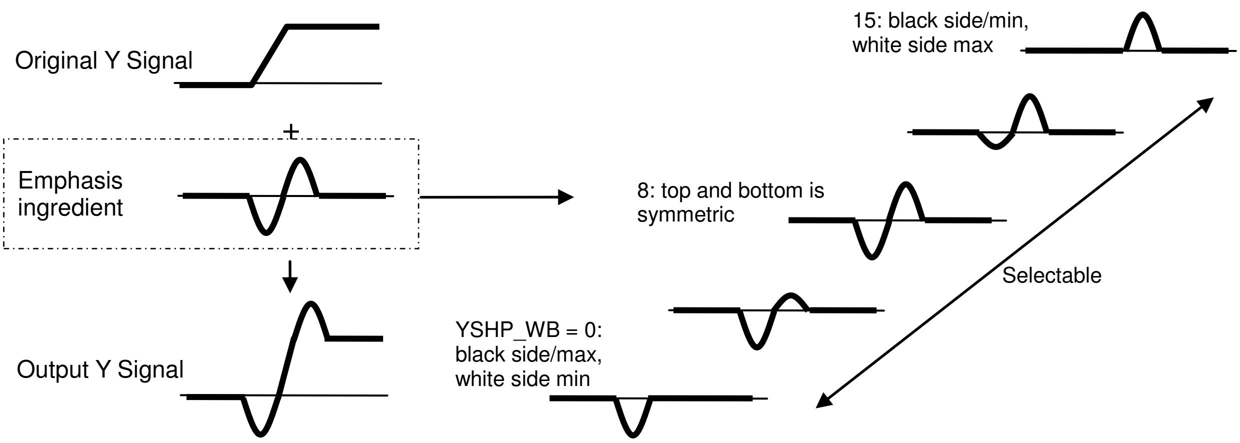


Figure 9.5.2 Y sharpness over, under balance

For color-difference signal (Cb/Cr), CTI function can improve a through rate of a color edge part of a picture. Edge detection has horizontal filter only. Center frequency can be changed by *CTI_F0* and level can be changed by *CTI_LEV*.

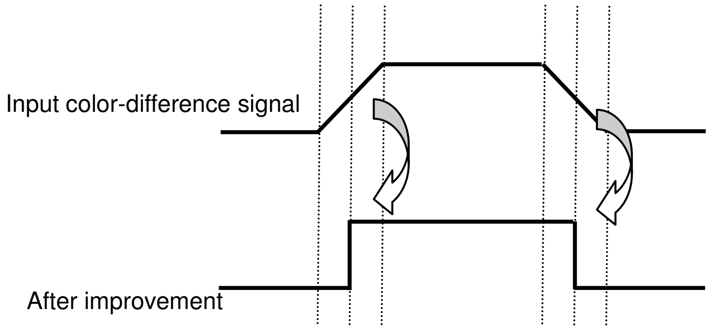
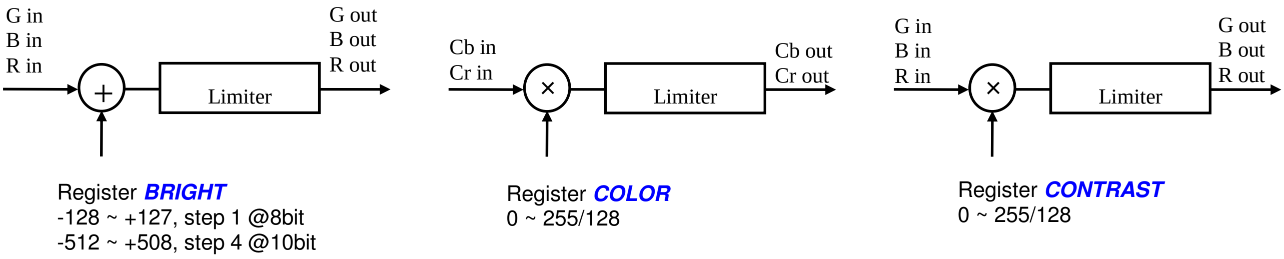


Figure 9.5.3 Color transient improvement

9.6. Basic user Controls

As other video signal processing, there are Brightness for GBR signals, Color saturation for Cb/Cr signals, and Static contrast for GBR signals.



(a) Brightness control (b) Color saturation control (c)Static Contrast control

Figure 9.6

9.7. MC-3DNR

This is MC-3DNR function for luminance signal. This function has following features, then reduces random noise in luminance signal. MC-3DNR uses compensation picture optimally according to reliability of motion estimation.

MC-3DNR is basically controlled by 3 registers. *YNR* controls MC-3DNR ON/OFF. *FBHISTTH* and *NLFB* control time constant of MC-3DNR filter.

And the effort of MC-3DNR is controlled by registers combination. Now 5 levels setting from weakest to strongest are available. For more information, see application note.

9.8. Basic user Controls

GRC(GRadation Creation) includes following two functions.

- Adaptive horizontal smoothing
- Adaptive horizontal and vertical coring
- Mosquito noise reduction (MNR)

When *GRC_EN* is enabled, adaptive horizontal smoothing function works for only low frequency component in input signal. For only high frequency component in input signal, adaptive horizontal and vertical coring is prepared. *GRC_HCORE* and *GRC_VCORE* are controlling registers. These three functions work to reduce pseudo outline.

MNR is mosquito noise reduction. For mosquito noise around edge signals, *MNR_FLAT_LEV* is used. If mosquito noise also exists in flat area, *MNR_FLAT_LEV* is more used.

9.9. SUPER RESOLUTON

This function achieves super resolution with noise inhibiting. It adjusts the most appropriate effect automatically by analyzing input picture pixel by pixel.

You can also adjust the effect of super resolution with the following items. If you want to control everything, there is manual control mode, too.

[Whole gain adjustment]　Relative I2C register: *VOLE_BVD, NSHIFT*

Increasing this gain, the effect of super resolution and noise reducing is up.

[Adjustment around TEXT]　Relative I2C register: *VOLERATIOMAX, VOLERATIOMIN*

This is used to control effect around text. If you don't like shoots around text or line, turn down this value.

[Control in pale orange area]　Relative I2C register: *HADAON, HADA_EFFECT, NLIMIT*

When you use this function, the effect of Super Resolution in pale orange area is reduced. And its degree is controllable.

[Manual control]　Relative I2C register: *ICONTON, VOLN, VOLR, VOLE*

You can stop Super Resolution automatic adjustment, and you can control the effect of super resolution and noise reducing according to your preference. Whole gain is able to be controlled.
Even if you select manual control mode, “Adjustment around TEXT” and “Control in pale orange area” are available.

About register's relation see **Figure 9.9.1**.

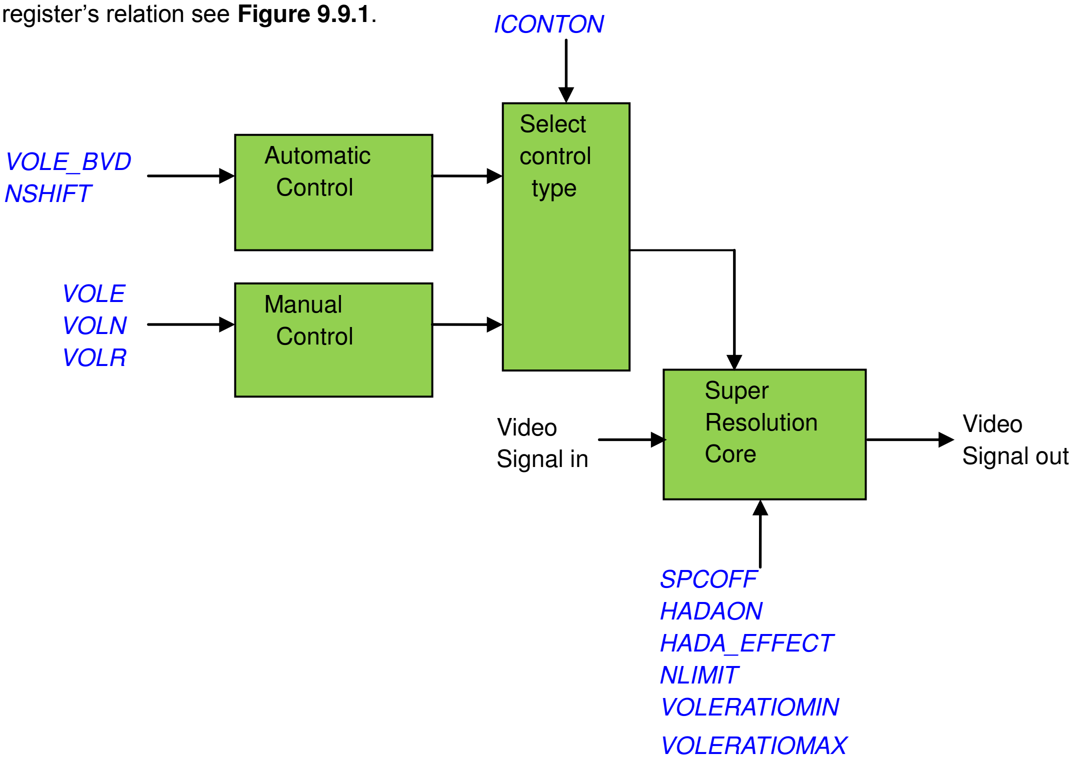


Figure 9.9.1　Super Resolution Block

9.10. Digital Gamma Function

This LSI includes digital gamma function with two look-up tables (Group A and B). Each group has GBR independent 12bit Full-Size LUT. While one group works, another group can be updated to arbitrary 12 bits curve by I^2C interface. Active group and inactive/updating group are changed by *GMTBL_SEL*.

All digital gamma function can be disabled by *GMTBL_EN*. At the power-on reset, *GMTBL_EN* is 0 (default is disabled). Change to enable this register after setup was completed.

Refer to the register map about details of LUT data transfer format (**Chapter 11.3.3** Digital Gamma Function Look-up Table Registers) and setup sequence (**Chapter 10.2** Digital Gamma Function Look-up Table Setup).

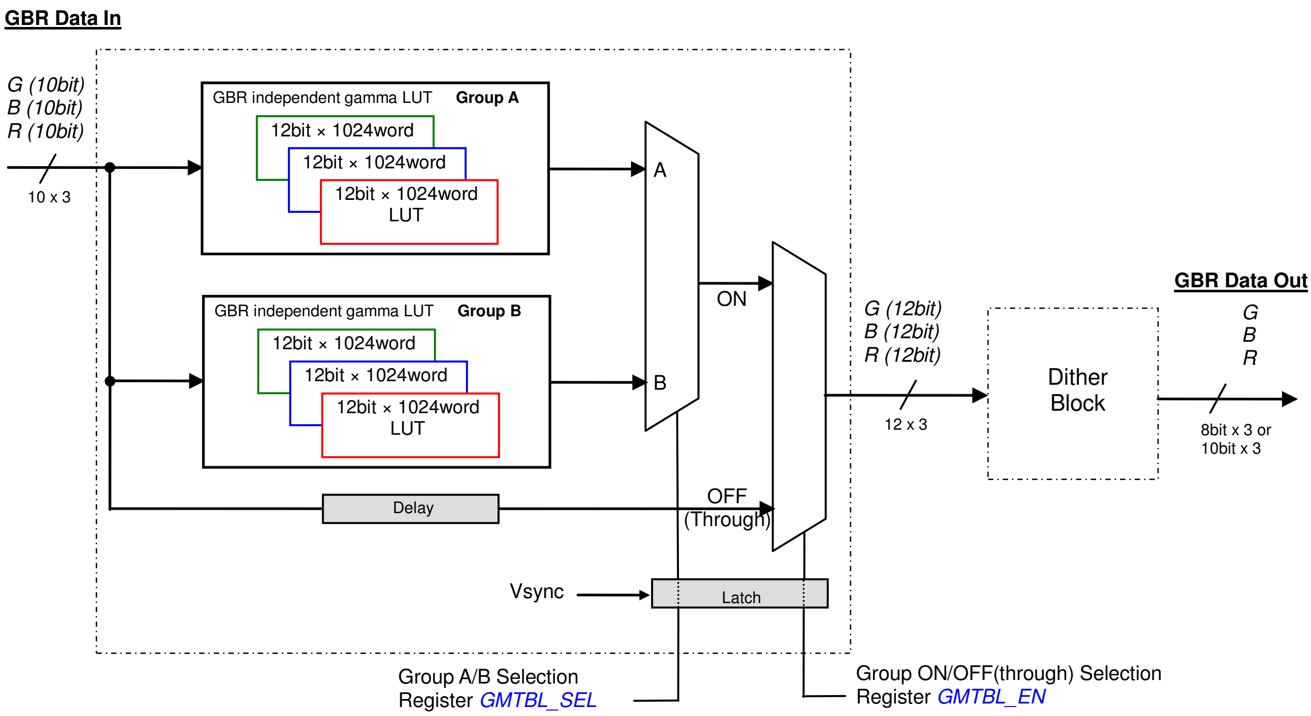


Figure 9.10 Digital Gamma Function and Dither Block

9.11. Dither

This function includes four methods to reduce the video data width from 12bit to 8 (or 10) bit. Those methods are Rounding, FRC (Frame rate conversion), 2 x 2 matrix pattern dithers, and 4 x 4 matrix pattern dithers. FRC and dither methods provide good gradation performance for 8bit/10bit panel. See the register map for details to control this function.

9.11.1. FRC (Frame rate conversion)

FRC is a time sharing process for lower 2bit of 12bit. As shown in **Figure 9.11.1**, the yellow frame means round-up and gray frame mean round-down.

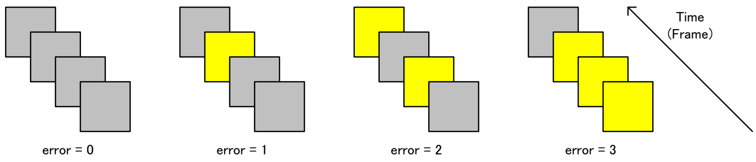


Figure 9.11.1 FRC Bit Processing

9.11.2. Pattern Dither

Pattern dither is a space error spreading process for lower 2bit/4bit of 12bit. As shown in **Figure 9.11.2**, the number in the box is threshold value for error. For example, in 2 x 2 pattern dither, if error = 2 then “0” and “1” pixels are round-up, “2” and “3” pixels are round-down. In 4 x 4 pattern dither, same procedure is used. Here the yellow box means round-up and gray box means round-down.

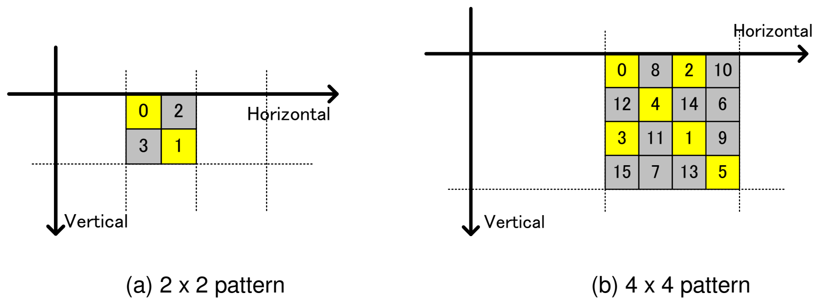


Figure 9.11.2 Pattern Dither

10. Description of Operation

10.1. Power and Reset Sequence

There is no constraint about the turn-on/off order of two power supply voltages (1.2V and 3.3V). But it is preferable to apply both voltages at the same time.

10.1.1. Turn on Sequence without External EEPROM

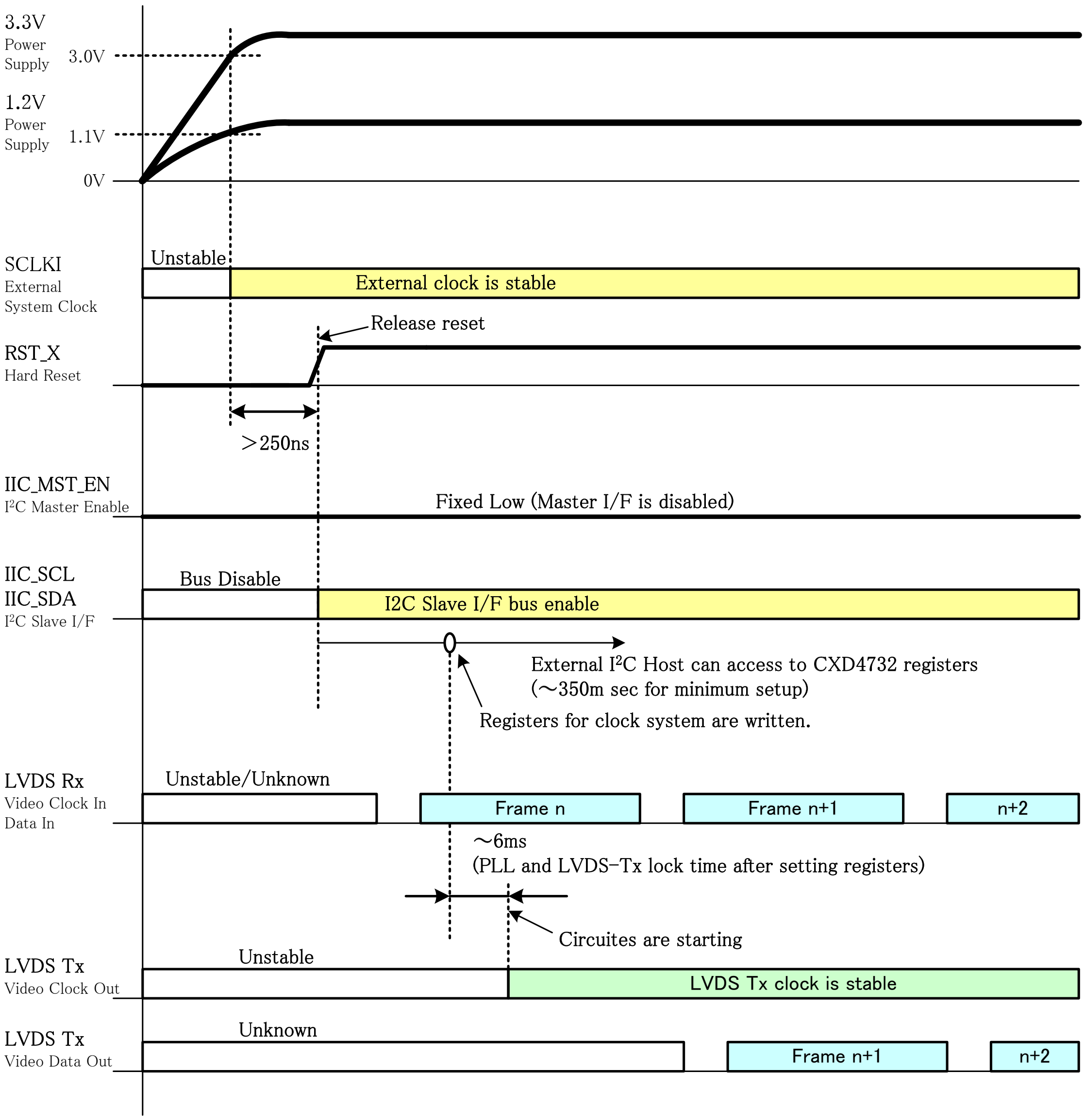


Figure 10.1.1 Power On and Reset Sequence (I^2C Slave I/F Only)

10.1.2. Turn on Sequence with External EEPROM

If the terminal **IIC_MST_EN** is high when the reset **RST_X** is released, the registers are initialized automatically by reading an initial value from an external EEPROM. (See the **Chapter 10.3.5** I^{2}C Master Interface for details)

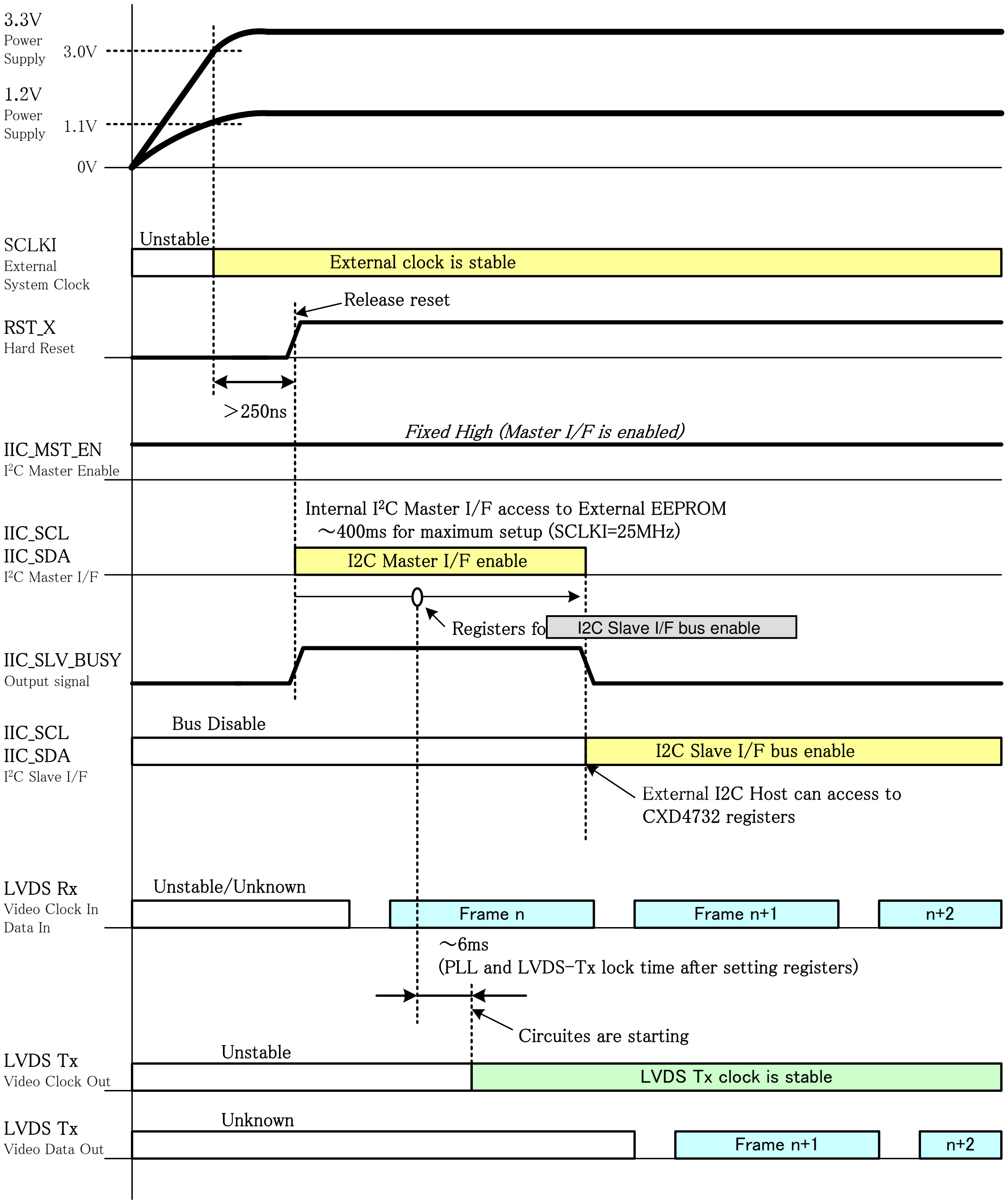


Figure 10.1.1 Power On and Reset Sequence (I^{2}C Slave I/F Only)

10.2. Gamma Correction Look-up Table Setup

The following sequence is required when writing/updating the gamma correction look-up table (LUT).

10.2.1. Initializing Gamma LUT Group-A

(1) Gamma correction function control registers setup: write registers as below,

Sub address FFh, data 1Fh // page change to 1Fh.

Sub address 03h, data 00h // gamma function disable

Sub address 00h, data 00h // Group-A I^2C write enable

Sub address 01h, data 00h // Group-A I^2C write enable

Sub address 02h, data 00h // Group-A I^2C write enable

Sub address 04h, data 01h // Group-B Normal mode

Sub address 05h, data 01h // Group-B Normal mode

Sub address 06h, data 01h // Group-B Normal mode

Sub address 07h, data 00h // Group-A/B select

If the table for Group-B is already initialized, it is possible to use the Gamma LUT Group-B while writing Group-A. In this case, Sub address 03h > data 01h, Sub address 07h > **data 01h.**

(2) Look-up table for Group A

(3) Exit LUT setup mode and go to Normal mode.

Sub address FFh, data 1Fh // page change to 1Fh.

Sub address 00h, data 01h // Group-A Normal mode

Sub address 01h, data 01h // Group-A Normal mode

Sub address 02h, data 01h // Group-A Normal mode

Sub address 04h, data 01h // Group-B Normal mode

Sub address 05h, data 01h // Group-B Normal mode

Sub address 06h, data 01h // Group-B Normal mode

Sub address 07h, data 00h // Group-A is selected

Sub address 03h, data 01h // gamma function enable

10.2.2. Initializing Gamma LUT Group-B

(1) Gamma correction function control registers setup: write registers as below,

Sub address FFh, data 1Fh	// page change to 1Fh.
Sub address 03h, data 00h	// gamma function disable
Sub address 00h, data 01h	// Group-A Normal mode
Sub address 01h, data 01h	// Group-A Normal mode
Sub address 02h, data 01h	// Group-A Normal mode
Sub address 04h, data 00h	// **Group-B I^2C write enable**
Sub address 05h, data 00h	// **Group-B I^2C write enable**
Sub address 06h, data 00h	// **Group-B I^2C write enable**
Sub address 07h, data 01h	// Group-A/B select

If the table for Group-A is already initialized, it is possible to use the Gamma LUT Group-A while writing Group-B. In this case, Sub address 03h > data 01h, Sub address 07h > **data 00h**.

(2) Look-up table for Group B

(3) Exit LUT setup mode and go to Normal mode.

Sub address FFh, data 1Fh	// page change to 1Fh.
Sub address 00h, data 01h	// Group-A Normal mode
Sub address 01h, data 01h	// Group-A Normal mode
Sub address 02h, data 01h	// Group-A Normal mode
Sub address 04h, data 01h	// Group-B Normal mode
Sub address 05h, data 01h	// Group-B Normal mode
Sub address 06h, data 01h	// Group-B Normal mode
Sub address 07h, data 01h	// **Group-B is selected**
Sub address 03h, data 01h	// gamma function enable

10.3. Host I/F

10.3.1. I²C Slave Interface

This LSI has an I²C bus slave transceiver. This supports 7 bits slave address and fast transfer mode (400kbit / sec). Slave address can be selectable from four addresses by setting external pin.

10.3.2. I²C Slave Write Cycle

After sending slave address from the external master interface to this slave interface, the write start sub- address is set by the master. The next cycle is 1st data to write control register and the write cycle is repeated by host I/F. When data is written in continually, the internal sub-address is automatically incremented.

S	Slave Address	W	A	Start Sub Address	A	Write Data	A	Last Write Data	A	P
	[7:1] (7bit)	"**0**"		(8bit)		(8bit)		(8bit)		

Note)
Gray: From Master (External Host) to Slave (CXD4732R).
White: From Slave to Master
S: Start Bit P: Stop Bit A: Acknowledge

10.3.3. I²C Slave Read Cycle

Before reading control registers, set the read start sub-address by the same method as write cycle. After then, the external master interface sends the slave address with read command and the internal slave interface returns the read data after next cycle. When data is read in continually, internal sub-address is automatically incremented.

S	Slave Address	W	A	Start Sub Address	A	P
	[7:1] (7bit)	"**0**"		(8bit)		

S	Slave Address	R	A	Read Data	A	Last Read Data	N	P
	[7:1] (7bit)	"**1**"		(8bit)		(8bit)		

Note)
Gray: From Master (External Host) to Slave (CXD4732R).
White: From Slave to Master
S: Start Bit P: Stop Bit A: Acknowledge N: No Acknowledge

10.3.4. I²C Slave Page Address

This LSI can transfer more than 256 bytes of register by using the Page Addressing method. The last 32bytes (E0h~FFh) of sub-address are used for common registers that include page address. Sub-address 00h~DFh are used for function registers. It have some pages (00h~1Fh pages) and the page is changed by common register **PAGE** (sub address: FFh, bit [4:0]). Total function registers are 224 address x 32 pages.

Refer to **Chapter 11.2** I²C Page Address Map.

To change the page address, the following sequence is required.

New page writing:

(1) Set/Change page

S	Slave Address	W	A	Page Sub Address	A	Write Page	A	P
	[7:1] (7bit)	"**0**"		**FFh**		(new page)		

(2) Write register

S	Slave Address	W	A	Start Sub Address	A	Write Data	A	Last Write Data	A	P
	[7:1] (7bit)	"**0**"		(8bit)		(8bit)		(8bit)		

New page reading:

(1) Set/Change page

S	Slave Address	W	A	Page Sub Address	A	Write Page	A	P
	[7:1] (7bit)	"**0**"		**FFh**		(new page)		

(2) Set start address for reading

S	Slave Address	W	A	Start Sub Address	A	P
	[7:1] (7bit)	"**0**"		(8bit)		

(3) Read register

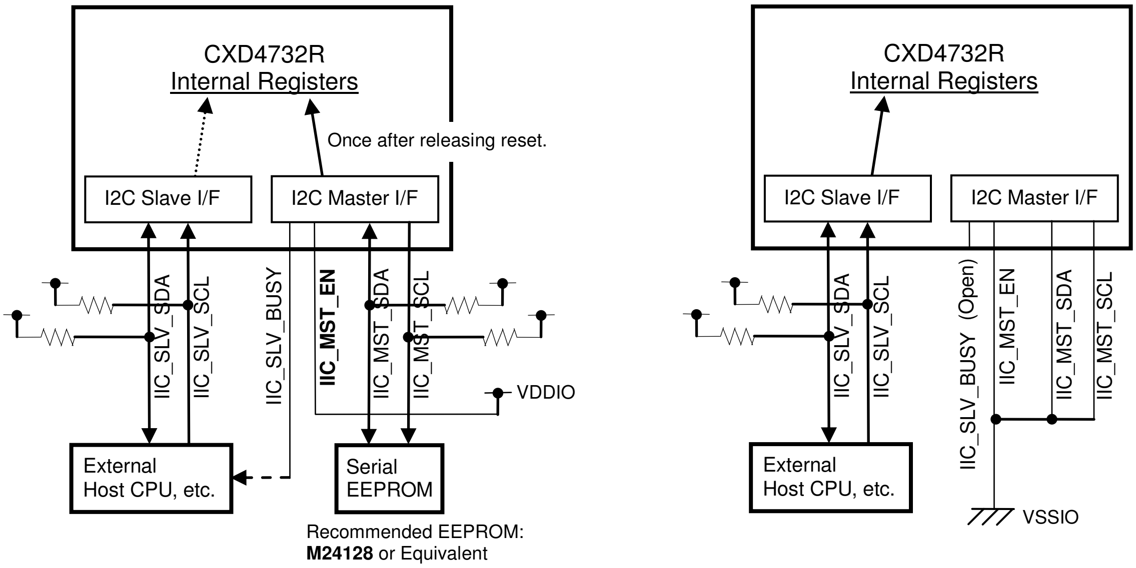
S	Slave Address	R	A	Read Data	A	Last Read Data	N	P
	[7:1] (7bit)	"**1**"		(8bit)		(8bit)		

Note)
Gray: From Master (External Host) to Slave (CXD4732R).
White: From Slave to Master
S: Start Bit P: Stop Bit A: Acknowledge

10.3.5. I²C Master Interface

This LSI includes I²C master interface. It operates once automatically after releasing hard reset to initialize the internal registers.

When the **IIC_MST_EN** pin is held High, I²C master I/F is enabled. After the hard reset pin **RST_X** becomes High from Low, I²C master interface automatically reads the initial register settings from external serial EEPROM which is connected to the I²C master interface, and write it to the internal registers. If it cannot read data correctly, the I²C master interface is stopped and the I²C slave interface is enabled.



(a) Using Serial EEPROM (b) I²C Slave interface only

Figure 10.3.5.1 I²C Interface

This LSI supports 128 Kbit I²C serial EEPROM. As shown in **Figure 10.3.5.1(a)**, the I²C master interface operates independently of I²C slave interface. While the I²C master interface operates, the I²C slave interface can only read. Therefore, before writing registers from external master device such as Host CPU through the I²C slave interface of this LSI, check the status by status register or the **IIC_SLV_BUSY** pin. (While the I²C master interface is operating, the I²C slave interface accepts write command and returns Acknowledge. Note that the internal data path is disconnected.)

In case of no external EEPROM as shown in **Figure 10.3.5.1(b)**, all registers must be written by external host device to initialize this LSI.

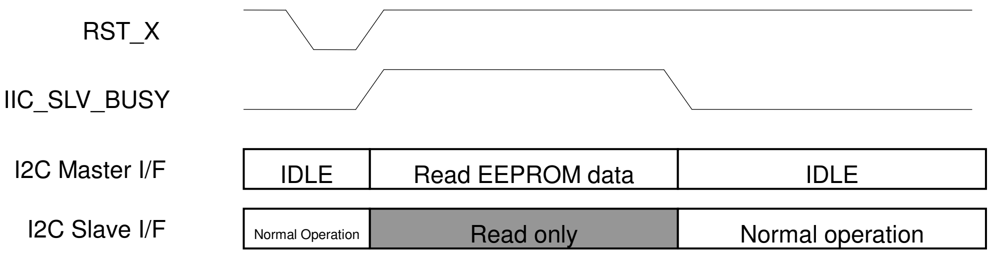


Figure 10.3.5.2 Startup sequence

10.3.6. I^{2}C Bus through mode

This LSI connects I^{2}C master interface and I^{2}C slave interface in I^{2}C Bus through mode, as shown in **Figure 10.3.6.1.** Host CPU can access EEPROM in this mode. When the *IIC_MUST_BTHR* = 1, it becomes I^{2}C Bus through mode.

Note) Please check the status of I^{2}C master interface by the status register *IIC_MST_BUSY* or the **IIC_SLV_BUSY** pin before switching into the I^{2}C Bus through mode.

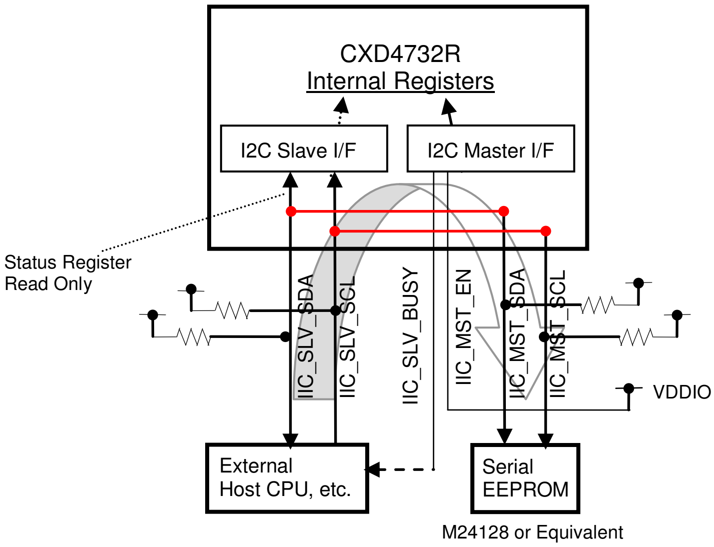


Figure 10.3.6.1 I^{2}C Bus through mode

11. Control Register Map

11.1. I²C Slave Address

Slave address in CXD4732R can be selected from four (for slave interface), two (for Master interface) in the list below by the combination of the **IIC_SLV_SADSEL0**, **IIC_SLV_SADSEL1**, and **IIC_MST_SADSEL** pins.

IIC_SLV_SADSEL1	IIC_SLV_SADSEL0	I²C Slave Address (write)	I²C Slave Address (read)
0	0	**90h**	**91h**
0	1	**92h**	**93h**
1	0	**94h**	**95h**
1	1	**96h**	**97h**

IIC_MST_SADSEL	EEPROM Slave Address (write)	EEPROM Slave Address (read)
0	**ACh**	**ADh**
1	**AEh**	**AFh**

11.2. I²C Page Address Map

Sub Address	Page Address															
	00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh
		Digital Gamma Table (Green)								Digital Gamma Table (Blue)						
00h ~ 7Fh	EXPRESSION Control Registers	Lower 8bit LUT 000h~07FFh	Lower 8bit LUT 080h~0FFh	Lower 8bit LUT 100h~17Fh	Lower 8bit LUT 180h~1FFh	Lower 8bit LUT 200h~27Fh	Lower 8bit LUT 280h~2FFh	Lower 8bit LUT 300h~37Fh	Lower 8bit LUT 380h~3FFh	Lower 8bit LUT 000h~07Fh	Lower 8bit LUT 080h~0FFh	Lower 8bit LUT 100h~17Fh	Lower 8bit LUT 180h~1FFh	Lower 8bit LUT 200h~27Fh	Lower 8bit LUT 280h~2FFh	Lower 8bit LUT 300h~37Fh
80h ~ BFh		Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit
C0h ~ DFh		(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)
E0h ~ FFh	Common Registers (FFh: Page Address Setting)															

Sub Address	Page Address (Continued) 10h (Blue)	11h Digital Gamma Table (Red)	12h	13h	14h	15h	16h	17h	18h	19h	1Ah	1Bh	1Ch	1Dh	1Eh	1Fh
00h ~ 3Fh	Lower 8bit LUT 380h~3FFh	Lower 8bit LUT 000h~07Fh	Lower 8bit LUT 080h~0FFh	Lower 8bit LUT 100h~17Fh	Lower 8bit LUT 180h~1FFh	Lower 8bit LUT 200h~27Fh	Lower 8bit LUT 280h~2FFh	Lower 8bit LUT 300h~37Fh	Lower 8bit LUT 380h~3FFh	(reserved)	Video Input Control Registers	MC-3DNR Control Registers	Super Resolution Control Registers	GRC Control Registers	System Control Registers	Gamma/Dither Control Registers
40h ~ 7Fh														System Control Registers	(reserved)	System Control Registers
80h ~ BFh	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit	Upper 4bit		Video Output Control Registers					(reserved)
C0h ~ DFh	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)					(reserved)		
E0h ~ FFh	Common Registers (FFh: Page Address Setting)															

11.3. I²C Sub Address Map

Explanatory note: when the fixed value is written in the list, the value with "h" indicates hexadecimal number and the other value of "0" or "1" indicates the binary number.

The “-“means “don’t care”. <u>The register with “*” requires to write the default settings values in accordance with a system.</u>

11.3.1. Common Registers (No Page Address, Sub Address = E0h~FFh)

Page	Addr.	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
-	E0h	****				CLK_RXCLK_SEL	***		
-	E1h ~ E5h	********							
-	E6h	***			LVTX_SWING	1	LVTX_ENB	LVTX_ENA	0
-	E7h	**		LVTX_SRSEL		LVTX_SSEL	LVTX_SSEN	LVTX_FRSEL	
-	E8h ~ E9h	********							
-	EAh	0	0	0	0	0	0	0	IIC_MST_BTHR
-	EBh ~ F1h	********							
-	F2h	-	-	-	-	-	-	-	VREG_VLTEN
	F3h	-	-	-	-	-	-	--	0
	F4h~ F6h	-							
-	F7h	-	-	-	-	-	IIC_MST_NVM_ERR		IIC_MST_BUSY
-	F8 ~ FEh	-							
-	FFh	0	0	0	PAGE				

11.3.2. EXPRESSION Control Registers (Page Address = 00h, Sub Address = 00h~DFh)

Page	Addr.	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
00h	00h	-							*
00h	01h	*******							I_GBR_RANGE
00h	02h~ 13h	********							
00h	14h	*******							O_GBR_RANGE

00h	15h	CONTRAST							
00h	16h	BRIGHT							
00h	17h	COLOR							
00h	18h~ 19h	-							
00h	1Ah	-							*
00h	1Bh	-							*
00h	1Ch	COM_GON_COL				-	COMACT_SEL	COM_GO_EN	COM_EN
00h	1Dh	COM_W_SX				COM_W_SY			
00h	1Eh	COM_G_SX				COM_G_SY			
00h	1Fh	COM_PO_SX				COM_PO_SY			
00h	20h	COM_R_SX				COM_R_SY			
00h	21h	COM_B_SX				COM_B_SY			
00h	22h	COM_Y_SX				COM_Y_SY			
00h	23h	COM_M_SX				COM_M_SY			
00h	24h	COM_C_SX				COM_C_SY			
00h	25h	COM_P_SX				COM_P_SY			
00h	26h	COM_W_DX				COM_W_DY			
00h	27h	COM_G_DX				COM_G_DY			
00h	28h	COM_PO_DX				COM_PO_DY			
00h	29h	COM_R_DX				COM_R_DY			
00h	2Ah	COM_B_DX				COM_B_DY			
00h	2Bh	COM_Y_DX				COM_Y_DY			
00h	2Ch	COM_M_DX				COM_M_DY			
00h	2Dh	COM_C_DX				COM_C_DY			
00h	2Eh	COM_P_DX				COM_P_DY			
00h	2Fh	***			COM_W_GAIN				
00h	30h	***			COM_G_GAIN				
00h	31h	***			COM_PO_GAIN				
00h	32h	***			COM_R_GAIN				
00h	33h	***			COM_B_GAIN				
00h	34h	***			COM_Y_GAIN				
00h	35h	***			COM_M_GAIN				
00h	36h	***			COM_C_GAIN				
00h	37h	***			COM_P_GAIN				
00h	38h	-							COM_MODE
00h	39h	-							*
00h	3Ah	ICE__A				ICE_B			

00h	3Bh	-				ICE_C			
00h	3Ch	-		*****					ICE_FILT_TC
00h	3Dh	-		ICE_COLOR_GAIN_A					
00h	3Eh	***		ICE_COLOR_GAIN_B					
00h	3Fh	ICE_SCENE_CHDET				-	ICE_COLOR_GAIN_LMT		
00h	40h	ICE_A_BLACKLEV1		-	ICE_BGFACT				
00h	41h	ICE_A_BLACKLEV2				ICE_B_BALANCE			
00h	42h	-					**		
00h	43h	YHSHP							
00h	44h	YVSHP							
00h	45h	YTSHP							
00h	46h	YHSHP_HBAND			YHSHP_VBAND	YVSHP_HBAND			YVSHP_VBAND
00h	47h	YSHP_WB				-	YSHP_CORE		
00h	48h	********							
00h	49h	-	CTI_F0			-	CTI_LEV		
00h	4A ~ DFh	-							

11.3.3. Digital Gamma Function Look-up Table Registers (Page Address = 01h~18h, Sub Address = 00h~BFh)

Page	Addr.	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
01h	00 ~ 7Fh	Digital Gamma LUT **Lower 8bit [7:0] for Green** Gamma table address = (*Sub Address* +000h)							
	80 ~ BFh	Digital Gamma LUT **Upper 4bit [11:8] for Green <Odd Code>** Gamma table address = ((*Sub Address* - 80h + 000h) * 2 + 1)				Digital Gamma LUT **Upper 4bit [11:8] for Green <Even Code>** Gamma table address = ((*Sub Address* - 80h + 000h) * 2 + 0)			
02h	00 ~ 7Fh	Digital Gamma LUT **Lower 8bit [7:0] for Green** Gamma table address = (*Sub Address* + 080h)							
	80 ~ BFh	Digital Gamma LUT **Upper 4bit [11:8] for Green <Odd Code>** Gamma table address = ((*Sub Address* - 80h + 080h) * 2 + 1)				Digital Gamma LUT **Upper 4bit [11:8] for Green <Even Code>** Gamma table address = ((*Sub Address* - 80h + 080h) * 2 + 0)			
03h	00 ~ 7Fh	Digital Gamma LUT **Lower 8bit [7:0] for Green** Gamma table address = (*Sub Address* + 100h)							
	80 ~ BFh	Digital Gamma LUT **Upper 4bit [11:8] for Green <Odd Code>** Gamma table address = ((*Sub Address* - 80h + 100h) * 2 + 1)				Digital Gamma LUT **Upper 4bit [11:8] for Green <Even Code>** Gamma table address = ((*Sub Address* - 80h + 100h) * 2 + 0)			
04h	00 ~ 7Fh	Digital Gamma LUT **Lower 8bit [7:0] for Green** Gamma table address = (*Sub Address* + 180h)							
	80 ~ BFh	Digital Gamma LUT **Upper 4bit [11:8] for Green <Odd Code>** Gamma table address = ((*Sub Address* - 80h + 180h) * 2 + 1)				Digital Gamma LUT **Upper 4bit [11:8] for Green <Even Code>** Gamma table address = ((*Sub Address* - 80h + 180h) * 2 + 0)			

05h	**00 ~ 7Fh**	Digital Gamma LUT **Lower 8bit [7:0] for Green** Gamma table address = (*Sub Address* + 200h)	
	80 ~ BFh	Digital Gamma LUT **Upper 4bit [11:8] for Green <Odd Code>** Gamma table address = ((*Sub Address* - 80h + 200h) * 2 + 1)	Digital Gamma LUT **Upper 4bit [11:8] for Green <Even Code>** Gamma table address = ((*Sub Address* - 80h + 200h) * 2 + 0)
06h	**00 ~ 7Fh**	Digital Gamma LUT **Lower 8bit [7:0] for Green** Gamma table address = (*Sub Address* + 280h)	
	80 ~ BFh	Digital Gamma LUT **Upper 4bit [11:8] for Green <Odd Code>** Gamma table address = ((*Sub Address* - 80h + 280h) * 2 + 1)	Digital Gamma LUT **Upper 4bit [11:8] for Green <Even Code>** Gamma table address = ((*Sub Address* - 80h + 280h) * 2 + 0)
07h	**00 ~ 7Fh**	Digital Gamma LUT **Lower 8bit [7:0] for Green** Gamma table address = (*Sub Address* + 300h)	
	80 ~ BFh	Digital Gamma LUT **Upper 4bit [11:8] for Green <Odd Code>** Gamma table address = ((*Sub Address* - 80h + 300h) * 2 + 1)	Digital Gamma LUT **Upper 4bit [11:8] for Green <Even Code>** Gamma table address = ((*Sub Address* - 80h + 300h) * 2 + 0)
08h	**00 ~ 7Fh**	Digital Gamma LUT **Lower 8bit [7:0] for Green** Gamma table address = (*Sub Address* + 380h)	
	80 ~ BFh	Digital Gamma LUT **Upper 4bit [11:8] for Green <Odd Code>** Gamma table address = ((*Sub Address* - 80h + 380h) * 2 + 1)	Digital Gamma LUT **Upper 4bit [11:8] for Green <Even Code>** Gamma table address = ((*Sub Address* - 80h + 380h) * 2 + 0)
09h	**00 ~ 7Fh**	Digital Gamma LUT **Lower 8bit [7:0] for Blue** Gamma table address = (*Sub Address* + 000h)	
	80 ~ BFh	Digital Gamma LUT **Upper 4bit [11:8] for Blue <Odd Code>** Gamma table address = ((*Sub Address* - 80h + 000h) * 2 + 1)	Digital Gamma LUT **Upper 4bit [11:8] for Blue <Even Code>** Gamma table address = ((*Sub Address* - 80h + 000h) * 2 + 0)
0Ah	**00 ~ 7Fh**	Digital Gamma LUT **Lower 8bit [7:0] for Blue** Gamma table address = (*Sub Address* + 080h)	
	80 ~ BFh	Digital Gamma LUT **Upper 4bit [11:8] for Blue <Odd Code>** Gamma table address = ((*Sub Address* - 80h + 080h) * 2 + 1)	Digital Gamma LUT **Upper 4bit [11:8] for Blue <Even Code>** Gamma table address = ((*Sub Address* - 80h + 080h) * 2 + 0)
0Bh	**00 ~ 7Fh**	Digital Gamma LUT **Lower 8bit [7:0] for Blue** Gamma table address = (*Sub Address* + 100h)	
	80 ~ BFh	Digital Gamma LUT **Upper 4bit [11:8] for Blue <Odd Code>** Gamma table address = ((*Sub Address* - 80h + 100h) * 2 + 1)	Digital Gamma LUT **Upper 4bit [11:8] for Blue <Even Code>** Gamma table address = ((*Sub Address* - 80h + 100h) * 2 + 0)
0Ch	**00 ~ 7Fh**	Digital Gamma LUT **Lower 8bit [7:0] for Blue** Gamma table address = (*Sub Address* + 180h)	
	80 ~ BFh	Digital Gamma LUT **Upper 4bit [11:8] for Blue <Odd Code>** Gamma table address = ((*Sub Address* - 80h + 180h) * 2 + 1)	Digital Gamma LUT **Upper 4bit [11:8] for Blue <Even Code>** Gamma table address = ((*Sub Address* - 80h + 180h) * 2 + 0)
0Dh	**00 ~ 7Fh**	Digital Gamma LUT **Lower 8bit [7:0] for Blue** Gamma table address = (*Sub Address* + 200h)	
	80 ~ BFh	Digital Gamma LUT **Upper 4bit [11:8] for Blue <Odd Code>** Gamma table address = ((*Sub Address* - 80h + 200h) * 2 + 1)	Digital Gamma LUT **Upper 4bit [11:8] for Blue <Even Code>** Gamma table address = ((*Sub Address* - 80h + 200h) * 2 + 0)
0Eh	**00 ~ 7Fh**	Digital Gamma LUT **Lower 8bit [7:0] for Blue** Gamma table address = (*Sub Address* + 280h)	

	80 ~	Digital Gamma LUT **Upper 4bit [11:8] for Blue <Odd Code>**	Digital Gamma LUT **Upper 4bit [11:8] for Blue <Even Code>**
	BFh	Gamma table address = ((*Sub Address* - 80h + 280h) * 2 + 1)	Gamma table address = ((*Sub Address* - 80h + 280h) * 2 + 0)
0Fh	**00 ~**	Digital Gamma LUT **Lower 8bit [7:0] for Blue**	
	7Fh	Gamma table address = (*Sub Address* + 300h)	
	80 ~	Digital Gamma LUT **Upper 4bit [11:8] for Blue <Odd Code>**	Digital Gamma LUT **Upper 4bit [11:8] for Blue <Even Code>**
	BFh	Gamma table address = ((*Sub Address* - 80h + 300h) * 2 + 1)	Gamma table address = ((*Sub Address* - 80h + 300h) * 2 + 0)
10h	**00 ~**	Digital Gamma LUT **Lower 8bit [7:0] for Blue**	
	7Fh	Gamma table address = (*Sub Address* + 380h)	
	80 ~	Digital Gamma LUT **Upper 4bit [11:8] for Blue <Odd Code>**	Digital Gamma LUT **Upper 4bit [11:8] for Blue <Even Code>**
	BFh	Gamma table address = ((*Sub Address* - 80h + 380h) * 2 + 1)	Gamma table address = ((*Sub Address* - 80h + 380h) * 2 + 0)
11h	**00 ~**	Digital Gamma LUT **Lower 8bit [7:0] for Red**	
	7Fh	Gamma table address = (*Sub Address* + 000h)	
	80 ~	Digital Gamma LUT **Upper 4bit [11:8] for Red <Odd Code>**	Digital Gamma LUT **Upper 4bit [11:8] for Red <Even Code>**
	BFh	Gamma table address = ((*Sub Address* - 80h + 000h) * 2 + 1)	Gamma table address = ((*Sub Address* - 80h + 000h) * 2 + 0)
12h	**00 ~**	Digital Gamma LUT **Lower 8bit [7:0] for Red**	
	7Fh	Gamma table address = (*Sub Address* + 080h)	
	80 ~	Digital Gamma LUT **Upper 4bit [11:8] for Red <Odd Code>**	Digital Gamma LUT **Upper 4bit [11:8] for Red <Even Code>**
	BFh	Gamma table address = ((*Sub Address* - 80h + 080h) * 2 + 1)	Gamma table address = ((*Sub Address* - 80h + 080h) * 2 + 0)
13h	**00 ~**	Digital Gamma LUT **Lower 8bit [7:0] for Red**	
	7Fh	Gamma table address = (*Sub Address* + 100h)	
	80 ~	Digital Gamma LUT **Upper 4bit [11:8] for Red <Odd Code>**	Digital Gamma LUT **Upper 4bit [11:8] for Red <Even Code>**
	BFh	Gamma table address = ((*Sub Address* - 80h + 100h) * 2 + 1)	Gamma table address = ((*Sub Address* - 80h + 100h) * 2 + 0)
14h	**00 ~**	Digital Gamma LUT **Lower 8bit [7:0] for Red**	
	7Fh	Gamma table address = (*Sub Address* + 180h)	
	80 ~	Digital Gamma LUT **Upper 4bit [11:8] for Red <Odd Code>**	Digital Gamma LUT **Upper 4bit [11:8] for Red <Even Code>**
	BFh	Gamma table address = ((*Sub Address* - 80h + 180h) * 2 + 1)	Gamma table address = ((*Sub Address* - 80h + 180h) * 2 + 0)
15h	**00 ~**	Digital Gamma LUT **Lower 8bit [7:0] for Red**	
	7Fh	Gamma table address = (*Sub Address* + 200h)	
	80 ~	Digital Gamma LUT **Upper 4bit [11:8] for Red <Odd Code>**	Digital Gamma LUT **Upper 4bit [11:8] for Red <Even Code>**
	BFh	Gamma table address = ((*Sub Address* - 80h + 200h) * 2 + 1)	Gamma table address = ((*Sub Address* - 80h + 200h) * 2 + 0)
16h	**00 ~**	Digital Gamma LUT **Lower 8bit [7:0] for Red**	
	7Fh	Gamma table address = (*Sub Address* + 280h)	
	80 ~	Digital Gamma LUT **Upper 4bit [11:8] for Red <Odd Code>**	Digital Gamma LUT **Upper 4bit [11:8] for Red <Even Code>**
	BFh	Gamma table address = ((*Sub Address* - 80h + 280h) * 2 + 1)	Gamma table address = ((*Sub Address* - 80h + 280h) * 2 + 0)
17h	**00 ~**	Digital Gamma LUT **Lower 8bit [7:0] for Red**	
	7Fh	Gamma table address = (*Sub Address* + 300h)	
	80 ~	Digital Gamma LUT **Upper 4bit [11:8] for Red <Odd Code>**	Digital Gamma LUT **Upper 4bit [11:8] for Red <Even Code>**
	BFh	Gamma table address = ((*Sub Address* - 80h + 300h) * 2 + 1)	Gamma table address = ((*Sub Address* - 80h + 300h) * 2 + 0)

18h	**00 ~ 7Fh**	Digital Gamma　LUT **Lower 8bit [7:0] for Red** Gamma table address = (*Sub Address* + 380h)	
	80 ~ BFh	Digital Gamma　LUT **Upper 4bit [11:8] for Red <Odd Code>** Gamma table address = ((*Sub Address* - 80h + 380h) * 2 + 1)	Digital Gamma　LUT **Upper 4bit [11:8] for Red <Even Code>** Gamma table address = ((*Sub Address* - 80h + 380h) * 2 + 0)

11.3.4. Video Input Control Registers (Page Address = 1Ah, Sub Address = 00h~7Fh)

Page	Addr.	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
1Ah	**00h**	0	0	0	0	0	0	VIN_LNKMS_SEL *	VIN_LINK_MD *
1Ah	**01h**	*	*	*	*	*	*	*	*
1Ah	**02h**	*	*	VIN_SYNC1					
1Ah	**03h**	*	*	VIN_SYNC2					
1Ah	**04h**	*	*	VIN_SYNC3					
1Ah	**05h**	*	*	*	*	*	*	DEVALID	*
1Ah	**06~ 0Fh**	*	*	*	*	*	*	*	*
1Ah	**10h**	VIN_LVRMP_8BSFT *		*	*	*	*	*	*
1Ah	**11h**	00h							
1Ah	**12h**	-					VIN_LVRM_LVFMTSEL*		*
1Ah	**13 ~ 48h**	00h							
1Ah	**49 ~ 7Fh**	-							

11.3.5. Video Output Control Registers (Page Address = 1Ah, Sub Address = 80h~DFh)

Page	Addr.	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
1Ah	**80h**	00h							VOT_LINK_MD
1Ah	**81h**	*	*	*	*	*	*	*	*
1Ah	**82h**	*	*	*	*	*	*	*	*
1Ah	**83h**	*	VOT_SYNC1			*	*	*	*
1Ah	**84 ~ 86h**	*	*	*	*	*	*	*	*
1Ah	**87h**	VOT_LVTMP_8BSFT *		00h			*	*	*
1Ah	**88h**	*	*	*	*	*	*	*	*
1Ah	**89h**	*	*	*	*	*	*	*	*
1Ah	**8Ah**	00h				VOT_LNKSWP	*	*	*
1Ah	**8Bh**	*	*	*	*	*	*	*	*

1Ah	8Ch	*	*	*	*	*	*	*	*
1Ah	8Dh	00h		VOT_LVTMP_LVFMTSEL *		00h			
1Ah	8E ~ AFh	00h							
1Ah	B0 ~ B3h	********							
1Ah	B4h	*	*	*	*	VWIDTH			
1Ah	B5h	*	HWIDTH						
1Ah	B6h	*	*	*	*	*	*	*	SYNC_MODE
1Ah	B7 ~ DFh	*******							

11.3.6. MC-3DNR Control Registers (Page Address = 1Bh, Sub Address = 00h~DFh)

Page	Addr.	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
1Bh	00h~ 0Bh	*******							
1Bh	0Ch	*******							YNR
1Bh	0Dh ~ 21h	*******							
1Bh	22h	*******		MINALFA					
1Bh	23h	*******		MAXALFA					
1Bh	24h~ 2Ch	*******							
1Bh	2Dh	*******			PNR_PK				
1Bh	2Eh	CLIPKMAX				*******			
1Bh	2Fh~ 32h	*******							
1Bh	33h	*******		FBHISTTH					
1Bh	34h	*******		NLFB					
1Bh	35h~ 57h	*******							
1Bh	58h	*******		BKYCTRL_DEFVOL					
1Bh	59h~ 5Ah	*******							
1Bh	5Bh	*******		BKYCTRL_VP					
1Bh	5Ch	BKYCTRL_GRDV_H							

1Bh	5Dh	BKYCTRL_GRDV_L
1Bh	5Eh ~ B9h	*******
1Bh	BAh ~ DFh	-
		Sony provides the register setting sets corresponding to the intensity of noise reduction.

11.3.7. Super Resolution Control Registers (Page Address = 1Ch, Sub Address = 00h~DFh)

Page	Addr.	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
1Ch	00h~ 0Fh	*******							
1Ch	10h	VOLN							
1Ch	11h	VOLR							
1Ch	12h	VOLE							
1Ch	13h~ 1Ah	*******							
1Ch	1Bh	VOLERATIOMIN							
1Ch	1Ch	VOLERATIOMAX							
1Ch	1Dh ~ 23h	*******							
1Ch	24h	*******				NSHIFT			
1Ch	25h~ 3Dh	*******							
1Ch	3Eh	VOLE_BVD							
1Ch	3Fh~ 6Ch	********							
1Ch	6Dh	NLIMIT				****			
1Ch	6Eh ~ 7Fh	*******							
1Ch	80h	HADAON	*******						
1Ch	81h~ 85h	*******							
1Ch	86h	SPCOFF	*******						

1Ch	87h	*******							
1Ch	88h	ICONTON	*******						
1Ch	89h~ 8Ah	*******							
1Ch	8Bh	*******						HADA_EFFECT	
1Ch	8Ch ~ DFh	*******							

11.3.8. GRC Control Registers (Page Address = 1Dh, Sub Address = 00h~DFh)

Page	Addr.	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
1Dh	00h~ 2Dh	*******							
1Dh	2Eh	*******							GRC_EN
1Dh	2Fh	*******	GRC_VCORE			*******	GRC_HCORE		
1Dh	30h	*******							
1Dh	31h	MNR_FLAT_LEV				*******		MNR_EDGE_LEV	
1Dh	32h~ DFh	*******							

11.3.9. Gamma and Dither Control Registers (Page Address = 1Fh, Sub Address = 00h~3Fh)

Page	Addr.	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
1Bh	00h	00h							TBLA_SCLK_MSK
1Bh	01h	00h							TBLA_RDEN
1Bh	02h	00h							TBLA_VCLK_EN
1Bh	03h	00h							GMTBL_EN
1Bh	04h	00h							TBLB_SCLK_MSK
1Bh	05h	00h							TBLB_RDEN
1Bh	06h	00h							TBLB_VCLK_EN
1Bh	07h	00h							GMTBL_SEL
1Bh	08h	0	DITH_BIT		DITH_MODE			DITH_EN	
1Bh	09h	00h					DITH_INC		
1Bh	0Ah	********							
1Bh	0B ~ 3Fh	-							

11.3.10. Other System Control Registers-1 (Page Address = 1Dh, Sub Address = 40h~DFh)

Page	Addr.	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
1Dh	40h ~ BFh	*******							
1Dh	C0h ~ DFh	-							

11.3.11. Other System Control Registers-2 (Page Address = 1Eh, Sub Address = 00h~DFh)

Page	Addr.	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
1Eh	00h ~ 3Fh	*******							
1Eh	40h ~ DFh	-							

11.3.12. Other System Control Registers-3 (Page Address = 1Fh, Sub Address = 40h~DFh)

Page	Addr.	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
1Fh	40 ~ 6Fh	*******							
1Fh	70h ~ DFh	-							

11.4. I²C Register Description

Explanatory note: The value with "h" indicates hexadecimal number, the value of "0" or "1" indicates the binary number, and other value indicates decimal number. In a row of Direction, “R” means Read Only Register, “W” means Write Only register, and “W/R” means both Write and Read Register. The registers with “*” are V-latched registers. Those register values are reflected by every V-sync.

11.4.1. Common Registers (No Page Address)

Function Category	Page	Addr.	bit	Direction	Register Name	Description
I²C Function	-	**FFh**	[4:0]	W/R	PAGE	Page select from 00h~1Bh
	-	**EAh**	[0]	W/R	IIC_BTHR	I²C slave port to master port through operation 0:disable 1:through operation enable
	-	**F7h**	[0]	R	IIC_MST_BUSY	I²C master busy flag. 0: master is not busy, so accessing to I²C slave is not inhibited 1: master is busy, so accessing to I²C slave port is inhibited.
	-	**F7h**	[2:1]	R	IIC_MST_NVM_ERR	NVM access error status 0: no error other: error
Clock Path	-	**E0h**	[3]	W/R	CLK_RXCLK_SEL	Video clock source select 0: LVDS Rx Link-A 1: LVDS Rx Link-B
LVDS Tx and SSCG control	-	**E6h**	[4]	W/R	LVTX_SWING	LVDS Tx all clocks and all data swing voltage select 0: 250mV 1: 350mV
	-	**E6h**	[1]	W/R	LVTX_ENA	LVDS Tx Link-A output enable 0: disable 1: enable
	-	**E6h**	[2]	W/R	LVTX_ENB	LVDS Tx Link-B output enable 0: disable 1: enable
	-	**E7h**	[2]	W/R	LVTX_SSEN	LVDS Tx spread spectrum clock (SSCG) enable 0: disable 1: enable
	-	**E7h**	[1:0]	W/R	LVTX_FRSEL	LVDS Tx SSCG modulation frequency select
	-	**E7h**	[3]	W/R	LVTX_SSEL	LVDS Tx SSCG spread spectrum select 0: center 1: N/A
	-	**E7h**	[5:4]	W/R	LVTX_SRSEL	LVDS Tx SSCG spread ratio select
		F2h	[0]	W/R	VREG_VLTEN	Image control register’s sync latch enable The registers that control video processing parameters are reflect every V-sync at only VREG_VLTEN=1. If VREG_VLTEN=0, the video processing registers are not reflect but written values are kept. If you change the video processing registers, set VREG_VLTEN=0 first, next update the video processing registers, and finally set VREG_VLTEN=1. 0:V-sync latch disable(default) 1:V-sync latch enable

11.4.2. EXPRESSION Registers

Function Category	Page	Addr.	bit	Direction	Register Name	Description
Color Management	**00h**	**1Ch**	[0]	W*/R	COM_EN	Color Management Function Enable 0: disable, 1: enable
	00h	**1Dh**	[7:4]	W*/R	COM_W_SX	White area location x 0:-max ~ 8:+/-0 ~ 15:+max
	00h	**1Dh**	[3:0]	W*/R	COM_W_SY	White area location y 0:-max ~ 8:+/-0 ~ 15:+max
	00h	**1Eh**	[7:4]	W*/R	COM_G_SX	Green area location x 0:-max ~ 8:+/-0 ~ 15:+max
	00h	**1Eh**	[3:0]	W*/R	COM_G_SY	Green area location y 0:-max ~ 8:+/-0 ~ 15:+max

	00h	1Fh	[7:4]	W*/R	COM_PO_SX	Pale orange area location x	0:-max ~ 8:+/-0 ~ 15:+max
	00h	1Fh	[3:0]	W*/R	COM_PO_SY	Pale orange area location y	0:-max ~ 8:+/-0 ~ 15:+max
	00h	20h	[7:4]	W*/R	COM_R_SX	Red area location x	0:-max ~ 8:+/-0 ~ 15:+max
	00h	20h	[3:0]	W*/R	COM_R_SY	Red are location y	0:-max ~ 8:+/-0 ~ 15:+max
	00h	21h	[7:4]	W*/R	COM_B_SX	Blue area location x	0:-max ~ 8:+/-0 ~ 15:+max
	00h	21h	[3:0]	W*/R	COM_B_SY	Blue area location y	0:-max ~ 8:+/-0 ~ 15:+max
	00h	22h	[7:4]	W*/R	COM_Y_SX	Yellow area location x	0:-max ~ 8:+/-0 ~ 15:+max
	00h	22h	[3:0]	W*/R	COM_Y_SY	Yellow area location y	0:-max ~ 8:+/-0 ~ 15:+max
	00h	23h	[7:4]	W*/R	COM_M_SX	Magenta area location x	0:-max ~ 8:+/-0 ~ 15:+max
	00h	23h	[3:0]	W*/R	COM_M_SY	Magenta area location y	0:-max ~ 8:+/-0 ~ 15:+max
	00h	24h	[7:4]	W*/R	COM_C_SX	Cyan area location x	0:-max ~ 8:+/-0 ~ 15:+max
	00h	24h	[3:0]	W*/R	COM_C_SY	Cyan area location y	0:-max ~ 8:+/-0 ~ 15:+max
	00h	25h	[7:4]	W*/R	COM_P_SX	Pink area location x (COM_MODE=0 only)	0:-max ~ 8:+/-0 ~ 15:+max
	00h	25h	[3:0]	W*/R	COM_P_SY	Pink area location y(COM_MODE=0 only)	0:-max ~ 8:+/-0 ~ 15:+max
	00h	26h	[7:4]	W*/R	COM_W_DX	Vector for White of x direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	26h	[3:0]	W*/R	COM_W_DY	Vector for White of y direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	27h	[7:4]	W*/R	COM_G_DX	Vector for Green of x direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	27h	[3:0]	W*/R	COM_G_DY	Vector for Green of y direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	28h	[7:4]	W*/R	COM_PO_DX	Vector for Pale orange of x direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	28h	[3:0]	W*/R	COM_PO_DY	Vector for Pale orange of y direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	29h	[7:4]	W*/R	COM_R_DX	Vector for Red of x direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	29h	[3:0]	W*/R	COM_R_DY	Vector for Red of y direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	2Ah	[7:4]	W*/R	COM_B_DX	Vector for Blue of x direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	2Ah	[3:0]	W*/R	COM_B_DY	Vector for Blue of y direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	2Bh	[7:4]	W*/R	COM_Y_DX	Vector for Yellow of x direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	2Bh	[3:0]	W*/R	COM_Y_DY	Vector for Yellow of y direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	2Ch	[7:4]	W*/R	COM_M_DX	Vector for Magenta of x direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	2Ch	[3:0]	W*/R	COM_M_DY	Vector for Magenta of y direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	2Dh	[7:4]	W*/R	COM_C_DX	Vector for Cyan of x direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	2Dh	[3:0]	W*/R	COM_C_DY	Vector for Cyan of y direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	2Eh	[7:4]	W*/R	COM_P_DX	Vector for Pink(COM_MODE=0) or Pale orange2 (COM_MODE=1) of x direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	2Eh	[3:0]	W*/R	COM_P_DY	Vector for Pink(COM_MODE=0) or Pale orange2 (COM_MODE=1) of y direction	0:-max ~ 8:+/-0 ~ 15:+max
	00h	2Fh	[4:0]	W*/R	COM_W_GAIN	Vector gain for White	0:0 ~ 63:max
	00h	30h	[4:0]	W*/R	COM_G_GAIN	Vector gain for Green	0:0 ~ 63:max
	00h	31h	[4:0]	W*/R	COM_PO_GAIN	Vector gain for Pale orange	0:0 ~ 63:max
	00h	32h	[4:0]	W*/R	COM_R_GAIN	Vector gain for Red	0:0 ~ 63:max

	00h	33h	[4:0]	W*/R	COM_B_GAIN	Vector gain for Blue 0:0 ~ 63:max
	00h	34h	[4:0]	W*/R	COM_Y_GAIN	Vector gain for Yellow 0:0 ~ 63:max
	00h	35h	[4:0]	W*/R	COM_M_GAIN	Vector gain for Magenta 0:0 ~ 63:max
	00h	36h	[4:0]	W*/R	COM_C_GAIN	Vector gain for Cyan 0:0 ~ 63:max
	00h	37h	[4:0]	W*/R	COM_P_GAIN	Vector gain for Pink 0:0 ~ 63:max
	00h	1Ch	[1]	W*/R	COM_GO_EN	Evaluation purpose only. Highlight display selected color area by COM_GON_COL 0: disable, 1: enable
	00h	1Ch	[7:4]	W*/R	COM_GON_COL	Evaluation purpose only, valid only when COM_GO_EN=1. Select a color 0:White, 1:Green, 2:Pale orange, 3:Red, 4:Blue, 5:Yellow, 6:Magenta, 7:Cyan, 8:Pink
	00h	38h	[0]	W*/R	COM_MODE	Set color area select mode 0: Select from 9-color area 1: Select from 8-color area and 1 fixed area
iCE	00h	3Ah	[7:4]	W*/R	ICE_A	iCE A function gain. 0: Off ~ 15: Max.
	00h	3Ah	[3:0]	W*/R	ICE_B	iCE B function gain. 0: Off ~ 15: Max.
	00h	3Bh	[3:0]	W*/R	ICE_C	iCE C function gain 0: Off ~ 15: Max.
	00h	3Ch	[0]	W*/R	ICE_FILT_TC	iCE filter time constant 0: Slow 1:Fast
	00h	3Dh	[5:0]	W*/R	ICE_COLOR_GAIN_A	iCE color gain compensation (DC) 0: Off ~ 63: Max.
	00h	3Eh	[5:0]	W*/R	ICE_COLOR_GAIN_B	iCE color gain compensation (differential gain) 0: Off ~ 63: Max.
	00h	3Fh	[7:4]	W*/R	ICE_SCENE_CHDET	iCE scene change detection sensitivity 0: High ~ 15: Low
	00h	3Fh	[2:0]	W*/R	ICE_COLOR_GAIN_LMT	iCE color gain compensation (Limiter) 0: 0dB, 1: 0.5dB, 2: 1.0dB, 3: 2.0dB, 4: 3.5dB, 5: 6.0dB, 6: 8.0dB, 7: 9.ddB
	00h	40h	[7:6]	W*/R	ICE_A_BLACKLEV1	Set black level correction curve fold point. 0: 30IRE 1: 30IRE 2: 50IRE 3: 60IRE
	00h	40h	[4:0]	W*/R	ICE_BGFACT	Background processing 0: Off ~ 31Max
	00h	41h	[7:4]	W*/R	ICE_A_BLACKLEV2	iCE A black level correction 0: Off ~ 7 Max. (8 ~15: N/A)
	00h	41h	[3:0]	W*/R	ICE_B_BALANCE	iCE B negative gain reduction 0: Off ~ 7 Max. (8 ~15: N/A)
2-D Sharpness	00h	43h	[7:0]	W*/R	YHSHP	Y horizontal sharpness level 0: -max ~ 128: OFF(0dB) ~ 255: +max(about +10dB)
	00h	44h	[7:0]	W*/R	YVSHP	Y vertical sharpness level 0: -max ~ 128: OFF(0dB) ~ 255: +max(about +10dB)
	00h	45h	[7:0]	W*/R	YTSHP	Y diagonal sharpness level 0: -max ~ 128: OFF(0dB) ~ 255: +max(about +10dB)
	00h	46h	[7:5]	W*/R	YHSHP_HBAND	Horizontal frequency band to apply Y horizontal sharpness 0: min. ~ 4: max (5~7: N/A)
	00h	46h	[4]	W*/R	YHSHP_VBAND	Vertical frequency band to apply Y horizontal sharpness. 0: low ~ 1: high

	00h	**46h**	[3:1]	W*/R	YVSHP_HBAND	Horizontal frequency band to apply Y vertical sharpness 0: min. ~ 4: max (5~7: N/A)
	00h	**46h**	[0]	W*/R	YVSHP_VBAND	Vertical frequency band to apply Y vertical sharpness 0: low ~ 1: high
	00h	**47h**	[7:4]	W*/R	YSHP_WB	Top and bottom characteristic of Y sharpness 0: black side/max, white side min ~ 8: top and bottom is symmetric ~ 15: black side/min, white side max
	00h	**47h**	[1:0]	W*/R	YSHP_CORE	Quantity of coring of Y sharpness 0: OFF ~ 3: max
	00h	**49h**	[6:4]	W*/R	CTI_F0	CTI F0 0: f0=min. ~ 7: f0=max.
	00h	**49h**	[1:0]	W*/R	CTI_LEV	CTI level 0: OFF ~ 3: max.
Other Image Control Registers	**00h**	**15h**	[7:0]	W*/R	CONTRAST	Output Contrast Control 0: x0 ~ 128: x1 ~ 255: x255/128
	00h	**16h**	[7:0]	W*/R	BRIGHT	Output Brightness Control 0: -128 ~ 128: +/-0 ~ 255: +127 (8bit) At 10bit, this value becomes quadruple.
	00h	**17h**	[7:0]	W*/R	COLOR	Output Color Saturation Control 0: x0 ~ 128: x1 ~ 255: x255/128
	00h	**01h**	[0]	W/R	I_GBR_RANGE	GBR Video Input Dynamic Range 0: 0~1023 (10bit), 0~255 (8bit) 1: 64-940 (10bit), 16~235 (8bit)
	00h	**14h**	[0]	W/R	O_GBR_RANGE	GBR Video Output Dynamic Range 0: 0~1023 (10bit) 0~255 (8bit) 1: 64-940 (10bit) 16~235 (8bit)

11.4.3. Video Input Control Registers (Page Address = 1Ah)

Function Category	Page	Addr.	bit	Direction	Register Name	Description
Video Input Control	**1Ah**	**00h**	[0]	W/R	VIN_LINK_MD	LVDS Rx Dual/Single Link Select 0:FHD (dual link) 1:WXGA (single link)
	1Ah	**00h**	[1]	W/R	VIN_LNKMS_SEL	LVDS Rx master link select (Link swap function) Note) this function selects only data and data enable. Clock is selected by other register. 0: 1st pixel input to link-A, 2nd pixel input to link-B 1: 2nd pixel input to link-A, 1st pixel input to link-B
	1Ah	**02h**	[5:0]	W/R	VIN_SYNC1	Trigger signal of LVDS Rx master link select Select from { lvrx_ch0[6:0], lvrx_ch1[6:0], lvrx_ch2[6:0], lvrx_ch3[6:0], lvrx_ch4[6:0] } Ex. for JEIDA,VASA 19: VS-rise 20 : DE-rise When you select 20 , DEVALID (page 1Ah sub address=05h, data[1]) must be set to 1 .
	1Ah	**03h**	[5:0]	W/R	VIN_SYNC2	Trigger signal of LVDS Rx slave link select Select from { lvrx_ch0[6:0], lvrx_ch1[6:0], lvrx_ch2[6:0], lvrx_ch3[6:0], lvrx_ch4[6:0] } Ex. for JEIDA,VASA 19: VS-rise 20 : DE-rise

						When you select 20 , DEVALID (page 1Ah sub address=05h, data[1]) must be set to 1 .
	1Ah	**04h**	[5:0]	W/R	VIN_SYNC3	Trigger signal of VIN fifo read start select Select from { lvrx_ch0[6:0], lvrx_ch1[6:0], lvrx_ch2[6:0], lvrx_ch3[6:0], lvrx_ch4[6:0] } Ex. for JEIDA,VASA 19: VS-rise 20 : DE-rise When you select 20 , DEVALID (page 1Ah sub address=05h, data[1]) must be set to 1 .
	1Ah	**05h**	[1]	W/R	DEVALID	DE valid signal enable 0: disenable (for Sync through mode) 1: enable (for DE-only mode)
	1Ah	**10h**	[7:6]	W/R	VIN_LVRMP_8BSFT	LVDS Rx format and bit width 0: VESA 10bit, JEIDA 10 and 8bit 3: VESA 8bit Other value is N/A.
	1Ah	**12h**	[2:1]	W/R	VIN_LVRM_LVFMTSEL	LVDS Rx format Select 0: VESA 1: JEIDA Other value is N/A.

11.4.4. Video Output Control Registers (Page Address = 1Ah)

Function Category	Page	Addr.	bit	Direction	Register Name	Description
Video Output Control	**1Ah**	**80h**	[0]	W/R	VOT_LINK_MD	LVDS Tx Dual/Single Link Select. Note) set the same value as VIN_LINK_MD. 0:FHD (dual link) 1:WXGA (single link)
	1Ah	**83h**	[6:4]	W/R	VOT_SYNC1	Trigger signal of VOT fifo read start select 000:DE-rise 001:VS-rise 010:HS-rise 011:ExternalTrigger-rise 100:sreset-fall
	1Ah	**87h**	[7:6]	W/R	VOT_LVTMP_8BSFT	LVDS Tx format and bit width 0: VESA 10bit, JEIDA 10 and 8bit 2: VESA 8bit Other value is N/A.
	1Ah	**8Ah**	[3]	W/R	VOT_LNKSWP	LVDS Tx link swap 0: swap disable (input A->output A, input B -> output B) 1: swap enable (input A->output B, input B -> output A)
	1Ah	**8Dh**	[5:4]	W/R	VOT_LVTMP_LVFMTSEL	LVDS Tx format 0: VESA 1: JEIDA Other value is N/A.
	1Ah	**B4h**	[3:0]	W/R	VWIDTH	Output VSYNC width select (For only Sync through mode) Unit:Line 0-: prohibited 15: 15Line
	1Ah	**B5h**	[6:0]	W/R	HWIDTH	Output VSYNC width select (For only Sync through mode) Unit:VCLK 0,1 : prohibited

						127: 127VCLK If you use SSCG (LVTX_SSEN=1), HWIDTH must be set over 44.
	1Ah	B6h	[0]	W/R	SYNC_MODE	Output synchronous signal select 0: For DE only mode、1: For Sync through mode

11.4.5. Gamma and Dither Control Registers (Page Address = 1Fh)

Function Category	Page	Addr.	bit	Direction	Register Name	Description
Gamma Function	1Fh	03h	[0]	W*/R	GMTBL_EN	Gamma block output select 0:input through 1:look up table read output
	1Fh	07h	[0]	W*/R	GMTBL_SEL	Gamma look up table A or B select 0:select table A 1:select table B
	1Fh	00h	[0]	W/R	TBLA_SCLK_MSK	Gamma Table-A I^2C clock mask enable (*1) 0:clock run 1:clock stop
	1Fh	04h	[0]	W/R	TBLB_SCLK_MSK	Gamma Table-B I^2C clock mask enable (*1) 0:clock run 1:clock stop
	1Fh	01h	[0]	W/R	TBLA_RDEN	Gamma Table-A mode switch (*1) 0: I^2C write mode 1:Normal mode
	1Fh	05h	[0]	W/R	TBLB_RDEN	Gamma Table-B mode switch (*1) 0: I^2C write mode 1:Normal mode
	1Fh	02h	[0]	W/R	TBLA_VCLK_EN	Gamma Table-A video clock run enable (*1) 0:clock stop 1:clock run
	1Fh	06h	[0]	W/R	TBLB_VCLK_EN	Gamma Table-B video clock run enable (*1) 0:clock stop 1:clock run
Dither Function	1Fh	08h	[0]	W/R	DITH_EN	Dither enable 0:diable 1:enable
	1Fh	08h	[3:1]	W/R	DITH_MODE	Dither mode select 0:Reserved 1:round 2:Framerate conversion 3:Reserved 4:2x2 matrix pattern 1 5:2x2 matrix pattern 2 6:4x4 matrix pattern 1 7:4x4 matrix pattern 2
	1Fh	08h	[5:4]	W/R	DITH_BIT	Operation bits 0: 10bit 2: 8bit Other value is N/A.
	1Fh	09h	[2:0]	W/R	DITH_INC	Pattern Increment mode 0: increment by pixel 1: increment by line 2: increment by frame 3: Reserved

11.4.6. MC-3DNR Control Registers (Page Address = 1Bh)

Function Category	Page	Addr.	bit	Direction	Register Name	Description
MC-3DNR Function	1Bh	0Ch	[0]	W/R	YNR	NR function enable 0: disable 1: enable
	1Bh	33h	[5:0]	W/R	FBHISTTH	Time constant of noise detector 0: fast 63: slow
	1Bh	34h	[5:0]	W/R	NLFB	Time constant of noise filter 0: fast 63: slow
	1Bh	22h	[5:0]	W/R	MINALFA	NR level control registers see application note
	1Bh	23h	[5:0]	W/R	MAXALFA	
	1Bh	2Dh	[4:0]	W/R	PNR_PK	
	1Bh	2Eh	[7:4]	W/R	CLIPKMAX	
	1Bh	58h	[5:0]	W/R	BKYCTRL_DEFVOL	

	1Bh	5Bh	[5:0]	W/R	BKYCTRL_VP	
	1Bh	5Ch	[7:0]	W/R	BKYCTRL_GRDV_H	
	1Bh	5Dh	[7:0]	W/R	BKYCTRL_GRDV_L	

11.4.7. GRC Control Registers (Page Address = 1Fh)

Function Category	Page	Addr.	bit	Direction	Register Name	Description
GRC Function	1Dh	2Eh	[0:0]	W/R	GRC_EN	Adaptive horizontal smoothing 0: disable 1: enable
	1Dh	2Fh	[2:0]	W/R	GRC_HCORE	Adaptive coring for horizontal high frequency component 0: off 7: max
	1Dh	2Fh	[6:4]	W/R	GRC_VCORE	Adaptive coring for vertical high frequency component 0: off 7: max
	1Dh	31h	[1:0]	W/R	MNR_EDGE_LEV	Mosquito NR for signal edge 0: off 3: max
	1Dh	31h	[7:4]	W/R	MNR_FLAT_LEV	Mosquito NR for all area 0: off 15: max

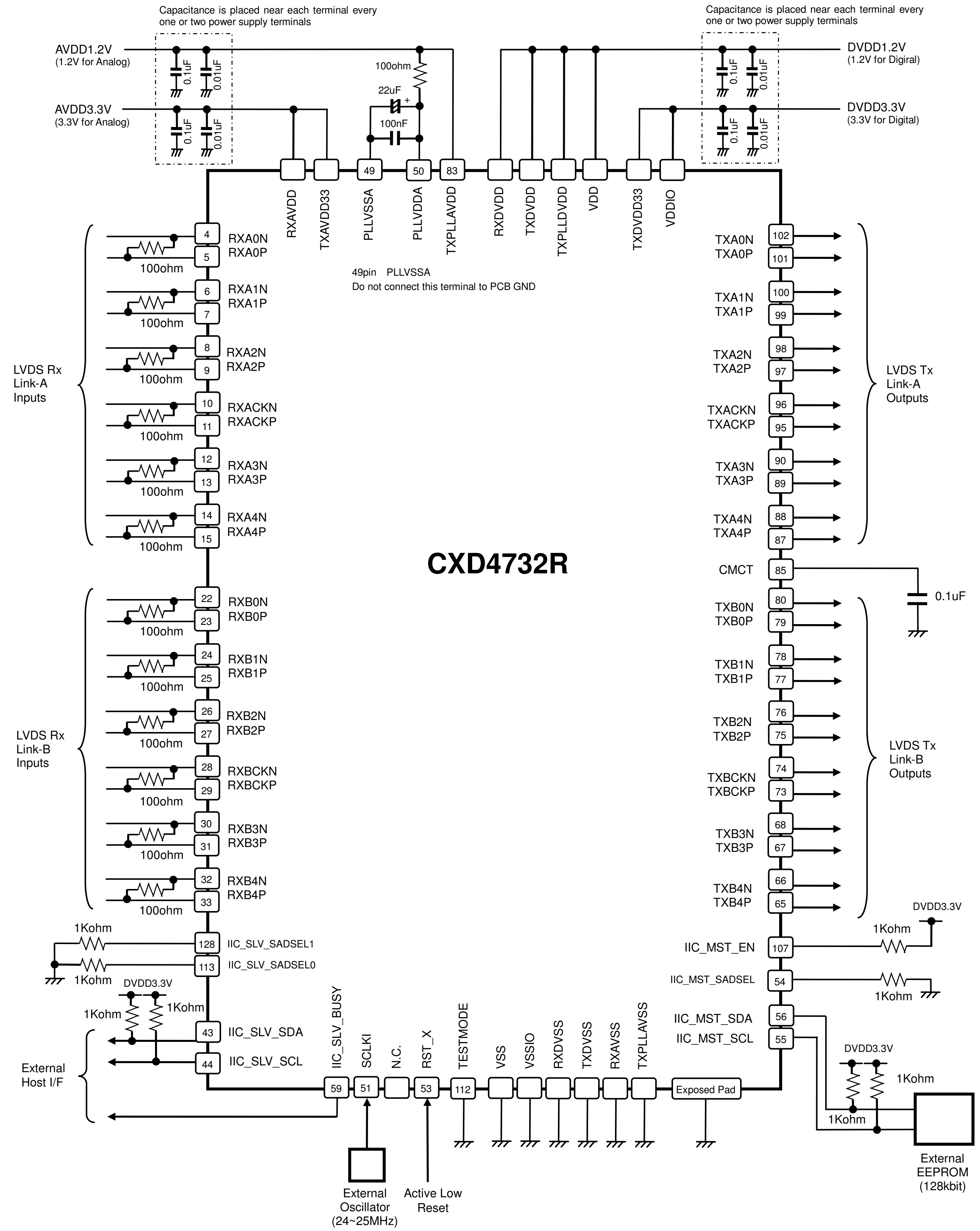
11.4.8. Super Resolution Control Registers (Page Address = 1Fh)

Function Category	Page	Addr.	bit	Direction	Register Name	Description
Super Resolution Function	1Ch	10h	[7:0]	W/R	VOLN	2DNR（ICONTON=0 only） 0 : min 255: max
	1Ch	11h	[7:0]	W/R	VOLR	Super Resolution （ICONTON=0 only） 0: min 255 : max
	1Ch	12h	[7:0]	W/R	VOLE	2DNR+ Super Resolution gain （ICONTON=0 only） 32: min 255: max
	1Ch	1Bh	[7:0]	W/R	VOLERATIOMIN	Effect around text data Base data is changed by value of VOLE_BVD or VOLE. Recommended value = 128*32 / VOLE_BVD (ICONTON=0 : 128*32/ VOLE ） Must be set more than recommended value 255: max
	1Ch	1Ch	[7:0]	W/R	VOLERATIOMAX	Effect control around text data Sony recommends 96d～128d
	1Ch	24h	[3:0]	W/R	NSHIFT	Control active noise range (ICONTON=1 only) 3: for net images , 4: for other images
	1Ch	3Eh	[7:0]	W/R	VOLE_BVD	2DNR+ Super Resolution gain（ICONTON=1 only） 32 : min 255 : max
	1Ch	6Dh	[7:4]	W/R	NLIMIT	limit block noise level. (HADAON-=1 only) 0: min F: max
	1Ch	80h	[7:7]	W/R	HADAON	Reduce Super Resolution effect in pale orange area 0: OFF 1: ON
	1Ch	86h	[7:7]	W/R	SPCOFF	Super Resolution enable 0: enable 1: disable

	1Ch	**88h**	[7:7]	W/R	ICONTON	SUPER RESOLUTION automatic control 0: OFF 1: ON
	1Ch	**8Bh**	[1:0]	W/R	HADA_EFFECT	Reduce level for SUPER RESOLUTION effect in pale orange area 0 : max 3: min

Note *1) refer to **Chapter 10.2** "Gamma Look-up Table Setup" for details.

12. Example of Application Circuit

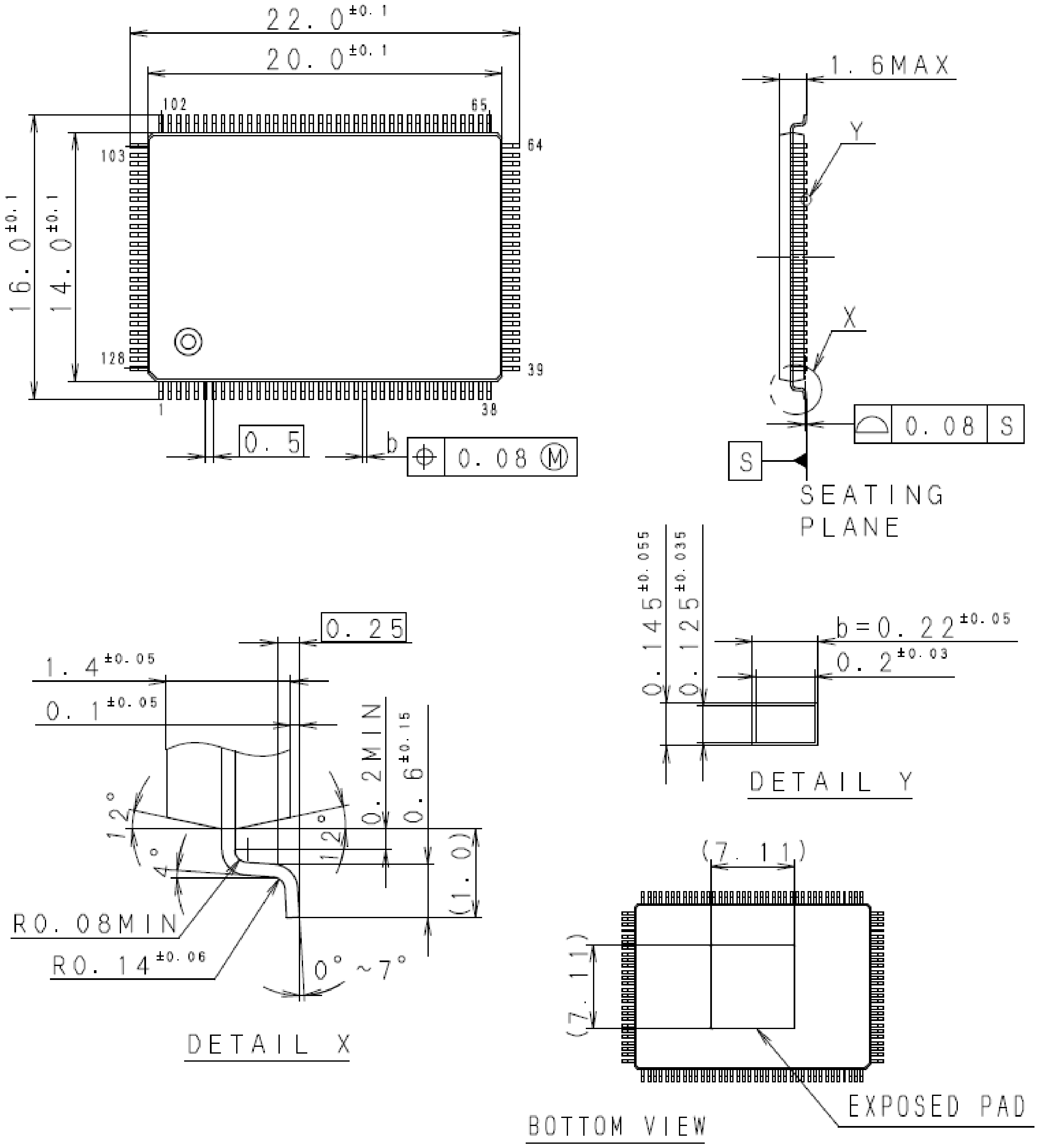


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

13. Package Outline

(Unit: mm)

128PIN LQFP (PLASTIC)

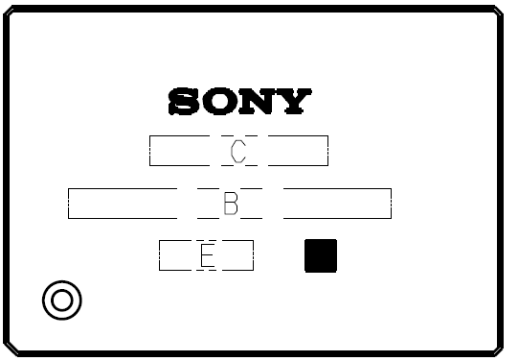


SONY CODE	LQFP-128P-L492
JEITA CODE	P-LQFP128-20X14-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	Sn PLATING
LEAD MATERIAL	COPPER
PACKAGE MASS	0.95g

14. Marking



MARKING C: CXD4732R

1) TYPE NO. (MAX 8 CHARACTERS) IN SECTION C.
(FOR MORE THAN 8 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
2) LOT NO. (MAX 13 CHARACTERS) IN SECTION B.
3) YEAR CODE. (2 CHARACTERS), WEEK CODE. (2 CHARACTERS) IN SECTION E.

Note