

High Power DPDT Switch with Logic Control

Description

This IC can be used in wireless communication systems, for example, W-CDMA handsets.

The IC has on-chip logic for operation with 2 CMOS control inputs.

The Sony JPHEMT process is used for low insertion loss and on-chip logic circuit.

Features

- Low insertion loss
- 2 CMOS compatible control line
- Small package size: 12-pin UQFN

Applications

- Antenna switch for cellular handsets
- Dual-Band W-CDMA

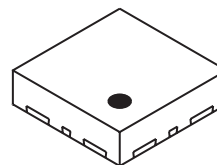
Structure

GaAs JPHEMT MMIC

Absolute Maximum Ratings (Ta = 25°C)

• Bias voltage	V _{DD}	7	V
• Control voltage	V _{ctl}	5	V
• Operating temperature	T _{opr}	–35 to +85	°C
• Storage temperature	T _{stg}	–65 to +150	°C

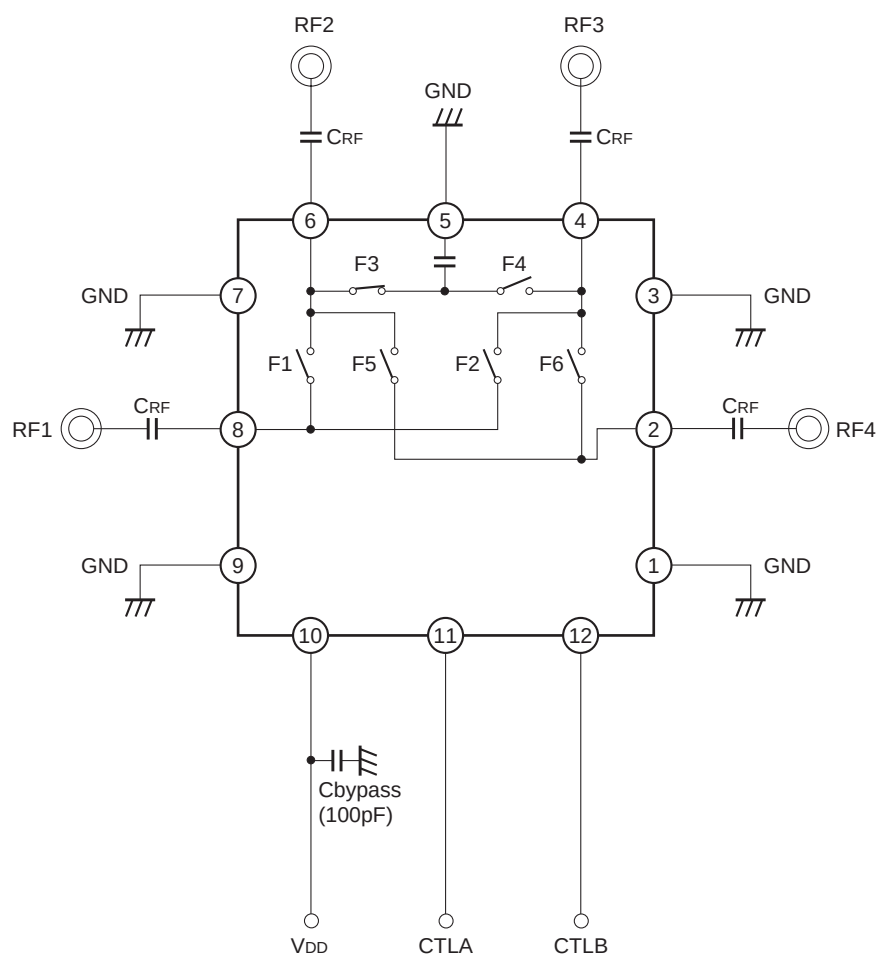
12 pin UQFN (Plastic)



GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

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Block Diagram and Recommended Circuit



When using this IC, the following external components should be used:

CRF: This capacitor is used for RF decoupling and must be used for all applications.

Cbypass: This capacitor is used for DC line filtering. 100pF is recommended.

Truth Table

State	CTLA	CTLB	ON State	F1	F2	F3	F4	F5	F6
1	L	L	RF4 – RF3	OFF	OFF	ON	OFF	OFF	ON
2	L	H	RF4 – RF2	OFF	OFF	OFF	ON	ON	OFF
3	H	L	RF1 – RF3	OFF	ON	ON	OFF	OFF	OFF
4	H	H	RF1 – RF2	ON	OFF	OFF	ON	OFF	OFF

DC Bias Conditions

(Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	2.0	2.85	3.6	V
Vctl (L)	0	—	0.4	V
VDD	2.5	2.85	3.6	V

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	State	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL		830 to 885MHz		0.25	0.45	dB
			1920 to 2170MHz		0.35	0.55	dB
Isolation	ISO.		830 to 885MHz	20	25		dB
			1920 to 2170MHz	15	20		dB
VSWR	VSWR		50Ω		1.2	1.5	—
Switching speed	TSW				5	10	μs
ACLR	ACLR1	±5MHz	*1		−60	−50	dBc
	ACLR2	±10MHz	*1		−65	−55	dBc
Harmonics	2fo		*1		−75	−60	dBc
	3fo		*1		−75	−60	dBc
Bias current	IDD		VDD = 2.85V		80	150	μA
Control current	Ictl		Vctl (H) = 2.85V		15	25	μA

*1 Pin = 25dBm, 0/2.85V control, VDD = 2.85V, 830 to 840MHz, 1920 to 1980MHz

Measurement system noise level: ACLR (±5MHz) < −60dBc, (±10MHz) < −65dBc, 2nd Harmonics < −90dBc,
3rd Harmonics < −90dBc

Unit: mm

The drawing shows a 12-pin connector with the following dimensions and features:

- Top View:** A square footprint with a width of 2.0 and a height of 2.0. Pin locations are numbered 1 through 12. A central circle is located at the intersection of the centerlines. A dashed line indicates the center of the connector.
- Side View:** Shows a total height of 0.55 ± 0.05 . The connector has a central slot and two side slots.
- Front View:** Shows the connector's profile with a width of 0.4 ± 0.1 . It features a central circular feature with a diameter of 0.6 and four rounded corners with a radius of $4-R0.2$. The pin pitch is 0.26 . The pin diameter is 0.14 . The pin length is 0.18 . The pin thickness is 0.07 . The pin width is 0.25 . The pin height is 0.4 . The pin diameter is 0.05 . The pin material is M . The pin surface is S . The pin finish is $A-B$. The pin tolerance is C .
- Detail View:** A close-up of the pin tip showing a diameter of 0.05 and a surface finish of S .
- Bottom View:** Shows the solder plating on the bottom of the connector. The solder plating thickness is $+0.09$ and -0.03 . The solder plating width is 0.14 and 0.25 . The solder plating height is 0.25 and 0.30 . The solder plating material is S .

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	UQFN-12P-01
EIAJ CODE	_____
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.01g

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm